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ANALOG DEVICES

*Click **here** to ask an associate for production status of specific part numbers.*

MAX86177

Quad-Channel AFE for Low-Power Heart Rate Monitor and Pulse Oximeter

General Description

The MAX86177 is an ultra-low-power optical data acquisition system with both transmit and receive channels. On the transmitter side, it has two, high-current 8-bit programmable LED drivers and supports up to six LEDs. On the receiver side, it has four low-noise charge integrating front-ends that each includes independent 20-bit analog-to-digital converters (ADCs) and best-in-class ambient light cancellation (ALC) circuits, producing the highest performing integrated optical data acquisition system in the market today.

Due to its low power consumption, compact size, ease and flexibility of use, the MAX86177 is ideal for a wide variety of optical sensing applications such as pulse oximetry and heart rate detection.

The MAX86177 operates on a 1.8V main supply voltage and a 3.1V to 5.5V LED driver supply voltage. The device supports both I^2C and SPI compatible interfaces in a fully autonomous way. The device has a large 512-word built-in FIFO. The MAX86177 is available in a 7 x 4 28-bump wafer level package (WLP) with dimensions of 2.83mm x 1.89mm, and operates over -40ºC to +85ºC temperature range.

Applications

- Wearable Devices for Fitness, Wellness, and Medical Applications
- Clinical Accuracy
- Suitable for Wrist, Finger, Ear, and Other Locations
- Optimized Performance to Detect
  - Optical Heart Rate
  - Heart Rate Variability
  - Oxygen Saturation (SpO_2)
  - Body Hydration
  - Muscle and Tissue Oxygen Saturation (SmO_2 & StO_2)
  - Maximum Oxygen Consumption (VO_2 Max)

Benefits and Features

- Complete Quad-Channel Optical Data Acquisition System
- Ultra-Low-Power Operation for Body Wearable Devices
  - Low-Power Operation, Optical Readout Channel < 11μA at 25fps
  - Exposure Integration Period Ranging from 14.6μs to 118.2μs
  - Low Shutdown Current < 1μA
- Excellent Top-End Dynamic Range: 98dB in White Card Loop-Back Test (Nyquist Sample-to-Sample Variance)
- Extended Dynamic Range up to 118dB (100fps, Measurement Averaging and Off-Chip Filtering)
- Supports Frame Rates from 1fps to 1.9kfps
- High Resolution 20-bit Charge Integrating ADCs
- Low Dark Current Noise of < 50pA RMS (Sample-to-Sample Variance in 118.2μs Integration Time)
- Excellent Ambient Range and Rejection Capability
  - > 200μA Ambient Photodetector Current
  - > 80dB Ambient Rejection at 120Hz (Measurement Averaging = 2)

Ordering Information appears at end of data sheet.

19-101246; Rev 1; 6/23

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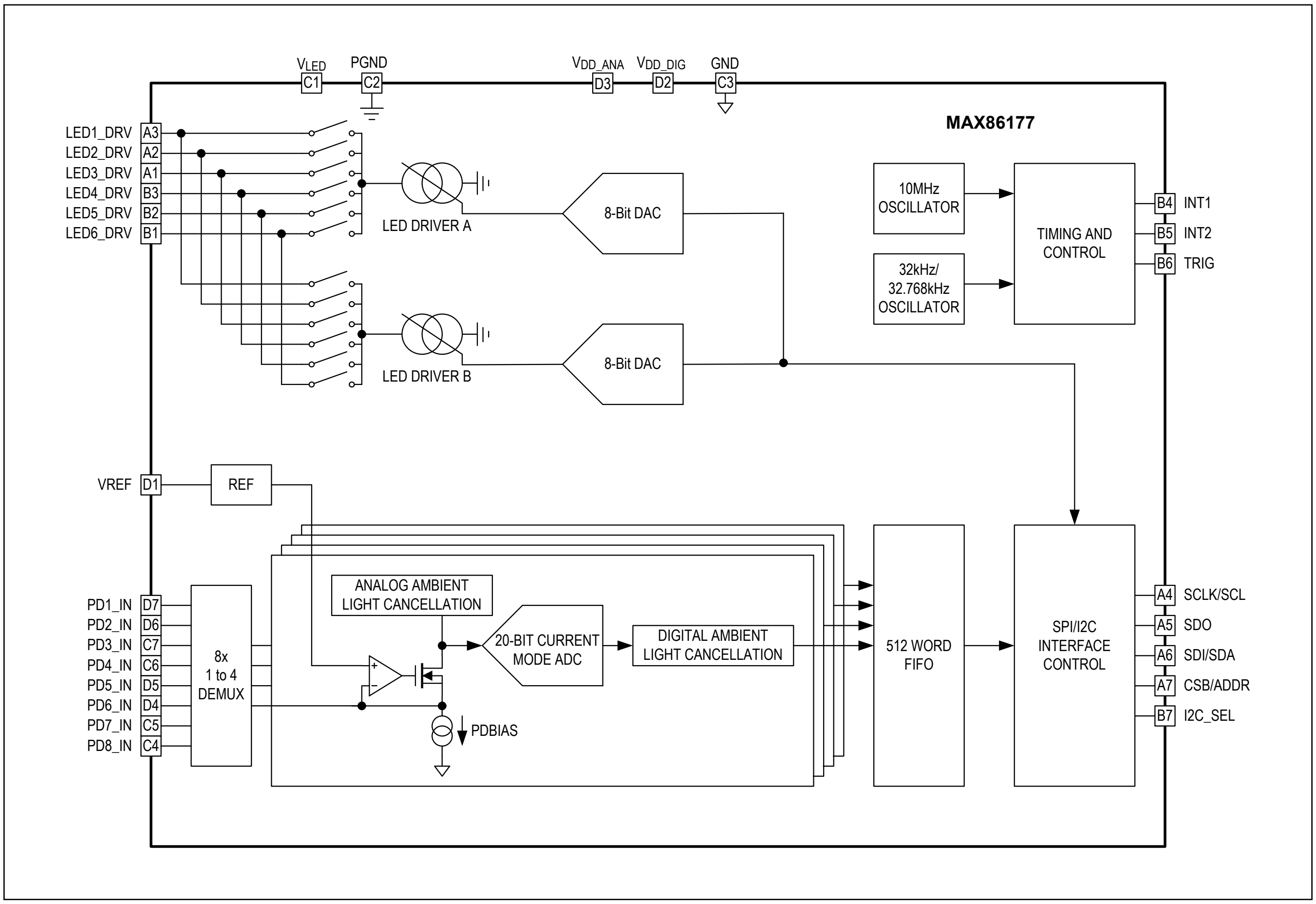
Simplified Block Diagram



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Absolute Maximum Ratings

V_{DD_ANA}, V_{DD_DIG} to GND .... -0.3V to +2.2V
V_{LED} to PGND .... -0.3V to +6.0V
PGND to GND .... -0.3V to +0.3V
PDm_IN to GND .... -0.3V to +2.2V
VREF to GND .... -0.3V to +2.2V
LEDn_DRV to PGND ....-0.3V to V_{LED} + 0.3V
SDO to GND...-0.3V to V_{DD_DIG} + 0.3V
SDI/SDA, SCLK/SCL, CSB/ADDR, I2C_SEL, INT1, INT2, TRIG to GND ....-0.3V to +6.0V
Output Short-Circuit Duration....................................Continuous
Continuous Input Current Into Any Pin (except LEDn_DRV Pins)..±50mA
Operating Temperature Range.............................-40°C to +85°C
Storage Temperature Range ....-40°C to +150°C
Soldering Temperature (reflow) ....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

28-Pin WLP

Package Code	N281C2+1
Outline Number	21-100579
Land Pattern Number	Refer to *Application Note 1891*
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	50.6°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{DD_ANA} = 1.8V, V_{DD_DIG} = 1.8V, V_{LED} = 3.7V, T_A = +25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
READOUT CHANNEL						
ADC Resolution				20		bits
ADC INL	INL_{RX}	MEASx_TINT = 118.2µs		±10		LSB
		MEASx_TINT = 14.6µs		±40		
ADC DNL	DNL_{RX}	MEASx_TINT = 118.2µs		±3		LSB
		MEASx_TINT = 14.6µs		±10		
ADC Full-Scale Input Current	I_{FS}	MEASx_PPGy_ADC_RGE = 0		16.0		µA
		MEASx_PPGy_ADC_RGE = 1		32.0		
ADC DC Cancellation Full-Scale Current		Programmable by MEASx_PPGy_DACOFF		48		µA
ADC Integration Time	t_{INT}	MEASx_TINT = 0x0		14.6		µs
		MEASx_TINT = 0x1		29.2		
		MEASx_TINT = 0x2		58.6		
		MEASx_TINT = 0x3		118.2		

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Electrical Characteristics (continued)

(V_{DD_ANA} = 1.8V, V_{DD_DIG} = 1.8V, V_{LED} = 3.7V, T_A = +25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Free-Running Frame Rate					1		FPS
Maximum Free-Running Frame Rate					1927.53		FPS
Internal Frame-Rate Clock	f_{FRAME_CLK}	FR_CLK_SEL = 32000		-2	±0.5	+2	%
		FR_CLK_SEL = 32768		-2	±0.5	+2	
TRIG External Frame-Clock Frequency	$f_{TRIG\_EXT\_CLK}$			31000		34000	Hz
TRIG Pulse-Width	t_{TRIG}			1			µs
Internal Power-Up Time					200		µs
ADC Clock Frequency	CLK			9.75	10.0	10.25	MHz
Maximum DC Ambient Light Rejection	ALR	When ALC_OVF goes from 0 to 1			200		µA
Dynamic Ambient Light Rejection		$I_{EXPOSURE}$ = 0µA, $I_{AMBIENT}$ = 8µA DC with ± 8µA_{P-P} 120Hz sine wave, MEASx_PPGy_ADC_RGE = 32µA, MEASx_TINT = 14.6µs, MEASx_AVER = 2x			84		dB
DC Ambient Light Rejection		$I_{EXPOSURE}$ = 1µA, $I_{AMBIENT}$ = 1µA and 30µA			0.5		nA
Dark Current Offset	DC_O	ALC = ON, PDm_BIAS = 0x1, MEASx_TINT = 118.2µs			±1		COUNTS
Dark Current Input Referred Noise		MEASx_TINT = 14.6µs			122		pA_{RMS}
		MEASx_TINT = 29.2µs			76		
		MEASx_TINT = 58.6µs			54		
		MEASx_TINT = 118.2µs			40		
LED DRIVER							
LED Current Resolution					8		Bits
Driver DNL	DNL_{TX}	MEASx_LED_RGE = 0x3		-1		+1	LSB
Driver INL	INL_{TX}	MEASx_LED_RGE = 0x3			1		LSB
Full-Scale LED Current	I_{LED}	MEASx_DRVz_PA = 0xFF	MEASx_LED_RGE = 0x0		32		mA
			MEASx_LED_RGE = 0x1		64		
			MEASx_LED_RGE = 0x2		96		
			MEASx_LED_RGE = 0x3	118	128	138	
LED Driver Rise Time		MEASx_DRVz_PA = 0xFF, 10% to 90%, all range settings				3	µs
LED Driver Fall Time		MEASx_DRVz_PA = 0xFF, 10% to 90%, all range settings				3	µs

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Electrical Characteristics (continued)

(V_{DD_ANA} = 1.8V, V_{DD_DIG} = 1.8V, V_{LED} = 3.7V, T_A = +25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Output Voltage	V_{OL}	MEASx_DRVz_PA = 0xFF, <5% change in LED current	MEASx_LED_RGE = 0x0		130		mV
			MEASx_LED_RGE = 0x1		255		
			MEASx_LED_RGE = 0x2		370		
			MEASx_LED_RGE = 0x3		485		
			MEASx_LED_RGE = 0x3, LED Drivers A and B connected to the same pin.		515	675	
LED Driver DC V_{LED} PSR		MEASx_DRVz_PA = 0xFF, V_{DD} = 1.8V, V_{LEDn_DRV} = 1.2V, V_{LED} = 3.1V to 5.5V	MEASx_LED_RGE = 0x0		±5		µA/V
			MEASx_LED_RGE = 0x1		±5		
			MEASx_LED_RGE = 0x2		±5		
			MEASx_LED_RGE = 0x3	-100	±5	+100	
LED Driver Compliance Interrupt Threshold		MEASx_LED_RGE = 0x0		120	148	180	mV
		MEASx_LED_RGE = 0x1		260	287	320	
		MEASx_LED_RGE = 0x2		395	425	460	
		MEASx_LED_RGE = 0x3		530	560	600	
POWER SUPPLY							
Power-Supply Voltage	V_{DD}			1.7	1.8	2.0	V
LED-Supply Voltage	V_{LED}	(Note 3)	Verified during PSRR Test	3.1		5.5	V

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Electrical Characteristics (continued)

(V_{DD_ANA} = 1.8V, V_{DD_DIG} = 1.8V, V_{LED} = 3.7V, T_A = +25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PPG Supply Current (I_{AVDD} + I_{DVDD})	I_{PPG}	Single-Channel, One Meas/Frame (Note 4a)	FR = 512fps		147	210	µA
			FR = 128fps		46		
			FR = 25fps		10.5		
		Single-Channel, Four Meas/Frame (Note 4a)	FR = 512fps		490	620	
			FR = 128fps		134		
			FR = 25fps		28		
		Dual-Channel, One Meas/Frame (Note 4b)	FR = 512fps		202	275	
			FR = 128fps		60		
			FR = 25fps		13		
		Dual-Channel, Four Meas/Frame (Note 4b)	FR = 512fps		720	900	
			FR = 128fps		190		
			FR = 25fps		40		
		Quad-Channel, One Meas/Frame (Note 4c)	FR = 512fps		316	410	
			FR = 128fps		88		
			FR = 25fps		19		
		Quad-Channel, Four Meas/Frame (Note 4c)	FR = 512fps		1160	1500	
			FR = 128fps		300		
			FR = 25fps		62		
V_{LED} Supply Current	I_{LED}	Single-Channel, One Meas/Frame (Note 4a)	FR = 512fps		850	950	µA
			FR = 128fps		220		
			FR = 25fps		43		
V_{DD} Current in Shutdown		T_A = +25°C			1	3	µA
V_{LED} Current in Shutdown		T_A = +25°C				0.1	µA
DIGITAL I/O CHARACTERISTICS							
Input Voltage Low	V_{IL}	I2C_SEL, CSB/ADDR, SDI/SDA, SCLK/SCL, TRIG				0.4	V
Input Voltage High	V_{IH}	I2C_SEL, CSB/ADDR, SDI/SDA, SCLK/SCL, TRIG		1.4			V
Input Hysteresis	V_{HYS}	I2C_SEL, CSB/ADDR, SDI/SDA, SCLK/SCL, TRIG			430		mV
Input Capacitance	C_{IN}	I2C_SEL, CSB/ADDR, SDI/SDA, SCLK/SCL, TRIG			10		pF
Input Leakage Current	I_{IN}	I2C_SEL, CSB/ADDR, SDI/SDA, SCLK/SCL, TRIG, T_A = +25°C, V_{IN} = 0V or 1.8V		-1	+0.01	+1	µA
Output-Low Voltage	V_{OL}	SDO, INT1, INT2, SDI/SDA (in I^2C mode), I_{SINK} = 4mA				0.4	V

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Electrical Characteristics (continued)

(V_{DD_ANA} = 1.8V, V_{DD_DIG} = 1.8V, V_{LED} = 3.7V, T_A = +25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output-High Voltage	V_{OH}	SDO, INT1, INT2, I_{SOURCE} = 4mA	V_{DD_DIG} - 0.4			V
Open-Drain Output-Low Voltage	V_{OL_OD}	INT1_OCFG = INT2_OCFG = 0x0, I_{SINK} = 4mA			0.4	V
SPI TIMING CHARACTERISTICS (Note 5)						
SCLK Frequency	f_{SCLK}				24	MHz
SCLK Period	t_{CP}		41.7			ns
SCLK Pulse-Width High	t_{CH}		18			ns
SCLK Pulse-Width Low	t_{CL}		18			ns
CSB Fall-to-SCLK Rise Setup Time	t_{CSS0}	Applies to 1st SCLK rising edge after CSB goes low	20			ns
CSB Fall-to-SCLK Rise Hold Time	t_{CSH0}	Applies to inactive rising edge preceding 1st rising edge	5			ns
Last SCLK Rise to CSB Rise	t_{CSH1}	Applies to last SCLK rising edge in a transaction	20			ns
Last SCLK Rise to Next CSB Fall	t_{CSF}	Applies to last SCLK rising edge to next CSB falling edge (new transaction)	60			ns
CSB Pulse-Width High	t_{CSPW}		40			ns
SDI to SCLK Rise Setup Time	t_{DS}		5			ns
SDI to SCLK Rise Hold Time	t_{DH}		5			ns
SCLK Fall to SDO Transition	t_{DOT}	C_{LOAD} = 30pF			15	ns
CSB Fall to SDO Enabled	t_{DOE}	C_{LOAD} = 0pF	10			ns
CSB Rise to SDO Hi-Z	t_{DOZ}	Disable time			5	ns
I²C TIMING CHARACTERISTICS (Note 5)						
I²C Write Address		CSB/ADDR = 0		E2		HEX
		CSB/ADDR = 1		E4		
I²C Read Address		CSB/ADDR = 0		E3		HEX
		CSB/ADDR = 1		E5		
Serial Clock Frequency	f_{SCL}		0		400	kHz
Bus Free-Time Between STOP and START Conditions	t_{BUF}		1.3			μs
Hold Time START and Repeat START Condition	t_{HD_STA}		0.6			μs
SCL Pulse-Width Low	t_{LOW}		1.3			μs
SCL Pulse-Width High	t_{HIGH}		0.6			μs

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Electrical Characteristics (continued)

(V_{DD_ANA} = 1.8V, V_{DD_DIG} = 1.8V, V_{LED} = 3.7V, T_A = +25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Setup Time for a Repeated START Condition	t_{SU_STA}		0.6			µs
Data Hold Time	t_{HD_DAT}		0		900	ns
Data Setup Time	t_{SU_DAT}		100			ns
Setup Time for STOP Condition	t_{SU_STO}		0.6			µs
Pulse-Width of Suppressed Spike	t_{SP}		0		50	ns
Bus Capacitance	CB				400	pF
SDA and SCL Receiving Rise Time	t_R		20 + 0.1CB		300	ns
SDA and SCL Receiving Fall Time	t_F		20 + 0.1CB		300	ns
SDA Transmitting Fall Time	t_{TF}		20 + 0.1CB		300	ns

Note 1: All devices are 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by Maxim Integrated's bench or proprietary automated test equipment (ATE) characterization.

Note 2: All register settings use the default values unless otherwise noted below or in specific EC conditions.

Key register settings are as follows:

MEASx_PPGy_ADC_RGE = 16µA (default)
MEASx_LED_RGE = 128mA (default)
MEASx_LED_SETLNG = 11.7µs (default)
PDm_BIAS = 0pF to 125pF (default)
FR_CLK_SEL = 32768kHz (default)
FR_CLK_DIV = 0x1000 (default)
f_{frame} = 100sps (default)

where:
# of measurements per frame: x = 1 to 20
# of PD inputs: m = 1 to 8
# of PPG channels: y = 1 to 4
# of LED Drivers: z = A, B

Definitions of terms:
1. Frame = All measurements made during a particular wake-up interval
2. Measurement = Ambient light corrected output

Register nomenclature:
1. ADC_RGE = Measurement full-scale range as defined by MEASx_PPGy_ADC_RGE[1;0]
2. TINT = ADC integration time as defined by MEASx_TINT[1:0]
3. PDm_BIAS = the photodiode bias setting
4. LED_RGE = Measurement full-scale range of the LED driver in the MEASx_LED_RGE register
5. DRVz_PA = Measurement LED driver DAC code in the MEASx_DRVz_PA register
6. LED_SETLNG = Measurement LED settling time in the MEASx_LED_SETLNG registers

Note 3: V_{LED} should be set greater than the LED driver minimum output voltage + LED forward voltage.

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Note 4: FR = PPG Frame Rate
a. MEASx_DRVz_PA = 0x7F, REF_CLK_SEL = 1, PPG1_PWRDN = 0, PPG2_PWRDN = 1, PPG3_PWRDN = 1, PPG4_PWRDN = 1
b. MEASx_DRVz_PA = 0x7F, REF_CLK_SEL = 1, PPG1_PWRDN = 0, PPG2_PWRDN = 0, PPG3_PWRDN = 1, PPG4_PWRDN = 1
c. MEASx_DRVz_PA = 0x7F, REF_CLK_SEL = 1, PPG1_PWRDN = 0, PPG2_PWRDN = 0, PPG3_PWRDN = 0, PPG4_PWRDN = 0

Note 5: For design guidance only. Not production tested.

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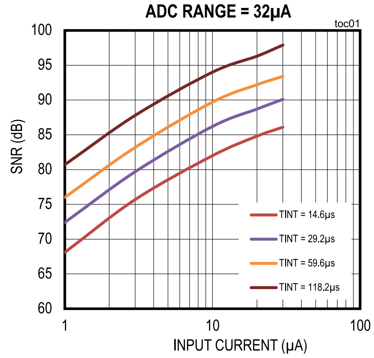
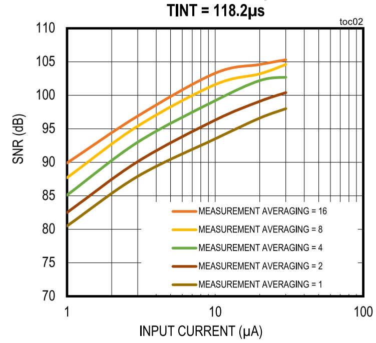
Typical Operating Characteristics

(V_{DD_ANA} = V_{DD_DIG} = 1.8V, V_{LED} = 5.0V, GND = PGND = 0V, T_A = +25°C, unless otherwise noted.)

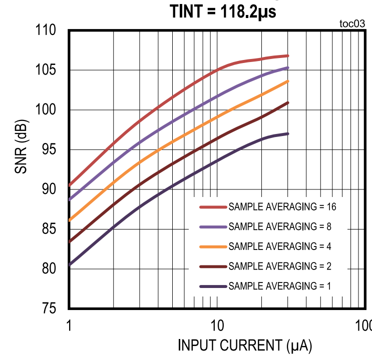
SNR vs. INPUT CURRENT
ADC RANGE = 32µA



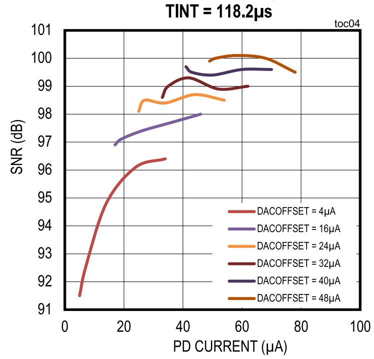
SNR vs. INPUT CURRENT
ADC RANGE = 32µA
TINT = 118.2µs



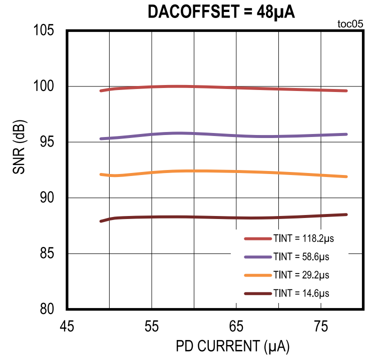
SNR vs. INPUT CURRENT
ADC RANGE = 32µA
TINT = 118.2µs



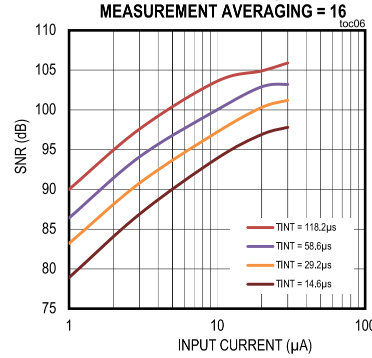
SNR vs. PD CURRENT
ADC RANGE = 32µA
TINT = 118.2µs



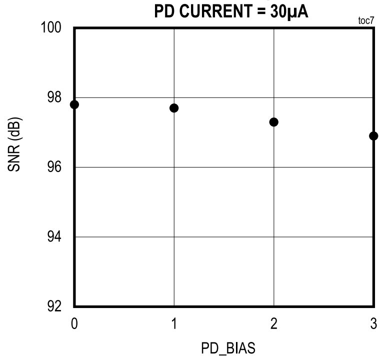
SNR vs. PD CURRENT
DACOFFSET = 48µA



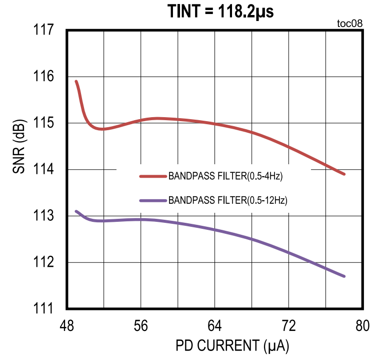
SNR vs. INPUT CURRENT
ADC RANGE = 32µA
MEASUREMENT AVERAGING = 16



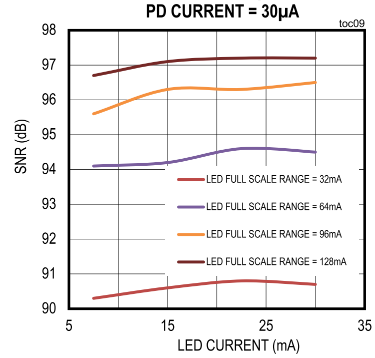
SNR vs. PD_BIAS
TINT = 118.2µs
PD CURRENT = 30µA



SNR vs. PD CURRENT
DACOFFSET = 48µA
TINT = 118.2µs



SNR vs. LED FULL SCALE RANGE
TINT = 118.2µs
PD CURRENT = 30µA



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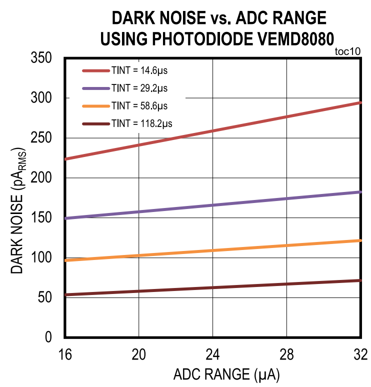
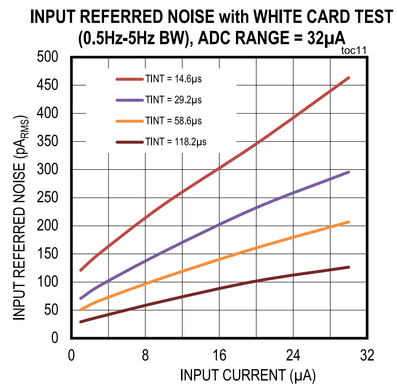
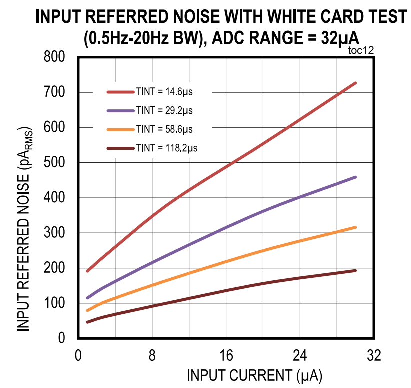
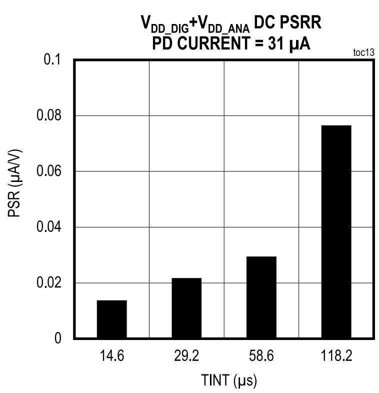
Typical Operating Characteristics (continued)

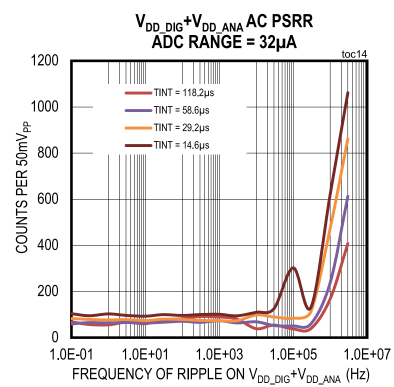
(V_{DD_ANA} = V_{DD_DIG} = 1.8V, V_{LED} = 5.0V, GND = PGND = 0V, T_A = +25°C, unless otherwise noted.)

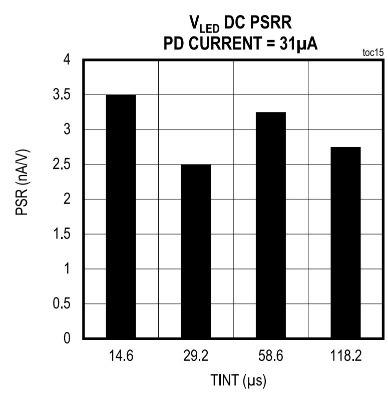


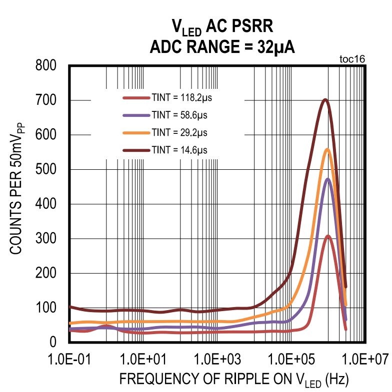


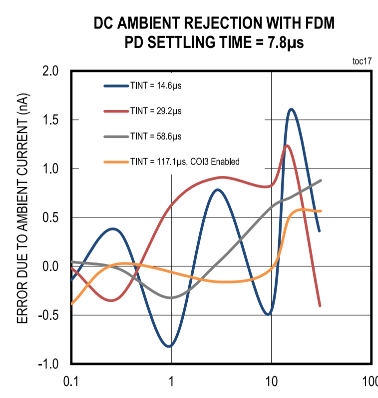


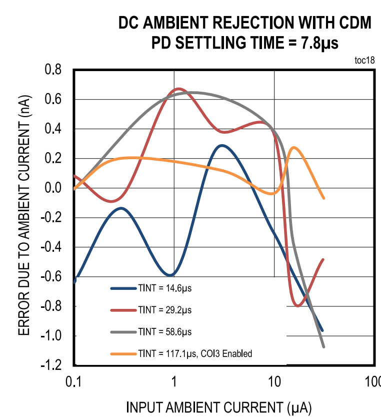












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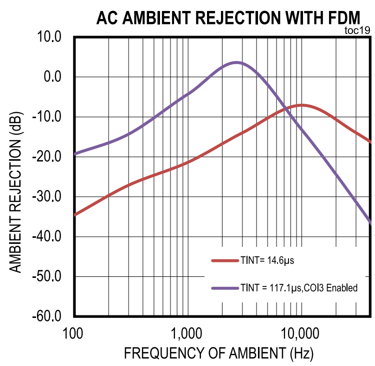
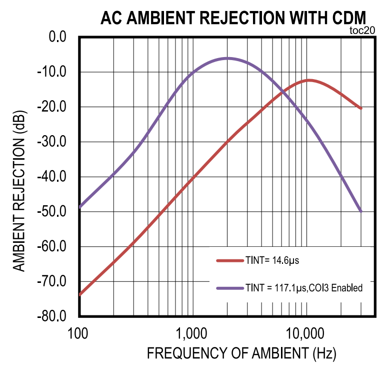
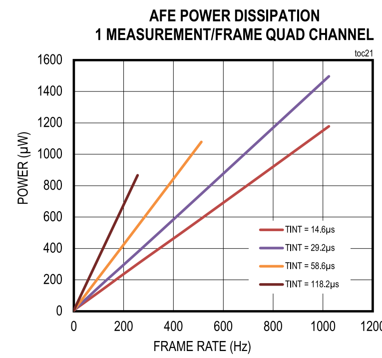
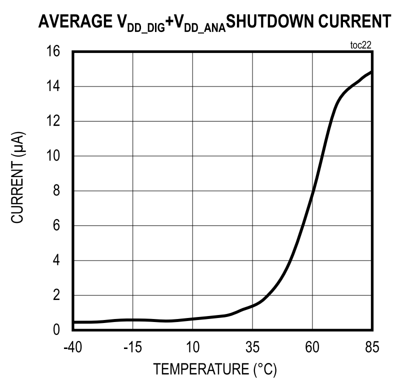
Typical Operating Characteristics (continued)

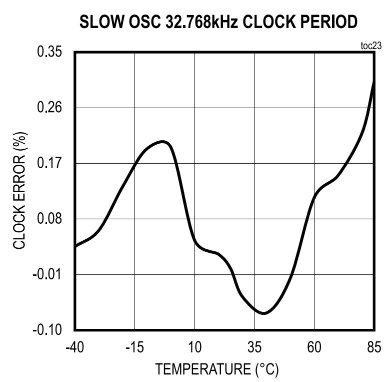
(V_{DD_ANA} = V_{DD_DIG} = 1.8V, V_{LED} = 5.0V, GND = PGND = 0V, T_A = +25°C, unless otherwise noted.)











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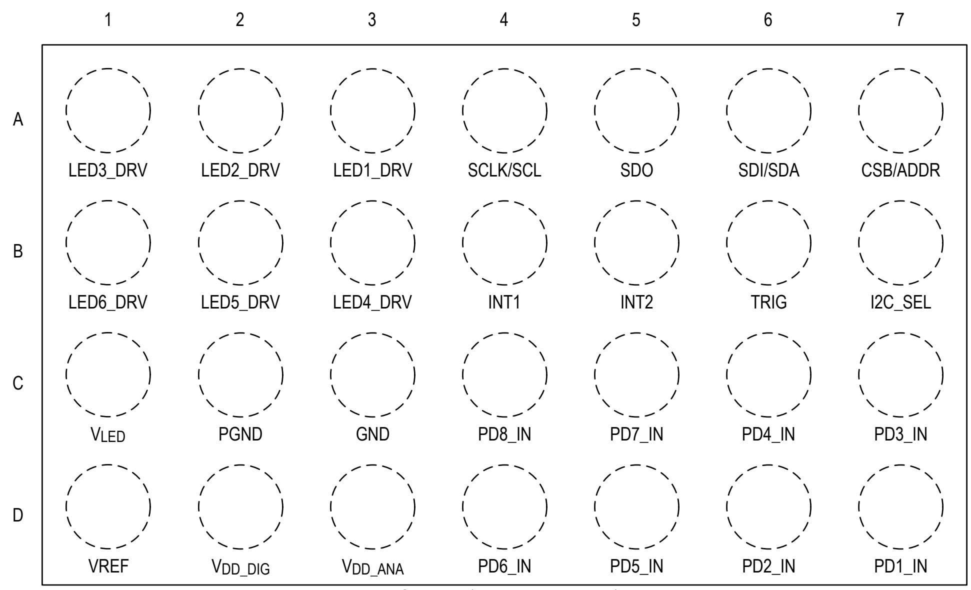
Pin Configuration

MAX86177



TOP VIEW (Bumps Facing Down)
WLP 7x4, 0.4mm Pitch

Pin Description

PIN	NAME	FUNCTION
POWER		
C2	PGND	LED Power Return. Connect to PCB Ground. For more information, see the *PCB Layout Guidelines* section.
C1	V_{LED}	LED Power-Supply Input. In a configuration with more than one LED supply, connect V_{LED} to the highest LED supply voltage. Bypass with a 10µF capacitor to PGND.
D2	V_{DD_DIG}	Digital Power Supply. Connect to an externally regulated supply. Bypass to GND with a 0.1µF and 10µF capacitor as close to the bump as possible. It can be shared with V_{DD_ANA}.
C3	GND	Main Power Supply Return. Connect to PCB Ground. For more information, see the *PCB Layout Guidelines* section.
D3	V_{DD_ANA}	Analog Power Supply. Connect to an externally regulated supply. Bypass to GND with a 0.1µF and 10µF capacitor as close to the bump as possible. It can be shared with V_{DD_DIG}.
CONTROL INTERFACE		
A4	SCLK/SCL	SPI Clock/I^2C Clock
A5	SDO	SPI Data Output. Tie to GND or V_{DD_DIG} when this pin is not used.
A6	SDI/SDA	SPI Data Input/I^2C Data
A7	CSB/ADDR	SPI Chip Select Input/I^2C Device Address Selector
B4	INT1	Interrupt 1 Output. When not used, it may be left unconnected.
B5	INT2	Interrupt 2 Output. When not used, it may be left unconnected.
B6	TRIG	External Clock or Start of Conversion Trigger Input. Tie to GND or VDD_DIG when this pin is not used.

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Pin Description (continued)

PIN	NAME	FUNCTION
B7	I2C_SEL	Input to Select I^2C or SPI Mode. When I2C_SEL is pulled high, the interface operates in I^2C mode. When I2C_SEL is pulled low, the interface operates in SPI mode.
OPTICAL PINS		
D7	PD1_IN	Photodiode Cathode Input. When not used, tie to GND.
D6	PD2_IN	Photodiode Cathode Input. When not used, tie to GND.
C7	PD3_IN	Photodiode Cathode Input. When not used, tie to GND.
C6	PD4_IN	Photodiode Cathode Input. When not used, tie to GND.
D5	PD5_IN	Photodiode Cathode Input. When not used, tie to GND.
D4	PD6_IN	Photodiode Cathode Input. When not used, tie to GND.
C5	PD7_IN	Photodiode Cathode Input. When not used, tie to GND.
C4	PD8_IN	Photodiode Cathode Input. When not used, tie to GND.
A3	LED1_DRV	LED Output Pin 1. Driven from LED driver A and B. Connect the LED cathode to LED1_DRV and its anode to the V_{LED} supply. When not used, it may be left unconnected.
A2	LED2_DRV	LED Output Pin 2. Driven from LED driver A and B. Connect the LED cathode to LED2_DRV and its anode to the V_{LED} supply. When not used, it may be left unconnected.
A1	LED3_DRV	LED Output Pin 3. Driven from LED driver A and B. Connect the LED cathode to LED3_DRV and its anode to the V_{LED} supply. When not used, it may be left unconnected.
B3	LED4_DRV	LED Output Pin 4. Driven from LED driver A and B. Connect the LED cathode to LED4_DRV and its anode to the V_{LED} supply. When not used, it may be left unconnected.
B2	LED5_DRV	LED Output Pin 5. Driven from LED driver A and B. Connect the LED cathode to LED5_DRV and its anode to the V_{LED} supply. When not used, it may be left unconnected.
B1	LED6_DRV	LED Output Pin 6. Driven from LED driver A and B. Connect the LED cathode to LED6_DRV and its anode to the V_{LED} supply. When not used, it may be left unconnected.
REFERENCE		
D1	VREF	Internal Reference Decoupling Point. Bypass with a 1μF capacitor to PCB Ground.

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Detailed Description

The MAX86177 is a complete integrated optical data-acquisition system ideal for various applications, including optical pulse-oximetry and heart-rate detection applications. It is designed for the demanding requirements of mobile and wearable devices and requires minimal external hardware components for integration into a wearable device. It includes high-resolution optical readout signal processing channels with robust ambient light cancellation and high-current LED driver digital-to-analog converters (DACs) to form a complete optical readout signal chain.

The MAX86177 is fully adjustable through software registers, and the digital output data is stored in a 512-word FIFO. The FIFO allows the MAX86177 to be connected to a microcontroller or a processor on a shared bus, I^2C, or SPI depending on hardware selection on the I2C_SEL pin. It operates in a fully autonomous mode for low-power battery applications.

The MAX86177 incorporates quad optical readout channels that operate simultaneously. The MAX86177 has two LED drivers. With the built-in MUX and control logic on the chip, the MAX86177 can support up to 6 LEDs and 8 PDs. It is well-suited for a wide variety of optical sensing applications.

The MAX86177 operates on a 1.8V main supply voltage, with a separate 3.1V to 5.5V LED driver power supply. This device has flexible exposure, timing, and shutdown configurations as well as control of individual blocks so that an optimized measurement can be made at minimum power levels.

Optical Transmitter Overview

The MAX86177 has two independent precision LED current drivers that are muxed to 6 LED driver pins. The two LED current DACs modulate LED pulses for a variety of optical measurements. The two LED current DACs have an 8-bit dynamic range with four programmable full-scale range settings of 32mA, 64mA, 96mA, and 128mA. The two current drivers, DRVA and DRVB, are connected to the 6 LED driver pins through internal multiplexers. The MEASx Selects (x = 1 to 20) registers (see the Register Map) define how each LED driver is connected for that particular measurement. Thus, the configuration of the LED drivers can be uniquely set for each measurement. Each measurement can use one or two LED drivers allowing for any of the 6 LED driver pins to sink up to 128mA or 256mA.

Note: MEASx Selects (x = 1 to 20) are at register addresses 0x17, 0x22, 0x2D, 0x38, 0x43, 0x4E, 0x59, 0x64, 0x6F, 0x7A, 0x85, 0x90, 0x9B, 0xA6, 0xB1, 0xBC, 0xC7, 0xD2, 0xDD, and 0xE8.

The two LED current DAC/Mux combinations are low-dropout current sources allowing for low-noise, power-supply independent LED currents to be sourced at the lowest supply voltage possible; thus, minimizing LED power consumption. The four full-scale range settings are provided to allow for a trade-off between LED driver noise, V_{LED} power supply rejection, and dropout voltage on the pins. Table 1 shows this trade-off.

Table 1. LED Driver Full-Scale Range Trade-Off

FULL-SCALE RANGE LED_RGE (mA)	LED DAC RESOLUTION (mA)	RECOMMENDED MINIMUM V_{LED_DRV} (mV)	PEAK SNR* (dB)
32	0.125	0.20	112.5
64	0.250	0.35	117
96	0.375	0.50	118
128	0.500	0.60	118

*Peak SNR is measured with TINT = 118.2us, Burst Averaging = 16x, FR = 100sps, ADC_RGE = 32uA, DACOFF = 48uA, COI2 decimation filter, PD current = 49uA and 0.5Hz-4Hz external filter

Optical Receiver Overview

The optical path in the MAX86177 is composed of a front-end photodiode (PD) biasing circuit with an analog ambient-light cancellation (ALC) sample-and-hold circuit that nulls the ambient light photodiode current at the input of the ADC. This front-end biasing circuit is followed by a current integrating, continuous-time sigma-delta ADC with a proprietary discrete time filter. This discrete time filter uses multiple darks and exposure optical samples to generate an accurate 20-bit effective exposure output signal with excellent low and high-frequency ambient-light cancellation.

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This combination of analog circuits and back-end digital filtering helps reduce shifts due to ambient light variations. An exposure signal varies less than 0.5nA, on a homogenous photodiode with ambient light variations from 0μA to over 30μA, or over 95dB of DC rejection, all but eliminating issues in high-intensity outdoor lighting conditions. This level of ambient-light cancellation is maintained under indoor lighting conditions with over 70dB of rejection at line (mains) rate, 100Hz and 120Hz. In addition, back-end filtering also suppresses the high rate of modulation of newer compact fluorescent and LED lighting as well.

The MAX86177 incorporates quad optical-signal paths and has 8 PD input pins. Each photodiode is connected to one of the four PPG signal paths or is left open by configuring MEASx_PDm_SEL (x = 1 to 20, m = 1 to 8) as needed, so that input to the four PPG ADCs is received simultaneously. For applications requiring less than four optical signal paths to be active (e.g., lower power consumption) any of the four channels can be powered down by setting PPGy_PWRDN (y = 1 to 8) to 1 in register 0x0D. See Figure 1.

Note: MEASx_PDm_SEL[2:0](x = 1 to 20, m = 1 to 8) are at register addresses 0x1F, 0x20, 0x21, 0x2A, 0x2B, 0x2C, 0x35, 0x36, 0x37, 0x40, 0x41, 0x42, 0x4B, 0x4C, 0x4D, 0x56, 0x57, 0x58, 0x61, 0x62, 0x63, 0x6C, 0x6D, 0x6E, 0x77, 0x78, 0x79, 0x82, 0x83, 0x84, 0x8D, 0x8E, 0x8F, 0x98, 0x99, 0x9A, 0xA3, 0xA4, 0xA5, 0xAE, 0xAF, 0xB0, 0xB9, 0xBA, 0xBB, 0xC4, 0xC5, 0xC6, 0xCF, 0xD0, 0xD1, 0xDA, 0xDB, 0xDC, 0xE5, 0xE6, and 0xE7.

Each optical signal path supports two full-scale range settings of 16μA and 32μA set in the MEASx_PPGy_ADC_RGE (x = 1 to 20, y = 1 to 4) field. Also supported are four options of integration times, which effectively modulate the optical channel bandwidth, allowing for a trade-off between light energy consumed and PPG signal quality. Each optical signal path also incorporates a 4-bit offset DAC for extending the optical dynamic range. This is especially useful under certain conditions that occur when attempting to limit the exposure LED current level (for example, red shift in SpO_2). The optical paths also support multiple photodiodes and LED settling times in order to support flexible multiparameter measurements for different types of photodiode/LED wavelength combinations.

Note: MEASx_PPGy_ADC_RGE[0] (x = 1 to 20, y = 1 to 4) are at register addresses 0x19, 0x24, 0x2F, 0x3A, 0x45, 0x50,0x5B, 0x66, 0x71, 0x7C, 0x87, 0x92, 0x9D, 0xA8, 0xB3, 0xBE, 0xC9, 0xD4, 0xDF, and 0xEA.

Most significantly, each MAX86177 signal path supports up to twenty unique combinations of the above configurations to be defined and easily enabled and disabled as needed. The goal is to allow a single optical AFE to support multiple optical measurements in a compact, energy efficient design.

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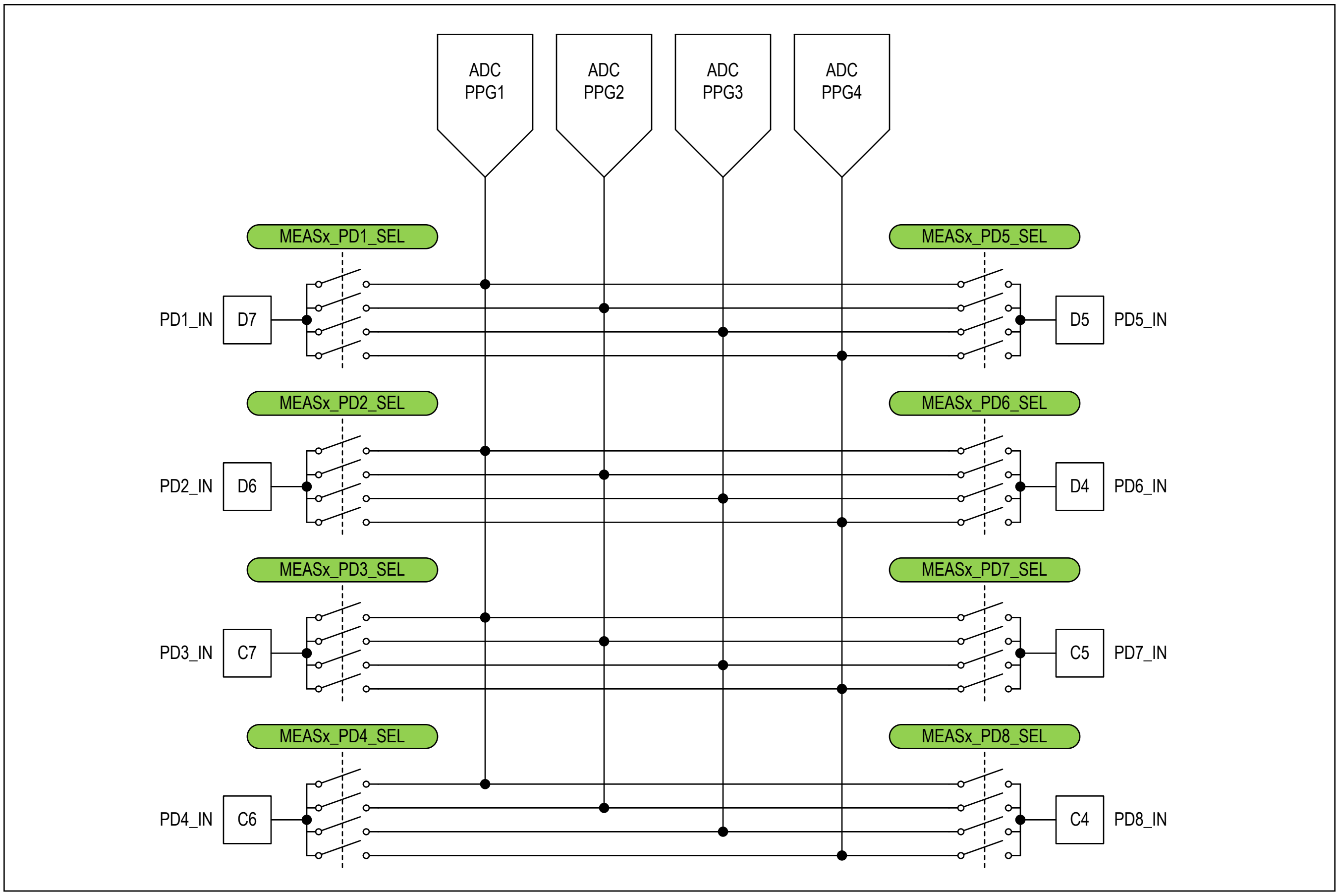

Figure 1. On-Chip Mux for the PDm_IN Pins

Photodiode Biasing

The MAX86177 provides three photodiode biasing options to support a large photodiode-capacitance range. Each photodiode input can have a separate bias setting, allowing different photodiodes to be accommodated. The PDm_BIAS[1:0] (m = 1 to 8) values in registers 0x15 and 0x16 adjust the PDm_IN bias point impedance to ensure that the photodiode settles rapidly enough to support the signal timing.

Table 2. PD BIAS Values Based on Photodiode Capacitance

PDm_BIAS[1:0]	PHOTODIODE CAPACITANCE (pF)
0x0	Do not use
0x1	0 to 125(POR default)
0x2	125 to 250
0x3	250 to 500

The PDm_BIAS value impacts the dark current noise of the MAX86177. The relationship between PDm_BIAS and noise with increasing photodiode capacitance is shown in TOC07 in the *Typical Operating Characteristics* section. Because of the increased noise with PDm_BIAS setting, the lowest recommended PDm_BIAS value should be used for any given photodiode capacitance.

Measurement Configuration and Timing

A measurement is essentially one combination of LED(s) and PD(s) that results in an optical measurement at one time slot on all enabled ADC channel(s). The MAX86177 supports 20 individual measurements, each of which can be

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configured independently. Each measurement can be configured in the MEASx Setup registers (x = 1 to 20). These registers help set up a varied set of parameters as outlined by the list below.

These parameters can be configured on a per measurement basis:

- Connections of each of the two LED drivers to one of the 6 LEDn_DRV pins
- Connection of each of the four channels to each of the 8 possible PDs
- LED driver range and drive currents
- LED settling time
- PD settling time
- Number of averages of each measurement
- Ambient-Light Cancellation scheme (CDM or FDM)
- Decimation filter selection (COI or SINC3)
- ADC integration time
- ADC range for each channel
- DAC offset for each channel
- Low-noise DAC selection

The MAX86177 optical controller is capable of being configured to make a variety of measurements.

The controller can be configured to pulse one or two LED drivers sequentially to make measurements at multiple wavelengths as is done in pulse oximetry measurements or simultaneously to drive multiple LEDs as is done with heart rate measurements on the wrist.

Each LED exposure is ambient light-compensated (see the *Ambient-Light Cancellation* section). The controller is also configurable to measure the direct ambient level for every exposure. The direct ambient measurement can be used to adjust the LED-drive level to compensate for increased noise levels when high interfering ambient signals are present.

The optical timing diagrams in Figure 2, Figure 3, Figure 4, Figure 5, Figure 6, Figure 7, and Figure 8 show several possible measurement configurations.

Figure 2 shows one measurement with only one of the LEDs active. No averaging is used. As shown in Figure 2, only one LED is pulsing during the exposure time. In this mode, each driver pulse results in a single optical sampled value for each PD input to be stored in the FIFO. In a single-channel configuration, only one sample is stored in the FIFO for each driver pulse but for a quad-channel configuration, four samples are stored in the FIFO for each driver pulse.

This timing mode in Figure 2 is used when heart rate is being measured with a single LED1.

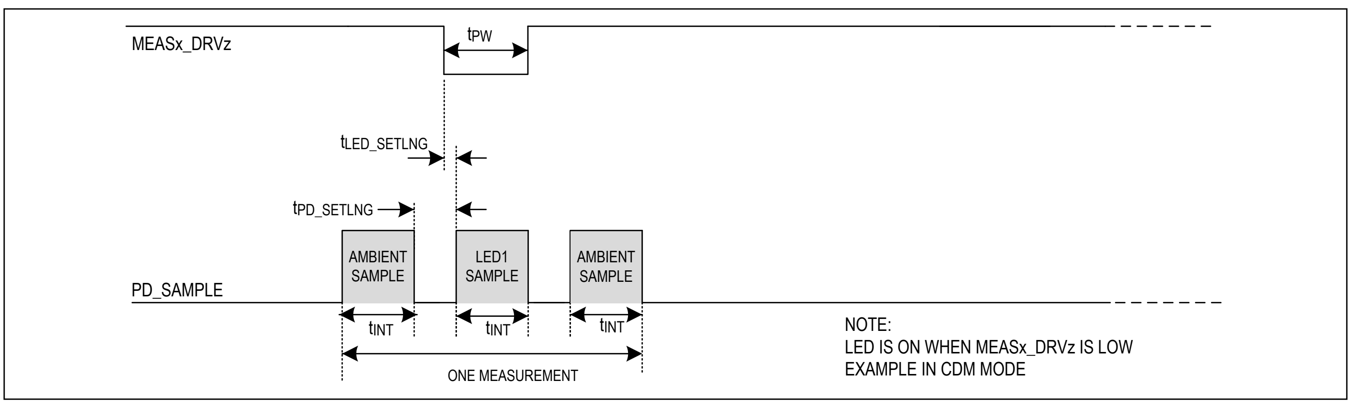

Figure 2. Measurement With One LED On

Frame

A frame is a combination of measurements from 1 (min) to 20 (max) by configuring MEASx_EN[0] (x = 1 to 20, at registers 0x11, 0x12, and 0x13). The frame rate defines how frequently a frame is repeated or frames per second (fps). The frame rate is defined by the FR_CLK_DIV[14:0] (at registers 0x0B and 0x0C) or the active edge of TRIG input depending on SYNC_MODE[1:0](register 0x0D).

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Any combination of measurements can be enabled, but measurements are done in a numerical order inside a frame. For example, it is valid to enable MEAS1, MEAS2, and MEAS5 while MEAS3 and MEAS4 are skipped. If a measurement of direct ambient is configured, then this measurement can be configured as any measurement in the frame.

The MAX86177 operates in a dynamic power-down mode, always powering down between frames; thus, minimizing power consumption. For more details on the power consumption at various frame rates, see the *Electrical Characteristics* table and *Typical Operating Characteristics* section.

Frame with One Measurement Only

Figure 3 shows the timing diagram for one measurement in each frame. This measurement has only one LED driver pulsing and configured in CDM mode (for more details, see the *Ambient-Light Cancellation* section).

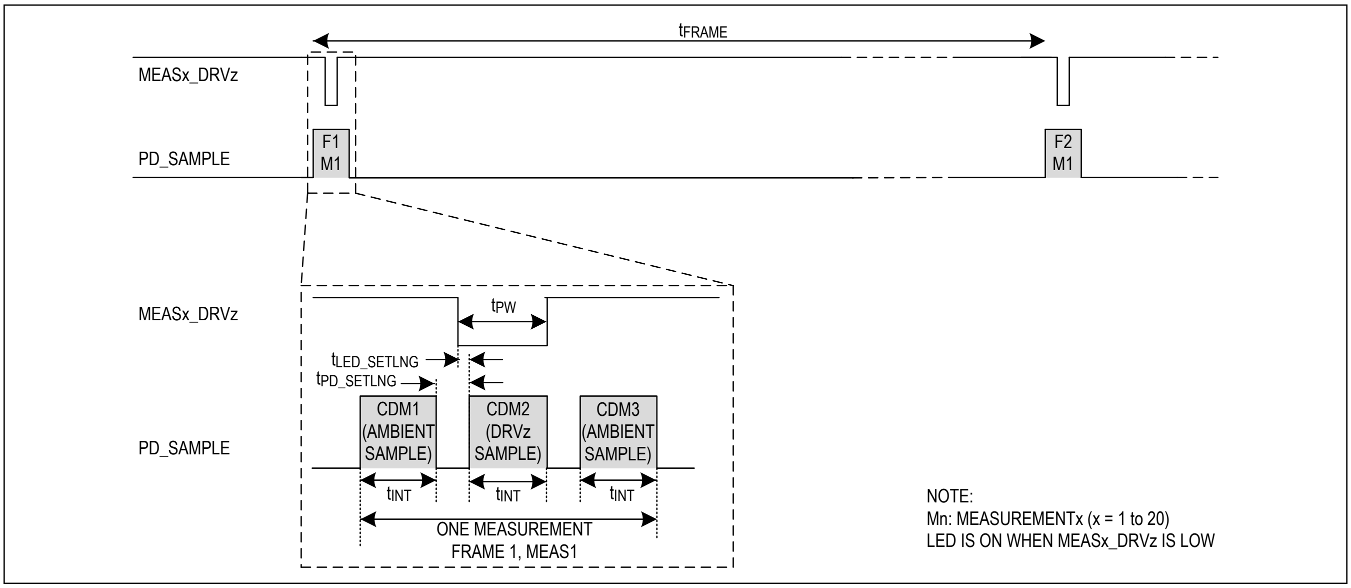

Figure 3. Frame with One Measurement

Frame with All Twenty Measurements Enabled

Figure 4 shows timing for twenty measurements in each frame. MEAS3 is configured as CDM (for more details, see the *Ambient-Light Cancellation* section) and one of MEAS3_DRVz (z = A, B) at register address 0x2D is sinking current.

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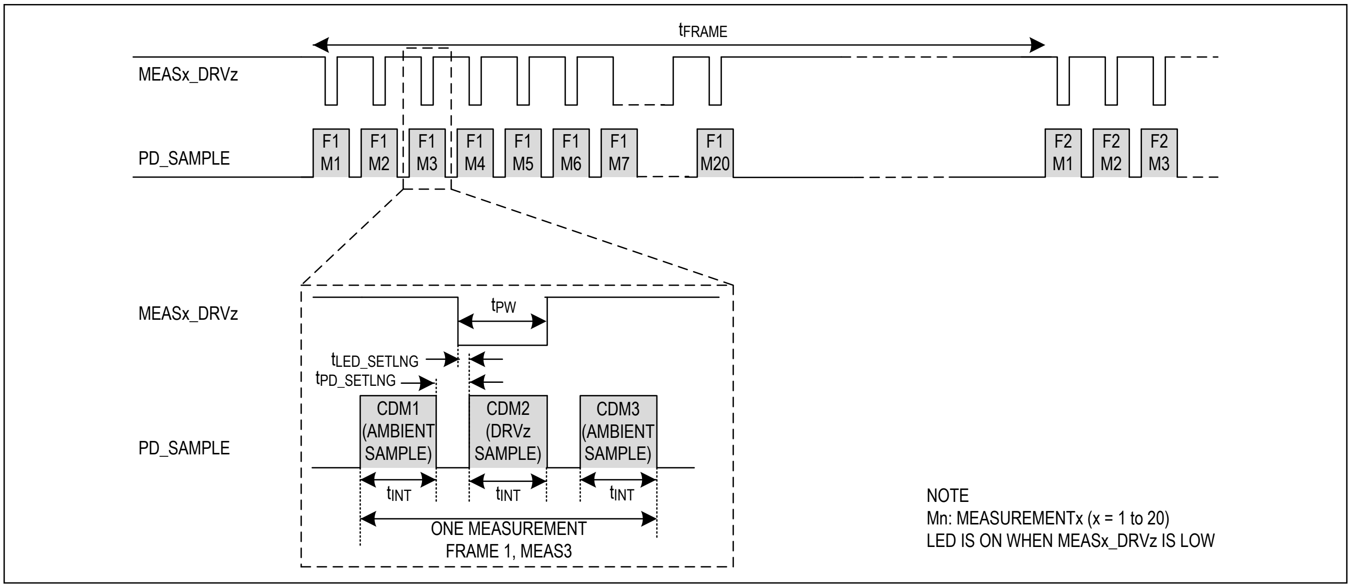

Figure 4. Frame with Twenty Measurements

Note that if using the internal frame trigger (default), changing the frame rate (registers FR Clock Divider MSB[7:0] and FR Clock Divider LSB[7:0]) restart the finite state machine (FSM), which forces the start of a new frame of measurements. Therefore, a glitch in the frame rate can be expected between the frames measured just before and just after the registered FR Clock Divider is written. The restart of the FSM machine also happens when other PPG configuration settings (like MEASx_PPGn_ADC_RGE or MEASx_AVER) are modified. It must be noted that modifying the LED current setting (MEASx_DRVm_PA) does not restart the FSM, allowing for a control loop (LED current vs. Photodiode input current) with no discontinuities in the frame rate. This restart of the FSM does not disrupt the PPG frame rate if using the external frame trigger (SYNC_MODE = 0x1), so if a consistent frame rate is required, using an external frame trigger is the ideal setup. If an external trigger is not available, writing to the PPG configuration registers just before the new frame starts would minimize the frame rate glitch, but the timing may be complicated as to when to start the write, how long the write takes, etc. To ensure that full frames are pushed to the FIFO, write to the PPG configuration registers only after a complete frame is ready (i.e., after a FRAME_READY interrupt or an A_FULL interrupt, where FIFO_A_FULL is in multiples of full frames) and the FIFO is read; otherwise, the FSM restarts before all measurements in the frame have been completed, thus leaving the FIFO with a partial frame. This is the case even when using an external frame trigger. Additionally, when using the internal trigger and multiple PPG configuration registers are written, flush the FIFO after the last register write because if the writes are slow, unwanted measurements may be pushed to the FIFO, and these are cleared by the flush. Optionally, setting the self-clearing bit FIFO_MARK pushes a special tag (code 0xFFFFFE) to the FIFO. This feature can be used for differentiating the data in the FIFO before and after the tag and potentially highlighting when the frame rate or PPG configuration is changed.

On-Chip Averaging

The MAX86177 incorporates both measurement (burst) average and sample (decimation) average on the chip. The measurement average applies to one measurement where a given number of LED bursts are fired. Sample average is frame-based where a given number of measurements from successive frames are averaged, resulting in a lower FIFO data rate.

Measurement Averaging

Figure 5 shows timing for twenty measurements in each frame with MEAS3 configured as CDM and on-chip average of 2. The result of MEAS3 measurement in each frame has only one FIFO data per enabled PPG channel pushed into FIFO. This FIFO data is the averaged data of N1 and N2 where N1 = N1CDM2 - (N1CDM1 + N1CMD3) / 2 and N2 = N2CDM2 - (N1CDM3 + N2CDM3) / 2. The averaging factor is configured by MEASx_AVER[2:0] (x = 1 to 20).

Note: MEASx_AVER[2:0] (x = 1 to 20) are at registers 0x18, 0x23, 0x2E, 0x39, 0x44, 0x4F, 0x5A, 0x65, 0x70, 0x7B,

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0x86, 0x91, 0x9C, 0xA7, 0xB2, 0xBD, 0xC8, 0xD3, 0xDE, and 0xE9.

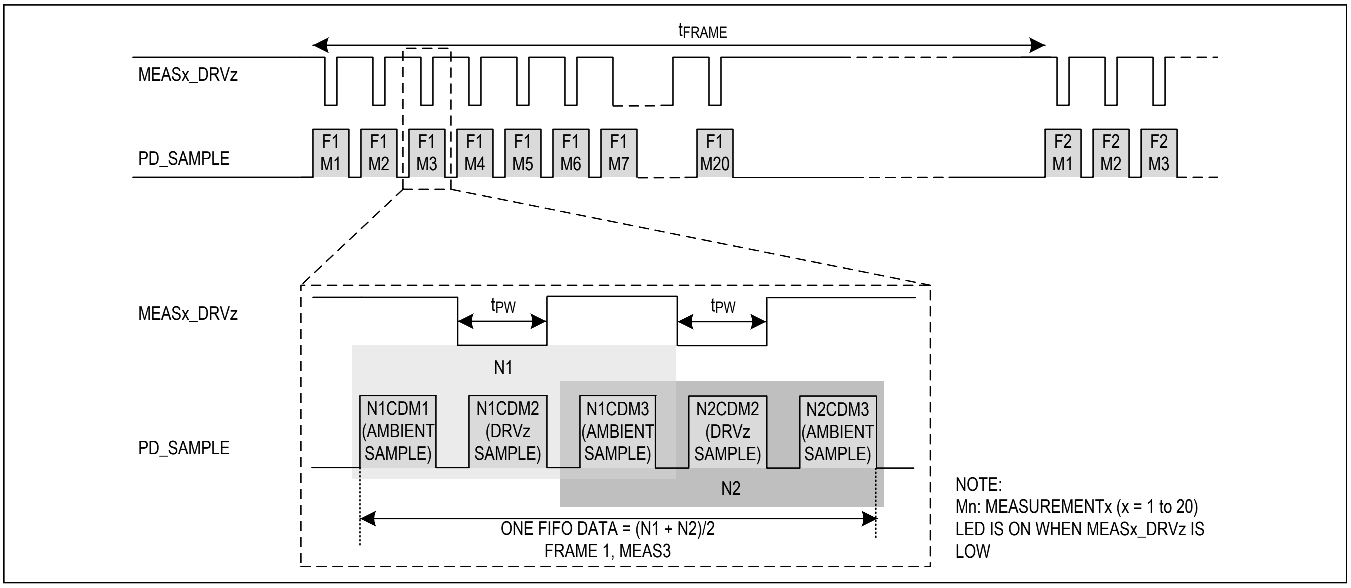

Figure 5. Measurement Averaging

Sample Averaging

Figure 6 shows timing with sample averaging of 2 in each frame (SMP_AVE[2:0] at register address 0x14 is set to 0x01). Each individual measurement in frame 1 (F1) and frame 2 (F2) is averaged, and the result is saved in FIFO as a single sample for each measurement. For example, the sample in FIFO for measurement 1 is (F1M1 + F2M1) / 2. Each enable measurement within every frame has its ambient sample(s) and exposure sample as detailed in Figure 2. When using sample averaging, the data output rate is reduced by the frame rate/sample averaging factor. Therefore, sample averaging also limits the bandwidth of the PPG data and helps improve the signal-to-noise ratio (SNR) of the AFE.

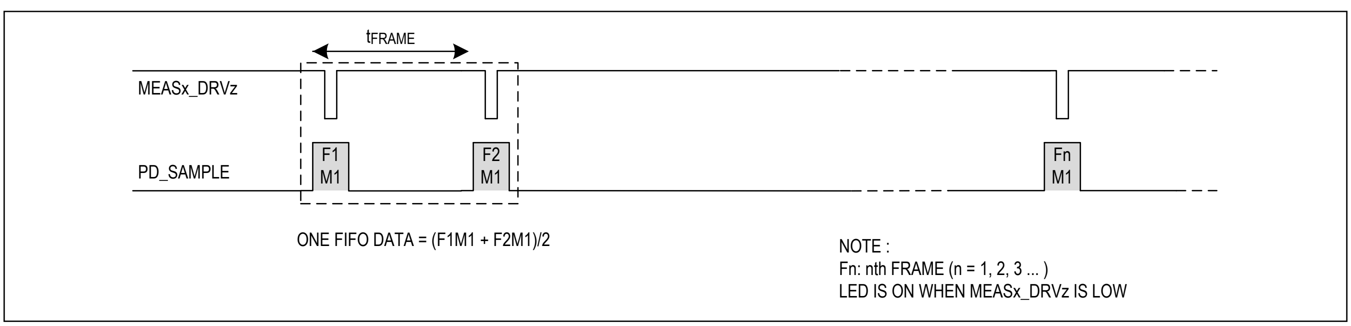

Figure 6. Sample Averaging

Ambient-Light Cancellation

The MAX86177 implements ambient-light cancellation in two steps, a coarse cancellation and a fine cancellation. Each MEASx gets its own ambient light cancellation. The coarse cancellation is in the analog domain. It is enabled by default and can be disabled by setting the ALC_DISABLE bit. The fine cancellation is a digital cancellation scheme and is configured as either central difference method (CDM) or forward difference method (FDM) (MEASx_FILT_SEL bit).

The ALC is an analog sample and hold circuit, which can cancel up to 200μA of DC photodiode current. Any drift or residual from ALC is cancelled by CDM/FDM cancellation.

The CDM is comprised of three ADC conversions which has two ambient and one exposure samples. The optical timing

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diagram in Figure 7 shows one measurement with only one LED driver active in CDM mode. No measurement averaging is used.

As shown in Figure 7, only MEASx_DRVA is pulsing during the exposure time. This timing mode is used when heart rate is being measured with a single LED. In this mode, three conversions (CDM1, CDM2, and CDM3) occur. The two ambient samples, CDM1 and CDM3, are used for ambient-light cancellation. The ambient-light cancelled result (CDM2 - (CDM1 + CDM3)/2) appears in the FIFO as a single optical-sampled value after ambient cancellation.

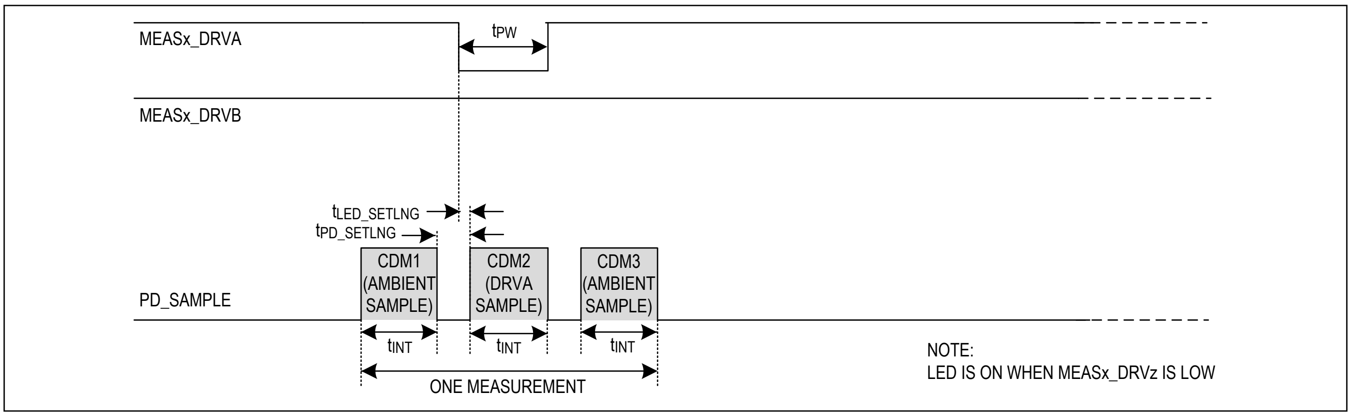

Figure 7. Central Difference Method (CDM)

The FDM is comprised of two ADC conversions which has only one ambient and one exposure sample. The optical timing diagram in Figure 8 shows DRVB pulsing with forward difference method mode enabled. In this mode, the two conversions (FDM1 and FDM2) occur.

The ambient sample FDM1 is only used for ambient cancellation. The ambient-light cancelled result (FDM2 - FDM1) appears in the FIFO as a single optical-sampled value after ambient cancellation.

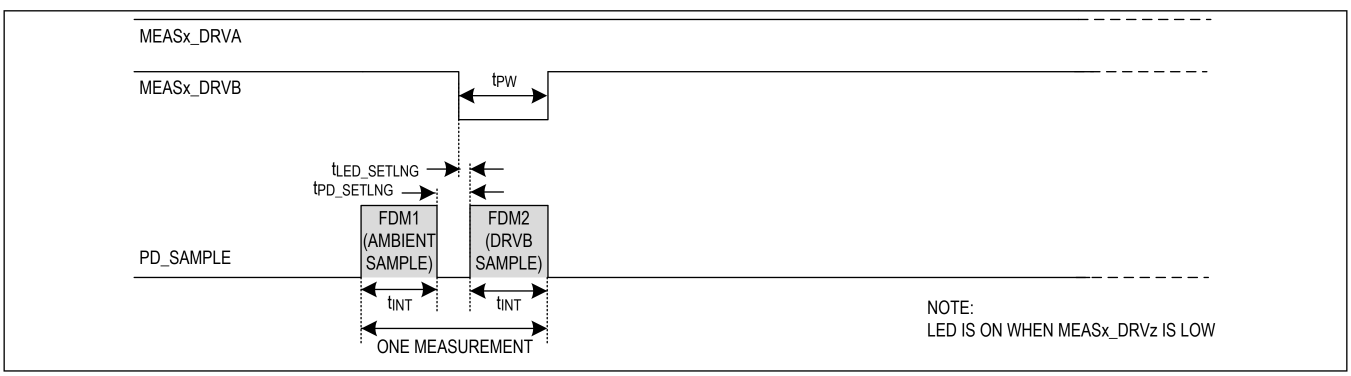

Figure 8. Forward Difference Method (FDM)

The ambient and exposure samples are used for digital cancellation of any residual error (from ALC) or drift (in ambient signal). The final computed value is the effective exposure signal, which is stored in the FIFO. See Figure 7 for the timing diagram of CDM and Figure 8 for the timing diagram of FDM.

Note: Ambient-Light cancellation in low-frequency ambient light improves when using a burst average by setting MEASx_AVER ≥ 0x2.

ADC Decimation Filter

Users can select a second-order decimation filter (COI2), a third-order decimation filter (COI3), or SINC3 decimation filter. The MAX86177 by default uses a second-order cascade of integrators (COI2) decimation filter. The third-order

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filter (COI3) provides excellent quantization, but only a 20dB/dec roll-off at higher frequencies. The COI2 has a narrower bandwidth as compared to the COI3, which improves the PPG SNR by about 1dB to 2dB. The SINC3 filter has a better rollover (60dB/dec), and, therefore, provides higher AC ambient-light cancellation at high frequencies and V_{LED} power-supply rejection. The SINC3 filter generates poor quantization performance and is, thus, only available on the longest integration time, MEASx_TINT[1:0] = 0x3. The SINC3 is selected for each measurement individually by setting MEASx_SINC3_SEL to 1. Both SINC3 and COI2 can only be used with the longest integration time (MEASx_TINT = 0x3).

Note: MEASx_TINT[1:0] (x = 1 to 20) are at registers 0x18, 0x23, 0x2E, 0x39, 0x44, 0x4F, 0x5A, 0x65, 0x70, 0x7B, 0x86, 0x91, 0x9C, 0xA7, 0xB2, 0xBD, 0xC8, 0xD3, 0xDE, 0xE9 and MEASx_SINC3_SEL[0] (x = 1 to 20) are at registers 0x19, 0x24, 0x2F, 0x3A, 0x45. 0x50, 0x5B, 0x66, 0x71, 0x7C, 0x87, 0x92, 0x9D, 0xA8, 0xB3, 0xBE, 0xC9, 0xD4, 0xDF, and 0xEA.

Table 3 shows the configuration for different ADC decimation filters. Combinations of the three parameters out of this table are not suggested.

Table 3. Configuration for ADC Decimation Filter

MEASx_SINC3_SEL[0]	MEASx_FILT2_SEL[0]	MEASx_TINT[1:0]	DECIMATION FILTER
0	0	All TINTs	COI3
0	1	TINT = 0x3	COI2 (Default)
1	0 or 1	TINT = 0x3	SINC3

See Figure 9 for the transfer function of different decimation filters.

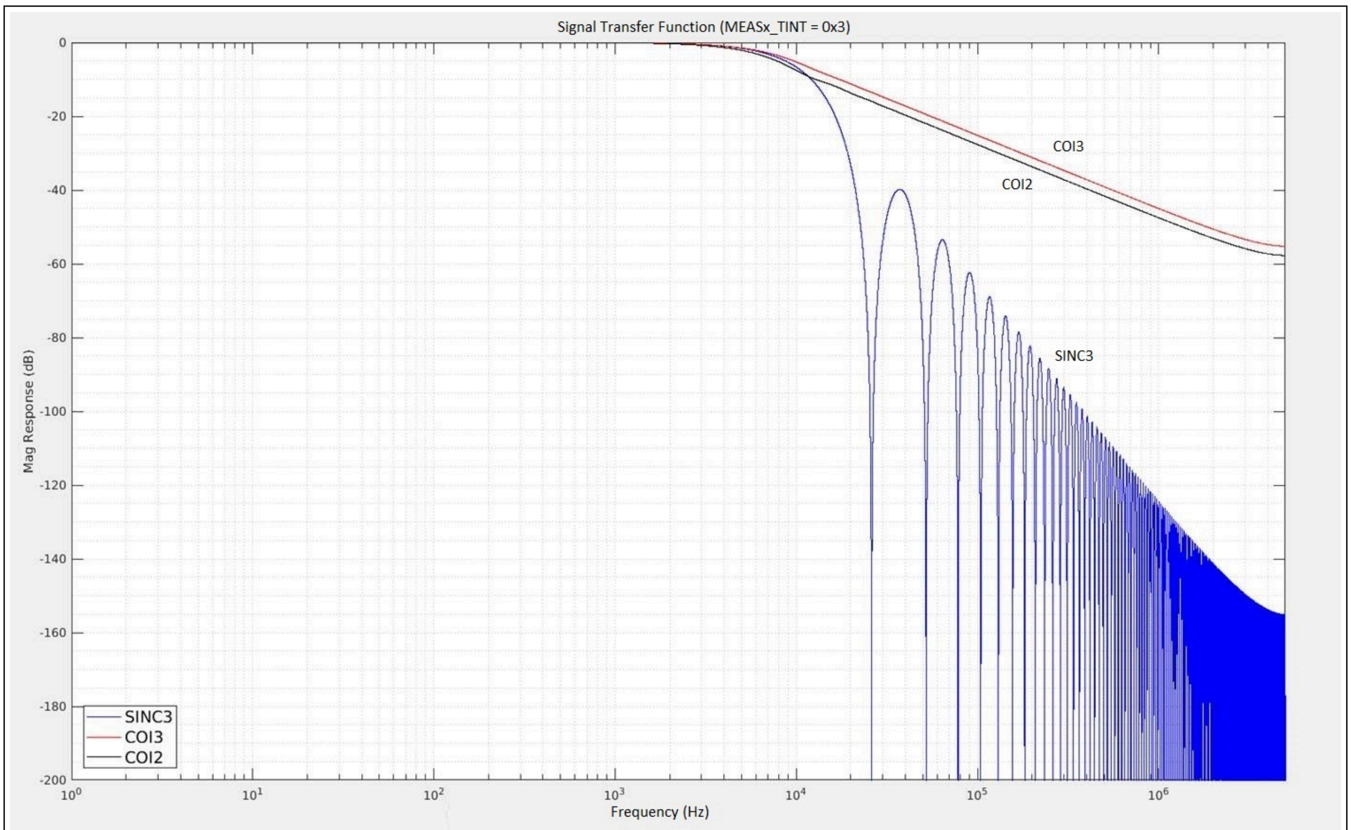

Figure 9. Signal Transfer Function of Decimation Filters

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Synchronization Modes

The MAX86177 supports both internally timed frame rates and externally triggered frames. The internally timed frame rate uses an on-chip generated 32768Hz/32000Hz clock from a low-power oscillator paired with a programmable divider. Frame rates of 32768/N or 32000/N, where: N = 11 to 32766, are directly programmable. The on-chip oscillator can also be fine-tuned (register 0x0A) to support thermal compensation. In addition, the MAX86177 allows for externally defined frame rates with either an external frame trigger input or an external 32768Hz/32000Hz clock input and the on-chip divider.

The MAX86177 supports three modes of frame rate controls. These are internally timed frame rates through an internal oscillator and divider, externally timed frame rates through an external frame trigger input, and externally timed frame rates through an external frame timing clock and the internal frame clock divider.

SYNC_MODE = 0x0, 0x3 Internal Frame Oscillator and Divider Mode

SYNC_MODE = 0x0, 0x3 is the free-running mode of operation. In this mode, the MAX86177 uses the internal frame rate oscillator (f_{FRAME_CLK}) and the internal user programmable divider (FR_CLK_DIV) to set the time between measurement instances or the frame rate. The FR_CLK_DIV register can be set to any value between 11 and 32766; thus, allowing a large variety of frame rates to be programmed. In addition, the internal oscillator (f_{FRAME_CLK}) can be set to one of two primary values, 32000Hz with the FR_CLK_SEL bit = 0 or 32768Hz with the FR_CLK_SEL bit = 1. This feature allows additional flexibility in the user-defined frame rate.

The MAX86177 also offers a fine adjust feature (FR_CLK_FINE_TUNE), which can be used in combination with a highly stable crystal-based real-time clock (RTC) oscillator in the host microcontroller to trim out the drift of the on-chip f_{FRAME_CLK} oscillator. By counting the time between the MAX86177 generated interrupts using the microcontroller-based RTC, it is possible to compute the error in the f_{FRAME_CLK} oscillator and trim that error to within ±0.2% of the microcontroller-based RTC.

SYNC_MODE = 0x1 External Frame Trigger Input Mode

SYNC_MODE = 0x1 enables the TRIG input pin to be a start for the frame sync signal. On either the falling edge (TRIG_ICFG = 0) or the rising edge (TRIG_ICFG = 1) of the TRIG input, the MAX86177 begins a measurement frame. This frame includes powering up and then executing each enabled measurement from MEAS1 to MEAS20. See SYNC_MODE[1:0] (0x0D).

SYNC_MODE = 0x2 External Frame Clock Input

SYNC_MODE = 0x2 enables the TRIG input to be an external frame clock input. This input clock effectively replaces the MAX86177 internal frame clock (f_{FRAME_CLK}) for the purpose of setting the time between the start of frame wake-up periods. The MAX86177 uses the FR_CLK_DIV register value to divide this external clock input to generate the start of the frame wake-up period. However, the stability of the frame rate is driven entirely by the external frame clock input.

This mode is useful when the microcontroller can output a 32kHz crystal-based clock. This mode can also be used to lock other sensors together through this same oscillator.

FIFO Description

The FIFO depth is 512 samples and is designed to support various data types. Each sample width is 4 bytes, which includes a 9-bit tag and data. The tag embedded in the FIFO_DATA[31:0] is used to identify the source and type of each sample data. The description of each tag is as shown in Table 4.

FIFO Data Format

The most significant bit in the 9-bit tag is 0 for any PPG data, and 1 for non-PPG data. The remaining 8 bits of the tag consists of a 2-bit PPG channel ID field, 5-bit measurement field, and 1-bit set field (it is 0 in normal mode). When there is no ALC_OVF or EXP_OVF detected, there are unique tags for each measurement data from each PPG channel. When ALC_OVF or EXP_OVF is detected for a measurement, the measurement field is replaced with ALC_OVF tag or EXP_OVF tag, and the measurement slot is identified by its relative position in the FIFO.

Note: ALC_OVF and EXP_OVF bit is at Status1 register address 0x00.

When there is a configuration change, the conversions for the current frame are aborted and a new frame starts with the new configuration. But part of the frame corresponding to the old configuration may have already been saved in

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the FIFO. Therefore, it is important to flush the FIFO after any configuration change. Otherwise, data alignment for the optical channels may be lost. Alternately, a marker may be saved in the FIFO using the FIFO_MARK bit in the FIFO Configuration 3 register at address 0x09. This marker may be used by the application to discard any stale data in the FIFO.

Computed data (for 2^{MEASx_AVER} pulses) is saved in the FIFO at the end of each measurement, along with the tag for that measurement.

When more than one of the ALC_OVF and EXP_OVF are detected for a measurement, the following priority is used for tag selection:

1. ALC_OVF Tag
2. EXP_OVF Tag
3. MEASx Tag

An attempt to read an empty FIFO returns the INVALID_DATA tag.

The FIFO tags and corresponding data types are explained in Table 4.

Table 4. FIFO Data and Tags

FIFO_DATA[31:0]						
Tag[8:0]				**Reserved**	**Data Type [19:0]**	**Description**
31	**30:29**	**28:24**	**23**	**22:20**	**19:0**	**4 bytes, 32 bits**
0	Chan	MEASx	Set	0x0	PPGy MEASx Data	Chan = 0 to 3 for PPG Channel y (y = 1 to 4) Measurement x (x = 1 to 0x14) data Set = 0 in normal mode
0	Chan	0x15	Set	0x0	PPGy MEASx Data	Chan = 0 to 3 for PPG Channel y (y = 1 to 4) ALC overflow data Measurement is implied by position Set = 0 in normal mode
0	Chan	0x16	Set	0x0	PPGy MEASx Data	Chan = 0 to 3 for PPG Channel y (y = 1 to 4) Exposure overflow data Measurement is implied by position Set = 0 in normal mode
0xFFFFFFFC						Reserved
0xFFFFFFFD						Reserved
0xFFFFFFFE						Marker saved using FIFO_MARK command
0xFFFFFFFF						Invalid Data implying that the FIFO is empty

FIFO Configuration Registers

There are eight registers (address 0x02 to 0x09) that control how the FIFO is configured and read out. Details of these registers are given in the Register Details section.

The configuration is best shown by a few examples.

Assume it is desired to perform an SpO2 measurement and also monitor the ambient level on the photodiode to adjust the IR and red LED intensity using dual Optical Channels with Photodiodes 1 and 2 selected. To perform this measurement, configure the following registers:

System Configuration

PPG3_PWRDN = 1 (Optical channel 3 is disabled)

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PPG4_PWRDN = 1	(Optical channel 4 is disabled)
MEAS1_EN = 1	(IR LED exposure)
MEAS2_EN = 1	(RED LED exposure)
MEAS3_EN = 1	(DIRECT AMBIENT exposure)
MEAS4_EN = 0	(NONE)
MEAS5_EN = 0	(NONE)
MEAS6_EN = 0	(NONE)
MEAS7_EN = 0	(NONE)
MEAS8_EN = 0	(NONE)
MEAS9_EN = 0	(NONE)
MEAS10_EN = 0	(NONE)
MEAS11_EN = 0	(NONE)
MEAS12_EN = 0	(NONE)
MEAS13_EN = 0	(NONE)
MEAS14_EN = 0	(NONE)
MEAS15_EN = 0	(NONE)
MEAS16_EN = 0	(NONE)
MEAS17_EN = 0	(NONE)
MEAS18_EN = 0	(NONE)
MEAS19_EN = 0	(NONE)
MEAS20_EN = 0	(NONE)

Measurement 1 Setup (IR LED on LED DRVA on LED1)

MEAS1_AMB = 0	(Ambient measurement off)
MEAS1_DRVA = 0x0	(LED Driver A on LED 1 and current is non-zero)
MEAS1_DRVB = 0x0	(Do not Care because current is 0)
MEAS1_PPG1_ADC_RGE = 1	(Full scale range for PPG channel 1)
MEAS1_PPG2_ADC_RGE = 1	(Full scale range for PPG channel 2)
MEAS1_PPG_TINT = 0x3	(LED pulse width control)
MEAS1_LED_RGE = 0x3	(LED drive current range)
MEAS1_PD_SETLNG = 0x1	(Photodiode settling time)
MEAS1_LED_SETLNG = 0x1	(LED settling time)
MEAS1_DRVA_PA = 0xF	(LED driver A current)
MEAS1_DRVB_PA = 0x0	(LED driver B current)
MEAS1_PD1_SEL = 0x4	(Photodiode 1 selected on optical channel 1)
MEAS1_PD2_SEL = 0x5	(Photodiode 2 selected on optical channel 2)
MEAS1_PD3_SEL = 0x0	(Photodiode 3 is not selected)
MEAS1_PD4_SEL = 0x0	(Photodiode 4 is not selected)
MEAS1_PD5_SEL = 0x0	(Photodiode 5 is not selected)
MEAS1_PD6_SEL = 0x0	(Photodiode 6 is not selected)
MEAS1_PD7_SEL = 0x0	(Photodiode 7 is not selected)
MEAS1_PD8_SEL = 0x0	(Photodiode 8 is not selected)

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Measurement 2 Setup (RED LED on LED DRVB on LED2)

MEAS2_AMB = 0	(Ambient measurement off)
MEAS2_DRVA = 0x0	(Do not Care because current is 0)
MEAS2_DRVB = 0x1	(LED Driver B on LED2 and current is non-zero)
MEAS2_PPG1_ADC_RGE = 1	(Full scale range for PPG channel 1)
MEAS2_PPG2_ADC_RGE = 1	(Full scale range for PPG channel 2)
MEAS2_PPG_TINT = 0x11	(LED pulse width control)
MEAS2_LED_RGE = 0x3	(LED drive current range)
MEAS2_PD_SETLNG = 0x1	(Photodiode settling time)
MEAS2_LED_SETLNG = 0x1	(LED settling time)
MEAS2_DRVA_PA = 0x0	(LED driver A current)
MEAS2_DRVB_PA = 0xA	(LED driver B current)
MEAS2_PD1_SEL = 0x4	(Photodiode 1 selected on optical channel 1)
MEAS2_PD2_SEL = 0x5	(Photodiode 2 selected on optical channel 2)
MEAS2_PD3_SEL = 0x0	(Photodiode 3 is not selected)
MEAS2_PD4_SEL = 0x0	(Photodiode 4 is not selected)
MEAS2_PD5_SEL = 0x0	(Photodiode 5 is not selected)
MEAS2_PD6_SEL = 0x0	(Photodiode 6 is not selected)
MEAS2_PD7_SEL = 0x0	(Photodiode 7 is not selected)
MEAS2_PD8_SEL = 0x0	(Photodiode 8 is not selected)

Measurement 3 Setup (Ambient measurement)

MEAS3_AMB = 1	(Ambient measurement selected)
MEAS3_DRVA = 0x0	(Do not Care because MEAS3_AMB = 1)
MEAS3_DRVB = 0x0	(Do not Care because MEAS3_AMB = 1)
MEAS3_PPG1_ADC_RGE = 1	(Full scale range for PPG channel 1)
MEAS3_PPG2_ADC_RGE = 1	(Full scale range for PPG channel 2)
MEAS3_PPG_TINT = 2'b11	(LED pulse width control)
MEAS3_LED_RGE = 0x0	(Do not Care because MEAS3_AMB = 1)
MEAS3_PD_SETLNG = 0x1	(Photodiode settling time)
MEAS3_LED_SETLNG = 0x1	(Do not Care because MEAS3_AMB = 1)
MEAS3_DRVA_PA = 0x0	(Do not care because MEAS3_AMB = 1)
MEAS3_DRVB_PA = 0x0	(Do not care because MEAS3_AMB = 1)
MEAS3_PD1_SEL = 0x4	(Photodiode 1 selected on optical channel 1)
MEAS3_PD2_SEL = 0x5	(Photodiode 2 selected on optical channel 2)
MEAS3_PD3_SEL = 0x0	(Photodiode 3 is not selected)
MEAS3_PD4_SEL = 0x0	(Photodiode 4 is not selected)
MEAS3_PD5_SEL = 0x0	(Photodiode 5 is not selected)
MEAS3_PD6_SEL = 0x0	(Photodiode 6 is not selected)
MEAS3_PD7_SEL = 0x0	(Photodiode 7 is not selected)
MEAS3_PD8_SEL = 0x0	(Photodiode 8 is not selected)

When done so, the sample sequence and the data format in the FIFO follow the time/location sequence mentioned below:

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channel 1 measurement 1, IR data
channel 2 measurement 1, IR data
channel 1 measurement 2, RED data
channel 2 measurement 2, RED data
channel 1 measurement 3, Ambient data
channel 2 measurement 3, Ambient data
channel 1 measurement 1, IR data
channel 2 measurement 1, IR data
channel 1 measurement 2, RED data
channel 2 measurement 2, RED data
channel 1 measurement 3, Ambient data
channel 2 measurement 3, Ambient data

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channel 1 measurement 1, IR data
channel 2 measurement 1, IR data
channel 1 measurement 2, RED data
channel 2 measurement 2, RED data
channel 1 measurement 3, Ambient data
channel 2 measurement 3, Ambient data

For a second example, it is to perform an SpO2 measurement and also monitor the ambient level on the photodiode to adjust the IR and red LED intensity using quad-optical channels with photodiodes 1 to 4 selected. To perform this measurement, configure the following registers:

System Configuration

PPG1_PWRDN = 0	(Optical channel 1 is enabled)
PPG2_PWRDN = 0	(Optical channel 2 is enabled)
PPG3_PWRDN = 0	(Optical channel 3 is enabled)
PPG4_PWRDN = 0	(Optical channel 4 is enabled)
MEAS1_EN = 1	(IR LED exposure)
MEAS2_EN = 1	(RED LED exposure)
MEAS3_EN = 1	(DIRECT AMBIENT exposure)
MEAS4_EN = 0	(NONE)
MEAS5_EN = 0	(NONE)
MEAS6_EN = 0	(NONE)
MEAS7_EN = 0	(NONE)
MEAS8_EN = 0	(NONE)
MEAS9_EN = 0	(NONE)
MEAS10_EN = 0	(NONE)
MEAS11_EN = 0	(NONE)
MEAS12_EN = 0	(NONE)
MEAS13_EN = 0	(NONE)
MEAS14_EN = 0	(NONE)
MEAS15_EN = 0	(NONE)
MEAS16_EN = 0	(NONE)
MEAS17_EN = 0	(NONE)
MEAS18_EN = 0	(NONE)
MEAS19_EN = 0	(NONE)
MEAS20_EN = 0	(NONE)

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Measurement 1 Setup (IR LED on LED DRVA on LED1)

MEAS1_AMB = 0	(Ambient measurement off)
MEAS1_DRVA = 0x0	(LED Driver A on LED1 and current is non-zero)
MEAS1_DRVB = 0x0	(Do not care because Current is 0)
MEAS1_PPG1_ADC_RGE = 1	(Full scale range for PPG channel 1)
MEAS1_PPG2_ADC_RGE = 1	(Full scale range for PPG channel 2)
MEAS1_PPG3_ADC_RGE = 1	(Full scale range for PPG channel 3)
MEAS1_PPG4_ADC_RGE = 1	(Full scale range for PPG channel 4)
MEAS1_PPG_TINT = 0x3	(LED pulse width control)
MEAS1_LED_RGE = 0x3	(LED drive current range)
MEAS1_PD_SETLNG = 0x1	(Photodiode settling time)
MEAS1_LED_SETLNG = 0x1	(LED settling time)
MEAS1_DRVA_PA = 0xF	(LED driver A current)
MEAS1_DRVB_PA = 0x0	(LED driver B current)
MEAS1_PD1_SEL = 0x4	(Photodiode 1 selected on optical channel 1)
MEAS1_PD2_SEL = 0x5	(Photodiode 2 selected on optical channel 2)
MEAS1_PD3_SEL = 0x0	(Photodiode 3 is not selected)
MEAS1_PD4_SEL = 0x0	(Photodiode 4 is not selected)
MEAS1_PD5_SEL = 0x6	(Photodiode 5 is selected on optical channel 3)
MEAS1_PD6_SEL = 0x7	(Photodiode 6 is selected on optical channel 4)
MEAS1_PD7_SEL = 0x0	(Photodiode 7 is not selected)
MEAS1_PD8_SEL = 0x0	(Photodiode 8 is not selected)

Measurement 2 Setup (RED LED on LED DRVB on LED2)

MEAS2_AMB = 0	(Ambient measurement off)
MEAS2_DRVA = 0x0	(Do not care because Current is 0)
MEAS2_DRVB = 0x1	(LED Driver B on LED2 and Current is non-zero)
MEAS2_PPG1_ADC_RGE = 1	(Full scale range for PPG channel 1)
MEAS2_PPG2_ADC_RGE = 1	(Full scale range for PPG channel 2)
MEAS2_PPG3_ADC_RGE = 1	(Full scale range for PPG channel 3)
MEAS2_PPG4_ADC_RGE = 1	(Full scale range for PPG channel 4)
MEAS2_PPG_TINT = 0x3	(LED pulse width control)
MEAS2_LED_RGE = 0x3	(LED drive current range)
MEAS2_PD_SETLNG = 0x1	(Photodiode settling time)
MEAS2_LED_SETLNG = 0x1	(LED settling time)
MEAS2_DRVA_PA = 0x0	(LED Driver A Current)
MEAS2_DRVB_PA = 0xA	(LED Driver B Current)
MEAS2_PD1_SEL = 0x4	(Photodiode 1 selected on optical channel 1)
MEAS2_PD2_SEL = 0x5	(Photodiode 2 selected on optical channel 2)
MEAS2_PD3_SEL = 0x0	(Photodiode 3 is not selected)
MEAS2_PD4_SEL = 0x0	(Photodiode 4 is not selected)
MEAS2_PD5_SEL = 0x6	(Photodiode 5 is selected on optical channel 3)
MEAS2_PD6_SEL = 0x7	(Photodiode 6 is selected on optical channel 4)
MEAS2_PD7_SEL = 0x0	(Photodiode 7 is not selected)
MEAS2_PD8_SEL = 0x0	(Photodiode 8 is not selected)

Measurement 3 Setup (Ambient measurement)

MEAS3_AMB = 1	(Ambient measurement selected)

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MEAS3_DRVA = 0x0	(Do not care because MEAS3_AMB = 1)
MEAS3_DRVB = 0x0	(Do not care because MEAS3_AMB = 1)
MEAS3_PPG1_ADC_RGE = 1	(Full scale range for PPG channel 1)
MEAS3_PPG2_ADC_RGE = 1	(Full scale range for PPG channel 2)
MEAS3_PPG3_ADC_RGE = 1	(Full scale range for PPG channel 3)
MEAS3_PPG4_ADC_RGE = 1	(Full scale range for PPG channel 4)
MEAS3_PPG_TINT = 0x3	(LED pulse width control)
MEAS3_LED_RGE = 0x3	(Do not care because MEAS3_AMB = 1))
MEAS3_PD_SETLNG = 0x1	(Photodiode settling time)
MEAS3_LED_SETLNG = 0x1	(Do not care because MEAS3_AMB = 1)
MEAS3_DRVA_PA = 0x0	(Do not care because MEAS3_AMB = 1)
MEAS3_DRVB_PA = 0x0	(Do not care because MEAS3_AMB = 1)
MEAS3_PD1_SEL = 0x4	(Photodiode 1 selected on optical channel 1)
MEAS3_PD2_SEL = 0x5	(Photodiode 2 selected on optical channel 2)
MEAS3_PD3_SEL = 0x0	(Photodiode 3 is not selected)
MEAS3_PD4_SEL = 0x0	(Photodiode 4 is not selected)
MEAS3_PD5_SEL = 0x6	(Photodiode 5 is selected on optical channel 3)
MEAS3_PD6_SEL = 0x7	(Photodiode 6 is selected on optical channel 4)
MEAS3_PD7_SEL = 0x0	(Photodiode 7 is not selected)
MEAS3_PD8_SEL = 0x0	(Photodiode 8 is not selected)

When done so, the sample sequence and the data format in the FIFO follow the time/ location sequence mentioned below:

channel 1 measurement 1, IR data
channel 2 measurement 1, IR data
channel 3 measurement 1, IR data
channel 4 measurement 1, IR data
channel 1 measurement 2, RED data
channel 2 measurement 2, RED data
channel 3 measurement 2, RED data
channel 4 measurement 2, RED data
channel 1 measurement 3, Ambient data
channel 2 measurement 3, Ambient data
channel 3 measurement 3, Ambient data
channel 4 measurement 3, Ambient data
channel 1 measurement 1, IR data
channel 2 measurement 1, IR data
channel 3 measurement 1, IR data
channel 4 measurement 1, IR data
channel 1 measurement 2, RED data
channel 2 measurement 2, RED data
channel 3 measurement 2, RED data
channel 4 measurement 2, RED data
channel 1 measurement 3, Ambient data
channel 2 measurement 3, Ambient data
channel 3 measurement 3, Ambient data
channel 4 measurement 3, Ambient data
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channel 1 measurement 1, IR data
channel 2 measurement 1, IR data

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channel 3 measurement 1, IR data
channel 4 measurement 1, IR data
channel 1 measurement 2, RED data
channel 2 measurement 2, RED data
channel 3 measurement 2, RED data
channel 4 measurement 2, RED data
channel 1 measurement 3, Ambient data
channel 2 measurement 3, Ambient data
channel 3 measurement 3, Ambient data
channel 4 measurement 3, Ambient data

The number of bytes of data for the four Optical Channels in one frame is given by: 2 x 4 x N, where:

N = the number of measurements enabled

If the application always responds much faster than the selected sample rate, it could just read 512 minus FIFO_A_FULL[8:0] (at register addresses 0x06 and 0x07) items when it gets an A_FULL interrupt, and be assured that all data from the FIFO is read. However, if there is a need to calculate the number of items available in the FIFO, one can perform the following pseudocode:

```
read the OVF_COUNTER register
read the FIFO_DATA_COUNT registers
if OVF_COUNTER == 0 //no overflow occurred
   NUM_AVAILABLE_SAMPLES = FIFO_DATA_COUNT
else
   NUM_AVAILABLE_SAMPLES = 512   // overflow occurred and data has been lost
endif
```

Threshold Detect Function

The MAX86177 includes a threshold detect function that significantly reduces the energy consumption and extends the battery life when the sensor is not in contact with skin. There are two thresholds available in the MAX86177: THRESHOLD1 and THRESHOLD2. Both are disabled by default.

The threshold detect function is enabled by setting THRESHx_MEAS_SEL[4:0](x = 1 and 2, at register address 0xF3 and 0xF4) to a valid measurement number. The threshold interrupts may be enabled using THRESHx_HILO_EN1 bit (x = 1, 2) in register 0xFA and THRESHx_HILO_EN2 bit (x = 1, 2) in register 0xFC. The threshold detect function can be set up for any of the four channels through THRESH1_PPG_SEL[1:0] and THRESH2_PPG_SEL [1:0](at register 0xF3 and 0xF4). To configure the threshold detect function, both an upper limit and a lower limit must be set. These can be configured in the THRESHOLD interrupts register block (address 0xF6 to 0xF9).

In addition, two features are available to make the threshold detect function more adaptable for various system and application requirements. These are Time Hysteresis and Level Hysteresis (TIME_HYST[1:0] and LEVEL_HYST[2:0] bits), and are configurable through the THRESHOLD_HYST register (0xF5).

If enabled, when the ADC counts of the assigned measurement on the specified PPG channel drop below the lower limit or exceed the upper limit (in consideration with LEVEL_HYST and TIME_HYST settings), the THRESHx_HILO status bits (at register address 0x00) is asserted. The upper threshold check may be disabled by setting THRESHx_UPPER[7:0] (at register address 0xF6, and 0xF8) to 0xFF. The LED configuration during the threshold detect active mode is determined by the firmware settings as needed for each application. The LED current, ADC integration time, and frame rate can be reduced significantly; thereby reducing power consumption during situations when there is no reflective returned signal.

Digital Interface

The MAX86177 has an I²C and SPI combination interface. The I2C_SEL pin selects between the two interfaces. When I2C_SEL is high, the interface is in the I²C mode and idles looking for a start bit to occur on the SCL and SDA pins, while the SPI interface is held in a reset state. When I2C_SEL is low, the I²C interface is in a reset state, the SPI interface is

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activated, and the SDO pin goes active. In the following sections, both interface timings and protocols are described.

SPI Timing

Detailed SPI Timing

The MAX86177 detailed SPI timing diagram is shown in Figure 10. The timings indicated are all specified in the *Electrical Characteristics* section.

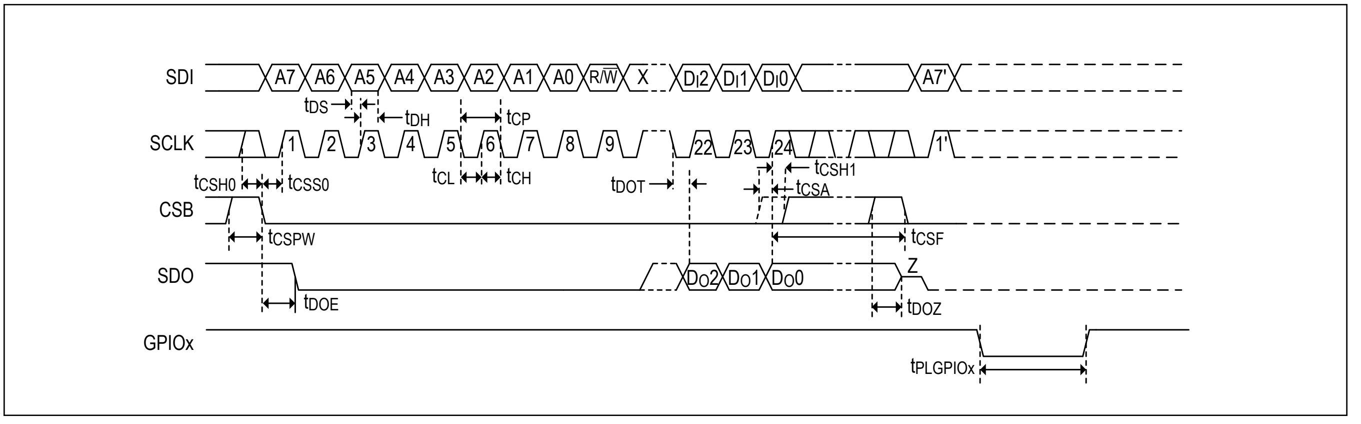

Figure 10. Detailed SPI Timing

Single-Word SPI Register Read/Write Transaction

The SPI interface on the MAX86177 is SPI-compatible, QSPI-compatible, Microwire-compatible, and DSP-compatible. The operation of the SPI interface is shown in Figure 11. Data is strobed into the MAX86177 on the SCLK rising edge while clocked out on the SCLK falling edge. All single-word SPI read and write operations are done in 3 bytes, a 24-clock-cycle SPI instruction framed by a CSB low interval. The content of the SPI operation consists of a 1 byte register address, A[7:0], followed by a 1 byte command word which defines the transaction as write or read, followed by a single-byte data word either written to or read from the register location provided in the first byte.

Write mode operations are executed on the 24th SCLK rising edge using the first 3 bytes of data available. In write mode, any data supplied after the 24th SCLK rising edge is ignored. Subsequent writes require CSB to deassert high and then assert low for the next write command. A rising CSB edge preceding the 24th rising edge of SCLK (Figure 10), results in the transaction being aborted.

Read mode operations access the requested data on the 16th SCLK rising edge, and present the MSB of the requested data on the following SCLK falling edge, allowing the SPI controller to latch the data MSB on the 17th SCLK rising edge as shown in Figure 12. Configuration and status registers are available using normal mode read-back sequences. FIFO reads must be done with a burst mode FIFO read (for more details, see the *SPI FIFO Burst Mode Read Transaction* section). If more than 24 SCLK rising edges are provided in a normal read sequence, then the excess edges are ignored and the device reads back zeros.

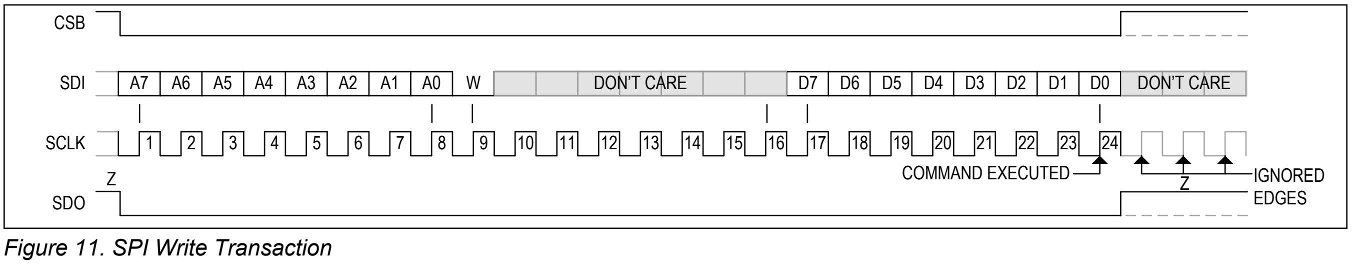

Figure 11. SPI Write Transaction

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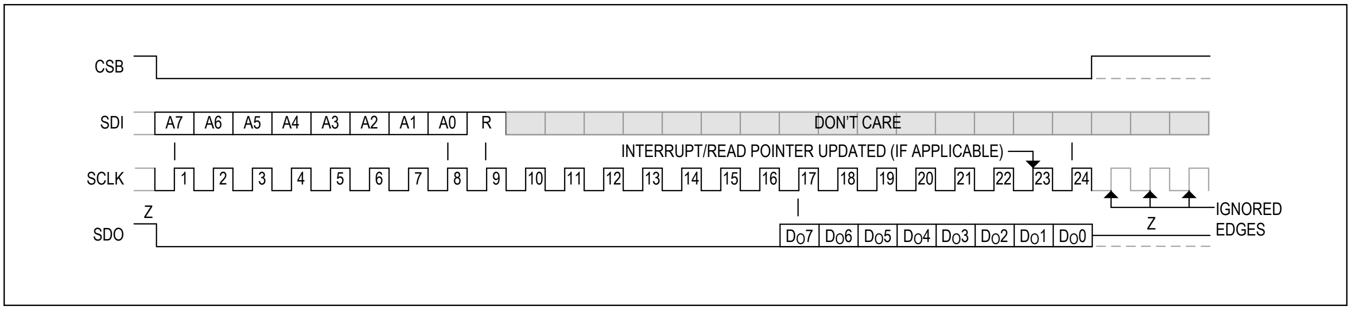

Figure 12. SPI Read Transaction

SPI FIFO Burst Mode Read Transaction

The MAX86177 provides a FIFO burst read mode to increase data transfer efficiency. The first 16 SCLK cycles operate exactly as described for the normal read mode, the first byte being the register address, the second being a read command. The subsequent SCLKs consist of FIFO data, 32 SCLKs per word. All words in the FIFO should be read with a single FIFO burst read command.

Each FIFO sample consists of 4 bytes per sample (for more details, see the *FIFO Data Format* section); thus, each sample requires 32 SCLKs per sample to read out. The first 2 bytes (SCLK 17 to 32) consist of a tag indicating the data type of the subsequent bits as well as the MSBs of the data. The next 2 bytes (SCLK 33 to 48) consist of data. For example, Figure 13 shows a FIFO burst read consisting of three PPG samples in FIFO, labelled A through C, each with a 9-bit tag and 20-bit data. The number of words in the FIFO depends on the FIFO configuration. For more details, see the FIFO_A_FULL (at register address 0x06, 0x07) registers.

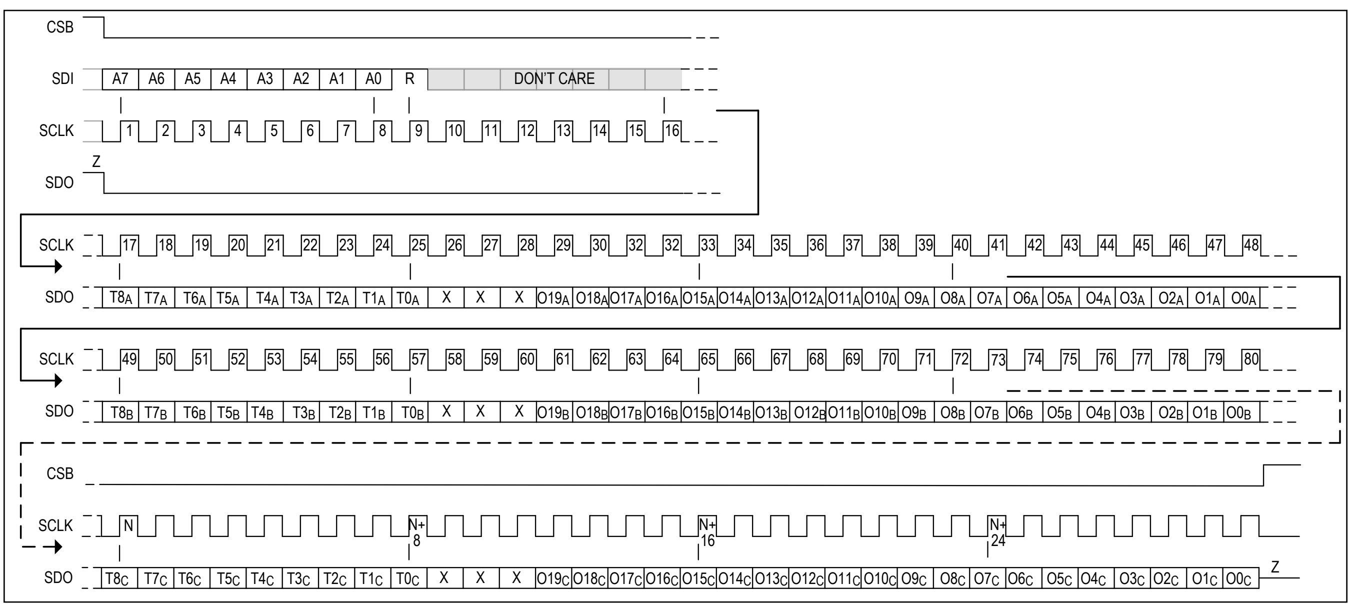

Figure 13. SPI FIFO Burst Mode Read Transaction

I²C-Compatible and SMBus-Compatible Serial Interface

The I²C interface on the MAX86177 is an I²C-compatible, SMBus-compatible, and 2-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). The SDA and SCL facilitate communication between the MAX86177 and the controller at clock rates up to 400kHz. Figure 14 shows the two-wire interface timing diagram. The controller generates SCL and initiates data transfer on the bus. The controller device writes data to the MAX86177 by transmitting the proper target address followed by the register address and then the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted to the MAX86177

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is 8-bit long and is followed by an acknowledge clock pulse. A controller reading data from the MAX86177 transmits the proper target address followed by a series of nine SCL pulses. The MAX86177 transmits data on SDA in sync with the controller-generated SCL pulses. The controller acknowledges receipt of each byte of data. Each read sequence is framed by a START (S) or REPEATED START (Sr) condition, a not-acknowledge, and a STOP (P) condition. The SDA operates as both an input and an open-drain output. A pullup resistor is required on SDA. The SCL only operates as an input. A pullup resistor is required on SCL if there are multiple controllers on the bus, or if the single controller has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the MAX86177 from high-voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus signals.

The detailed timing diagram of various electrical characteristics is shown in Figure 14.

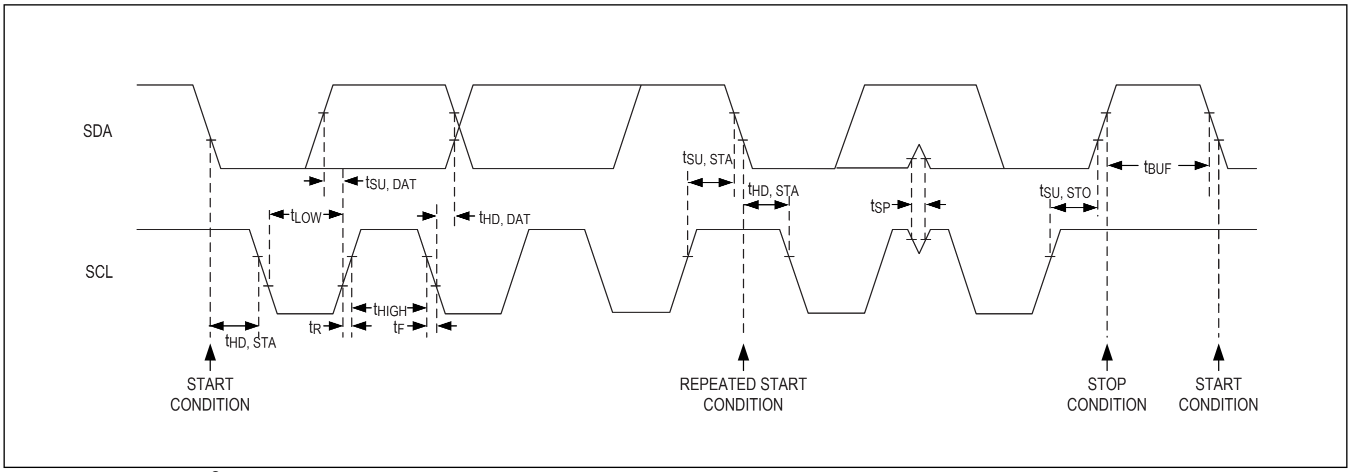

Figure 14. Detailed I²C Timing Diagram

Target Address

The target address is defined as the seven most significant bits (MSBs) followed by the read/write bit. The address is the first byte of information sent to the IC after the START condition. For more details, see the *Electrical Characteristics* table.

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (for more details, see the *START and STOP Conditions* section).

START and STOP Conditions

The SDA and SCL idle high when the bus is not in use. A controller initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 15). A START condition from the controller signals the beginning of a transmission to the MAX86177. The controller terminates the transmission and frees the bus by issuing a STOP condition. The bus remains active if a REPEATED START condition is generated instead of a STOP condition.

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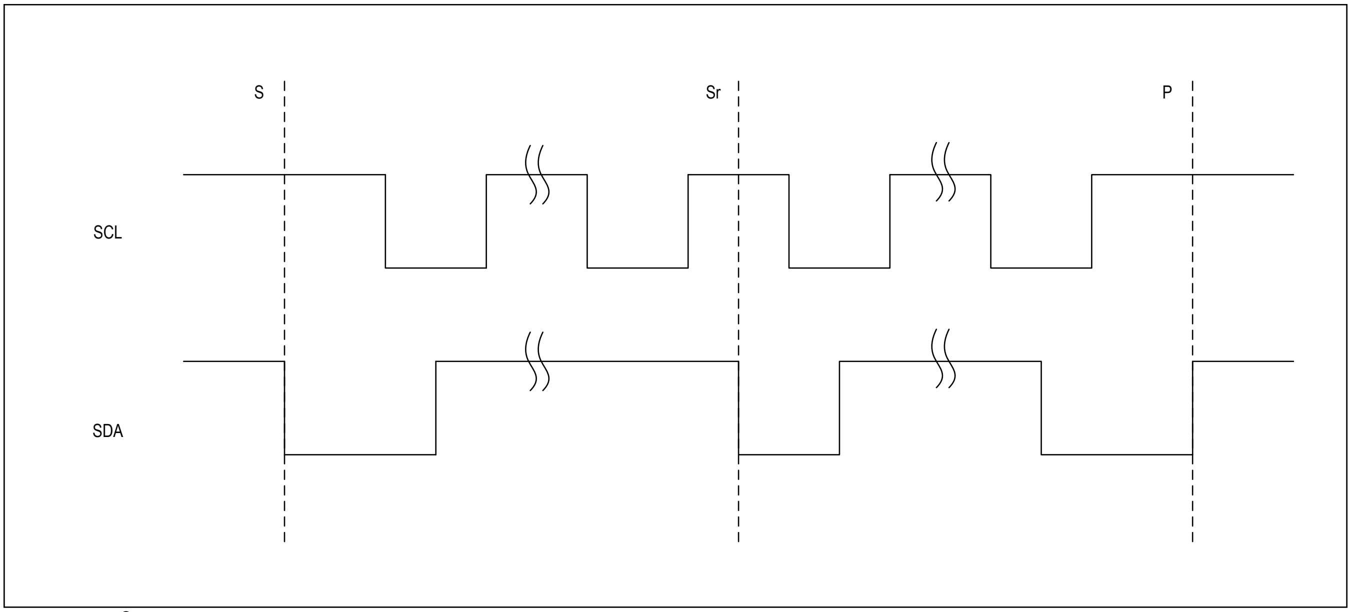

Figure 15. I²C START, STOP, and REPEATED START Conditions

Early STOP Conditions

The MAX86177 recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

Acknowledge Bit

The acknowledge bit (ACK) is a clocked 9th bit that the MAX86177 uses to handshake receipt of each byte of data when in write mode (Figure 16). The MAX86177 pulls down SDA during the entire controller-generated 9th clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus controller retries communication. The controller pulls down SDA during the 9th clock cycle to acknowledge receipt of data when the MAX86177 is in read mode. An acknowledge is sent by the controller after each read byte to allow data transfer to continue. A not-acknowledge (NACK) is sent when the controller reads the final byte of data from the MAX86177 followed by a STOP condition.

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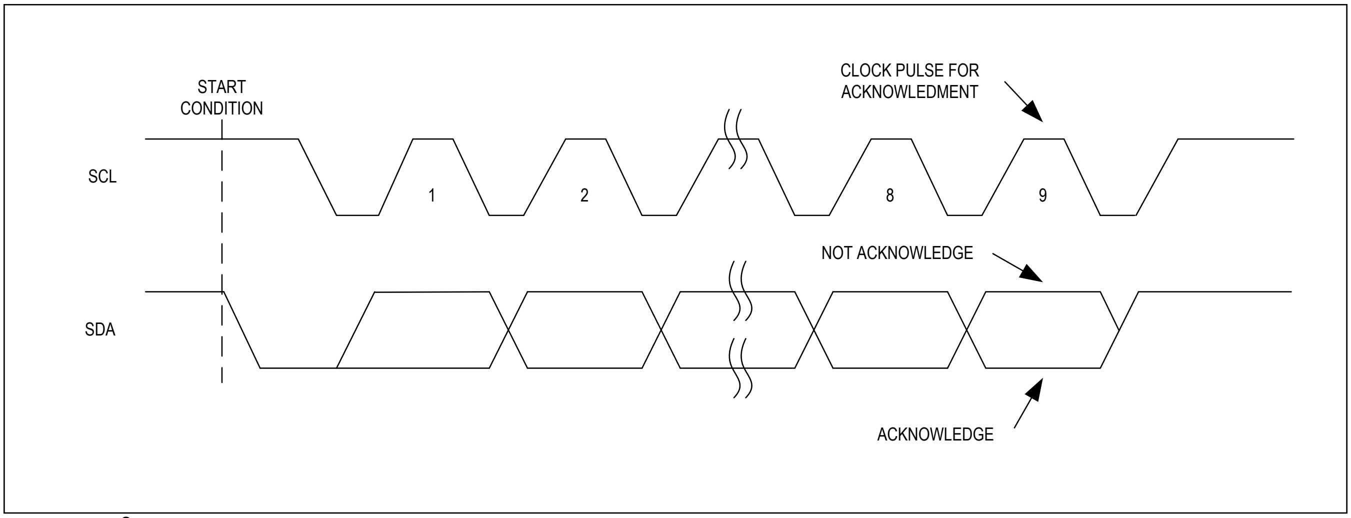

Figure 16. I2C Acknowledge Bit

I2C Write Data Format

A write to the MAX86177 includes transmission of a START condition, the target address with the R/$\overline{W}$ bit set to 0, 1 byte of data to configure the internal register address pointer, one or more bytes of data, and a STOP condition. Figure 17 shows the proper frame format for writing 1 byte of data to the MAX86177. Figure 18 shows the frame format for writing n-bytes of data to the MAX86177.

The target address with the R/$\overline{W}$ bit set to 0 indicates that the controller intends to write data to the MAX86177. The MAX86177 acknowledges receipt of the address byte during the controller-generated 9th SCL pulse.

The second byte transmitted from the controller configures the MAX86177 internal register address pointer. The pointer tells the MAX86177 where to write the next byte of data. An acknowledge pulse is sent by the MAX86177 upon receipt of the address pointer data.

The third byte sent to the MAX86177 contains the data that is written to the chosen register. An acknowledge pulse from the MAX86177 signals receipt of the data byte. The address pointer autoincrements to the next register address after each received data byte. This autoincrement feature allows a controller to write to sequential registers within one continuous frame. The controller signals the end of transmission by issuing a STOP condition. The autoincrement feature is disabled when there is an attempt to write to the FIFO_DATA register.

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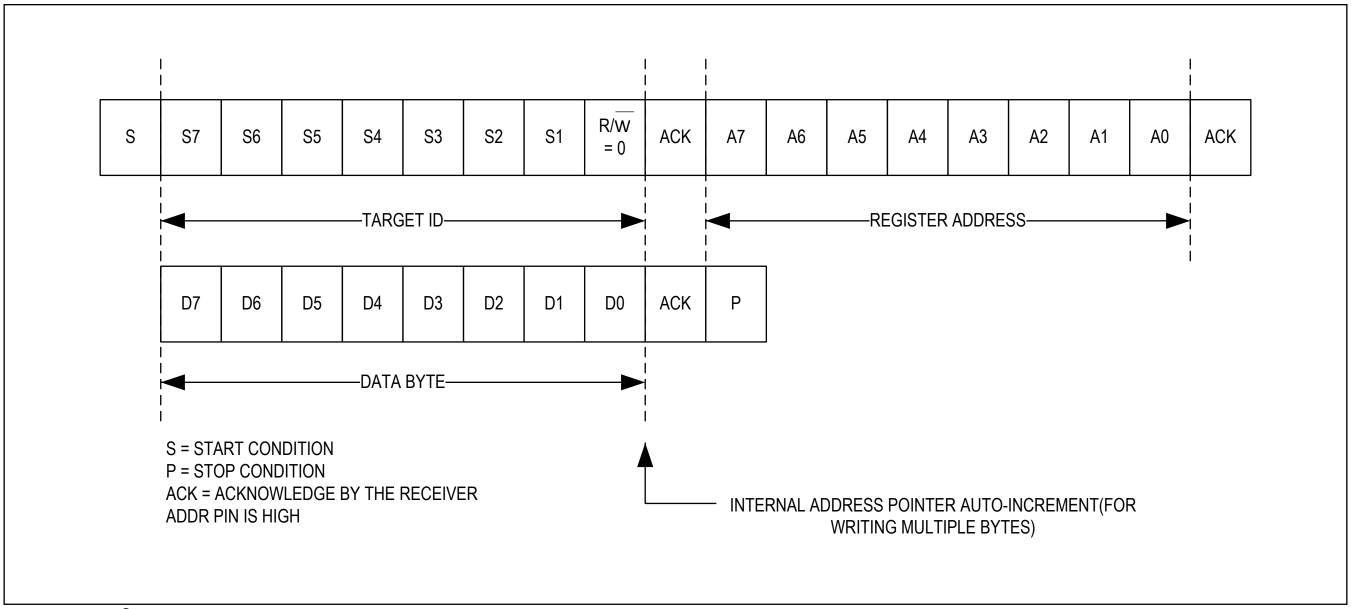

Figure 17. I2C Single-Byte Write Transaction

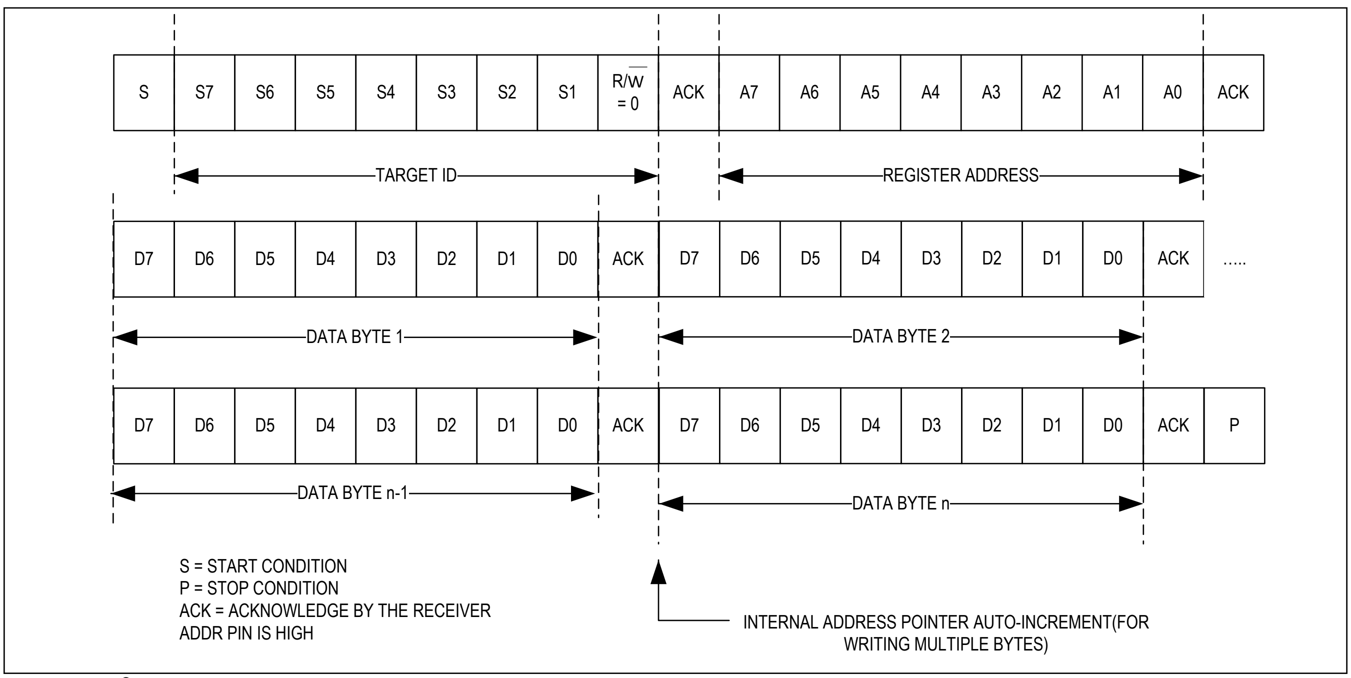

Figure 18. I2C Multi-Byte Write Transaction

I2C Read Data Format

Send the target address with the R/W bit set to 1 to initiate a read operation. The MAX86177 acknowledges receipt of its target address by pulling SDA low during the 9th SCL clock pulse. A START command followed by a read command resets the address pointer to register 0x00.

The first byte transmitted from the MAX86177 is the content of register 0x00. Transmitted data is valid on the rising edge of the SCL. The address pointer autoincrements after each read data byte. This autoincrement feature allows all registers

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to be read sequentially within one continuous frame. The autoincrement feature is disabled when there is an attempt to read from the FIFO_DATA register. A STOP condition can be issued after any number of read data bytes. If a STOP condition is issued followed by another read operation, the first data byte to be read is from register 0x00.

The address pointer can be preset to a specific register before a read command is issued. The controller presets the address pointer by first sending the MAX86177 target address with the R/$\overline{W}$ bit set to 0 followed by the register address. A REPEATED START condition is then sent followed by the target address with the R/$\overline{W}$ bit set to 1. The MAX86177 then transmits the contents of the specified register. The address pointer autoincrements after transmitting the first byte.

The controller acknowledges receipt of each read byte during the acknowledge clock pulse. The controller must acknowledge all the correctly received bytes except the last byte. The final byte must be followed by a NACK from the controller and then a STOP condition. Figure 19 shows the frame format for reading 1 byte from the MAX86177. Figure 20 shows the frame format for reading multiple bytes from the MAX86177.

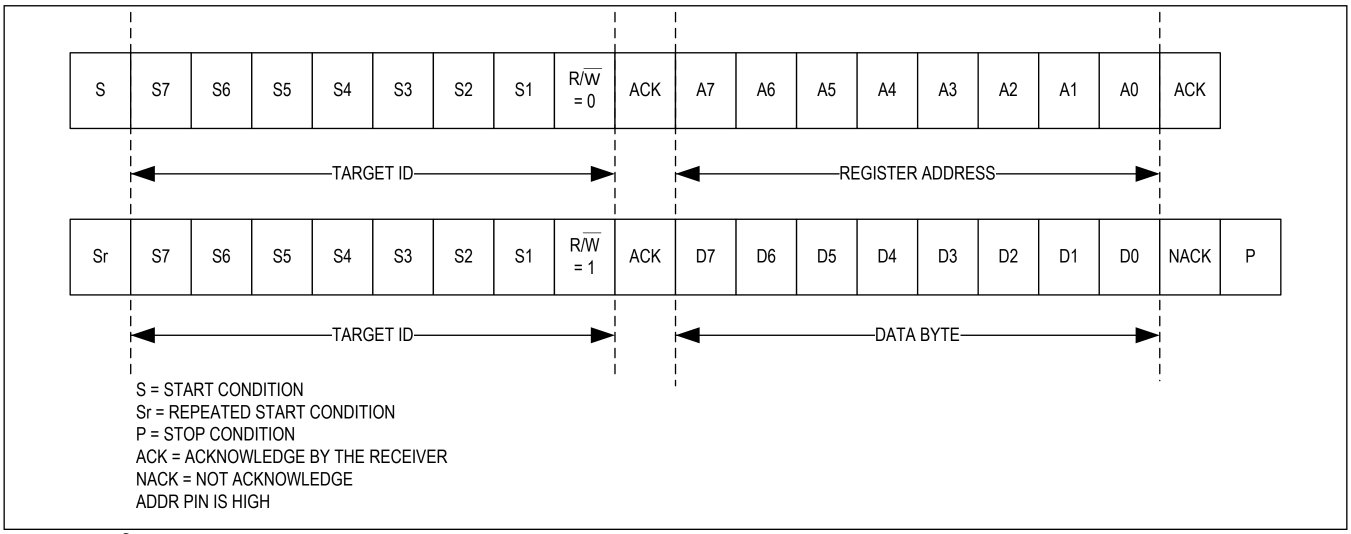

Figure 19. I2C Single-Byte Read Transaction

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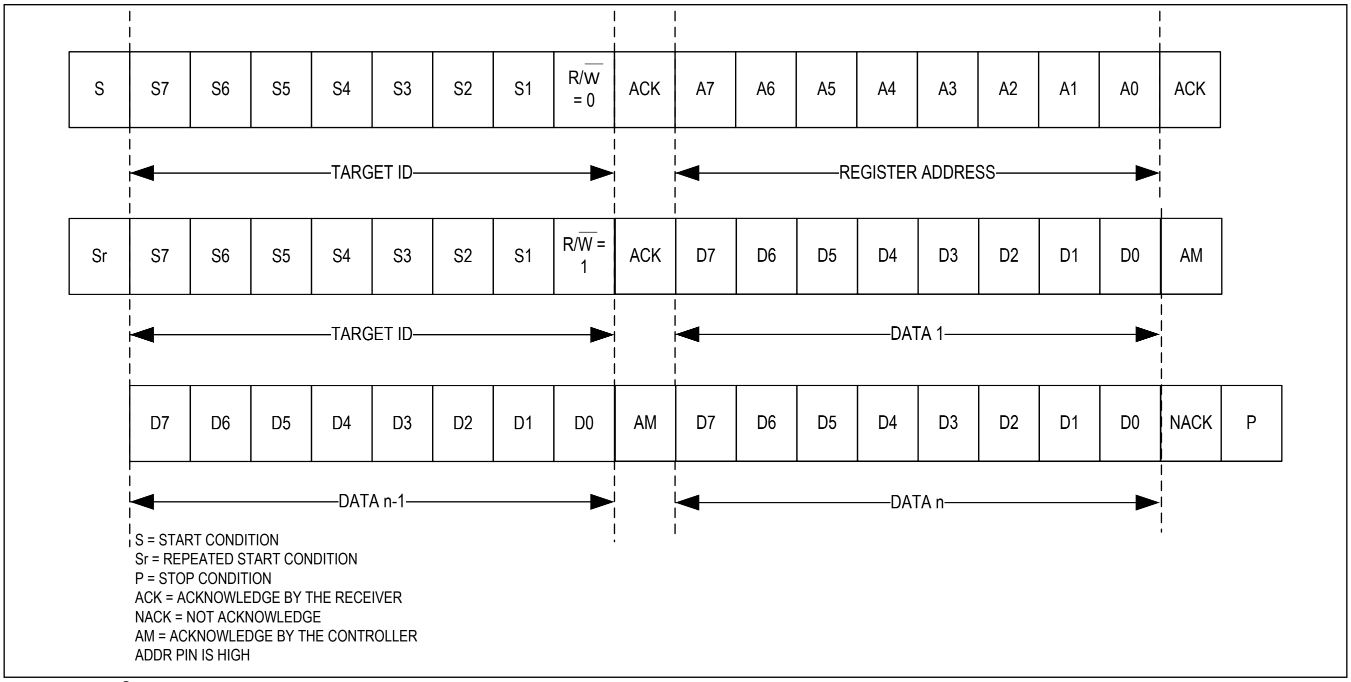

Figure 20. I²C Multi-Byte Read Transaction

PCB Layout Guidelines

The MAX86177 is a high dynamic-range analog front-end (AFE), and its performance can be adversely impacted by the physical printed circuit board (PCB) layout. It is important that all bypass recommendations shown in the *Pin Description* table are followed. Specifically, it is recommended that the V_{DD_ANA} and V_{DD_DIG} pins be shorted at the PCB. It is also recommended that GND and PGND be shorted to a single PCB ground plane.

The combined V_{DD_ANA} and V_{DD_DIG} pins should then be decoupled with a 0.1µF and a larger ceramic chip capacitor around 10µF (effective) to the PCB ground plane. In addition, the VREF pin should be decoupled to the PCB ground plane with a 1.0µF ceramic capacitor. The voltage on the VREF pin is nominally 1.21V, so a 6.3V-rated ceramic capacitor should be adequate for this purpose. It is recommended that all decoupling caps use individual vias to the PCB ground plane to avoid mutual impedance coupling between decoupled supplies when sharing vias.

The most critical aspect of the PCB layout of the MAX86177 is the handling of the PDm_IN (m = 1 to 8) and GND nodes. Parasitic capacitive coupling to the PDm_IN can result in additional noise being injected into the MAX86177 front end. To minimize external interference coupling to PDm_IN, it is recommended that the PDm_IN node be fully shielded by the virtual PD_GND node. An example of this recommendation is shown in Figure 21.

The top layer on which the MAX86177 is mounted, PDm_IN node should be shielded with a coplanar virtual PD_GND trace. On the bottom layer (Figure 22), the photodiode cathode is entirely shielded with the virtual PD_GND node, which is also the photodiode anode. Note also that the PD_GND shield extends below the photodiode. This is done because in most photodiodes, the cathode is the bulk of the silicon. Thus, shielding beneath the photodiode terminates the capacitance due to the bulk or cathode side to the reference node, PD_GND. On the layer just above the bottom, layer 5 in this case (Figure 23), the section of the GND plane has been opened up, connected to PD_GND to shield the PD_IN node below the photodiode cathode contact. Finally, the virtual PD_GND should only be attached to the AFE GND pin in only one point.

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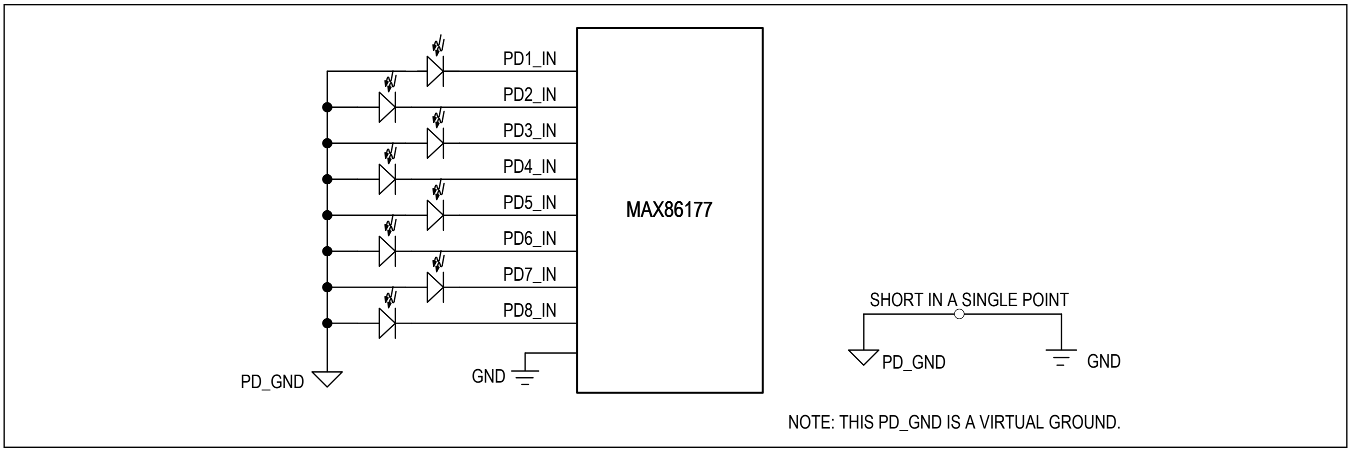

Figure 21. PCB Layout Recommendation

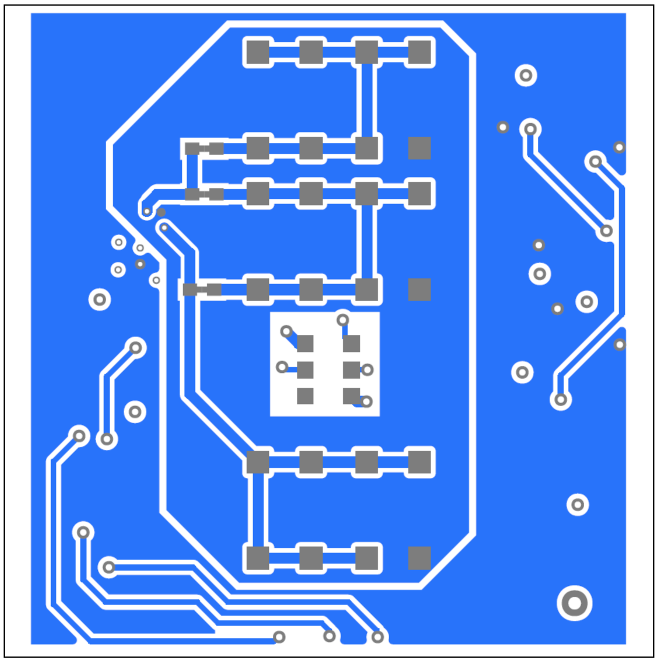

Figure 22. Bottom Layer-Optics Layer

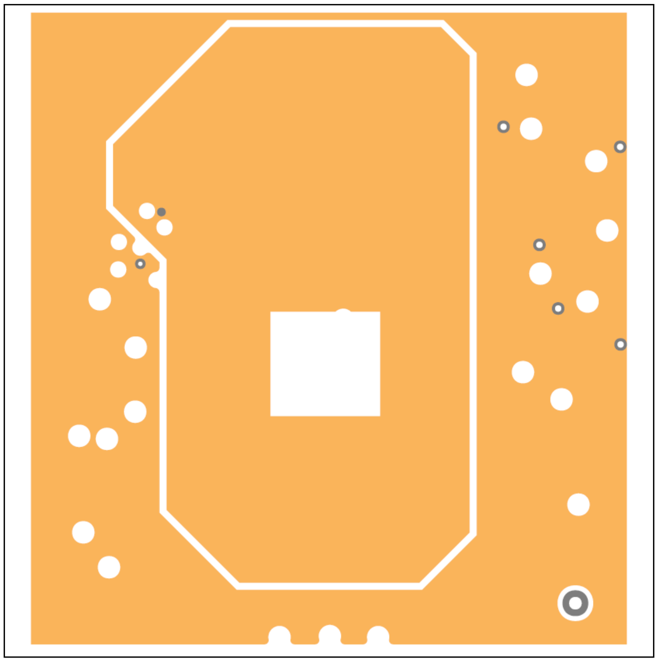

Figure 23. Layer 5- Virtual PD_GND Shields PD_IN

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Register Map

User Register Map

ADDRESS	NAME	MSB							LSB
Status									
0x00	Status 1[7:0]	A_FULL	FRAME_RDY	FIFO_DATA_RDY	ALC_OVF	EXP_OVF	THRESH2_HILO	THRESH1_HILO	PWR_RDY
0x01	Status 2[7:0]	INVALID_CFG	–	LED6_COMPB	LED5_COMPB	LED4_COMPB	LED3_COMPB	LED2_COMPB	LED1_COMPB
FIFO									
0x02	FIFO Write Pointer[7:0]	FIFO_WR_PTR[7:0]							
0x03	FIFO Counter 1[7:0]	FIFO_DATA_COUNT[9:8]		OVF_COUNTER[4:0]					FIFO_WR_PTR[8]
0x04	FIFO Counter 2[7:0]	FIFO_DATA_COUNT[7:0]							
0x05	FIFO Read Pointer[7:0]	FIFO_RD_PTR[7:0]							
0x06	FIFO Configuration 1[7:0]	FIFO_A_FULL[8]	–	–	–	–	–	–	FIFO_RD_PTR[8]
0x07	FIFO Configuration 2[7:0]	FIFO_A_FULL[7:0]							
0x08	FIFO Data Register[7:0]	FIFO_DATA[7:0]							
0x09	FIFO Configuration 3[7:0]	–	–	FIFO_MARK	FLUSH_FIFO	FIFO_STAT_CLR	A_FULL_TYPE	FIFO_RO	–
Frame Rate Clock									
0x0A	FR Clock Frequency Select[7:0]	–	–	FR_CLK_SEL	FR_CLK_FINE_TUNE[4:0]				
0x0B	FR Clock Divider MSB[7:0]	–	FR_CLK_DIV_H[6:0]						
0x0C	FR Clock Divider LSB[7:0]	FR_CLK_DIV_L[7:0]							
System Control									
0x0D	System Configuration 1[7:0]	SYNC_MODE[1:0]		PPG4_PWRDN	PPG3_PWRDN	PPG2_PWRDN	PPG1_PWRDN	SHDN	RESET
0x0E	Pin Functional Configuration[7:0]	–	–	–	INT2_FCFG[1:0]		INT1_FCFG[1:0]		TRIG_ICFG
0x0F	Output Pin Configuration[7:0]	–	–	–	INT2_OCFG[1:0]		INT1_OCFG[1:0]		–
0x10	System Sync[7:0]	–	SW_FORCE_SYNC	–	–	–	–	–	–
PPG Setup									
0x11	PPG MEAS Select 1[7:0]	–	–	–	–	MEAS20_EN	MEAS19_EN	MEAS18_EN	MEAS17_EN
0x12	PPG MEAS Select 2[7:0]	MEAS16_EN	MEAS15_EN	MEAS14_EN	MEAS13_EN	MEAS12_EN	MEAS11_EN	MEAS10_EN	MEAS9_EN

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ADDRESS	NAME	MSB							LSB
0x13	PPG MEAS Select 3[7:0]	MEAS8_EN	MEAS7_EN	MEAS6_EN	MEAS5_EN	MEAS4_EN	MEAS3_EN	MEAS2_EN	MEAS1_EN
0x14	PPG Filter Setup[7:0]	–	SMP_AVE[2:0]			ALC_DISABLE	–	–	MEAS1_CONFIG_SEL
0x15	Photo Diode Bias 1[7:0]	PD4_BIAS[1:0]		PD3_BIAS[1:0]		PD2_BIAS[1:0]		PD1_BIAS[1:0]	
0x16	Photo Diode Bias 2[7:0]	PD8_BIAS[1:0]		PD7_BIAS[1:0]		PD6_BIAS[1:0]		PD5_BIAS[1:0]	
MEAS1 Setup									
0x17	MEAS1 Selects[7:0]	–	MEAS1_AMB	MEAS1_DRVB[2:0]			MEAS1_DRVA[2:0]		
0x18	MEAS1 Configuration 1[7:0]	–	MEAS1_DAC_LO_NOISE	MEAS1_FILT2_SEL	MEAS1_TINT[1:0]		MEAS1_AVER[2:0]		
0x19	MEAS1 Configuration 2[7:0]	MEAS1_SINC3_SEL	MEAS1_FILT_SEL	–	–	MEAS1_PPG4_ADC_RGE	MEAS1_PPG3_ADC_RGE	MEAS1_PPG2_ADC_RGE	MEAS1_PPG1_ADC_RGE
0x1A	MEAS1 Configuration 3[7:0]	MEAS1_PPG2_DACOFF[3:0]				MEAS1_PPG1_DACOFF[3:0]			
0x1B	MEAS1 Configuration 4[7:0]	MEAS1_PPG4_DACOFF[3:0]				MEAS1_PPG3_DACOFF[3:0]			
0x1C	MEAS1 Configuration 5[7:0]	MEAS1_PD_SETLNG[1:0]		MEAS1_LED_SETLNG[1:0]		–	–	MEAS1_LED_RGE[1:0]	
0x1D	MEAS1 LEDA Current[7:0]	MEAS1_DRVA_PA[7:0]							
0x1E	MEAS1 LEDB Current[7:0]	MEAS1_DRVB_PA[7:0]							
0x1F	MEAS1 PD SEL 1[7:0]	MEAS1_PD3_SEL[2:1]		MEAS1_PD2_SEL[2:0]			MEAS1_PD1_SEL[2:0]		
0x20	MEAS1 PD SEL 2[7:0]	MEAS1_PD6_SEL[2]	MEAS1_PD5_SEL[2:0]			MEAS1_PD4_SEL[2:0]			MEAS1_PD3_SEL[0]
0x21	MEAS1 PD SEL 3[7:0]	MEAS1_PD8_SEL[2:0]			MEAS1_PD7_SEL[2:0]			MEAS1_PD6_SEL[1:0]	
MEAS2 Setup									
0x22	MEAS2 Selects[7:0]	–	MEAS2_AMB	MEAS2_DRVB[2:0]			MEAS2_DRVA[2:0]		
0x23	MEAS2 Configuration 1[7:0]	–	MEAS2_DAC_LO_NOISE	MEAS2_FILT2_SEL	MEAS2_TINT[1:0]		MEAS2_AVER[2:0]		
0x24	MEAS2 Configuration 2[7:0]	MEAS2_SINC3_SEL	MEAS2_FILT_SEL	–	–	MEAS2_PPG4_ADC_RGE	MEAS2_PPG3_ADC_RGE	MEAS2_PPG2_ADC_RGE	MEAS2_PPG1_ADC_RGE
0x25	MEAS2 Configuration 3[7:0]	MEAS2_PPG2_DACOFF[3:0]				MEAS2_PPG1_DACOFF[3:0]			
0x26	MEAS2 Configuration 4[7:0]	MEAS2_PPG4_DACOFF[3:0]				MEAS2_PPG3_DACOFF[3:0]			
0x27	MEAS2 Configuration 5[7:0]	MEAS2_PD_SETLNG[1:0]		MEAS2_LED_SETLNG[1:0]		–	–	MEAS2_LED_RGE[1:0]	
0x28	MEAS2 LEDA Current[7:0]	MEAS2_DRVA_PA[7:0]							

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ADDRESS	NAME	MSB							LSB
0x29	MEAS2 LEDB Current[7:0]	MEAS2_DRVB_PA[7:0]							
0x2A	MEAS2 PD SEL 1[7:0]	MEAS2_PD3_SEL[2:1]		MEAS2_PD2_SEL[2:0]			MEAS2_PD1_SEL[2:0]		
0x2B	MEAS2 PD SEL 2[7:0]	MEAS2_PD6_SEL[2]	MEAS2_PD5_SEL[2:0]			MEAS2_PD4_SEL[2:0]			MEAS2_PD3_SEL[0]
0x2C	MEAS2 PD SEL 3[7:0]	MEAS2_PD8_SEL[2:0]			MEAS2_PD7_SEL[2:0]			MEAS2_PD6_SEL[1:0]	
MEAS3 Setup									
0x2D	MEAS3 Selects[7:0]	–	MEAS3_AMB	MEAS3_DRVB[2:0]			MEAS3_DRVA[2:0]		
0x2E	MEAS3 Configuration 1[7:0]	–	MEAS3_DAC_LO_NOISE	MEAS3_FILT2_SEL	MEAS3_TINT[1:0]		MEAS3_AVER[2:0]		
0x2F	MEAS3 Configuration 2[7:0]	MEAS3_SINC3_SEL	MEAS3_FILT_SEL	–	–	MEAS3_PPG4_ADC_RGE	MEAS3_PPG3_ADC_RGE	MEAS3_PPG2_ADC_RGE	MEAS3_PPG1_ADC_RGE
0x30	MEAS3 Configuration 3[7:0]	MEAS3_PPG2_DACOFF[3:0]				MEAS3_PPG1_DACOFF[3:0]			
0x31	MEAS3 Configuration 4[7:0]	MEAS3_PPG4_DACOFF[3:0]				MEAS3_PPG3_DACOFF[3:0]			
0x32	MEAS3 Configuration 5[7:0]	MEAS3_PD_SETLNG[1:0]		MEAS3_LED_SETLNG[1:0]		–	–	MEAS3_LED_RGE[1:0]	
0x33	MEAS3 LEDA Current[7:0]	MEAS3_DRVA_PA[7:0]							
0x34	MEAS3 LEDB Current[7:0]	MEAS3_DRVB_PA[7:0]							
0x35	MEAS3 PD SEL 1[7:0]	MEAS3_PD3_SEL[2:1]		MEAS3_PD2_SEL[2:0]			MEAS3_PD1_SEL[2:0]		
0x36	MEAS3 PD SEL 2[7:0]	MEAS3_PD6_SEL[2]	MEAS3_PD5_SEL[2:0]			MEAS3_PD4_SEL[2:0]			MEAS3_PD3_SEL[0]
0x37	MEAS3 PD SEL 3[7:0]	MEAS3_PD8_SEL[2:0]			MEAS3_PD7_SEL[2:0]			MEAS3_PD6_SEL[1:0]	
MEAS4 Setup									
0x38	MEAS4 Selects[7:0]	–	MEAS4_AMB	MEAS4_DRVB[2:0]			MEAS4_DRVA[2:0]		
0x39	MEAS4 Configuration 1[7:0]	–	MEAS4_DAC_LO_NOISE	MEAS4_FILT2_SEL	MEAS4_TINT[1:0]		MEAS4_AVER[2:0]		
0x3A	MEAS4 Configuration 2[7:0]	MEAS4_SINC3_SEL	MEAS4_FILT_SEL	–	–	MEAS4_PPG4_ADC_RGE	MEAS4_PPG3_ADC_RGE	MEAS4_PPG2_ADC_RGE	MEAS4_PPG1_ADC_RGE
0x3B	MEAS4 Configuration 3[7:0]	MEAS4_PPG2_DACOFF[3:0]				MEAS4_PPG1_DACOFF[3:0]			
0x3C	MEAS4 Configuration 4[7:0]	MEAS4_PPG4_DACOFF[3:0]				MEAS4_PPG3_DACOFF[3:0]			
0x3D	MEAS4 Configuration 5[7:0]	MEAS4_PD_SETLNG[1:0]		MEAS4_LED_SETLNG[1:0]		–	–	MEAS4_LED_RGE[1:0]	

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ADDRESS	NAME	MSB							LSB
0x3E	MEAS4 LEDA Current[7:0]	MEAS4_DRVA_PA[7:0]							
0x3F	MEAS4 LEDB Current[7:0]	MEAS4_DRVB_PA[7:0]							
0x40	MEAS4 PD SEL 1[7:0]	MEAS4_PD3_SEL[2:1]		MEAS4_PD2_SEL[2:0]			MEAS4_PD1_SEL[2:0]		
0x41	MEAS4 PD SEL 2[7:0]	MEAS4_PD6_SEL[2]	MEAS4_PD5_SEL[2:0]			MEAS4_PD4_SEL[2:0]			MEAS4_PD3_SEL[0]
0x42	MEAS4 PD SEL 3[7:0]	MEAS4_PD8_SEL[2:0]			MEAS4_PD7_SEL[2:0]			MEAS4_PD6_SEL[1:0]	
MEAS5 Setup									
0x43	MEAS5 Selects[7:0]	–	MEAS5_AMB	MEAS5_DRVB[2:0]			MEAS5_DRVA[2:0]		
0x44	MEAS5 Configuration 1[7:0]	–	MEAS5_DAC_LO_NOISE	MEAS5_FILT2_SEL	MEAS5_TINT[1:0]		MEAS5_AVER[2:0]		
0x45	MEAS5 Configuration 2[7:0]	MEAS5_SINC3_SEL	MEAS5_FILT_SEL	–	–	MEAS5_PPG4_ADC_RGE	MEAS5_PPG3_ADC_RGE	MEAS5_PPG2_ADC_RGE	MEAS5_PPG1_ADC_RGE
0x46	MEAS5 Configuration 3[7:0]	MEAS5_PPG2_DACOFF[3:0]				MEAS5_PPG1_DACOFF[3:0]			
0x47	MEAS5 Configuration 4[7:0]	MEAS5_PPG4_DACOFF[3:0]				MEAS5_PPG3_DACOFF[3:0]			
0x48	MEAS5 Configuration 5[7:0]	MEAS5_PD_SETLNG[1:0]		MEAS5_LED_SETLNG[1:0]		–	–	MEAS5_LED_RGE[1:0]	
0x49	MEAS5 LEDA Current[7:0]	MEAS5_DRVA_PA[7:0]							
0x4A	MEAS5 LEDB Current[7:0]	MEAS5_DRVB_PA[7:0]							
0x4B	MEAS5 PD SEL 1[7:0]	MEAS5_PD3_SEL[2:1]		MEAS5_PD2_SEL[2:0]			MEAS5_PD1_SEL[2:0]		
0x4C	MEAS5 PD SEL 2[7:0]	MEAS5_PD6_SEL[2]	MEAS5_PD5_SEL[2:0]			MEAS5_PD4_SEL[2:0]			MEAS5_PD3_SEL[0]
0x4D	MEAS5 PD SEL 3[7:0]	MEAS5_PD8_SEL[2:0]			MEAS5_PD7_SEL[2:0]			MEAS5_PD6_SEL[1:0]	
MEAS6 Setup									
0x4E	MEAS6 Selects[7:0]	–	MEAS6_AMB	MEAS6_DRVB[2:0]			MEAS6_DRVA[2:0]		
0x4F	MEAS6 Configuration 1[7:0]	–	MEAS6_DAC_LO_NOISE	MEAS6_FILT2_SEL	MEAS6_TINT[1:0]		MEAS6_AVER[2:0]		
0x50	MEAS6 Configuration 2[7:0]	MEAS6_SINC3_SEL	MEAS6_FILT_SEL	–	–	MEAS6_PPG4_ADC_RGE	MEAS6_PPG3_ADC_RGE	MEAS6_PPG2_ADC_RGE	MEAS6_PPG1_ADC_RGE
0x51	MEAS6 Configuration 3[7:0]	MEAS6_PPG2_DACOFF[3:0]				MEAS6_PPG1_DACOFF[3:0]			
0x52	MEAS6 Configuration 4[7:0]	MEAS6_PPG4_DACOFF[3:0]				MEAS6_PPG3_DACOFF[3:0]			

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ADDRESS	NAME	MSB							LSB
0x53	MEAS6 Configuration 5[7:0]	MEAS6_PD_SETLNG[1:0]		MEAS6_LED_SETLNG[1:0]		–	–	MEAS6_LED_RGE[1:0]	
0x54	MEAS6 LEDA Current[7:0]	MEAS6_DRVA_PA[7:0]							
0x55	MEAS6 LEDB Current[7:0]	MEAS6_DRVB_PA[7:0]							
0x56	MEAS6 PD SEL 1[7:0]	MEAS6_PD3_SEL[2:1]		MEAS6_PD2_SEL[2:0]			MEAS6_PD1_SEL[2:0]		
0x57	MEAS6 PD SEL 2[7:0]	MEAS6_PD6_SEL[2]	MEAS6_PD5_SEL[2:0]			MEAS6_PD4_SEL[2:0]			MEAS6_PD3_SEL[0]
0x58	MEAS6 PD SEL 3[7:0]	MEAS6_PD8_SEL[2:0]			MEAS6_PD7_SEL[2:0]			MEAS6_PD6_SEL[1:0]	
MEAS7 Setup									
0x59	MEAS7 Selects[7:0]	–	MEAS7_AMB	MEAS7_DRVB[2:0]			MEAS7_DRVA[2:0]		
0x5A	MEAS7 Configuration 1[7:0]	–	MEAS7_DAC_LO_NOISE	MEAS7_FILT2_SEL	MEAS7_TINT[1:0]		MEAS7_AVER[2:0]		
0x5B	MEAS7 Configuration 2[7:0]	MEAS7_SINC3_SEL	MEAS7_FILT_SEL	–	–	MEAS7_PPG4_ADC_RGE	MEAS7_PPG3_ADC_RGE	MEAS7_PPG2_ADC_RGE	MEAS7_PPG1_ADC_RGE
0x5C	MEAS7 Configuration 3[7:0]	MEAS7_PPG2_DACOFF[3:0]				MEAS7_PPG1_DACOFF[3:0]			
0x5D	MEAS7 Configuration 4[7:0]	MEAS7_PPG4_DACOFF[3:0]				MEAS7_PPG3_DACOFF[3:0]			
0x5E	MEAS7 Configuration 5[7:0]	MEAS7_PD_SETLNG[1:0]		MEAS7_LED_SETLNG[1:0]		–	–	MEAS7_LED_RGE[1:0]	
0x5F	MEAS7 LEDA Current[7:0]	MEAS7_DRVA_PA[7:0]							
0x60	MEAS7 LEDB Current[7:0]	MEAS7_DRVB_PA[7:0]							
0x61	MEAS7 PD SEL 1[7:0]	MEAS7_PD3_SEL[2:1]		MEAS7_PD2_SEL[2:0]			MEAS7_PD1_SEL[2:0]		
0x62	MEAS7 PD SEL 2[7:0]	MEAS7_PD6_SEL[2]	MEAS7_PD5_SEL[2:0]			MEAS7_PD4_SEL[2:0]			MEAS7_PD3_SEL[0]
0x63	MEAS7 PD SEL 3[7:0]	MEAS7_PD8_SEL[2:0]			MEAS7_PD7_SEL[2:0]			MEAS7_PD6_SEL[1:0]	
MEAS8 Setup									
0x64	MEAS8 Selects[7:0]	–	MEAS8_AMB	MEAS8_DRVB[2:0]			MEAS8_DRVA[2:0]		
0x65	MEAS8 Configuration 1[7:0]	–	MEAS8_DAC_LO_NOISE	MEAS8_FILT2_SEL	MEAS8_TINT[1:0]		MEAS8_AVER[2:0]		
0x66	MEAS8 Configuration 2[7:0]	MEAS8_SINC3_SEL	MEAS8_FILT_SEL	–	–	MEAS8_PPG4_ADC_RGE	MEAS8_PPG3_ADC_RGE	MEAS8_PPG2_ADC_RGE	MEAS8_PPG1_ADC_RGE
0x67	MEAS8 Configuration 3[7:0]	MEAS8_PPG2_DACOFF[3:0]				MEAS8_PPG1_DACOFF[3:0]			

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ADDRESS	NAME	MSB							LSB
0x68	MEAS8 Configuration 4[7:0]	MEAS8_PPG4_DACOFF[3:0]				MEAS8_PPG3_DACOFF[3:0]			
0x69	MEAS8 Configuration 5[7:0]	MEAS8_PD_SETLNG[1:0]		MEAS8_LED_SETLNG[1:0]		–	–	MEAS8_LED_RGE[1:0]	
0x6A	MEAS8 LEDA Current[7:0]	MEAS8_DRVA_PA[7:0]							
0x6B	MEAS8 LEDB Current[7:0]	MEAS8_DRVB_PA[7:0]							
0x6C	MEAS8 PD SEL 1[7:0]	MEAS8_PD3_SEL[2:1]		MEAS8_PD2_SEL[2:0]			MEAS8_PD1_SEL[2:0]		
0x6D	MEAS8 PD SEL 2[7:0]	MEAS8_PD6_SEL[2]	MEAS8_PD5_SEL[2:0]			MEAS8_PD4_SEL[2:0]			MEAS8_PD3_SEL[0]
0x6E	MEAS8 PD SEL 3[7:0]	MEAS8_PD8_SEL[2:0]			MEAS8_PD7_SEL[2:0]			MEAS8_PD6_SEL[1:0]	
MEAS9 Setup									
0x6F	MEAS9 Selects[7:0]	–	MEAS9_AMB	MEAS9_DRVB[2:0]			MEAS9_DRVA[2:0]		
0x70	MEAS9 Configuration 1[7:0]	–	MEAS9_DAC_LO_NOISE	MEAS9_FILT2_SEL	MEAS9_TINT[1:0]		MEAS9_AVER[2:0]		
0x71	MEAS9 Configuration 2[7:0]	MEAS9_SINC3_SEL	MEAS9_FILT_SEL	–	–	MEAS9_PPG4_ADC_RGE	MEAS9_PPG3_ADC_RGE	MEAS9_PPG2_ADC_RGE	MEAS9_PPG1_ADC_RGE
0x72	MEAS9 Configuration 3[7:0]	MEAS9_PPG2_DACOFF[3:0]				MEAS9_PPG1_DACOFF[3:0]			
0x73	MEAS9 Configuration 4[7:0]	MEAS9_PPG4_DACOFF[3:0]				MEAS9_PPG3_DACOFF[3:0]			
0x74	MEAS9 Configuration 5[7:0]	MEAS9_PD_SETLNG[1:0]		MEAS9_LED_SETLNG[1:0]		–	–	MEAS9_LED_RGE[1:0]	
0x75	MEAS9 LEDA Current[7:0]	MEAS9_DRVA_PA[7:0]							
0x76	MEAS9 LEDB Current[7:0]	MEAS9_DRVB_PA[7:0]							
0x77	MEAS9 PD SEL 1[7:0]	MEAS9_PD3_SEL[2:1]		MEAS9_PD2_SEL[2:0]			MEAS9_PD1_SEL[2:0]		
0x78	MEAS9 PD SEL 2[7:0]	MEAS9_PD6_SEL[2]	MEAS9_PD5_SEL[2:0]			MEAS9_PD4_SEL[2:0]			MEAS9_PD3_SEL[0]
0x79	MEAS9 PD SEL 3[7:0]	MEAS9_PD8_SEL[2:0]			MEAS9_PD7_SEL[2:0]			MEAS9_PD6_SEL[1:0]	
MEAS10 Setup									
0x7A	MEAS10 Selects[7:0]	–	MEAS10_AMB	MEAS10_DRVB[2:0]			MEAS10_DRVA[2:0]		
0x7B	MEAS10 Configuration 1[7:0]	–	MEAS10_DAC_LO_NOISE	MEAS10_FILT2_SEL	MEAS10_TINT[1:0]		MEAS10_AVER[2:0]		

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ADDRESS	NAME	MSB							LSB
0x7C	MEAS10 Configuration 2[7:0]	MEAS10_SINC3_SEL	MEAS10_FILT_SEL	–	–	MEAS10_PPG4_ADC_RGE	MEAS10_PPG3_ADC_RGE	MEAS10_PPG2_ADC_RGE	MEAS10_PPG1_ADC_RGE
0x7D	MEAS10 Configuration 3[7:0]	MEAS10_PPG2_DACOFF[3:0]				MEAS10_PPG1_DACOFF[3:0]			
0x7E	MEAS10 Configuration 4[7:0]	MEAS10_PPG4_DACOFF[3:0]				MEAS10_PPG3_DACOFF[3:0]			
0x7F	MEAS10 Configuration 5[7:0]	MEAS10_PD_SETLNG[1:0]		MEAS10_LED_SETLNG[1:0]		–	–	MEAS10_LED_RGE[1:0]	
0x80	MEAS10 LEDA Current[7:0]	MEAS10_DRVA_PA[7:0]							
0x81	MEAS10 LEDB Current[7:0]	MEAS10_DRVB_PA[7:0]							
0x82	MEAS10 PD SEL 1[7:0]	MEAS10_PD3_SEL[2:1]		MEAS10_PD2_SEL[2:0]			MEAS10_PD1_SEL[2:0]		
0x83	MEAS10 PD SEL 2[7:0]	MEAS10_PD6_SEL[2]	MEAS10_PD5_SEL[2:0]			MEAS10_PD4_SEL[2:0]			MEAS10_PD3_SEL[0]
0x84	MEAS10 PD SEL 3[7:0]	MEAS10_PD8_SEL[2:0]			MEAS10_PD7_SEL[2:0]			MEAS10_PD6_SEL[1:0]	
MEAS11 Setup									
0x85	MEAS11 Selects[7:0]	–	MEAS11_AMB	MEAS11_DRVB[2:0]			MEAS11_DRVA[2:0]		
0x86	MEAS11 Configuration 1[7:0]	–	MEAS11_DAC_LO_NOISE	MEAS11_FILT2_SEL	MEAS11_TINT[1:0]		MEAS11_AVER[2:0]		
0x87	MEAS11 Configuration 2[7:0]	MEAS11_SINC3_SEL	MEAS11_FILT_SEL	–	–	MEAS11_PPG4_ADC_RGE	MEAS11_PPG3_ADC_RGE	MEAS11_PPG2_ADC_RGE	MEAS11_PPG1_ADC_RGE
0x88	MEAS11 Configuration 3[7:0]	MEAS11_PPG2_DACOFF[3:0]				MEAS11_PPG1_DACOFF[3:0]			
0x89	MEAS11 Configuration 4[7:0]	MEAS11_PPG4_DACOFF[3:0]				MEAS11_PPG3_DACOFF[3:0]			
0x8A	MEAS11 Configuration 5[7:0]	MEAS11_PD_SETLNG[1:0]		MEAS11_LED_SETLNG[1:0]		–	–	MEAS11_LED_RGE[1:0]	
0x8B	MEAS11 LEDA Current[7:0]	MEAS11_DRVA_PA[7:0]							
0x8C	MEAS11 LEDB Current[7:0]	MEAS11_DRVB_PA[7:0]							
0x8D	MEAS11 PD SEL 1[7:0]	MEAS11_PD3_SEL[2:1]		MEAS11_PD2_SEL[2:0]			MEAS11_PD1_SEL[2:0]		
0x8E	MEAS11 PD SEL 2[7:0]	MEAS11_PD6_SEL[2]	MEAS11_PD5_SEL[2:0]			MEAS11_PD4_SEL[2:0]			MEAS11_PD3_SEL[0]
0x8F	MEAS11 PD SEL 3[7:0]	MEAS11_PD8_SEL[2:0]			MEAS11_PD7_SEL[2:0]			MEAS11_PD6_SEL[1:0]	

ADDRESS	NAME	MSB							LSB
MEAS12 Setup									
0x90	MEAS12 Selects[7:0]	–	MEAS12_AMB	MEAS12_DRVB[2:0]			MEAS12_DRVA[2:0]		
0x91	MEAS12 Configuration 1[7:0]	–	MEAS12_DAC_LO_NOISE	MEAS12_FILT2_SEL	MEAS12_TINT[1:0]		MEAS12_AVER[2:0]		
0x92	MEAS12 Configuration 2[7:0]	MEAS12_SINC3_SEL	MEAS12_FILT_SEL	–	–	MEAS12_PPG4_ADC_RGE	MEAS12_PPG3_ADC_RGE	MEAS12_PPG2_ADC_RGE	MEAS12_PPG1_ADC_RGE
0x93	MEAS12 Configuration 3[7:0]	MEAS12_PPG2_DACOFF[3:0]				MEAS12_PPG1_DACOFF[3:0]			
0x94	MEAS12 Configuration 4[7:0]	MEAS12_PPG4_DACOFF[3:0]				MEAS12_PPG3_DACOFF[3:0]			
0x95	MEAS12 Configuration 5[7:0]	MEAS12_PD_SETLNG[1:0]		MEAS12_LED_SETLNG[1:0]		–	–	MEAS12_LED_RGE[1:0]	
0x96	MEAS12 LEDA Current[7:0]	MEAS12_DRVA_PA[7:0]							
0x97	MEAS12 LEDB Current[7:0]	MEAS12_DRVB_PA[7:0]							
0x98	MEAS12 PD SEL 1[7:0]	MEAS12_PD3_SEL[2:1]		MEAS12_PD2_SEL[2:0]			MEAS12_PD1_SEL[2:0]		
0x99	MEAS12 PD SEL 2[7:0]	MEAS12_PD6_SEL[2]	MEAS12_PD5_SEL[2:0]			MEAS12_PD4_SEL[2:0]			MEAS12_PD3_SEL[0]
0x9A	MEAS12 PD SEL 3[7:0]	MEAS12_PD8_SEL[2:0]			MEAS12_PD7_SEL[2:0]			MEAS12_PD6_SEL[1:0]	
MEAS13 Setup									
0x9B	MEAS13 Selects[7:0]	–	MEAS13_AMB	MEAS13_DRVB[2:0]			MEAS13_DRVA[2:0]		
0x9C	MEAS13 Configuration 1[7:0]	–	MEAS13_DAC_LO_NOISE	MEAS13_FILT2_SEL	MEAS13_TINT[1:0]		MEAS13_AVER[2:0]		
0x9D	MEAS13 Configuration 2[7:0]	MEAS13_SINC3_SEL	MEAS13_FILT_SEL	–	–	MEAS13_PPG4_ADC_RGE	MEAS13_PPG3_ADC_RGE	MEAS13_PPG2_ADC_RGE	MEAS13_PPG1_ADC_RGE
0x9E	MEAS13 Configuration 3[7:0]	MEAS13_PPG2_DACOFF[3:0]				MEAS13_PPG1_DACOFF[3:0]			
0x9F	MEAS13 Configuration 4[7:0]	MEAS13_PPG4_DACOFF[3:0]				MEAS13_PPG3_DACOFF[3:0]			
0xA0	MEAS13 Configuration 5[7:0]	MEAS13_PD_SETLNG[1:0]		MEAS13_LED_SETLNG[1:0]		–	–	MEAS13_LED_RGE[1:0]	
0xA1	MEAS13 LEDA Current[7:0]	MEAS13_DRVA_PA[7:0]							
0xA2	MEAS13 LEDB Current[7:0]	MEAS13_DRVB_PA[7:0]							
0xA3	MEAS13 PD SEL 1[7:0]	MEAS13_PD3_SEL[2:1]		MEAS13_PD2_SEL[2:0]			MEAS13_PD1_SEL[2:0]		

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ADDRESS	NAME	MSB							LSB
0xA4	MEAS13 PD SEL 2[7:0]	MEAS13_PD6_SEL[2]	MEAS13_PD5_SEL[2:0]			MEAS13_PD4_SEL[2:0]			MEAS13_PD3_SEL[0]
0xA5	MEAS13 PD SEL 3[7:0]	MEAS13_PD8_SEL[2:0]			MEAS13_PD7_SEL[2:0]			MEAS3_PD6_SEL[1:0]	
MEAS14 Setup									
0xA6	MEAS14 Selects[7:0]	–	MEAS14_AMB	MEAS14_DRVB[2:0]			MEAS14_DRVA[2:0]		
0xA7	MEAS14 Configuration 1[7:0]	–	MEAS14_DAC_LO_NOISE	MEAS14_FILT2_SEL	MEAS14_TINT[1:0]		MEAS14_AVER[2:0]		
0xA8	MEAS14 Configuration 2[7:0]	MEAS14_SINC3_SEL	MEAS14_FILT_SEL	–	–	MEAS14_PPG4_ADC_RGE	MEAS14_PPG3_ADC_RGE	MEAS14_PPG2_ADC_RGE	MEAS14_PPG1_ADC_RGE
0xA9	MEAS14 Configuration 3[7:0]	MEAS14_PPG2_DACOFF[3:0]				MEAS14_PPG1_DACOFF[3:0]			
0xAA	MEAS14 Configuration 4[7:0]	MEAS14_PPG4_DACOFF[3:0]				MEAS14_PPG3_DACOFF[3:0]			
0xAB	MEAS14 Configuration 5[7:0]	MEAS14_PD_SETLNG[1:0]		MEAS14_LED_SETLNG[1:0]		–	–	MEAS14_LED_RGE[1:0]	
0xAC	MEAS14 LEDA Current[7:0]	MEAS14_DRVA_PA[7:0]							
0xAD	MEAS14 LEDB Current[7:0]	MEAS14_DRVB_PA[7:0]							
0xAE	MEAS14 PD SEL 1[7:0]	MEAS14_PD3_SEL[2:1]		MEAS14_PD2_SEL[2:0]			MEAS14_PD1_SEL[2:0]		
0xAF	MEAS14 PD SEL 2[7:0]	MEAS14_PD6_SEL[2]	MEAS14_PD5_SEL[2:0]			MEAS14_PD4_SEL[2:0]			MEAS14_PD3_SEL[0]
0xB0	MEAS14 PD SEL 3[7:0]	MEAS14_PD8_SEL[2:0]			MEAS14_PD7_SEL[2:0]			MEAS14_PD6_SEL[1:0]	
MEAS15 Setup									
0xB1	MEAS15 Selects[7:0]	–	MEAS15_AMB	MEAS15_DRVB[2:0]			MEAS15_DRVA[2:0]		
0xB2	MEAS15 Configuration 1[7:0]	–	MEAS15_DAC_LO_NOISE	MEAS15_FILT2_SEL	MEAS15_TINT[1:0]		MEAS15_AVER[2:0]		
0xB3	MEAS15 Configuration 2[7:0]	MEAS15_SINC3_SEL	MEAS15_FILT_SEL	–	–	MEAS15_PPG4_ADC_RGE	MEAS15_PPG3_ADC_RGE	MEAS15_PPG2_ADC_RGE	MEAS15_PPG1_ADC_RGE
0xB4	MEAS15 Configuration 3[7:0]	MEAS15_PPG2_DACOFF[3:0]				MEAS15_PPG1_DACOFF[3:0]			
0xB5	MEAS15 Configuration 4[7:0]	MEAS15_PPG4_DACOFF[3:0]				MEAS15_PPG3_DACOFF[3:0]			
0xB6	MEAS15 Configuration 5[7:0]	MEAS15_PD_SETLNG[1:0]		MEAS15_LED_SETLNG[1:0]		–	–	MEAS15_LED_RGE[1:0]	

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ADDRESS	NAME	MSB							LSB
0xB7	MEAS15 LEDA Current[7:0]	MEAS15_DRVA_PA[7:0]							
0xB8	MEAS15 LEDB Current[7:0]	MEAS15_DRVB_PA[7:0]							
0xB9	MEAS15 PD SEL 1[7:0]	MEAS15_PD3_SEL[2:1]		MEAS15_PD2_SEL[2:0]			MEAS15_PD1_SEL[2:0]		
0xBA	MEAS15 PD SEL 2[7:0]	MEAS15_PD6_SEL[2]	MEAS15_PD5_SEL[2:0]			MEAS15_PD4_SEL[2:0]			MEAS15_PD3_SEL[0]
0xBB	MEAS15 PD SEL 3[7:0]	MEAS15_PD8_SEL[2:0]			MEAS15_PD7_SEL[2:0]			MEAS15_PD6_SEL[1:0]	
MEAS16 Setup									
0xBC	MEAS16 Selects[7:0]	–	MEAS16_AMB	MEAS16_DRVB[2:0]			MEAS16_DRVA[2:0]		
0xBD	MEAS16 Configuration 1[7:0]	–	MEAS16_DAC_LO_NOISE	MEAS16_FILT2_SEL	MEAS16_TINT[1:0]		MEAS16_AVER[2:0]		
0xBE	MEAS16 Configuration 2[7:0]	MEAS16_SINC3_SEL	MEAS16_FILT_SEL	–	–	MEAS16_PPG4_ADC_RGE	MEAS16_PPG3_ADC_RGE	MEAS16_PPG2_ADC_RGE	MEAS16_PPG1_ADC_RGE
0xBF	MEAS16 Configuration 3[7:0]	MEAS16_PPG2_DACOFF[3:0]				MEAS16_PPG1_DACOFF[3:0]			
0xC0	MEAS16 Configuration 4[7:0]	MEAS16_PPG4_DACOFF[3:0]				MEAS16_PPG3_DACOFF[3:0]			
0xC1	MEAS16 Configuration 5[7:0]	MEAS16_PD_SETLNG[1:0]		MEAS16_LED_SETLNG[1:0]		–	–	MEAS16_LED_RGE[1:0]	
0xC2	MEAS16 LEDA Current[7:0]	MEAS16_DRVA_PA[7:0]							
0xC3	MEAS16 LEDB Current[7:0]	MEAS16_DRVB_PA[7:0]							
0xC4	MEAS16 PD SEL 1[7:0]	MEAS16_PD3_SEL[2:1]		MEAS16_PD2_SEL[2:0]			MEAS16_PD1_SEL[2:0]		
0xC5	MEAS16 PD SEL 2[7:0]	MEAS16_PD6_SEL[2]	MEAS16_PD5_SEL[2:0]			MEAS16_PD4_SEL[2:0]			MEAS16_PD3_SEL[0]
0xC6	MEAS16 PD SEL 3[7:0]	MEAS16_PD8_SEL[2:0]			MEAS16_PD7_SEL[2:0]			MEAS16_PD6_SEL[1:0]	
MEAS17 Setup									
0xC7	MEAS17 Selects[7:0]	–	MEAS17_AMB	MEAS17_DRVB[2:0]			MEAS17_DRVA[2:0]		
0xC8	MEAS17 Configuration 1[7:0]	–	MEAS17_DAC_LO_NOISE	MEAS17_FILT2_SEL	MEAS17_TINT[1:0]		MEAS17_AVER[2:0]		
0xC9	MEAS17 Configuration 2[7:0]	MEAS17_SINC3_SEL	MEAS17_FILT_SEL	–	–	MEAS17_PPG4_ADC_RGE	MEAS17_PPG3_ADC_RGE	MEAS17_PPG2_ADC_RGE	MEAS17_PPG1_ADC_RGE

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ADDRESS	NAME	MSB							LSB
0xCA	MEAS17 Configuration 3[7:0]	MEAS17_PPG2_DACOFF[3:0]				MEAS17_PPG1_DACOFF[3:0]			
0xCB	MEAS17 Configuration 4[7:0]	MEAS17_PPG4_DACOFF[3:0]				MEAS17_PPG3_DACOFF[3:0]			
0xCC	MEAS17 Configuration 5[7:0]	MEAS17_PD_SETLNG[1:0]		MEAS17_LED_SETLNG[1:0]		–	–	MEAS17_LED_RGE[1:0]	
0xCD	MEAS17 LEDA Current[7:0]	MEAS17_DRVA_PA[7:0]							
0xCE	MEAS17 LEDB Current[7:0]	MEAS17_DRVB_PA[7:0]							
0xCF	MEAS17 PD SEL 1[7:0]	MEAS17_PD3_SEL[2:1]		MEAS17_PD2_SEL[2:0]			MEAS17_PD1_SEL[2:0]		
0xD0	MEAS17 PD SEL 2[7:0]	MEAS17_PD6_SEL[2]	MEAS17_PD5_SEL[2:0]			MEAS17_PD4_SEL[2:0]			MEAS17_PD3_SEL[0]
0xD1	MEAS17 PD SEL 3[7:0]	MEAS17_PD8_SEL[2:0]			MEAS17_PD7_SEL[2:0]			MEAS17_PD6_SEL[1:0]	
MEAS18 Setup									
0xD2	MEAS18 Selects[7:0]	–	MEAS18_AMB	MEAS18_DRVB[2:0]			MEAS18_DRVA[2:0]		
0xD3	MEAS18 Configuration 1[7:0]	–	MEAS18_DAC_LO_NOISE	MEAS18_FILT2_SEL	MEAS18_TINT[1:0]		MEAS18_AVER[2:0]		
0xD4	MEAS18 Configuration 2[7:0]	MEAS18_SINC3_SEL	MEAS18_FILT_SEL	–	–	MEAS18_PPG4_ADC_RGE	MEAS18_PPG3_ADC_RGE	MEAS18_PPG2_ADC_RGE	MEAS18_PPG1_ADC_RGE
0xD5	MEAS18 Configuration 3[7:0]	MEAS18_PPG2_DACOFF[3:0]				MEAS18_PPG1_DACOFF[3:0]			
0xD6	MEAS18 Configuration 4[7:0]	MEAS18_PPG4_DACOFF[3:0]				MEAS18_PPG3_DACOFF[3:0]			
0xD7	MEAS18 Configuration 5[7:0]	MEAS18_PD_SETLNG[1:0]		MEAS18_LED_SETLNG[1:0]		–	–	MEAS18_LED_RGE[1:0]	
0xD8	MEAS18 LEDA Current[7:0]	MEAS18_DRVA_PA[7:0]							
0xD9	MEAS18 LEDB Current[7:0]	MEAS18_DRVB_PA[7:0]							
0xDA	MEAS18 PD SEL 1[7:0]	MEAS18_PD3_SEL[2:1]		MEAS18_PD2_SEL[2:0]			MEAS18_PD1_SEL[2:0]		
0xDB	MEAS18 PD SEL 2[7:0]	MEAS18_PD6_SEL[2]	MEAS18_PD5_SEL[2:0]			MEAS18_PD4_SEL[2:0]			MEAS18_PD3_SEL[0]
0xDC	MEAS18 PD SEL 3[7:0]	MEAS18_PD8_SEL[2:0]			MEAS18_PD7_SEL[2:0]			MEAS18_PD6_SEL[1:0]	
MEAS19 Setup									
0xDD	MEAS19 Selects[7:0]	–	MEAS19_AMB	MEAS19_DRVB[2:0]			MEAS19_DRVA[2:0]		

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ADDRESS	NAME	MSB							LSB
0xDE	MEAS19 Configuration 1[7:0]	–	MEAS19_DAC_LO_NOISE	MEAS19_FILT2_SEL	MEAS19_TINT[1:0]		MEAS19_AVER[2:0]		
0xDF	MEAS19 Configuration 2[7:0]	MEAS19_SINC3_SEL	MEAS19_FILT_SEL	–	–	MEAS19_PPG4_ADC_RGE	MEAS19_PPG3_ADC_RGE	MEAS19_PPG2_ADC_RGE	MEAS19_PPG1_ADC_RGE
0xE0	MEAS19 Configuration 3[7:0]	MEAS19_PPG2_DACOFF[3:0]				MEAS19_PPG1_DACOFF[3:0]			
0xE1	MEAS19 Configuration 4[7:0]	MEAS19_PPG4_DACOFF[3:0]				MEAS19_PPG3_DACOFF[3:0]			
0xE2	MEAS19 Configuration 5[7:0]	MEAS19_PD_SETLNG[1:0]		MEAS19_LED_SETLNG[1:0]		–	–	MEAS19_LED_RGE[1:0]	
0xE3	MEAS19 LEDA Current[7:0]	MEAS19_DRVA_PA[7:0]							
0xE4	MEAS19 LEDB Current[7:0]	MEAS19_DRVB_PA[7:0]							
0xE5	MEAS19 PD SEL 1[7:0]	MEAS19_PD3_SEL[2:1]		MEAS19_PD2_SEL[2:0]			MEAS19_PD1_SEL[2:0]		
0xE6	MEAS19 PD SEL 2[7:0]	MEAS19_PD6_SEL[2]	MEAS19_PD5_SEL[2:0]			MEAS19_PD4_SEL[2:0]			MEAS19_PD3_SEL[0]
0xE7	MEAS19 PD SEL 3[7:0]	MEAS19_PD8_SEL[2:0]			MEAS19_PD7_SEL[2:0]			MEAS19_PD6_SEL[1:0]	
MEAS20 Setup									
0xE8	MEAS20 Selects[7:0]	–	MEAS20_AMB	MEAS20_DRVB[2:0]			MEAS20_DRVA[2:0]		
0xE9	MEAS20 Configuration 1[7:0]	–	MEAS20_DAC_LO_NOISE	MEAS20_FILT2_SEL	MEAS20_TINT[1:0]		MEAS20_AVER[2:0]		
0xEA	MEAS20 Configuration 2[7:0]	MEAS20_SINC3_SEL	MEAS20_FILT_SEL	–	–	MEAS20_PPG4_ADC_RGE	MEAS20_PPG3_ADC_RGE	MEAS20_PPG2_ADC_RGE	MEAS20_PPG1_ADC_RGE
0xEB	MEAS20 Configuration 3[7:0]	MEAS20_PPG2_DACOFF[3:0]				MEAS20_PPG1_DACOFF[3:0]			
0xEC	MEAS20 Configuration 4[7:0]	MEAS20_PPG4_DACOFF[3:0]				MEAS20_PPG3_DACOFF[3:0]			
0xED	MEAS20 Configuration 5[7:0]	MEAS20_PD_SETLNG[1:0]		MEAS20_LED_SETLNG[1:0]		–	–	MEAS20_LED_RGE[1:0]	
0xEE	MEAS20 LEDA Current[7:0]	MEAS20_DRVA_PA[7:0]							
0xEF	MEAS20 LEDB Current[7:0]	MEAS20_DRVB_PA[7:0]							
0xF0	MEAS20 PD SEL 1[7:0]	MEAS20_PD3_SEL[2:1]		MEAS20_PD2_SEL[2:0]			MEAS20_PD1_SEL[2:0]		
0xF1	MEAS20 PD SEL 2[7:0]	MEAS20_PD6_SEL[2]	MEAS20_PD5_SEL[2:0]			MEAS20_PD4_SEL[2:0]			MEAS20_PD3_SEL[0]

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ADDRESS	NAME	MSB							LSB
0xF2	MEAS20 PD SEL 3[7:0]	MEAS20_PD8_SEL[2:0]			MEAS20_PD7_SEL[2:0]			MEAS20_PD6_SEL[1:0]	
Threshold Interrupts									
0xF3	THRESHOLD1 MEAS SEL[7:0]	THRESH1_PPG_SEL[1:0]		–	THRESH1_MEAS_SEL[4:0]				
0xF4	THRESHOLD2 MEAS SEL[7:0]	THRESH2_PPG_SEL[1:0]		–	THRESH2_MEAS_SEL[4:0]				
0xF5	THRESHOLD HYST[7:0]	–	–	–	TIME_HYST[1:0]		LEVEL_HYST[2:0]		
0xF6	PPG HI THRESHOLD1[7:0]	THRESHOLD1_UPPER[7:0]							
0xF7	PPG LO THRESHOLD1[7:0]	THRESHOLD1_LOWER[7:0]							
0xF8	PPG HI THRESHOLD2[7:0]	THRESHOLD2_UPPER[7:0]							
0xF9	PPG LO THRESHOLD2[7:0]	THRESHOLD2_LOWER[7:0]							
Interrupt Enables									
0xFA	Interrupt1 Enable 1[7:0]	A_FULL_EN1	FRAME_RDY_EN1	FIFO_DATA_RDY_EN1	ALC_OVF_EN1	EXP_OVF_EN1	THRESH2_HILO_EN1	THRESH1_HILO_EN1	LED_TX_EN1
0xFB	Interrupt1 Enable 2[7:0]	INVALID_CFG_EN1	–	LED6_COMPB_EN1	LED5_COMPB_EN1	LED4_COMPB_EN1	LED3_COMPB_EN1	LED2_COMPB_EN1	LED1_COMPB_EN1
0xFC	Interrupt2 Enable 1[7:0]	A_FULL_EN2	FRAME_RDY_EN2	FIFO_DATA_RDY_EN2	ALC_OVF_EN2	EXP_OVF_EN2	THRESH2_HILO_EN2	THRESH1_HILO_EN2	LED_TX_EN2
0xFD	Interrupt2 Enable 2[7:0]	INVALID_CFG_EN2	–	LED6_COMPB_EN2	LED5_COMPB_EN2	LED4_COMPB_EN2	LED3_COMPB_EN2	LED2_COMPB_EN2	LED1_COMPB_EN2
Part ID									
0xFF	Part ID[7:0]	PART_ID[7:0]							

Register Details

Status 1 (0x00)

BIT	7	6	5	4	3	2	1	0
Field	A_FULL	FRAME_RDY	FIFO_DATA_RDY	ALC_OVF	EXP_OVF	THRESH2_HILO	THRESH1_HILO	PWR_RDY
Reset	0	0	0	0	0	0	0	1
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

A_FULL

A_FULL is set to 1 when the FIFO has reached the threshold programmed in the FIFO_A_FULL register. This is a read-only bit. This bit is cleared when the Status 1 Register is read. It is also cleared when FIFO Data Register is read, if FIFO_STAT_CLR = 1.

A_FULL	DECODE

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0	Normal Operation.
1	Indicates that the FIFO buffer has reached the threshold set by FIFO_A_FULL[8:0].

FRAME_RDY

A frame consists of FIFO data for all the PPG ADC conversions for the sequence programmed in the MEASx (x = 1 to 20) enable registers. FRAME_RDY bit is set to 1 when a full-frame conversion has completed. This is a read-only bit and it is cleared by reading the Status 1 Register (0x00). It is also cleared by reading the FIFO Data Register if FIFO_STAT_CLR = 1.

FRAME_RDY	DECODE
0	Normal Operation.
1	This interrupt triggers when a complete sample is available in the FIFO.

FIFO_DATA_RDY

FIFO_DATA_RDY bit is set to 1 when new data is available in the FIFO. This is a read-only bit and it is cleared by reading the Status 1 register (0x00). It is also cleared by reading the FIFO Data Register if FIFO_STAT_CLR = 1.

FIFO_DATA_RDY	DECODE
0	Normal Operation.
1	There is new data in the FIFO.

ALC_OVF

ALC_OVF bit is set to 1 when a dark current measurement is either under ranged or over ranged for any of the assigned measurements. This is a read-only bit and is cleared by reading the Status 1 register (0x00). A measurement is over ranged if it is positive full-scale (0x7FFFF, 524287), and under ranged if it is less than negative full-scale/4 (< 0xE0000, -131072).

ALC_OVF	DECODE
0	Normal Operation.
1	The ambient light cancellation function of the photodiode has reached its maximum limit due to overflow, and, therefore, ambient light is affecting the output of the ADC.

EXP_OVF

EXP_OVF bit is set to 1 when an exposure current measurement is either under ranged or over ranged. It is also set to 1 if photodiode forward bias is detected. This is a read-only bit and is cleared by reading the Status 1 register (0x00). A measurement is over ranged if it is positive full-scale (0x7FFFF, 524287), and under ranged if it is less than negative full-scale/4 (< 0xE0000, -131072).

EXP_OVF	DECODE
0	Normal Operation.
1	The exposure signal has reached its maximum limit due to overflow.

THRESH2_HILO

THRESH2_HILO bit is set to 1 when the THRESH2_MEAS instance as defined qualifies as above the THRESHOLD2_UPPER or below the THRESHOLD2_LOWER. This is a read-only bit and is cleared by reading the Status 1 register (0x00).

For a complete explanation of how the two threshold instances operate, see the Threshold Event Generator section in the Detailed Description.

THRESH2_HILO	DECODE
0	ADC reading is below the defined THRESHOLD2_UPPER level and above the THRESHOLD2_LOWER level.

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1	ADC reading is above the defined THRESHOLD2_UPPER level or below the THRESHOLD2_LOWER level.

THRESH1_HILO

THRESH1_HILO bit is set to 1 when the THRESH1_MEAS instance as defined qualifies as above the THRESHOLD1_UPPER or below the THRESHOLD1_LOWER. This is a read-only bit and is cleared by reading the Status 1 register (0x00).

For a complete explanation of how the two threshold instances operate, see the Threshold Event Generator section in the Detailed Description.

THRESH1_HILO	DECODE
0	ADC reading is below the defined THRESHOLD1_UPPER level and above the THRESHOLD1_LOWER level.
1	ADC reading is above the defined THRESHOLD1_UPPER level or below the THRESHOLD1_LOWER level.

PWR_RDY

PWR_RDY bit is set to 1 when V_{DD_ANA} or V_{DD_DIG} had gone below undervoltage lockout (UVLO) threshold , which is approximately 1.3V. If this condition occurs, all registers within the MAX86177 are reset to their PORb state. This bit is not triggered by a soft reset. This is a read-only bit and is cleared when Status 1 register is read, or by setting SHDN bit to 1.

PWR_RDY is a non-maskable interrupt. So it gets asserted only on INT1.

PWR_RDY	DECODE
0	Normal Operation.
1	Indicates that V_{DD_ANA} or V_{DD_DIG} went below the UVLO threshold.

Status 2 (0x01)

BIT	7	6	5	4	3	2	1	0
Field	INVALID_CFG	–	LED6_COMPB	LED5_COMPB	LED4_COMPB	LED3_COMPB	LED2_COMPB	LED1_COMPB
Reset	0	–	0	0	0	0	0	0
Access Type	Read Only	–	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

INVALID_CFG

INVALID_CFG is set to 1 when the Frame Rate programmed using the clock dividers FR_CLK_DIV_H[6:0] and FR_CLK_DIV_L[7:0] is too fast to accommodate the measurement sequences enabled in a frame. This is a read-only bit and it gets cleared when the Status 2 register is read.

INVALID_CFG	DECODE
0	Configuration timing is valid.
1	Configuration timing is not valid.

LED6_COMPB

LEDn (n = 1 to 6) is not compliant. If the LEDn_DRV pin voltage drops below the compliance voltage threshold at the end of each exposure interval, the LEDn_COMPB status bit is asserted. LEDn_COMPB is a read-only bit. It is cleared when the corresponding status register is read.

LEDn_COMPLIANTB (n = 1 to 6)	DECODE
0	LEDn_DRV pin has sufficient voltage for the driver to be saturated.

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1	LEDn_DRV pin voltage is below compliance. Power supply rejection on LEDn is degraded and LEDn current inaccurate.

LED5_COMPB

For details, see the LED6_COMPB.

LED4_COMPB

For details, see the LED6_COMPB.

LED3_COMPB

For details, see the LED6_COMPB.

LED2_COMPB

For details, see the LED6_COMPB.

LED1_COMPB

For details, see the LED6_COMPB.

FIFO Write Pointer (0x02)

BIT	7	6	5	4	3	2	1	0
Field	FIFO_WR_PTR[7:0]							
Reset	0x00							
Access Type	Read Only							

FIFO_WR_PTR

FIFO_WR_PTR[7:0] has the lower 8 bits of the 9-bit FIFO_WR_PTR[8:0]. The most significant bit is in the FIFO_WR_PTR[8] at register address 0x03.

FIFO_WR_PTR[8:0] is a read-only register, which points to the FIFO location where the next data is written. This pointer advances for each data item pushed on to the FIFO by the internal conversion process. The write pointer is a 9-bit counter and wraps around to count 0x000 on the next data after count 0x1FF.

FIFO Counter 1 (0x03)

BIT	7	6	5	4	3	2	1	0
Field	FIFO_DATA_COUNT[9:8]		OVF_COUNTER[4:0]					FIFO_WR_PTR[8]
Reset	0x0		0x00					0
Access Type	Read Only		Read Only					Read Only

FIFO_DATA_COUNT

FIFO_DATA_COUNT[9:8] has two most significant bits of the 10-bit FIFO_DATA_COUNT[9:0] register. The lower 8 bits are in the FIFO_DATA_COUNT_LSB[7:0] at register address 0x04.

FIFO_DATA_COUNT[9:0] is a read-only register which holds the number of items available in the FIFO for the host to read. This increments when a new item is pushed to the FIFO, and decrements when the host reads an item from the FIFO.

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OVF_COUNTER

OVF_COUNTER[4:0] logs the number of data items lost if the FIFO is not read in a timely fashion. This counter holds/saturates at the count value 0x1F. When a complete data item is popped from the FIFO (when the read pointer advances), the OVF_COUNTER is reset to zero. This counter is essentially a debug tool. It should be read immediately before reading the FIFO in order to check if an overflow condition has occurred. For more details, see the FIFO_RO.

FIFO_WR_PTR

FIFO_WR_PTR[8] has the most significant bit of the 9-bit FIFO_WR_PTR[8:0].

For details, see the FIFO_WR_PTR[7:0] at register address 0x02.

FIFO Counter 2 (0x04)

BIT	7	6	5	4	3	2	1	0
Field	FIFO_DATA_COUNT[7:0]							
Reset	0x00							
Access Type	Read Only							

FIFO_DATA_COUNT

FIFO_DATA_COUNT[7:0] is a read-only register which holds the lower 8 bits of the number of items available in the FIFO for the host to read.

For details, see the FIFO_DATA_COUNT[9:8] at register address 0x03 description.

FIFO Read Pointer (0x05)

BIT	7	6	5	4	3	2	1	0
Field	FIFO_RD_PTR[7:0]							
Reset	0x00							
Access Type	Read Only							

FIFO_RD_PTR

FIFO_RD_PTR[7:0] holds the lower 8 bits of the 9-bit FIFO_RD_PTR[8:0]. The most significant bit is in the FIFO_RD_PTR[8] at register address 0x06. FIFO_RD_PTR[8:0] is a read-only register, which points to the location from where the next data from the FIFO is read via the serial interface. This advances each time a data item is read from the FIFO. The read pointer is updated from a 9-bit counter and wrapped around to count 0x000 from count 0x1FF.

FIFO Configuration 1 (0x06)

BIT	7	6	5	4	3	2	1	0
Field	FIFO_A_FULL[8]	–	–	–	–	–	–	FIFO_RD_PTR[8]
Reset	0	–	–	–	–	–	–	0
Access Type	Write, Read	–	–	–	–	–	–	Read Only

FIFO_A_FULL

The FIFO_A_FULL[8:0] field in the FIFO Configuration 1 and FIFO Configuration 2 registers (0x06, and 0x07) sets the watermark for the FIFO and determines when the A_FULL bit in the Status register (0x00) gets asserted.

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The A_FULL bit is set when the number of data in FIFO is equal to 512 minus FIFO_A_FULL[8:0]. The interrupt is routed to the INT1 if A_FULL_EN1 mask bit in the Interrupt 1 Enable 1 register (0xFA) is set, and on the INT2 pin if A_FULL_EN2 mask bit in Interrupt 2 Enable 1 register (0xFC) is set. This condition should prompt the applications processor to read samples from the FIFO immediately. The A_FULL bit is cleared when the status register is read.

The application processor can read both the FIFO_WR_PTR[8:0] and FIFO_RD_PTR[8:0] to calculate the number of data items available in the FIFO, or just read the OVF_COUNTER[4:0] and FIFO_DATA_COUNT[9:0] registers, and read as many data items as it needs to empty the FIFO.

Alternatively, if the application always responds much faster than the selected sample rate, it can read 512 minus FIFO_A_FULL[8:0] number of data items every time it gets an A_FULL interrupt and be assured that all data from the FIFO are read. This is the preferred way to minimize the traffic on the serial interface. FIFO_WR_PTR, FIFO_RD_PTR, FIFO_DATA_COUNT, and OVF_COUNTER registers are available for debug purposes, if needed.

For example, if set to 0x0F (decimal 15), the A_FULL interrupt triggers when there are 15 empty spaces left (497 entries), and so on.

FIFO_A_FULL[8:0]	FREE SPACE BEFORE INTERRUPT	NUMBER OF SAMPLES IN FIFO
0x000	0	512
0x001	1	511
0x002	2	510
0x003	3	509
----	----	----
0x1FE	510	2
0x1FF	511	1

FIFO_RD_PTR

FIFO_RD_PTR[8] has the most significant bit of the 9-bit FIFO_RD_PTR[8:0].

For details, see the FIFO_RD_PTR[7:0] at register address 0x05.

FIFO Configuration 2 (0x07)

BIT	7	6	5	4	3	2	1	0
Field	FIFO_A_FULL[7:0]							
Reset	0xFF							
Access Type	Write, Read							

FIFO_A_FULL

FIFO_A_FULL[7:0] has the lower byte of the 9-bit FIFO_A_FULL[8:0] register. The most significant bit is in FIFO_A_FULL[8] register.

For details, see the FIFO_A_FULL[8] register description.

FIFO Data Register (0x08)

BIT	7	6	5	4	3	2	1	0
Field	FIFO_DATA[7:0]							
Reset	0xFF							
Access Type	Read Only							

FIFO_DATA

FIFO_DATA[7:0] is a read-only register used to retrieve data from the FIFO. It is important to burst read the data from the FIFO. Each data item is 4 bytes. So burst reading 4 bytes at FIFO_DATA register via the serial interface advances the FIFO_RD_PTR[8:0]. The format and data type of the data stored in the FIFO is determined by the Tag associated with the data. Readout from the FIFO follows a progression defined by measurements enabled by MEAS1_EN to MEAS20_EN bits in the PPG MEAS Select 1 (register 0x11), PPG MEAS Select 2 (register 0x12), and PPG MEAS Select 3 (register 0x13) registers, starting from MEAS1_EN. The source of the data in the FIFO is obtained from the tag associated with the data.

FIFO Configuration 3 (0x09)

BIT	7	6	5	4	3	2	1	0
Field	–	–	FIFO_MARK	FLUSH_FIFO	FIFO_STAT_CLR	A_FULL_TYPE	FIFO_RO	–
Reset	–	–	0	0	1	0	0	–
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	–

FIFO_MARK

When FIFO_MARK is set to 1, data is pushed to the FIFO with the 32-bit Marker tag. FIFO_MARK is a self-clearing bit.

The marker tag is useful for differentiating the data in the FIFO before and after the tag.

For the Marker Tag information, see the FIFO Description.

FLUSH_FIFO

The FIFO Flush bit is used for flushing the FIFO. The FIFO becomes empty and the FIFO_WR_PTR[8:0], FIFO_RD_PTR[8:0], FIFO_DATA_COUNT[9:0], and OVF_COUNTER[4:0] get reset to zero. FLUSH_FIFO is a self-clearing bit.

FIFO_STAT_CLR

The FIFO_STAT_CLR bit defines whether the A_FULL interrupt should get cleared by FIFO_DATA[7:0] register read. If FIFO_STAT_CLR is set low, A_FULL and FIFO_DATA_RDY interrupts do not get cleared by FIFO_DATA register read but get cleared by status register read. If FIFO_STAT_CLR is set high, A_FULL and FIFO_DATA_RDY interrupts get cleared by a FIFO_DATA register read or a status register read.

FIFO_STAT_CLR	DECODE
0	A_FULL, FRAME_RDY and FIFO_DATA_RDY status and interrupts do not get cleared by FIFO_DATA[7:0] register read. They get cleared by a status register read.
1	A_FULL, FRAME_RDY and FIFO_DATA_RDY status and interrupts get cleared by FIFO_DATA[7:0] register read or status register read (Default).

A_FULL_TYPE

The A_FULL_TYPE bit defines the behavior of the A_FULL interrupt. If the A_FULL_TYPE bit is set low, the A_FULL interrupt gets asserted when the A_FULL condition is detected and cleared by status register read, but reasserts for every sample if the A_FULL condition persists. If A_FULL_TYPE bit is set high, the A_FULL interrupt gets asserted only when a new A_FULL condition is detected. The interrupt gets cleared on Interrupt Status 1 register read, and does not re-assert for every sample until a new A_FULL condition is detected.

A_FULL_TYPE	DECODE
0	A_FULL interrupt gets asserted when the a_full condition is detected. It is cleared by status register read, but re-asserts for every sample if the a_full condition persists.

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1	A_FULL interrupt gets asserted only when the a_full condition is detected. The interrupt gets cleared on status register read, and does not re-assert for every sample until a new a_full condition is detected.

FIFO_RO

The FIFO_RO bit in the FIFO Configuration 3 register (0x09) determines whether samples get pushed on to the FIFO when it is full. If FIFO_RO is set to 1, push is enabled when FIFO is full, old samples are lost. Both FIFO_WR_PTR and FIFO_RD_PTR increment for each data item pushed to the FIFO after it is full. If FIFO_RO is set to 0, the new sample is dropped, and the FIFO is not updated. FIFO_WR_PTR and FIFO_RD_PTR do not increment until a data item is read from the FIFO.

FIFO_RO	DECODE
0	The FIFO stops on full.
1	The FIFO automatically rolls over on full.

FR Clock Frequency Select (0x0A)

BIT	7	6	5	4	3	2	1	0
Field	–	–	FR_CLK_SEL	FR_CLK_FINE_TUNE[4:0]				
Reset	–	–	1	0x00				
Access Type	–	–	Write, Read	Write, Read				

FR_CLK_SEL

When FR_CLK_SEL is set to 0, the internal frame rate primary clock is trimmed to 32kHz. When FR_CLK_SEL is set to 1, the internal frame rate primary clock is trimmed to 32.768kHz. The measurement frame rate is the primary clock rate divided by the program divider ratio, FR_CLK_DIV.

FR_CLK_SEL	DECODE
0	The internal frame rate primary clock is 32000Hz.
1	The internal frame rate primary clock is 32768Hz.

FR_CLK_FINE_TUNE

FR_CLK_FINE_TUNE[4:0] is used to fine tune the internal 32kHz/32.768kHz frame rate clock. This register can be used to compensate the internal oscillator for thermal drift. This can be accomplished by measuring the time between interrupts using a microcontroller crystal based real-time oscillator as a reference and computing the error in the time between interrupts. FR_CLK_FINE_TUNE[4:0] is a two's complement code with a resolution of 0.2%/LSB. The total range is +3.0% to -3.2% around the factory trimmed value. See table below for the shift in the internal primary frame rate clock vs trim code.

FR_CLK_FINE_TUNE[4:0]	SHIFT IN OSCILLATOR FREQUENCY (%)
0x10	-3.2
0x11	-3.0
0x12	-2.8
0x13	-2.6
0x14	-2.4
0x15	-2.2
0x16	-2.0
0x17	-1.8
0x18	-1.6

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0x19	-1.4
0x1A	-1.2
0x1B	-1.0
0x1C	-0.8
0x1D	-0.6
0x1E	-0.4
0x1F	-0.2
0x00	0.0
0x01	0.2
0x02	0.4
0x03	0.6
0x04	0.8
0x05	1.0
0x06	1.2
0x07	1.4
0x08	1.6
0x09	1.8
0x0A	2.0
0x0B	2.2
0x0C	2.4
0x0D	2.6
0x0E	2.8
0x0F	3.0

FR Clock Divider MSB (0x0B)

BIT	7	6	5	4	3	2	1	0
Field	–	FR_CLK_DIV_H[6:0]						
Reset	–	0x01						
Access Type	–	Write, Read						

FR_CLK_DIV_H

FR_CLK_DIV_H[6:0] is the upper 7 bits of the 15-bit FR_CLK_DIV[14:0] clock divider, which defines frame rate at which every enabled measurement is made.

The FR_CLK_DIV[14:0] should be programmed such that the all the conversions selected in the MEASx_EN (x = 1 to 20) bits in the System Configuration 1 and 2 registers can be completed within the frame period. In the event that the number of enabled measurements as well as the integration time and number of averages of each enabled measurement results in a frame measurement time that is longer than the primary frame clock period divided by FR_CLK_DIV, then a timing error occurs. This timing error produces the INVALID_CFG bit in the Status register 2 to be set.

FR_CLK_DIV = 0x7FFF and FR_CLK_DIV[14:0] < 0x0011 are reserved. FR_CLK_DIV[14:0] should be at least 0x0011, which corresponds to the period for the smallest frame.

The time for each frame to complete is given by:

$t_{MEASUREMENT} = t_{init1} + t_{MEAS1} + t_{MEAS2} + t_{MEAS3} + ... + t_{MEAS20}$

where:

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if the MEASx_SINC3 = 1 or MEASx_FILT = 0 then:

t_{MEASx} = [t_{init} + MEASx_TINT x (2 x 2^{MEASx_AVER} + 1) + 2 x 2^{MEASx_AVER}x MEASx_PD_SETLNG] x MEASx_EN

if MEASx_SINC3 = 0 and MEASx_FILT = 1 then:

t_{MEASx} = [t_{init} + 2xMEASx_TINT + MEASx_PD_SETLNG] x MEASx_EN

t_{init1} = 8xt_{CLOCK}

t_{init} = 6xt_{CLOCK}

MEASx_TINT = the integration time defined in measurement x = 1 to 20

MEASx_EN = 1 if the measurement is enabled and 0 if it is not, for measurement x = 1 to 20

MEASx_AVER = number of averages defined in measurement x = 1 to 20

MEASx_PD_SETLNG = photodiode settling time defined in measurement x = 1 to 20

t_{CLOCK} = the frame clock period which can be 1/32768 sec or 1/32000 sec depending on the FR_CLK_SEL bit

In SYNC_MODE = 0 and 2 a valid measurement requires:

$t_{MEASUREMENT}$ < FR_CLK_DIV/$f_{Primary\_Frame\_Clock}$

where:

$f_{Primary\_Frame\_Clock}$ = either the internal primary frame clock (SYNC_MODE=0) or the external frame clock input through the TRIG input (SYNC_MODE=2)

In SYNC_MODE = 1, a valid measurement requires:

$t_{MEASUREMENT}$ < t_{TRIG_PERIOD}

where:

t_{TRIG_PERIOD} = the period of the TRIG input signal

Frame Rate=$f_{Primary\_Frame\_Clock}$/FR_CLK_DIV[14:0] for 0x0011<=FR_DIV[14:0]<=0x7FFE

fPrimary_Frame_Clock	**32768Hz**
FR_CLK_DIV[14:0]	**Frame Rate [Hz]**
7FFF	Reserved
7FFE	1.000061
7FFD	1.000092
….	….
0012	1820.44
0011	1927.53
0010 to 0000	Reserved

FR Clock Divider LSB (0x0C)

BIT	7	6	5	4	3	2	1	0
Field	FR_CLK_DIV_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

FR_CLK_DIV_L

FR_CLK_DIV_L[7:0] is the lower byte of the 15-bit FR_CLK_DIV[14:0] clock divider that defines the frame rate.

For more details, see the FR_CLK_DIV_H.

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System Configuration 1 (0x0D)

BIT	7	6	5	4	3	2	1	0
Field	SYNC_MODE[1:0]		PPG4_PWRDN	PPG3_PWRDN	PPG2_PWRDN	PPG1_PWRDN	SHDN	RESET
Reset	0x0		0	0	0	0	0	0
Access Type	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

SYNC_MODE

SYNC_MODE[1:0] bits are used for programming the frame synchronization modes as described in the table below.

SYNC_MODE[1:0]	OPERATING MODES	TRIG INPUT	DECODE
0x0, 0x3	Internal Frame Sync	Not Used	The device is in free-running mode. Frame-sync pulses are generated internally using the internal 32KHz/32.768KHz frame clock and the frame rate divider set by FR_CLK_DIV. ADC Sync signals are generated internally using the 10MHz ADC clock.
0x1	External Frame Sync	Frame Sync	The device is in one-shot mode. A frame cycle begins upon receipt of an active edge on the TRIG input. A frame cycle consists of a power-up cycle and the execution of each enabled measurement. ADC Sync signals are generated internally using the 10MHz ADC clock. The internal 32KHz/32.768KHz frame clock is disabled.
0x2	External Clock	EXT_CLK, External Frame Rate Clock	The internal 32KHz/32.768KHz frame clock is disabled and the internal frame clock is driven by the TRIG pin. Frame-sync pulses are generated internally using the external TRIG input 32KHz/32.768KHz frame clock and the frame rate divider set by FR_CLK_DIV. ADC Sync signals are generated internally using the 10MHz ADC clock. The start of the sampling process can be controlled by the SPI software Sync command, which zeros out the frame rate divider and restarts the frame counting process. The device then advances with the external TRIG input clock. The subsequent software Sync commands abort the current frame and restart the new frame.

PPG4_PWRDN

When PPG4_PWRDN is set 0, the optical channel 4 is enabled. When PPG4_PWRDN is set to 1, this channel is powered down to save power.

PPG4_PWRDN	DECODE
0	Optical Channel 4 is enabled.
1	Optical Channel 4 is powered down.

PPG3_PWRDN

When PPG3_PWRDN is set 0, the optical channel 3 is enabled. When PPG3_PWRDN is set to 1, this channel is powered down to save power.

PPG3_PWRDN	DECODE
0	Optical Channel 3 is enabled.
1	Optical Channel 3 is powered down.

PPG2_PWRDN

When PPG2_PWRDN is set 0, the optical channel 2 is enabled. When PPG2_PWRDN is set to 1, this channel is

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powered down to save power.

PPG2_PWRDN	DECODE
0	Optical Channel 2 is enabled.
1	Optical Channel 2 is powered down.

PPG1_PWRDN

When PPG1_PWRDN is set 0, the optical channel 1 is enabled. When PPG1_PWRDN is set to 1, this channel is powered down to save power.

PPG1_PWRDN	DECODE
0	Optical Channel 1 is enabled.
1	Optical Channel 1 is powered down.

SHDN

The part can be put into a power-save mode by setting SHDN bit to 1. While in power-save mode, all configuration registers retain their values and write/read operations function as normal. All interrupts are cleared to zero in this mode. Set SHDN to 0 to put the part in normal mode.

SHDN	DECODE
0	The part is in normal operation. No action is taken.
1	The part can be put into a power-save mode by writing a ‘1’ to this bit. While in this mode, all the configuration registers remain accessible and retain their data. ADC conversion data contained in the registers are previous values. Writeable registers also remain accessible in shutdown. All interrupts are cleared. In this mode, the oscillator is shut down and the part draws minimum current. If this bit is asserted during an active conversion, then the conversion is aborted.

RESET

When RESET bit is set to 1, the MAX86177 undergoes a forced power-on-reset sequence. All configuration, threshold, and data registers are reset to their power-on-state. This bit then automatically becomes ‘0’ after the reset sequence is completed.

RESET	DECODE
0	The part is in normal operation. No action is taken.
1	The MAX86177 undergoes a forced power-on-reset sequence. All configuration, threshold, and data registers are reset to their power-on-state. This bit then automatically becomes ‘0’ after the reset sequence is completed.

Pin Functional Configuration (0x0E)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	INT2_FCFG[1:0]		INT1_FCFG[1:0]		TRIG_ICFG
Reset	–	–	–	0x0		0x1		0
Access Type	–	–	–	Write, Read		Write, Read		Write, Read

INT2_FCFG

INTx_FCFG[1:0] (x = 1, 2)set the functional configuration of the INTx pin. This interrupt can be configured to be disabled, cleared on status byte read or to self-clear after two optional prescribed times. See table below for options.

INTx_FCFG[1:0] (x = 1,2)	DECODE
0x0	Disabled
0x1	INTx is enabled and is cleared upon reading of any status register or FIFO.

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0x2	INTx is enabled and is self-clearing after 30.5µsec.
0x3	INTx is enabled and is self-clearing after 244µsec.

INT1_FCFG

For details, see the INT2_FCFG[1:0].

TRIG_ICFG

TRIG_ICFG bit sets the input active edge of the TRIG pin. Active edge is the edge for which the TRIG input responds.

TRIG_ICFG	DECODE
0	TRIG active edge is falling (PORb default).
1	TRIG active edge is rising.

Output Pin Configuration (0x0F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	INT2_OCFG[1:0]		INT1_OCFG[1:0]		–
Reset	–	–	–	0x0		0x0		–
Access Type	–	–	–	Write, Read		Write, Read		–

INT2_OCFG

INTx_OCFG[1:0] (x = 1, 2) selects the output drive type for the INTx pin, as shown in the table below.

INTx_OCFG[1:0] (x = 1, 2)	DECODE
0x0	Open drain, up to 6V compliant, active low output (PORb default).
0x1	Active drive to V_{DD_DIG} & GND, the active level is a high output.
0x2	Active drive to V_{DD_DIG} & GND, the active level is a low output.
0x3	Not defined

INT1_OCFG

For details, see the INT2_OCFG[1:0].

System Sync (0x10)

BIT	7	6	5	4	3	2	1	0
Field	–	SW_FORCE_SYNC	–	–	–	–	–	–
Reset	–	0	–	–	–	–	–	–
Access Type	–	Write, Read	–	–	–	–	–	–

SW_FORCE_SYNC

Writing 1 to this bit, aborts the current frame and starts a new frame. This is a self-clearing bit.

PPG MEAS Select 1 (0x11)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	MEAS20_EN	MEAS19_EN	MEAS18_EN	MEAS17_EN
Reset	–	–	–	–	0	0	0	0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

MEAS20_EN

Set MEASx_EN (x = 1 to 20) to 0 to disable measurement programmed in MEASx_SETUP registers in the measurement sequence. Set MEASx_EN to 1 to enable measurement programmed in MEASx_SETUP registers in the measurement sequence. The sequence consists of all the enabled measurement starting from MEAS1_EN till MEAS20_EN.

MEASx_EN (x = 1 to {{max_ppg_meas}])	DECODE
0	Disable Measurement x.
1	Enable Measurement x.

MEAS19_EN

For details, see the MEAS20_EN.

MEAS18_EN

For details, see the MEAS20_EN.

MEAS17_EN

For details, see the MEAS20_EN.

PPG MEAS Select 2 (0x12)

BIT	7	6	5	4	3	2	1	0
Field	MEAS16_EN	MEAS15_EN	MEAS14_EN	MEAS13_EN	MEAS12_EN	MEAS11_EN	MEAS10_EN	MEAS9_EN
Reset	0	0	0	0	0	0	0	0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

MEAS16_EN

For details, see the MEAS20_EN.

MEAS15_EN

For details, see the MEAS20_EN.

MEAS14_EN

For details, see the MEAS20_EN.

MEAS13_EN

For details, see the MEAS20_EN.

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MEAS12_EN

For details, see the MEAS20_EN.

MEAS11_EN

For details, see the MEAS20_EN.

MEAS10_EN

For details, see the MEAS20_EN.

MEAS9_EN

For details, see the MEAS20_EN.

PPG MEAS Select 3 (0x13)

BIT	7	6	5	4	3	2	1	0
Field	MEAS8_EN	MEAS7_EN	MEAS6_EN	MEAS5_EN	MEAS4_EN	MEAS3_EN	MEAS2_EN	MEAS1_EN
Reset	0	0	0	0	0	0	0	0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

MEAS8_EN

For details, see the MEAS20_EN.

MEAS7_EN

For details, see the MEAS20_EN.

MEAS6_EN

For details, see the MEAS20_EN.

MEAS5_EN

For details, see the MEAS20_EN.

MEAS4_EN

For details, see the MEAS20_EN.

MEAS3_EN

For details, see the MEAS20_EN.

MEAS2_EN

For details, see the MEAS20_EN.

MEAS1_EN

For details, see the MEAS20_EN.

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PPG Filter Setup (0x14)

BIT	7	6	5	4	3	2	1	0
Field	–	SMP_AVE[2:0]			ALC_DISABLE	–	–	MEAS1_CONFIG_SEL
Reset	–	0x0			0	–	–	0
Access Type	–	Write, Read			Write, Read	–	–	Write, Read

SMP_AVE

To reduce the amount of data throughput, adjacent samples (in each individual channel) can be averaged and decimated on the chip by programming the SMP_AVE[2:0] register.

These bits set the number of samples that are averaged on the chip before being written to the FIFO.

SMP_AVE must be programmed to 0 when Threshold Interrupts are enabled or when External Frame Sync is used.

SMP_AVE[2:0]	NUMBER OF SAMPLES AVERAGED
0x0	1 (No averaging)
0x1	2
0x2	4
0x3	8
0x4 to 0x7	16

ALC_DISABLE

The ALC_DISABLE bit inhibits the front-end analog ambient light cancellation circuit. This bit does not alter the backend ambient subtraction.

ALC_DISABLE	DECODE
0	Front-end ambient light cancelation is enabled.
1	Front-end ambient light cancelation is disabled.

MEAS1_CONFIG_SEL

When MEAS1_CONFIG_SEL bit is set to 0, all enabled measurements use the unique configuration defined in each MEASx setup.

When MEAS1_CONFIG_SEL bit is set to 1, all enabled measurements use the following configuration settings defined in MEAS1 setup. This allows for a reduced setup configuration writes.

MEAS1_FILT_SEL

MEAS1_FILT2_SEL

MEAS1_SINC3_SEL

MEAS1_TINT

MEAS1_AVER

MEAS1_PD_SETLNG

MEAS1_LED_SETLNG

MEAS1_PD1_SEL

MEAS1_PD2_SEL

MEAS1_PD3_SEL

MEAS1_PD4_SEL

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MEAS1_PD5_SEL
MEAS1_PD6_SEL
MEAS1_PD7_SEL
MEAS1_PD8_SEL
MEAS1_LED_RGE
MEAS1_PPG1_ADC_RGE
MEAS1_PPG2_ADC_RGE
MEAS1_PPG3_ADC_RGE
MEAS1_PPG4_ADC_RGE

MEAS1_CONFIG_SEL	DECODE
0	Use measurement specific configuration defined in each measurement register.
1	Use MEAS1 configuration for all enabled measurements.

Photo Diode Bias 1 (0x15)

BIT	7	6	5	4	3	2	1	0
Field	PD4_BIAS[1:0]		PD3_BIAS[1:0]		PD2_BIAS[1:0]		PD1_BIAS[1:0]	
Reset	0x1		0x1		0x1		0x1	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

PD4_BIAS

PDm_BIAS[1:0] (m = 1 to 8) selects the bias for Photodiode x as shown in the table below.

If more than one PD input is selected for an Optical Channel using the MEASx_PDm_SEL[1:0] (x = 1 to 20, m = 1 to 8), the maximum PD_BIAS setting for these PDs is used for the bias.

PDm_BIAS[1:0] (m = 1 to 8)	PHOTO DIODE CAPACITANCE (pF)
0x0	Not recommended
0x1	0 to 125 (POR default)
0x2	125 to 250
0x3	250 to 500

For more information, see the Photo Diode Biasing section.

PD3_BIAS

For details, see the PD4_BIAS[1:0].

PD2_BIAS

For details, see the PD4_BIAS[1:0].

PD1_BIAS

For details, see the PD4_BIAS[1:0].

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Photo Diode Bias 2 (0x16)

BIT	7	6	5	4	3	2	1	0
Field	PD8_BIAS[1:0]		PD7_BIAS[1:0]		PD6_BIAS[1:0]		PD5_BIAS[1:0]	
Reset	0x1		0x1		0x1		0x1	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

PD8_BIAS

For details, see the PD4_BIAS[1:0].

PD7_BIAS

For details, see the PD4_BIAS[1:0].

PD6_BIAS

For details, see the PD4_BIAS[1:0].

PD5_BIAS

For details, see the PD4_BIAS[1:0].

MEAS1 Selects (0x17)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS1_AMB	MEAS1_DRVB[2:0]			MEAS1_DRVA[2:0]		
Reset	–	0	0x0			0x0		
Access Type	–	Write, Read	Write, Read			Write, Read		

MEAS1_AMB

Set MEASx_AMB (x = 1 to 20) to 1 to enable a direct ambient measurement. Set MEASx_AMB to 0 to allow normal exposure measurements to be made. When MEASx_AMB is set to 1, MEASx_DRVA[1:0] and MEASx_DRVB[1:0] are ignored.

MEASx_AMB (x = 1 to 20)	DECODE
0	Enable normal exposure measurements for MEASx.
1	Enable direct ambient conversion for MEASx.

MEAS1_DRVB

Program MEASx_DRVB[2:0] (x = 1 to 20) measurement to select the LEDn_DRV pin (n = 1 to 6) for LED Driver B as shown in the table below.

MEASx_DRVB[2:0] (x = 1 to 20)	DECODE
0x0	LED Driver B drives LED 1.
0x1	LED Driver B drives LED 2.
0x2	LED Driver B drives LED 3.
0x3	LED Driver B drives LED 4.
0x4	LED Driver B drives LED 5.

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0x5	LED Driver B drives LED 6.
0x6, 0x7	Reserved

MEAS1_DRVA

Program MEASx_DRVA[2:0] (x = 1 to 20) measurement to select the LEDn_DRV pin (n = 1 to 6) for LED Driver A as shown in the table below.

MEASx_DRVA[2:0] (x = 1 to 20)	DECODE
0x0	LED Driver A drives LED 1.
0x1	LED Driver A drives LED 2.
0x2	LED Driver A drives LED 3.
0x3	LED Driver A drives LED 4.
0x4	LED Driver A drives LED 5.
0x5	LED Driver A drives LED 6.
0x6, 0x7	Reserved

MEAS1 Configuration 1 (0x18)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS1_DAC_LO_NOISE	MEAS1_FILT2_SEL	MEAS1_TINT[1:0]		MEAS1_AVER[2:0]		
Reset	–	0	1	0x3		0x0		
Access Type	–	Write, Read	Write, Read	Write, Read		Write, Read		

MEAS1_DAC_LO_NOISE

Recommend to set MEASx_DAC_LO_NOISE, (x = 1 to 20) to 1 when DC cancel DAC is used. Default is 0.

MEASx_DAC_LO_NOISE (x = 1 to 20)	DECODE
0	Recommended when DC Cancel DAC is not used.
1	Recommended when DC Cancel DAC is used.

MEAS1_FILT2_SEL

Use the second order decimation filter instead of the third order. Second order is only used for measurement x (x = 1 to 20) if MEASx_FILT2_SEL = 1 and MEASx_SINC3_SEL = 0 and MEASx_TINT = 0x3.

For Integration Time, see the MEAS1_TINT[1:0] description.

MEAS1_TINT

MEASx_TINT[1:0] (x = 1 to 20) bits set the integration time of PPG ADC as shown in the table below.

MEASx_TINT[1:0] (x = 1 to 20)	INTEGRATION TIME (μs) (COI3 ENABLED)	INTEGRATION TIME (μs) (COI2 ENABLED)
0x0	14.6	-
0x1	29.2	-
0x2	58.6	-
0x3	117.0	118.2

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MEAS1_AVER

MEASx_AVER[2:0] (x = 1 to 20) sets the number of exposures (LED pulses) that is averaged to improve the exposure SNR and improve ambient light cancellation. MEASx_AVER only works with MEASx_FILT_SEL = 0. When MEASx_FILT_SEL = 0, (2 * 2^{MEASx_AVER} + 1) ADC conversions of interleaved dark and exposure measurements are made and a weighted computed average saved in the FIFO.

MEASx_AVER[2:0] (x = 1 to 20)	NUMBER OF LED PULSES
0x0	1
0x1	2
0x2	4
0x3	8
0x4	16
0x5	32
0x6	64
0x7	128

MEAS1 Configuration 2 (0x19)

BIT	7	6	5	4	3	2	1	0
Field	MEAS1_SINC3_SEL	MEAS1_FILT_SEL	–	–	MEAS1_PPG4_ADC_RGE	MEAS1_PPG3_ADC_RGE	MEAS1_PPG2_ADC_RGE	MEAS1_PPG1_ADC_RGE
Reset	0	0	–	–	0	0	0	0
Access Type	Write, Read	Write, Read	–	–	Write, Read	Write, Read	Write, Read	Write, Read

MEAS1_SINC3_SEL

MEASx_SINC3_SEL (x = 1 to 20) enables the SINC3 decimation filter for the delta-sigma ADC for measurement x. This filter provides improved high-frequency roll-off which also improves high-frequency ambient light rejection and V_{LED} power supply rejection. The SINC3 filter generates poor quantization performance and is thus only available on the longest integration time, MEASx_TINT=0x3. However, the SINC3 filter provides a 60dB/dec roll-off at out of band frequencies, thus providing improved ambient and V_{LED} rejection.

Set MEASx_SINC3 low to use the COI2 or COI3 decimation filter as selected by MEASx_FILT2_SEL.

Set MEASx_SINC3 high to select the SINC3 decimation filter, which is only used if the MEASx_TINT= 0x3 for this measurement.

MEASx_SINC3_SEL (x = 1 to 20)	DECODE
0	SINC3 filter is not used.
1	SINC3 decimation filter is used only if MEASx_TINT=0x3 (118.2us).

MEAS1_FILT_SEL

MEASx_FILT_SEL (x = 1 to 20) sets the backend ambient-light cancellation method to be used. Set MEASx_FILT_SEL to 0 to use the central difference method where ambient light estimation is made from dark measurements before and after the exposure measurement. Set MEASx_FILT_SEL to 1 to use the forward difference method where the ambient light is estimated by a dark measurement before the exposure measurement.

When MEASx_FILT_SEL is set to 0, (2 * 2^{MEASx_AVER} + 1) ADC conversions of interleaved dark and exposure measurements are made and a weighted computed average loaded into the FIFO. When MEASx_FILT_SEL is set to 1, only one dark and exposure ADC conversion are made, regardless of the value of MEASx_AVER.

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MEASx_FILT_SEL	DECODE
0	Ambient-Light Cancellation is done using the central difference method.
1	Ambient-Light Cancellation is done using the forward difference method.

MEAS1_PPG4_ADC_RGE

MEASx_PPGy_ADC_RGE (x = 1 to 20, y = 1 to 4) bits set the ADC positive full-scale range of the optical channel y in measurement x, as shown in the table below.

MEASx_PPGy_ADC_RGE (x = 1 to 20, y = 1 to 4)	LSB (pA)	FULL SCALE (µA)
0	30.5	16.0
1	61.0	32.0

MEAS1_PPG3_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS1_PPG2_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS1_PPG1_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS1 Configuration 3 (0x1A)

BIT	7	6	5	4	3	2	1	0
Field	MEAS1_PPG2_DACOFF[3:0]				MEAS1_PPG1_DACOFF[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

MEAS1_PPG2_DACOFF

MEASx_PPGy_DACOFF[3:0] (x = 1 to 20, y = 1 to 4) sets the value of the offset DAC during the exposure interval. This allows for a larger convertible exposure range by sourcing some of the exposure currents from the offset DAC. Set MEASx_PPGy_DACOFF[3:0] to select the desired offset current as shown in the table below.

MEASx_PPGy_DACOFF[3:0] (x = 1 to 20, y = 1 to 4)	INJECTED OFFSET DAC CURRENT (µA)
0x0	0
0x1	4
0x2	8
0x3	12
0x4	16
0x5	20
0x6	24
0x7	28
0x8	32
0x9	36
0xA	40
0xB	44

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0xC to 0xF	48

MEAS1_PPG1_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS1 Configuration 4 (0x1B)

BIT	7	6	5	4	3	2	1	0
Field	MEAS1_PPG4_DACOFF[3:0]				MEAS1_PPG3_DACOFF[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

MEAS1_PPG4_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS1_PPG3_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS1 Configuration 5 (0x1C)

BIT	7	6	5	4	3	2	1	0
Field	MEAS1_PD_SETLNG[1:0]		MEAS1_LED_SETLNG[1:0]		–	–	MEAS1_LED_RGE[1:0]	
Reset	0x1		0x1		–	–	0x3	
Access Type	Write, Read		Write, Read		–	–	Write, Read	

MEAS1_PD_SETLNG

MEASx_PD_SETLNG[1:0] (x = 1 to 20) sets the time between dark and exposure samples as shown in the table below. This time can be used to allow for longer photodiode settling.

Note that the MEASx_LED_SETLNG[1:0] time must be less than MEASx_PD_SETLNG[1:0] setting.

MEASx_PD_SETLNG[1:0] (x = 1 to 20)	TIME BETWEEN SAMPLES (µs)
0x0	7.8
0x1	11.8 (Default)
0x2	15.8
0x3	23.8

MEAS1_LED_SETLNG

MEASx_LED_SETLNG (x = 1 to 20) selects the delay from the rising edge of LED to start of the exposure ADC integration. This allows for the LED current to settle before the start of ADC integration. LED settling time for a measurement must always be less than the photodiode settling time for the same measurement.

For more information, see the MEAS1_PD_SETLNG description.

t_{LED_SETLNG} MEASx_LED_SETLNG[1:0] (x = 1 to 20)	SETLLING TIME (µs)
0x0	7.7

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0x1	11.7 (default)
0x2	15.7
0x3	23.7

MEAS1_LED_RGE

MEASn_LED_RGE (n=1 to 9) sets the range of the two LED current DRVA and DRVB for the nth measurement. For more details, see the MEAS1_LEDA_PA[7:0].

MEASn_LED_RGE [1:0]	LED FULL SCALE RANGE (mA)
0x0	32
0x1	64
0x2	96
0x3	128

MEAS1 LEDA Current (0x1D)

BIT	7	6	5	4	3	2	1	0
Field	MEAS1_DRVA_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS1_DRVA_PA

MEASx_DRVz_PA[7:0] (x = 1 to 20, z = A, B) sets the LED drive current on each of the two LED drivers DRVA and DRVB for the nth measurement. Each of the two LED drivers is routed to the LEDn_DRV (n =1 to 6) as set by the MEASx_DRVA, MEASx_DRVB multiplexer settings. The full-scale range of the two LED drivers is set by the MEASx_LED_RGE[1:0] bits.

Set MEASx_DRVz_PA[7:0] (x = 1 to 20, z = A, B) code to set the desired current according to the table below. If MEASx_DRVz_PA[7:0] is set to 0x00, LED Driver z is disabled for measurement x.

MEASx_LED_RGE[1:0] (x = 1 to 20)	0	1	2	3
MEASx_DRVz_PA[7:0] (x = 1 to 20, z = A, B)	LED CURRENT (mA)	LED CURRENT (mA)	LED CURRENT (mA)	LED CURRENT (mA)
0x00	0.000	0.000	0.000	0.000
0x01	0.125	0.250	0.375	0.500
0x02	0.250	0.500	0.750	1.000
0x03	0.375	0.750	1.125	1.500
....	....	....	....	....
0xFC	31.500	63.000	94.500	126.000
0xFD	31.625	63.250	94.875	126.500
0xFE	31.750	63.500	95.250	127.000
0xFF	31.875	63.750	95.625	127.500
LSB	0.125	0.250	0.375	0.500

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MEAS1 LEDB Current (0x1E)

BIT	7	6	5	4	3	2	1	0
Field	MEAS1_DRVB_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS1_DRVB_PA

For details, see the MEAS1_DRVA_PA[7:0].

MEAS1 PD SEL 1 (0x1F)

BIT	7	6	5	4	3	2	1	0
Field	MEAS1_PD3_SEL[2:1]		MEAS1_PD2_SEL[2:0]			MEAS1_PD1_SEL[2:0]		
Reset	0x3		0x5			0x4		
Access Type	Write, Read		Write, Read			Write, Read		

MEAS1_PD3_SEL

MEASx_PD3_SEL[2:1] (x = 1 to 20) has 2 most significant bits of MEASx_PD3_SEL[2:0]. Bit 0 is in MEASx_PD3_SEL[0](register address 0x20).

For details, see the MEAS1_PD1_SEL[2:0].

MEAS1_PD2_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS1_PD1_SEL

MEASx_PDm_SEL[2:0] (x = 1 to 20, m = 1 to 8) bits selects PDm input to each of the Optical Channels. PDm (1 to 8) if not selected on any optical channel (1 to 4) must be set to the value 0x0 explicitly for proper ADC conversions.

MEASx_PDm_SEL[2:0] (x = 1 to 20, m = 1 to 8)	DECODE
0x0	PDm not selected.
0x4	PDm goes to Optical Channel 1(POR default).
0x5	PDm goes to Optical Channel 2.
0x6	PDm goes to Optical Channel 3.
0x7	PDm goes to Optical Channel 4.

MEAS1 PD SEL 2 (0x20)

BIT	7	6	5	4	3	2	1	0
Field	MEAS1_PD6_SEL[2]	MEAS1_PD5_SEL[2:0]			MEAS1_PD4_SEL[2:0]			MEAS1_PD3_SEL[0]
Reset	0	0x0			0x7			0
Access Type	Write, Read	Write, Read			Write, Read			Write, Read

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MEAS1_PD6_SEL

MEASx_PD6_SEL[2] (x = 1 to 20) has the most significant bit of MEASx_PD6_SEL[2:0]. Lower 2 bits are in MEASx_PD6_SEL[1:0] (register address 0x21).

For details, see the MEAS1_PD1_SEL[1:0].

MEAS1_PD5_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS1_PD4_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS1_PD3_SEL

MEASx_PD3_SEL[0] (x = 1 to 20) has bit 0 of MEASx_PD3_SEL[2:0]. Most signifcant 2 bits are in MEASx_PD3_SEL[2:1] (register address 0x1F).

For details, see the MEAS1_PD1_SEL[2:0].

MEAS1 PD SEL 3 (0x21)

BIT	7	6	5	4	3	2	1	0
Field	MEAS1_PD8_SEL[2:0]			MEAS1_PD7_SEL[2:0]			MEAS1_PD6_SEL[1:0]	
Reset	0x0			0x0			0x0	
Access Type	Write, Read			Write, Read			Write, Read	

MEAS1_PD8_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS1_PD7_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS1_PD6_SEL

MEASx_PD6_SEL[1:0] (x = 1 to 20) has lower 2 bits of MEASx_PD6_SEL[2:0]. Most significant bit is in MEASx_PD6_SEL[2] (register address 0x20).

For details, see the MEAS1_PD1_SEL[2:0].

MEAS2 Selects (0x22)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS2_AMB	MEAS2_DRVB[2:0]			MEAS2_DRVA[2:0]		
Reset	–	0	0x0			0x0		
Access Type	–	Write, Read	Write, Read			Write, Read		

MEAS2_AMB

For details, see the MEAS1_AMB.

MEAS2_DRVB

For details, see the MEAS1_DRVB[2:0].

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MEAS2_DRVA

For details, see the MEAS1_DRVA[2:0].

MEAS2 Configuration 1 (0x23)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS2_DAC_LO_NOISE	MEAS2_FILT2_SEL	MEAS2_TINT[1:0]		MEAS2_AVER[2:0]		
Reset	–	0	1	0x3		0x0		
Access Type	–	Write, Read	Write, Read	Write, Read		Write, Read		

MEAS2_DAC_LO_NOISE

For details, see the MEAS1_DAC_LO_NOISE.

MEAS2_FILT2_SEL

For details, see the MEAS1_FILT2_SEL.

MEAS2_TINT

For details, see the MEAS1_TINT[1:0].

MEAS2_AVER

For details, see the MEAS1_AVER[2:0].

MEAS2 Configuration 2 (0x24)

BIT	7	6	5	4	3	2	1	0
Field	MEAS2_SINC3_SEL	MEAS2_FILT_SEL	–	–	MEAS2_PPG4_ADC_RGE	MEAS2_PPG3_ADC_RGE	MEAS2_PPG2_ADC_RGE	MEAS2_PPG1_ADC_RGE
Reset	0	0	–	–	0	0	0	0
Access Type	Write, Read	Write, Read	–	–	Write, Read	Write, Read	Write, Read	Write, Read

MEAS2_SINC3_SEL

For details, see the MEAS1_SINC3_SEL.

MEAS2_FILT_SEL

For details, see the MEAS1_FILT_SEL.

MEAS2_PPG4_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS2_PPG3_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS2_PPG2_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

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MEAS2_PPG1_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS2 Configuration 3 (0x25)

BIT	7	6	5	4	3	2	1	0
Field	MEAS2_PPG2_DACOFF[3:0]				MEAS2_PPG1_DACOFF[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

MEAS2_PPG2_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS2_PPG1_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS2 Configuration 4 (0x26)

BIT	7	6	5	4	3	2	1	0
Field	MEAS2_PPG4_DACOFF[3:0]				MEAS2_PPG3_DACOFF[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

MEAS2_PPG4_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS2_PPG3_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS2 Configuration 5 (0x27)

BIT	7	6	5	4	3	2	1	0
Field	MEAS2_PD_SETLNG[1:0]		MEAS2_LED_SETLNG[1:0]		–	–	MEAS2_LED_RGE[1:0]	
Reset	0x1		0x1		–	–	0x3	
Access Type	Write, Read		Write, Read		–	–	Write, Read	

MEAS2_PD_SETLNG

For details, see the MEAS1_PD_SETLNG[1:0].

MEAS2_LED_SETLNG

For details, see the MEAS1_LED_SETLNG[1:0].

MEAS2_LED_RGE

For details, see the MEAS1_LED_RGE[1:0].

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MEAS2 LEDA Current (0x28)

BIT	7	6	5	4	3	2	1	0
Field	MEAS2_DRVA_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS2_DRVA_PA

For details, see the MEAS1_DRVA_PA[7:0].

MEAS2 LEDB Current (0x29)

BIT	7	6	5	4	3	2	1	0
Field	MEAS2_DRVB_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS2_DRVB_PA

For details, see the MEAS1_DRVA_PA[7:0].

MEAS2 PD SEL 1 (0x2A)

BIT	7	6	5	4	3	2	1	0
Field	MEAS2_PD3_SEL[2:1]		MEAS2_PD2_SEL[2:0]			MEAS2_PD1_SEL[2:0]		
Reset	0x3		0x5			0x4		
Access Type	Write, Read		Write, Read			Write, Read		

MEAS2_PD3_SEL

For details, see the MEAS1_PD3_SEL[2:1] and the MEAS1_PD1_SEL[2:0].

MEAS2_PD2_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS2_PD1_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS2 PD SEL 2 (0x2B)

BIT	7	6	5	4	3	2	1	0
Field	MEAS2_PD6_SEL[2]	MEAS2_PD5_SEL[2:0]			MEAS2_PD4_SEL[2:0]			MEAS2_PD3_SEL[0]
Reset	0	0x0			0x7			0
Access Type	Write, Read	Write, Read			Write, Read			Write, Read

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MEAS2_PD6_SEL

For details, see the MEAS1_PD6_SEL[2] and the MEAS1_PD1_SEL[2:0].

MEAS2_PD5_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS2_PD4_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS2_PD3_SEL

For details, see the MEAS1_PD3_SEL[0] and the MEAS1_PD1_SEL[2:0].

MEAS2 PD SEL 3 (0x2C)

BIT	7	6	5	4	3	2	1	0
Field	MEAS2_PD8_SEL[2:0]			MEAS2_PD7_SEL[2:0]			MEAS2_PD6_SEL[1:0]	
Reset	0x0			0x0			0x0	
Access Type	Write, Read			Write, Read			Write, Read	

MEAS2_PD8_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS2_PD7_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS2_PD6_SEL

For details, see the MEAS1_PD6_SEL[1:0] and the MEAS1_PD1_SEL[2:0].

MEAS3 Selects (0x2D)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS3_AMB	MEAS3_DRVB[2:0]			MEAS3_DRVA[2:0]		
Reset	–	0	0x0			0x0		
Access Type	–	Write, Read	Write, Read			Write, Read		

MEAS3_AMB

For details, see the MEAS1_AMB.

MEAS3_DRVB

For details, see the MEAS1_DRVB[2:0].

MEAS3_DRVA

For details, see the MEAS1_DRVA[2:0].

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MEAS3 Configuration 1 (0x2E)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS3_DAC_LO_NOISE	MEAS3_FILT2_SEL	MEAS3_TINT[1:0]		MEAS3_AVER[2:0]		
Reset	–	0	1	0x3		0x0		
Access Type	–	Write, Read	Write, Read	Write, Read		Write, Read		

MEAS3_DAC_LO_NOISE

For details, see the MEAS1_DAC_LO_NOISE.

MEAS3_FILT2_SEL

For details, see the MEAS1_FILT2_SEL.

MEAS3_TINT

For details, see the MEAS1_TINT.

MEAS3_AVER

For details, see the MEAS1_AVER[2:0].

MEAS3 Configuration 2 (0x2F)

BIT	7	6	5	4	3	2	1	0
Field	MEAS3_SINC3_SEL	MEAS3_FILT_SEL	–	–	MEAS3_PPG4_ADC_RGE	MEAS3_PPG3_ADC_RGE	MEAS3_PPG2_ADC_RGE	MEAS3_PPG1_ADC_RGE
Reset	0	0	–	–	0	0	0	0
Access Type	Write, Read	Write, Read	–	–	Write, Read	Write, Read	Write, Read	Write, Read

MEAS3_SINC3_SEL

For details, see the MEAS1_SINC3_SEL.

MEAS3_FILT_SEL

For details, see the MEAS1_FILT_SEL.

MEAS3_PPG4_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS3_PPG3_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS3_PPG2_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS3_PPG1_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

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MEAS3 Configuration 3 (0x30)

BIT	7	6	5	4	3	2	1	0
Field	MEAS3_PPG2_DACOFF[3:0]				MEAS3_PPG1_DACOFF[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

MEAS3_PPG2_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS3_PPG1_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS3 Configuration 4 (0x31)

BIT	7	6	5	4	3	2	1	0
Field	MEAS3_PPG4_DACOFF[3:0]				MEAS3_PPG3_DACOFF[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

MEAS3_PPG4_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS3_PPG3_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS3 Configuration 5 (0x32)

BIT	7	6	5	4	3	2	1	0
Field	MEAS3_PD_SETLNG[1:0]		MEAS3_LED_SETLNG[1:0]		–	–	MEAS3_LED_RGE[1:0]	
Reset	0x1		0x1		–	–	0x3	
Access Type	Write, Read		Write, Read		–	–	Write, Read	

MEAS3_PD_SETLNG

For details, see the MEAS1_PD_SETLNG[1:0].

MEAS3_LED_SETLNG

For details, see the MEAS1_LED_SETLNG[1:0].

MEAS3_LED_RGE

For details, see the MEAS1_LED_RGE[1:0].

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MEAS3 LEDA Current (0x33)

BIT	7	6	5	4	3	2	1	0
Field	MEAS3_DRVA_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS3_DRVA_PA

For details, see the MEAS1_DRVA_PA[7:0].

MEAS3 LEDB Current (0x34)

BIT	7	6	5	4	3	2	1	0
Field	MEAS3_DRVB_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS3_DRVB_PA

For details, see the MEAS1_DRVA_PA[7:0].

MEAS3 PD SEL 1 (0x35)

BIT	7	6	5	4	3	2	1	0
Field	MEAS3_PD3_SEL[2:1]		MEAS3_PD2_SEL[2:0]			MEAS3_PD1_SEL[2:0]		
Reset	0x3		0x5			0x4		
Access Type	Write, Read		Write, Read			Write, Read		

MEAS3_PD3_SEL

For details, see the MEAS1_PD3_SEL[2:1] and the MEAS1_PD1_SEL[2:0].

MEAS3_PD2_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS3_PD1_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS3 PD SEL 2 (0x36)

BIT	7	6	5	4	3	2	1	0
Field	MEAS3_PD6_SEL[2]	MEAS3_PD5_SEL[2:0]			MEAS3_PD4_SEL[2:0]			MEAS3_PD3_SEL[0]
Reset	0	0x0			0x7			0
Access Type	Write, Read	Write, Read			Write, Read			Write, Read

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MEAS3_PD6_SEL

For details, see the MEAS1_PD6_SEL[2] and the MEAS1_PD1_SEL[2:0].

MEAS3_PD5_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS3_PD4_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS3_PD3_SEL

For details, see the MEAS1_PD3_SEL[0] and the MEAS1_PD1_SEL[2:0].

MEAS3 PD SEL 3 (0x37)

BIT	7	6	5	4	3	2	1	0
Field	MEAS3_PD8_SEL[2:0]			MEAS3_PD7_SEL[2:0]			MEAS3_PD6_SEL[1:0]	
Reset	0x0			0x0			0x0	
Access Type	Write, Read			Write, Read			Write, Read	

MEAS3_PD8_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS3_PD7_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS3_PD6_SEL

For details, see the MEAS1_PD6_SEL[1:0] and the MEAS1_PD1_SEL[2:0].

MEAS4 Selects (0x38)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS4_AMB	MEAS4_DRVB[2:0]			MEAS4_DRVA[2:0]		
Reset	–	0	0x0			0x0		
Access Type	–	Write, Read	Write, Read			Write, Read		

MEAS4_AMB

For details, see the MEAS1_AMB.

MEAS4_DRVB

For details, see the MEAS1_DRVB[2:0].

MEAS4_DRVA

For details, see the MEAS1_DRVA[2:0].

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MEAS4 Configuration 1 (0x39)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS4_DAC_LO_NOISE	MEAS4_FILT2_SEL	MEAS4_TINT[1:0]		MEAS4_AVER[2:0]		
Reset	–	0	1	11		0		
Access Type	–	Write, Read	Write, Read	Write, Read		Write, Read		

MEAS4_DAC_LO_NOISE

For details, see the MEAS1_DAC_LO_NOISE.

MEAS4_FILT2_SEL

For details, see the MEAS1_FILT2_SEL.

MEAS4_TINT

For details, see the MEAS1_TINT.

MEAS4_AVER

For details, see the MEAS1_AVER[2:0].

MEAS4 Configuration 2 (0x3A)

BIT	7	6	5	4	3	2	1	0
Field	MEAS4_SINC3_SEL	MEAS4_FILT_SEL	–	–	MEAS4_PPG4_ADC_RGE	MEAS4_PPG3_ADC_RGE	MEAS4_PPG2_ADC_RGE	MEAS4_PPG1_ADC_RGE
Reset	0	0	–	–	0	0	0	0
Access Type	Write, Read	Write, Read	–	–	Write, Read	Write, Read	Write, Read	Write, Read

MEAS4_SINC3_SEL

For details, see the MEAS1_SINC3_SEL.

MEAS4_FILT_SEL

For details, see the MEAS1_FILT_SEL.

MEAS4_PPG4_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS4_PPG3_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS4_PPG2_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS4_PPG1_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

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MEAS4 Configuration 3 (0x3B)

BIT	7	6	5	4	3	2	1	0
Field	MEAS4_PPG2_DACOFF[3:0]				MEAS4_PPG1_DACOFF[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

MEAS4_PPG2_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS4_PPG1_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS4 Configuration 4 (0x3C)

BIT	7	6	5	4	3	2	1	0
Field	MEAS4_PPG4_DACOFF[3:0]				MEAS4_PPG3_DACOFF[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

MEAS4_PPG4_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS4_PPG3_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS4 Configuration 5 (0x3D)

BIT	7	6	5	4	3	2	1	0
Field	MEAS4_PD_SETLNG[1:0]		MEAS4_LED_SETLNG[1:0]		–	–	MEAS4_LED_RGE[1:0]	
Reset	0x1		0x1		–	–	0x3	
Access Type	Write, Read		Write, Read		–	–	Write, Read	

MEAS4_PD_SETLNG

For details, see the MEAS1_PD_SETLNG[1:0].

MEAS4_LED_SETLNG

For details, see the MEAS1_LED_SETLNG[1:0].

MEAS4_LED_RGE

For details, see the MEAS1_LED_RGE[1:0].

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MEAS4 LEDA Current (0x3E)

BIT	7	6	5	4	3	2	1	0
Field	MEAS4_DRVA_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS4_DRVA_PA

For details, see the MEAS1_DRVA_PA[7:0].

MEAS4 LEDB Current (0x3F)

BIT	7	6	5	4	3	2	1	0
Field	MEAS4_DRVB_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS4_DRVB_PA

For details, see the MEAS1_DRVA_PA[7:0].

MEAS4 PD SEL 1 (0x40)

BIT	7	6	5	4	3	2	1	0
Field	MEAS4_PD3_SEL[2:1]		MEAS4_PD2_SEL[2:0]			MEAS4_PD1_SEL[2:0]		
Reset	0x3		0x5			0x4		
Access Type	Write, Read		Write, Read			Write, Read		

MEAS4_PD3_SEL

For details, see the MEAS1_PD3_SEL[2:1] and the MEAS1_PD1_SEL[2:0].

MEAS4_PD2_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS4_PD1_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS4 PD SEL 2 (0x41)

BIT	7	6	5	4	3	2	1	0
Field	MEAS4_PD6_SEL[2]	MEAS4_PD5_SEL[2:0]			MEAS4_PD4_SEL[2:0]			MEAS4_PD3_SEL[0]
Reset	0	0x0			0x7			0
Access Type	Write, Read	Write, Read			Write, Read			Write, Read

MEAS4_PD6_SEL

For details, see the MEAS1_PD6_SEL[2] and the MEAS1_PD1_SEL[2:0].

MEAS4_PD5_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS4_PD4_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS4_PD3_SEL

For details, see the MEAS1_PD3_SEL[0] and the MEAS1_PD1_SEL[2:0].

MEAS4 PD SEL 3 (0x42)

BIT	7	6	5	4	3	2	1	0
Field	MEAS4_PD8_SEL[2:0]			MEAS4_PD7_SEL[2:0]			MEAS4_PD6_SEL[1:0]	
Reset	0x0			0x0			0x0	
Access Type	Write, Read			Write, Read			Write, Read	

MEAS4_PD8_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS4_PD7_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS4_PD6_SEL

For details, see the MEAS1_PD6_SEL[1:0] and the MEAS1_PD1_SEL[2:0].

MEAS5 Selects (0x43)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS5_AMB	MEAS5_DRVB[2:0]			MEAS5_DRVA[2:0]		
Reset	–	0	0x0			0x0		
Access Type	–	Write, Read	Write, Read			Write, Read		

MEAS5_AMB

For details, see the MEAS1_AMB.

MEAS5_DRVB

For details, see the MEAS1_DRVB[2:0].

MEAS5_DRVA

For details, see the MEAS1_DRVA[2:0].

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MEAS5 Configuration 1 (0x44)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS5_DAC_LO_NOISE	MEAS5_FILT2_SEL	MEAS5_TINT[1:0]		MEAS5_AVER[2:0]		
Reset	–	0	1	0x3		0x0		
Access Type	–	Write, Read	Write, Read	Write, Read		Write, Read		

MEAS5_DAC_LO_NOISE

For details, see the MEAS1_DAC_LO_NOISE.

MEAS5_FILT2_SEL

For details, see the MEAS1_FILT2_SEL.

MEAS5_TINT

For details, see the MEAS1_TINT.

MEAS5_AVER

For details, see the MEAS1_AVER[2:0].

MEAS5 Configuration 2 (0x45)

BIT	7	6	5	4	3	2	1	0
Field	MEAS5_SINC3_SEL	MEAS5_FILT_SEL	–	–	MEAS5_PPG4_ADC_RGE	MEAS5_PPG3_ADC_RGE	MEAS5_PPG2_ADC_RGE	MEAS5_PPG1_ADC_RGE
Reset	0	0	–	–	0	0	0	0
Access Type	Write, Read	Write, Read	–	–	Write, Read	Write, Read	Write, Read	Write, Read

MEAS5_SINC3_SEL

For details, see the MEAS1_SINC3_SEL.

MEAS5_FILT_SEL

For details, see the MEAS1_FILT_SEL.

MEAS5_PPG4_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS5_PPG3_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS5_PPG2_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS5_PPG1_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

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MEAS5 Configuration 3 (0x46)

BIT	7	6	5	4	3	2	1	0
Field	MEAS5_PPG2_DACOFF[3:0]				MEAS5_PPG1_DACOFF[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

MEAS5_PPG2_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS5_PPG1_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS5 Configuration 4 (0x47)

BIT	7	6	5	4	3	2	1	0
Field	MEAS5_PPG4_DACOFF[3:0]				MEAS5_PPG3_DACOFF[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

MEAS5_PPG4_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS5_PPG3_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS5 Configuration 5 (0x48)

BIT	7	6	5	4	3	2	1	0
Field	MEAS5_PD_SETLNG[1:0]		MEAS5_LED_SETLNG[1:0]		–	–	MEAS5_LED_RGE[1:0]	
Reset	0x1		0x1		–	–	0x3	
Access Type	Write, Read		Write, Read		–	–	Write, Read	

MEAS5_PD_SETLNG

For details, see the MEAS1_PD_SETLNG[1:0].

MEAS5_LED_SETLNG

For details, see the MEAS1_LED_SETLNG[1:0].

MEAS5_LED_RGE

For details, see the MEAS1_LED_RGE[1:0].

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MEAS5 LEDA Current (0x49)

BIT	7	6	5	4	3	2	1	0
Field	MEAS5_DRVA_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS5_DRVA_PA

For details, see the MEAS1_DRVA_PA[7:0].

MEAS5 LEDB Current (0x4A)

BIT	7	6	5	4	3	2	1	0
Field	MEAS5_DRVB_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS5_DRVB_PA

For details, see the MEAS1_DRVA_PA[7:0].

MEAS5 PD SEL 1 (0x4B)

BIT	7	6	5	4	3	2	1	0
Field	MEAS5_PD3_SEL[2:1]		MEAS5_PD2_SEL[2:0]			MEAS5_PD1_SEL[2:0]		
Reset	0x3		0x5			0x4		
Access Type	Write, Read		Write, Read			Write, Read		

MEAS5_PD3_SEL

For details, see the MEAS1_PD3_SEL[2:1] and the MEAS1_PD1_SEL[2:0].

MEAS5_PD2_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS5_PD1_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS5 PD SEL 2 (0x4C)

BIT	7	6	5	4	3	2	1	0
Field	MEAS5_PD6_SEL[2]	MEAS5_PD5_SEL[2:0]			MEAS5_PD4_SEL[2:0]			MEAS5_PD3_SEL[0]
Reset	0	0x0			0x7			0
Access Type	Write, Read	Write, Read			Write, Read			Write, Read

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MEAS5_PD6_SEL

For details, see the MEAS1_PD6_SEL[2] and the MEAS1_PD1_SEL[2:0].

MEAS5_PD5_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS5_PD4_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS5_PD3_SEL

For details, see the MEAS1_PD3_SEL[0] and the MEAS1_PD1_SEL[2:0].

MEAS5 PD SEL 3 (0x4D)

BIT	7	6	5	4	3	2	1	0
Field	MEAS5_PD8_SEL[2:0]			MEAS5_PD7_SEL[2:0]			MEAS5_PD6_SEL[1:0]	
Reset	0x0			0x0			0x0	
Access Type	Write, Read			Write, Read			Write, Read	

MEAS5_PD8_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS5_PD7_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS5_PD6_SEL

For details, see the MEAS1_PD6_SEL[1:0] and the MEAS1_PD1_SEL[2:0].

MEAS6 Selects (0x4E)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS6_AMB	MEAS6_DRVB[2:0]			MEAS6_DRVA[2:0]		
Reset	–	0	0x0			0x0		
Access Type	–	Write, Read	Write, Read			Write, Read		

MEAS6_AMB

For details, see the MEAS1_AMB.

MEAS6_DRVB

For details, see the MEAS1_DRVB[2:0].

MEAS6_DRVA

For details, see the MEAS1_DRVA[2:0].

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MEAS6 Configuration 1 (0x4F)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS6_DAC_LO_NOISE	MEAS6_FILT2_SEL	MEAS6_TINT[1:0]		MEAS6_AVER[2:0]		
Reset	–	0	1	0x3		0x0		
Access Type	–	Write, Read	Write, Read	Write, Read		Write, Read		

MEAS6_DAC_LO_NOISE

For details, see the MEAS1_DAC_LO_NOISE.

MEAS6_FILT2_SEL

For details, see the MEAS1_FILT2_SEL.

MEAS6_TINT

For details, see the MEAS1_TINT.

MEAS6_AVER

For details, see the MEAS1_AVER[2:0].

MEAS6 Configuration 2 (0x50)

BIT	7	6	5	4	3	2	1	0
Field	MEAS6_SINC3_SEL	MEAS6_FILT_SEL	–	–	MEAS6_PPG4_ADC_RGE	MEAS6_PPG3_ADC_RGE	MEAS6_PPG2_ADC_RGE	MEAS6_PPG1_ADC_RGE
Reset	0	0	–	–	0	0	0	0
Access Type	Write, Read	Write, Read	–	–	Write, Read	Write, Read	Write, Read	Write, Read

MEAS6_SINC3_SEL

For details, see the MEAS1_SINC3_SEL.

MEAS6_FILT_SEL

For details, see the MEAS1_FILT_SEL.

MEAS6_PPG4_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS6_PPG3_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS6_PPG2_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS6_PPG1_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

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MEAS6 Configuration 3 (0x51)

BIT	7	6	5	4	3	2	1	0
Field	MEAS6_PPG2_DACOFF[3:0]				MEAS6_PPG1_DACOFF[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

MEAS6_PPG2_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS6_PPG1_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS6 Configuration 4 (0x52)

BIT	7	6	5	4	3	2	1	0
Field	MEAS6_PPG4_DACOFF[3:0]				MEAS6_PPG3_DACOFF[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

MEAS6_PPG4_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS6_PPG3_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS6 Configuration 5 (0x53)

BIT	7	6	5	4	3	2	1	0
Field	MEAS6_PD_SETLNG[1:0]		MEAS6_LED_SETLNG[1:0]		–	–	MEAS6_LED_RGE[1:0]	
Reset	0x1		0x1		–	–	0x3	
Access Type	Write, Read		Write, Read		–	–	Write, Read	

MEAS6_PD_SETLNG

For details, see the MEAS1_PD_SETLNG[1:0].

MEAS6_LED_SETLNG

For details, see the MEAS1_LED_SETLNG[1:0].

MEAS6_LED_RGE

For details, see the MEAS1_LED_RGE[1:0].

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MEAS6 LEDA Current (0x54)

BIT	7	6	5	4	3	2	1	0
Field	MEAS6_DRVA_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS6_DRVA_PA

For details, see the MEAS1_DRVA_PA[7:0].

MEAS6 LEDB Current (0x55)

BIT	7	6	5	4	3	2	1	0
Field	MEAS6_DRVB_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS6_DRVB_PA

For details, see the MEAS1_DRVA_PA[7:0].

MEAS6 PD SEL 1 (0x56)

BIT	7	6	5	4	3	2	1	0
Field	MEAS6_PD3_SEL[2:1]		MEAS6_PD2_SEL[2:0]			MEAS6_PD1_SEL[2:0]		
Reset	0x3		0x5			0x4		
Access Type	Write, Read		Write, Read			Write, Read		

MEAS6_PD3_SEL

For details, see the MEAS1_PD3_SEL[2:1] and the MEAS1_PD1_SEL[2:0].

MEAS6_PD2_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS6_PD1_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS6 PD SEL 2 (0x57)

BIT	7	6	5	4	3	2	1	0
Field	MEAS6_PD6_SEL[2]	MEAS6_PD5_SEL[2:0]			MEAS6_PD4_SEL[2:0]			MEAS6_PD3_SEL[0]
Reset	0	0x0			0x7			0
Access Type	Write, Read	Write, Read			Write, Read			Write, Read

MEAS6_PD6_SEL

For details, see the MEAS1_PD6_SEL[2] and the MEAS1_PD1_SEL[2:0].

MEAS6_PD5_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS6_PD4_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS6_PD3_SEL

For details, see the MEAS1_PD3_SEL[0] and the MEAS1_PD1_SEL[2:0].

MEAS6 PD SEL 3 (0x58)

BIT	7	6	5	4	3	2	1	0
Field	MEAS6_PD8_SEL[2:0]			MEAS6_PD7_SEL[2:0]			MEAS6_PD6_SEL[1:0]	
Reset	0x0			0x0			0x0	
Access Type	Write, Read			Write, Read			Write, Read	

MEAS6_PD8_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS6_PD7_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS6_PD6_SEL

For details, see the MEAS1_PD6_SEL[1:0] and the MEAS1_PD1_SEL[2:0].

MEAS7 Selects (0x59)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS7_AMB	MEAS7_DRVB[2:0]			MEAS7_DRVA[2:0]		
Reset	–	0	0x0			0x0		
Access Type	–	Write, Read	Write, Read			Write, Read		

MEAS7_AMB

For details, see the MEAS1_AMB.

MEAS7_DRVB

For details, see the MEAS1_DRVB[2:0].

MEAS7_DRVA

For details, see the MEAS1_DRVA[2:0].

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MEAS7 Configuration 1 (0x5A)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS7_DAC_LO_NOISE	MEAS7_FILT2_SEL	MEAS7_TINT[1:0]		MEAS7_AVER[2:0]		
Reset	–	0	1	0x3		0x0		
Access Type	–	Write, Read	Write, Read	Write, Read		Write, Read		

MEAS7_DAC_LO_NOISE

For details, see the MEAS1_DAC_LO_NOISE.

MEAS7_FILT2_SEL

For details, see the MEAS1_FILT2_SEL.

MEAS7_TINT

For details, see the MEAS1_TINT.

MEAS7_AVER

For details, see the MEAS1_AVER[2:0].

MEAS7 Configuration 2 (0x5B)

BIT	7	6	5	4	3	2	1	0
Field	MEAS7_SINC3_SEL	MEAS7_FILT_SEL	–	–	MEAS7_PPG4_ADC_RGE	MEAS7_PPG3_ADC_RGE	MEAS7_PPG2_ADC_RGE	MEAS7_PPG1_ADC_RGE
Reset	0	0	–	–	0	0	0	0
Access Type	Write, Read	Write, Read	–	–	Write, Read	Write, Read	Write, Read	Write, Read

MEAS7_SINC3_SEL

For details, see the MEAS1_SINC3_SEL.

MEAS7_FILT_SEL

For details, see the MEAS1_FILT_SEL.

MEAS7_PPG4_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS7_PPG3_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS7_PPG2_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS7_PPG1_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

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MEAS7 Configuration 3 (0x5C)

BIT	7	6	5	4	3	2	1	0
Field	MEAS7_PPG2_DACOFF[3:0]				MEAS7_PPG1_DACOFF[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

MEAS7_PPG2_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS7_PPG1_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS7 Configuration 4 (0x5D)

BIT	7	6	5	4	3	2	1	0
Field	MEAS7_PPG4_DACOFF[3:0]				MEAS7_PPG3_DACOFF[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

MEAS7_PPG4_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS7_PPG3_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS7 Configuration 5 (0x5E)

BIT	7	6	5	4	3	2	1	0
Field	MEAS7_PD_SETLNG[1:0]		MEAS7_LED_SETLNG[1:0]		–	–	MEAS7_LED_RGE[1:0]	
Reset	0x1		0x1		–	–	0x3	
Access Type	Write, Read		Write, Read		–	–	Write, Read	

MEAS7_PD_SETLNG

For details, see the MEAS1_PD_SETLNG[1:0].

MEAS7_LED_SETLNG

For details, see the MEAS1_LED_SETLNG[1:0].

MEAS7_LED_RGE

For details, see the MEAS1_LED_RGE[1:0].

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MEAS7 LEDA Current (0x5F)

BIT	7	6	5	4	3	2	1	0
Field	MEAS7_DRVA_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS7_DRVA_PA

For details, see the MEAS1_DRVA_PA[7:0].

MEAS7 LEDB Current (0x60)

BIT	7	6	5	4	3	2	1	0
Field	MEAS7_DRVB_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS7_DRVB_PA

For details, see the MEAS1_DRVA_PA[7:0].

MEAS7 PD SEL 1 (0x61)

BIT	7	6	5	4	3	2	1	0
Field	MEAS7_PD3_SEL[2:1]		MEAS7_PD2_SEL[2:0]			MEAS7_PD1_SEL[2:0]		
Reset	0x3		0x5			0x4		
Access Type	Write, Read		Write, Read			Write, Read		

MEAS7_PD3_SEL

For details, see the MEAS1_PD3_SEL[2:1] and the MEAS1_PD1_SEL[2:0].

MEAS7_PD2_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS7_PD1_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS7 PD SEL 2 (0x62)

BIT	7	6	5	4	3	2	1	0
Field	MEAS7_PD6_SEL[2]	MEAS7_PD5_SEL[2:0]			MEAS7_PD4_SEL[2:0]			MEAS7_PD3_SEL[0]
Reset	0	0x0			0x7			0
Access Type	Write, Read	Write, Read			Write, Read			Write, Read

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MEAS7_PD6_SEL

For details, see the MEAS1_PD6_SEL[2] and the MEAS1_PD1_SEL[2:0].

MEAS7_PD5_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS7_PD4_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS7_PD3_SEL

For details, see the MEAS1_PD3_SEL[0] and the MEAS1_PD1_SEL[2:0].

MEAS7 PD SEL 3 (0x63)

BIT	7	6	5	4	3	2	1	0
Field	MEAS7_PD8_SEL[2:0]			MEAS7_PD7_SEL[2:0]			MEAS7_PD6_SEL[1:0]	
Reset	0x0			0x0			0x0	
Access Type	Write, Read			Write, Read			Write, Read	

MEAS7_PD8_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS7_PD7_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS7_PD6_SEL

For details, see the MEAS1_PD6_SEL[1:0] and the MEAS1_PD1_SEL[2:0].

MEAS8 Selects (0x64)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS8_AMB	MEAS8_DRVB[2:0]			MEAS8_DRVA[2:0]		
Reset	–	0	0x0			0x0		
Access Type	–	Write, Read	Write, Read			Write, Read		

MEAS8_AMB

For details, see the MEAS1_AMB.

MEAS8_DRVB

For details, see the MEAS1_DRVB[2:0].

MEAS8_DRVA

For details, see the MEAS1_DRVA[2:0].

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MEAS8 Configuration 1 (0x65)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS8_DAC_LO_NOISE	MEAS8_FILT2_SEL	MEAS8_TINT[1:0]		MEAS8_AVER[2:0]		
Reset	–	0	1	0x3		0x0		
Access Type	–	Write, Read	Write, Read	Write, Read		Write, Read		

MEAS8_DAC_LO_NOISE

For details, see the MEAS1_DAC_LO_NOISE.

MEAS8_FILT2_SEL

For details, see the MEAS1_FILT2_SEL.

MEAS8_TINT

For details, see the MEAS1_TINT.

MEAS8_AVER

For details, see the MEAS1_AVER[2:0].

MEAS8 Configuration 2 (0x66)

BIT	7	6	5	4	3	2	1	0
Field	MEAS8_SINC3_SEL	MEAS8_FILT_SEL	–	–	MEAS8_PPG4_ADC_RGE	MEAS8_PPG3_ADC_RGE	MEAS8_PPG2_ADC_RGE	MEAS8_PPG1_ADC_RGE
Reset	0	0	–	–	0	0	0	0
Access Type	Write, Read	Write, Read	–	–	Write, Read	Write, Read	Write, Read	Write, Read

MEAS8_SINC3_SEL

For details, see the MEAS1_SINC3_SEL.

MEAS8_FILT_SEL

For details, see the MEAS1_FILT_SEL.

MEAS8_PPG4_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS8_PPG3_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS8_PPG2_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS8_PPG1_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

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MEAS8 Configuration 3 (0x67)

BIT	7	6	5	4	3	2	1	0
Field	MEAS8_PPG2_DACOFF[3:0]				MEAS8_PPG1_DACOFF[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

MEAS8_PPG2_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS8_PPG1_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS8 Configuration 4 (0x68)

BIT	7	6	5	4	3	2	1	0
Field	MEAS8_PPG4_DACOFF[3:0]				MEAS8_PPG3_DACOFF[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

MEAS8_PPG4_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS8_PPG3_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS8 Configuration 5 (0x69)

BIT	7	6	5	4	3	2	1	0
Field	MEAS8_PD_SETLNG[1:0]		MEAS8_LED_SETLNG[1:0]		–	–	MEAS8_LED_RGE[1:0]	
Reset	0x1		0x1		–	–	0x3	
Access Type	Write, Read		Write, Read		–	–	Write, Read	

MEAS8_PD_SETLNG

For details, see the MEAS1_PD_SETLNG[1:0].

MEAS8_LED_SETLNG

For details, see the MEAS1_LED_SETLNG[1:0].

MEAS8_LED_RGE

For details, see the MEAS1_LED_RGE[1:0].

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MEAS8 LEDA Current (0x6A)

BIT	7	6	5	4	3	2	1	0
Field	MEAS8_DRVA_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS8_DRVA_PA

For details, see the MEAS1_DRVA_PA[7:0].

MEAS8 LEDB Current (0x6B)

BIT	7	6	5	4	3	2	1	0
Field	MEAS8_DRVB_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS8_DRVB_PA

For details, see the MEAS1_DRVA_PA[7:0].

MEAS8 PD SEL 1 (0x6C)

BIT	7	6	5	4	3	2	1	0
Field	MEAS8_PD3_SEL[2:1]		MEAS8_PD2_SEL[2:0]			MEAS8_PD1_SEL[2:0]		
Reset	0x3		0x5			0x4		
Access Type	Write, Read		Write, Read			Write, Read		

MEAS8_PD3_SEL

For details, see the MEAS1_PD3_SEL[2:1] and the MEAS1_PD1_SEL[2:0].

MEAS8_PD2_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS8_PD1_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS8 PD SEL 2 (0x6D)

BIT	7	6	5	4	3	2	1	0
Field	MEAS8_PD6_SEL[2]	MEAS8_PD5_SEL[2:0]			MEAS8_PD4_SEL[2:0]			MEAS8_PD3_SEL[0]
Reset	0	0x0			0x7			0
Access Type	Write, Read	Write, Read			Write, Read			Write, Read

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MEAS8_PD6_SEL

For details, see the MEAS1_PD6_SEL[2] and the MEAS1_PD1_SEL[2:0].

MEAS8_PD5_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS8_PD4_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS8_PD3_SEL

For details, see the MEAS1_PD3_SEL[0] and the MEAS1_PD1_SEL[2:0].

MEAS8 PD SEL 3 (0x6E)

BIT	7	6	5	4	3	2	1	0
Field	MEAS8_PD8_SEL[2:0]			MEAS8_PD7_SEL[2:0]			MEAS8_PD6_SEL[1:0]	
Reset	0x0			0x0			0x0	
Access Type	Write, Read			Write, Read			Write, Read	

MEAS8_PD8_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS8_PD7_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS8_PD6_SEL

For details, see the MEAS1_PD6_SEL[1:0] and the MEAS1_PD1_SEL[2:0].

MEAS9 Selects (0x6F)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS9_AMB	MEAS9_DRVB[2:0]			MEAS9_DRVA[2:0]		
Reset	–	0	0x0			0x0		
Access Type	–	Write, Read	Write, Read			Write, Read		

MEAS9_AMB

For details, see the MEAS1_AMB.

MEAS9_DRVB

For details, see the MEAS1_DRVB[2:0].

MEAS9_DRVA

For details, see the MEAS1_DRVA[2:0].

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MEAS9 Configuration 1 (0x70)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS9_DAC_LO_NOISE	MEAS9_FILT2_SEL	MEAS9_TINT[1:0]		MEAS9_AVER[2:0]		
Reset	–	0	1	0x3		0x0		
Access Type	–	Write, Read	Write, Read	Write, Read		Write, Read		

MEAS9_DAC_LO_NOISE
For details, see the MEAS1_DAC_LO_NOISE.

MEAS9_FILT2_SEL
For details, see the MEAS1_FILT2_SEL.

MEAS9_TINT
For details, see the MEAS1_TINT.

MEAS9_AVER
For details, see the MEAS1_AVER[2:0].

MEAS9 Configuration 2 (0x71)

BIT	7	6	5	4	3	2	1	0
Field	MEAS9_SINC3_SEL	MEAS9_FILT_SEL	–	–	MEAS9_PPG4_ADC_RGE	MEAS9_PPG3_ADC_RGE	MEAS9_PPG2_ADC_RGE	MEAS9_PPG1_ADC_RGE
Reset	0	0	–	–	0	0	0	0
Access Type	Write, Read	Write, Read	–	–	Write, Read	Write, Read	Write, Read	Write, Read

MEAS9_SINC3_SEL
For details, see the MEAS1_SINC3_SEL.

MEAS9_FILT_SEL
For details, see the MEAS1_FILT_SEL.

MEAS9_PPG4_ADC_RGE
For details, see the MEAS1_PPG4_ADC_RGE.

MEAS9_PPG3_ADC_RGE
For details, see the MEAS1_PPG4_ADC_RGE.

MEAS9_PPG2_ADC_RGE
For details, see the MEAS1_PPG4_ADC_RGE.

MEAS9_PPG1_ADC_RGE
For details, see the MEAS1_PPG4_ADC_RGE.

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MEAS9 Configuration 3 (0x72)

BIT	7	6	5	4	3	2	1	0
Field	MEAS9_PPG2_DACOFF[3:0]				MEAS9_PPG1_DACOFF[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

MEAS9_PPG2_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS9_PPG1_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS9 Configuration 4 (0x73)

BIT	7	6	5	4	3	2	1	0
Field	MEAS9_PPG4_DACOFF[3:0]				MEAS9_PPG3_DACOFF[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

MEAS9_PPG4_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS9_PPG3_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS9 Configuration 5 (0x74)

BIT	7	6	5	4	3	2	1	0
Field	MEAS9_PD_SETLNG[1:0]		MEAS9_LED_SETLNG[1:0]		–	–	MEAS9_LED_RGE[1:0]	
Reset	0x1		0x1		–	–	0x3	
Access Type	Write, Read		Write, Read		–	–	Write, Read	

MEAS9_PD_SETLNG

For details, see the MEAS1_PD_SETLNG[1:0].

MEAS9_LED_SETLNG

For details, see the MEAS1_LED_SETLNG[1:0].

MEAS9_LED_RGE

For details, see the MEAS1_LED_RGE[1:0].

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MEAS9 LEDA Current (0x75)

BIT	7	6	5	4	3	2	1	0
Field	MEAS9_DRVA_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS9_DRVA_PA

For details, see the MEAS1_DRVA_PA[7:0].

MEAS9 LEDB Current (0x76)

BIT	7	6	5	4	3	2	1	0
Field	MEAS9_DRVB_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS9_DRVB_PA

For details, see the MEAS1_DRVA_PA[7:0].

MEAS9 PD SEL 1 (0x77)

BIT	7	6	5	4	3	2	1	0
Field	MEAS9_PD3_SEL[2:1]		MEAS9_PD2_SEL[2:0]			MEAS9_PD1_SEL[2:0]		
Reset	0x3		0x5			0x4		
Access Type	Write, Read		Write, Read			Write, Read		

MEAS9_PD3_SEL

For details, see the MEAS1_PD3_SEL[2:1] and the MEAS1_PD1_SEL[2:0].

MEAS9_PD2_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS9_PD1_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS9 PD SEL 2 (0x78)

BIT	7	6	5	4	3	2	1	0
Field	MEAS9_PD6_SEL[2]	MEAS9_PD5_SEL[2:0]			MEAS9_PD4_SEL[2:0]			MEAS9_PD3_SEL[0]
Reset	0	0x0			0x7			0
Access Type	Write, Read	Write, Read			Write, Read			Write, Read

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MEAS9_PD6_SEL

For details, see the MEAS1_PD6_SEL[2] and the MEAS1_PD1_SEL[2:0].

MEAS9_PD5_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS9_PD4_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS9_PD3_SEL

For details, see the MEAS1_PD3_SEL[0] and the MEAS1_PD1_SEL[2:0].

MEAS9 PD SEL 3 (0x79)

BIT	7	6	5	4	3	2	1	0
Field	MEAS9_PD8_SEL[2:0]			MEAS9_PD7_SEL[2:0]			MEAS9_PD6_SEL[1:0]	
Reset	0x0			0x0			0x0	
Access Type	Write, Read			Write, Read			Write, Read	

MEAS9_PD8_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS9_PD7_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS9_PD6_SEL

For details, see the MEAS1_PD6_SEL[1:0] and the MEAS1_PD1_SEL[2:0].

MEAS10 Selects (0x7A)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS10_AMB	MEAS10_DRVB[2:0]			MEAS10_DRVA[2:0]		
Reset	–	0	0x0			0x0		
Access Type	–	Write, Read	Write, Read			Write, Read		

MEAS10_AMB

For details, see the MEAS1_AMB.

MEAS10_DRVB

For details, see the MEAS1_DRVB[2:0].

MEAS10_DRVA

For details, see the MEAS1_DRVA[2:0].

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MEAS10 Configuration 1 (0x7B)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS10_DAC_LO_NOISE	MEAS10_FILT2_SEL	MEAS10_TINT[1:0]		MEAS10_AVER[2:0]		
Reset	–	0	1	0x3		0x0		
Access Type	–	Write, Read	Write, Read	Write, Read		Write, Read		

MEAS10_DAC_LO_NOISE

For details, see the MEAS1_DAC_LO_NOISE.

MEAS10_FILT2_SEL

For details, see the MEAS1_FILT2_SEL.

MEAS10_TINT

For details, see the MEAS1_TINT.

MEAS10_AVER

For details, see the MEAS1_AVER[2:0].

MEAS10 Configuration 2 (0x7C)

BIT	7	6	5	4	3	2	1	0
Field	MEAS10_SINC3_SEL	MEAS10_FILT_SEL	–	–	MEAS10_PPG4_ADC_RGE	MEAS10_PPG3_ADC_RGE	MEAS10_PPG2_ADC_RGE	MEAS10_PPG1_ADC_RGE
Reset	0	0	–	–	0	0	0	0
Access Type	Write, Read	Write, Read	–	–	Write, Read	Write, Read	Write, Read	Write, Read

MEAS10_SINC3_SEL

For details, see the MEAS1_SINC3_SEL.

MEAS10_FILT_SEL

For details, see the MEAS1_FILT_SEL.

MEAS10_PPG4_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS10_PPG3_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS10_PPG2_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS10_PPG1_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

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MEAS10 Configuration 3 (0x7D)

BIT	7	6	5	4	3	2	1	0
Field	MEAS10_PPG2_DACOFF[3:0]				MEAS10_PPG1_DACOFF[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

MEAS10_PPG2_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS10_PPG1_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS10 Configuration 4 (0x7E)

BIT	7	6	5	4	3	2	1	0
Field	MEAS10_PPG4_DACOFF[3:0]				MEAS10_PPG3_DACOFF[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

MEAS10_PPG4_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS10_PPG3_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS10 Configuration 5 (0x7F)

BIT	7	6	5	4	3	2	1	0
Field	MEAS10_PD_SETLNG[1:0]		MEAS10_LED_SETLNG[1:0]		–	–	MEAS10_LED_RGE[1:0]	
Reset	0x1		0x1		–	–	0x3	
Access Type	Write, Read		Write, Read		–	–	Write, Read	

MEAS10_PD_SETLNG

For details, see the MEAS1_PD_SETLNG[1:0].

MEAS10_LED_SETLNG

For details, see the MEAS1_LED_SETLNG[1:0].

MEAS10_LED_RGE

For details, see the MEAS1_LED_RGE[1:0].

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MEAS10 LEDA Current (0x80)

BIT	7	6	5	4	3	2	1	0
Field	MEAS10_DRVA_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS10_DRVA_PA

For details, see the MEAS1_DRVA_PA[7:0].

MEAS10 LEDB Current (0x81)

BIT	7	6	5	4	3	2	1	0
Field	MEAS10_DRVB_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS10_DRVB_PA

For details, see the MEAS1_DRVA_PA[7:0].

MEAS10 PD SEL 1 (0x82)

BIT	7	6	5	4	3	2	1	0
Field	MEAS10_PD3_SEL[2:1]		MEAS10_PD2_SEL[2:0]			MEAS10_PD1_SEL[2:0]		
Reset	0x3		0x5			0x4		
Access Type	Write, Read		Write, Read			Write, Read		

MEAS10_PD3_SEL

For details, see the MEAS1_PD3_SEL[2:1] and the MEAS1_PD1_SEL[2:0].

MEAS10_PD2_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS10_PD1_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS10 PD SEL 2 (0x83)

BIT	7	6	5	4	3	2	1	0
Field	MEAS10_PD6_SEL[2]	MEAS10_PD5_SEL[2:0]			MEAS10_PD4_SEL[2:0]			MEAS10_PD3_SEL[0]
Reset	0	0x0			0x7			0
Access Type	Write, Read	Write, Read			Write, Read			Write, Read

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MEAS10_PD6_SEL

For details, see the MEAS1_PD6_SEL[2] and the MEAS1_PD1_SEL[2:0].

MEAS10_PD5_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS10_PD4_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS10_PD3_SEL

For details, see the MEAS1_PD3_SEL[0] and the MEAS1_PD1_SEL[2:0].

MEAS10 PD SEL 3 (0x84)

BIT	7	6	5	4	3	2	1	0
Field	MEAS10_PD8_SEL[2:0]			MEAS10_PD7_SEL[2:0]			MEAS10_PD6_SEL[1:0]	
Reset	0x0			0x0			0x0	
Access Type	Write, Read			Write, Read			Write, Read	

MEAS10_PD8_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS10_PD7_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS10_PD6_SEL

For details, see the MEAS1_PD6_SEL[1:0] and the MEAS1_PD1_SEL[2:0].

MEAS11 Selects (0x85)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS11_AMB	MEAS11_DRVB[2:0]			MEAS11_DRVA[2:0]		
Reset	–	0	0x0			0x0		
Access Type	–	Write, Read	Write, Read			Write, Read		

MEAS11_AMB

For details, see the MEAS1_AMB.

MEAS11_DRVB

For details, see the MEAS1_DRVB[2:0].

MEAS11_DRVA

For details, see the MEAS1_DRVA[2:0].

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MEAS11 Configuration 1 (0x86)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS11_DAC_LO_NOISE	MEAS11_FILT2_SEL	MEAS11_TINT[1:0]		MEAS11_AVER[2:0]		
Reset	–	0	1	0x3		0x0		
Access Type	–	Write, Read	Write, Read	Write, Read		Write, Read		

MEAS11_DAC_LO_NOISE

For details, see the MEAS1_DAC_LO_NOISE.

MEAS11_FILT2_SEL

For details, see the MEAS1_FILT2_SEL.

MEAS11_TINT

For details, see the MEAS1_TINT.

MEAS11_AVER

For details, see the MEAS1_AVER[2:0].

MEAS11 Configuration 2 (0x87)

BIT	7	6	5	4	3	2	1	0
Field	MEAS11_SINC3_SEL	MEAS11_FILT_SEL	–	–	MEAS11_PPG4_ADC_RGE	MEAS11_PPG3_ADC_RGE	MEAS11_PPG2_ADC_RGE	MEAS11_PPG1_ADC_RGE
Reset	0	0	–	–	0	0	0	0
Access Type	Write, Read	Write, Read	–	–	Write, Read	Write, Read	Write, Read	Write, Read

MEAS11_SINC3_SEL

For details, see the MEAS1_SINC3_SEL.

MEAS11_FILT_SEL

For details, see the MEAS1_FILT_SEL.

MEAS11_PPG4_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS11_PPG3_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS11_PPG2_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS11_PPG1_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

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MEAS11 Configuration 3 (0x88)

BIT	7	6	5	4	3	2	1	0
Field	MEAS11_PPG2_DACOFF[3:0]				MEAS11_PPG1_DACOFF[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

MEAS11_PPG2_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS11_PPG1_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS11 Configuration 4 (0x89)

BIT	7	6	5	4	3	2	1	0
Field	MEAS11_PPG4_DACOFF[3:0]				MEAS11_PPG3_DACOFF[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

MEAS11_PPG4_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS11_PPG3_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS11 Configuration 5 (0x8A)

BIT	7	6	5	4	3	2	1	0
Field	MEAS11_PD_SETLNG[1:0]		MEAS11_LED_SETLNG[1:0]		–	–	MEAS11_LED_RGE[1:0]	
Reset	0x1		0x1		–	–	0x3	
Access Type	Write, Read		Write, Read		–	–	Write, Read	

MEAS11_PD_SETLNG

For details, see the MEAS1_PD_SETLNG[1:0].

MEAS11_LED_SETLNG

For details, see the MEAS1_LED_SETLNG[1:0].

MEAS11_LED_RGE

For details, see the MEAS1_LED_RGE[1:0].

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MEAS11 LEDA Current (0x8B)

BIT	7	6	5	4	3	2	1	0
Field	MEAS11_DRVA_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS11_DRVA_PA

For details, see the MEAS1_DRVA_PA[7:0].

MEAS11 LEDB Current (0x8C)

BIT	7	6	5	4	3	2	1	0
Field	MEAS11_DRVB_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS11_DRVB_PA

For details, see the MEAS1_DRVA_PA[7:0].

MEAS11 PD SEL 1 (0x8D)

BIT	7	6	5	4	3	2	1	0
Field	MEAS11_PD3_SEL[2:1]		MEAS11_PD2_SEL[2:0]			MEAS11_PD1_SEL[2:0]		
Reset	0x3		0x5			0x4		
Access Type	Write, Read		Write, Read			Write, Read		

MEAS11_PD3_SEL

For details, see the MEAS1_PD3_SEL[2:1] and the MEAS1_PD1_SEL[2:0].

MEAS11_PD2_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS11_PD1_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS11 PD SEL 2 (0x8E)

BIT	7	6	5	4	3	2	1	0
Field	MEAS11_PD6_SEL[2]	MEAS11_PD5_SEL[2:0]			MEAS11_PD4_SEL[2:0]			MEAS11_PD3_SEL[0]
Reset	0	0x0			0x7			0
Access Type	Write, Read	Write, Read			Write, Read			Write, Read

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MEAS11_PD6_SEL

For details, see the MEAS1_PD6_SEL[2] and the MEAS1_PD1_SEL[2:0].

MEAS11_PD5_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS11_PD4_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS11_PD3_SEL

For details, see the MEAS1_PD3_SEL[0] and the MEAS1_PD1_SEL[2:0].

MEAS11 PD SEL 3 (0x8F)

BIT	7	6	5	4	3	2	1	0
Field	MEAS11_PD8_SEL[2:0]			MEAS11_PD7_SEL[2:0]			MEAS11_PD6_SEL[1:0]	
Reset	0x0			0x0			0x0	
Access Type	Write, Read			Write, Read			Write, Read	

MEAS11_PD8_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS11_PD7_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS11_PD6_SEL

For details, see the MEAS1_PD6_SEL[1:0] and the MEAS1_PD1_SEL[2:0].

MEAS12 Selects (0x90)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS12_AMB	MEAS12_DRVB[2:0]			MEAS12_DRVA[2:0]		
Reset	–	0	0x0			0x0		
Access Type	–	Write, Read	Write, Read			Write, Read		

MEAS12_AMB

For details, see the MEAS1_AMB.

MEAS12_DRVB

For details, see the MEAS1_DRVB[2:0].

MEAS12_DRVA

For details, see the MEAS1_DRVA[2:0].

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MEAS12 Configuration 1 (0x91)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS12_DAC_LO_NOISE	MEAS12_FILT2_SEL	MEAS12_TINT[1:0]		MEAS12_AVER[2:0]		
Reset	–	0	1	0x3		0x0		
Access Type	–	Write, Read	Write, Read	Write, Read		Write, Read		

MEAS12_DAC_LO_NOISE

For details, see the MEAS1_DAC_LO_NOISE.

MEAS12_FILT2_SEL

For details, see the MEAS1_FILT2_SEL.

MEAS12_TINT

For details, see the MEAS1_TINT.

MEAS12_AVER

For details, see the MEAS1_AVER[2:0].

MEAS12 Configuration 2 (0x92)

BIT	7	6	5	4	3	2	1	0
Field	MEAS12_SINC3_SEL	MEAS12_FILT_SEL	–	–	MEAS12_PPG4_ADC_RGE	MEAS12_PPG3_ADC_RGE	MEAS12_PPG2_ADC_RGE	MEAS12_PPG1_ADC_RGE
Reset	0	0	–	–	0	0	0	0
Access Type	Write, Read	Write, Read	–	–	Write, Read	Write, Read	Write, Read	Write, Read

MEAS12_SINC3_SEL

For details, see the MEAS1_SINC3_SEL.

MEAS12_FILT_SEL

For details, see the MEAS1_FILT_SEL.

MEAS12_PPG4_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS12_PPG3_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS12_PPG2_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS12_PPG1_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

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MEAS12 Configuration 3 (0x93)

BIT	7	6	5	4	3	2	1	0
Field	MEAS12_PPG2_DACOFF[3:0]				MEAS12_PPG1_DACOFF[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

MEAS12_PPG2_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS12_PPG1_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS12 Configuration 4 (0x94)

BIT	7	6	5	4	3	2	1	0
Field	MEAS12_PPG4_DACOFF[3:0]				MEAS12_PPG3_DACOFF[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

MEAS12_PPG4_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS12_PPG3_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS12 Configuration 5 (0x95)

BIT	7	6	5	4	3	2	1	0
Field	MEAS12_PD_SETLNG[1:0]		MEAS12_LED_SETLNG[1:0]		–	–	MEAS12_LED_RGE[1:0]	
Reset	0x1		0x1		–	–	0x3	
Access Type	Write, Read		Write, Read		–	–	Write, Read	

MEAS12_PD_SETLNG

For details, see the MEAS1_PD_SETLNG[1:0].

MEAS12_LED_SETLNG

For details, see the MEAS1_LED_SETLNG[1:0].

MEAS12_LED_RGE

For details, see the MEAS1_LED_RGE[1:0].

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MEAS12 LEDA Current (0x96)

BIT	7	6	5	4	3	2	1	0
Field	MEAS12_DRVA_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS12_DRVA_PA

For details, see the MEAS1_DRVA_PA[7:0].

MEAS12 LEDB Current (0x97)

BIT	7	6	5	4	3	2	1	0
Field	MEAS12_DRVB_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS12_DRVB_PA

For details, see the MEAS1_DRVA_PA[7:0].

MEAS12 PD SEL 1 (0x98)

BIT	7	6	5	4	3	2	1	0
Field	MEAS12_PD3_SEL[2:1]		MEAS12_PD2_SEL[2:0]			MEAS12_PD1_SEL[2:0]		
Reset	0x3		0x5			0x4		
Access Type	Write, Read		Write, Read			Write, Read		

MEAS12_PD3_SEL

For details, see the MEAS1_PD3_SEL[2:1] and the MEAS1_PD1_SEL[2:0].

MEAS12_PD2_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS12_PD1_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS12 PD SEL 2 (0x99)

BIT	7	6	5	4	3	2	1	0
Field	MEAS12_PD6_SEL[2]	MEAS12_PD5_SEL[2:0]			MEAS12_PD4_SEL[2:0]			MEAS12_PD3_SEL[0]
Reset	0	0x0			0x7			0
Access Type	Write, Read	Write, Read			Write, Read			Write, Read

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MEAS12_PD6_SEL

For details, see the MEAS1_PD6_SEL[2] and the MEAS1_PD1_SEL[2:0].

MEAS12_PD5_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS12_PD4_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS12_PD3_SEL

For details, see the MEAS1_PD3_SEL[0] and the MEAS1_PD1_SEL[2:0].

MEAS12 PD SEL 3 (0x9A)

BIT	7	6	5	4	3	2	1	0
Field	MEAS12_PD8_SEL[2:0]			MEAS12_PD7_SEL[2:0]			MEAS12_PD6_SEL[1:0]	
Reset	0x0			0x0			0x0	
Access Type	Write, Read			Write, Read			Write, Read	

MEAS12_PD8_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS12_PD7_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS12_PD6_SEL

For details, see the MEAS1_PD6_SEL[1:0] and the MEAS1_PD1_SEL[2:0].

MEAS13 Selects (0x9B)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS13_AMB	MEAS13_DRVB[2:0]			MEAS13_DRVA[2:0]		
Reset	–	0	0x0			0x0		
Access Type	–	Write, Read	Write, Read			Write, Read		

MEAS13_AMB

For details, see the MEAS1_AMB.

MEAS13_DRVB

For details, see the MEAS1_DRVB[2:0].

MEAS13_DRVA

For details, see the MEAS1_DRVA[2:0].

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MEAS13 Configuration 1 (0x9C)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS13_DAC_LO_NOISE	MEAS13_FILT2_SEL	MEAS13_TINT[1:0]		MEAS13_AVER[2:0]		
Reset	–	0	1	0x3		0x0		
Access Type	–	Write, Read	Write, Read	Write, Read		Write, Read		

MEAS13_DAC_LO_NOISE

For details, see the MEAS1_DAC_LO_NOISE.

MEAS13_FILT2_SEL

For details, see the MEAS1_FILT2_SEL.

MEAS13_TINT

For details, see the MEAS1_TINT.

MEAS13_AVER

For details, see the MEAS1_AVER[2:0].

MEAS13 Configuration 2 (0x9D)

BIT	7	6	5	4	3	2	1	0
Field	MEAS13_SINC3_SEL	MEAS13_FILT_SEL	–	–	MEAS13_PPG4_ADC_RGE	MEAS13_PPG3_ADC_RGE	MEAS13_PPG2_ADC_RGE	MEAS13_PPG1_ADC_RGE
Reset	0	0	–	–	0	0	0	0
Access Type	Write, Read	Write, Read	–	–	Write, Read	Write, Read	Write, Read	Write, Read

MEAS13_SINC3_SEL

For details, see the MEAS1_SINC3_SEL.

MEAS13_FILT_SEL

For details, see the MEAS1_FILT_SEL.

MEAS13_PPG4_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS13_PPG3_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS13_PPG2_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS13_PPG1_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

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MEAS13 Configuration 3 (0x9E)

BIT	7	6	5	4	3	2	1	0
Field	MEAS13_PPG2_DACOFF[3:0]				MEAS13_PPG1_DACOFF[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

MEAS13_PPG2_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS13_PPG1_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS13 Configuration 4 (0x9F)

BIT	7	6	5	4	3	2	1	0
Field	MEAS13_PPG4_DACOFF[3:0]				MEAS13_PPG3_DACOFF[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

MEAS13_PPG4_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS13_PPG3_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS13 Configuration 5 (0xA0)

BIT	7	6	5	4	3	2	1	0
Field	MEAS13_PD_SETLNG[1:0]		MEAS13_LED_SETLNG[1:0]		–	–	MEAS13_LED_RGE[1:0]	
Reset	0x1		0x1		–	–	0x3	
Access Type	Write, Read		Write, Read		–	–	Write, Read	

MEAS13_PD_SETLNG

For details, see the MEAS1_PD_SETLNG[1:0].

MEAS13_LED_SETLNG

For details, see the MEAS1_LED_SETLNG[1:0].

MEAS13_LED_RGE

For details, see the MEAS1_LED_RGE[1:0].

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MEAS13 LEDA Current (0xA1)

BIT	7	6	5	4	3	2	1	0
Field	MEAS13_DRVA_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS13_DRVA_PA

For details, see the MEAS1_DRVA_PA[7:0].

MEAS13 LEDB Current (0xA2)

BIT	7	6	5	4	3	2	1	0
Field	MEAS13_DRVB_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS13_DRVB_PA

For details, see the MEAS1_DRVA_PA[7:0].

MEAS13 PD SEL 1 (0xA3)

BIT	7	6	5	4	3	2	1	0
Field	MEAS13_PD3_SEL[2:1]		MEAS13_PD2_SEL[2:0]			MEAS13_PD1_SEL[2:0]		
Reset	0x3		0x5			0x4		
Access Type	Write, Read		Write, Read			Write, Read		

MEAS13_PD3_SEL

For details, see the MEAS1_PD3_SEL[2:1] and the MEAS1_PD1_SEL[2:0].

MEAS13_PD2_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS13_PD1_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS13 PD SEL 2 (0xA4)

BIT	7	6	5	4	3	2	1	0
Field	MEAS13_PD6_SEL[2]	MEAS13_PD5_SEL[2:0]			MEAS13_PD4_SEL[2:0]			MEAS13_PD3_SEL[0]
Reset	0	0x0			0x7			0
Access Type	Write, Read	Write, Read			Write, Read			Write, Read

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MEAS13_PD6_SEL

For details, see the MEAS1_PD6_SEL[2] and the MEAS1_PD1_SEL[2:0].

MEAS13_PD5_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS13_PD4_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS13_PD3_SEL

For details, see the MEAS1_PD3_SEL[0] and the MEAS1_PD1_SEL[2:0].

MEAS13 PD SEL 3 (0xA5)

BIT	7	6	5	4	3	2	1	0
Field	MEAS13_PD8_SEL[2:0]			MEAS13_PD7_SEL[2:0]			MEAS3_PD6_SEL[1:0]	
Reset	0x0			0x0			0x0	
Access Type	Write, Read			Write, Read			Write, Read	

MEAS13_PD8_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS13_PD7_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS3_PD6_SEL

For details, see the MEAS1_PD6_SEL[1:0] and the MEAS1_PD1_SEL[2:0].

MEAS14 Selects (0xA6)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS14_AMB	MEAS14_DRVB[2:0]			MEAS14_DRVA[2:0]		
Reset	–	0	0x0			0x0		
Access Type	–	Write, Read	Write, Read			Write, Read		

MEAS14_AMB

For details, see the MEAS1_AMB.

MEAS14_DRVB

For details, see the MEAS1_DRVB[2:0].

MEAS14_DRVA

For details, see the MEAS1_DRVA[2:0].

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MEAS14 Configuration 1 (0xA7)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS14_DAC_LO_NOISE	MEAS14_FILT2_SEL	MEAS14_TINT[1:0]		MEAS14_AVER[2:0]		
Reset	–	0	1	0x3		0x0		
Access Type	–	Write, Read	Write, Read	Write, Read		Write, Read		

MEAS14_DAC_LO_NOISE

For details, see the MEAS1_DAC_LO_NOISE.

MEAS14_FILT2_SEL

For details, see the MEAS1_FILT2_SEL.

MEAS14_TINT

For details, see the MEAS1_TINT.

MEAS14_AVER

For details, see the MEAS1_AVER[2:0].

MEAS14 Configuration 2 (0xA8)

BIT	7	6	5	4	3	2	1	0
Field	MEAS14_SINC3_SEL	MEAS14_FILT_SEL	–	–	MEAS14_PPG4_ADC_RGE	MEAS14_PPG3_ADC_RGE	MEAS14_PPG2_ADC_RGE	MEAS14_PPG1_ADC_RGE
Reset	0	0	–	–	0	0	0	0
Access Type	Write, Read	Write, Read	–	–	Write, Read	Write, Read	Write, Read	Write, Read

MEAS14_SINC3_SEL

For details, see the MEAS1_SINC3_SEL.

MEAS14_FILT_SEL

For details, see the MEAS1_FILT_SEL.

MEAS14_PPG4_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS14_PPG3_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS14_PPG2_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS14_PPG1_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

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MEAS14 Configuration 3 (0xA9)

BIT	7	6	5	4	3	2	1	0
Field	MEAS14_PPG2_DACOFF[3:0]				MEAS14_PPG1_DACOFF[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

MEAS14_PPG2_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS14_PPG1_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS14 Configuration 4 (0xAA)

BIT	7	6	5	4	3	2	1	0
Field	MEAS14_PPG4_DACOFF[3:0]				MEAS14_PPG3_DACOFF[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

MEAS14_PPG4_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS14_PPG3_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS14 Configuration 5 (0xAB)

BIT	7	6	5	4	3	2	1	0
Field	MEAS14_PD_SETLNG[1:0]		MEAS14_LED_SETLNG[1:0]		–	–	MEAS14_LED_RGE[1:0]	
Reset	0x1		0x1		–	–	0x3	
Access Type	Write, Read		Write, Read		–	–	Write, Read	

MEAS14_PD_SETLNG

For details, see the MEAS1_PD_SETLNG[1:0].

MEAS14_LED_SETLNG

For details, see the MEAS1_LED_SETLNG[1:0].

MEAS14_LED_RGE

For details, see the MEAS1_LED_RGE[1:0].

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MEAS14 LEDA Current (0xAC)

BIT	7	6	5	4	3	2	1	0
Field	MEAS14_DRVA_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS14_DRVA_PA

For details, see the MEAS1_DRVA_PA[7:0].

MEAS14 LEDB Current (0xAD)

BIT	7	6	5	4	3	2	1	0
Field	MEAS14_DRVB_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS14_DRVB_PA

For details, see the MEAS1_DRVA_PA[7:0].

MEAS14 PD SEL 1 (0xAE)

BIT	7	6	5	4	3	2	1	0
Field	MEAS14_PD3_SEL[2:1]		MEAS14_PD2_SEL[2:0]			MEAS14_PD1_SEL[2:0]		
Reset	0x3		0x5			0x4		
Access Type	Write, Read		Write, Read			Write, Read		

MEAS14_PD3_SEL

For details, see the MEAS1_PD3_SEL[2:1] and the MEAS1_PD1_SEL[2:0].

MEAS14_PD2_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS14_PD1_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS14 PD SEL 2 (0xAF)

BIT	7	6	5	4	3	2	1	0
Field	MEAS14_PD6_SEL[2]	MEAS14_PD5_SEL[2:0]			MEAS14_PD4_SEL[2:0]			MEAS14_PD3_SEL[0]
Reset	0	0x0			0x7			0
Access Type	Write, Read	Write, Read			Write, Read			Write, Read

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MEAS14_PD6_SEL

For details, see the MEAS1_PD6_SEL[2] and the MEAS1_PD1_SEL[2:0].

MEAS14_PD5_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS14_PD4_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS14_PD3_SEL

For details, see the MEAS1_PD3_SEL[0] and the MEAS1_PD1_SEL[2:0].

MEAS14 PD SEL 3 (0xB0)

BIT	7	6	5	4	3	2	1	0
Field	MEAS14_PD8_SEL[2:0]			MEAS14_PD7_SEL[2:0]			MEAS14_PD6_SEL[1:0]	
Reset	0x0			0x0			0x0	
Access Type	Write, Read			Write, Read			Write, Read	

MEAS14_PD8_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS14_PD7_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS14_PD6_SEL

For details, see the MEAS1_PD6_SEL[1:0] and the MEAS1_PD1_SEL[2:0].

MEAS15 Selects (0xB1)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS15_AMB	MEAS15_DRVB[2:0]			MEAS15_DRVA[2:0]		
Reset	–	0	0x0			0x0		
Access Type	–	Write, Read	Write, Read			Write, Read		

MEAS15_AMB

For details, see the MEAS1_AMB.

MEAS15_DRVB

For details, see the MEAS1_DRVB[2:0].

MEAS15_DRVA

For details, see the MEAS1_DRVA[2:0].

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MEAS15 Configuration 1 (0xB2)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS15_DAC_LO_NOISE	MEAS15_FILT2_SEL	MEAS15_TINT[1:0]		MEAS15_AVER[2:0]		
Reset	–	0	1	0x3		0x0		
Access Type	–	Write, Read	Write, Read	Write, Read		Write, Read		

MEAS15_DAC_LO_NOISE
For details, see the MEAS1_DAC_LO_NOISE.

MEAS15_FILT2_SEL
For details, see the MEAS1_FILT2_SEL.

MEAS15_TINT
For details, see the MEAS1_TINT.

MEAS15_AVER
For details, see the MEAS1_AVER[2:0].

MEAS15 Configuration 2 (0xB3)

BIT	7	6	5	4	3	2	1	0
Field	MEAS15_SINC3_SEL	MEAS15_FILT_SEL	–	–	MEAS15_PPG4_ADC_RGE	MEAS15_PPG3_ADC_RGE	MEAS15_PPG2_ADC_RGE	MEAS15_PPG1_ADC_RGE
Reset	0	0	–	–	0	0	0	0
Access Type	Write, Read	Write, Read	–	–	Write, Read	Write, Read	Write, Read	Write, Read

MEAS15_SINC3_SEL
For details, see the MEAS1_SINC3_SEL.

MEAS15_FILT_SEL
For details, see the MEAS1_FILT_SEL.

MEAS15_PPG4_ADC_RGE
For details, see the MEAS1_PPG4_ADC_RGE.

MEAS15_PPG3_ADC_RGE
For details, see the MEAS1_PPG4_ADC_RGE.

MEAS15_PPG2_ADC_RGE
For details, see the MEAS1_PPG4_ADC_RGE.

MEAS15_PPG1_ADC_RGE
For details, see the MEAS1_PPG4_ADC_RGE.

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MEAS15 Configuration 3 (0xB4)

BIT	7	6	5	4	3	2	1	0
Field	MEAS15_PPG2_DACOFF[3:0]				MEAS15_PPG1_DACOFF[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

MEAS15_PPG2_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS15_PPG1_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS15 Configuration 4 (0xB5)

BIT	7	6	5	4	3	2	1	0
Field	MEAS15_PPG4_DACOFF[3:0]				MEAS15_PPG3_DACOFF[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

MEAS15_PPG4_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS15_PPG3_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS15 Configuration 5 (0xB6)

BIT	7	6	5	4	3	2	1	0
Field	MEAS15_PD_SETLNG[1:0]		MEAS15_LED_SETLNG[1:0]		–	–	MEAS15_LED_RGE[1:0]	
Reset	0x1		0x1		–	–	0x3	
Access Type	Write, Read		Write, Read		–	–	Write, Read	

MEAS15_PD_SETLNG

For details, see the MEAS1_PD_SETLNG[1:0].

MEAS15_LED_SETLNG

For details, see the MEAS1_LED_SETLNG[1:0].

MEAS15_LED_RGE

For details, see the MEAS1_LED_RGE[1:0].

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MEAS15 LEDA Current (0xB7)

BIT	7	6	5	4	3	2	1	0
Field	MEAS15_DRVA_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS15_DRVA_PA

For details, see the MEAS1_DRVA_PA[7:0].

MEAS15 LEDB Current (0xB8)

BIT	7	6	5	4	3	2	1	0
Field	MEAS15_DRVB_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS15_DRVB_PA

For details, see the MEAS1_DRVA_PA[7:0].

MEAS15 PD SEL 1 (0xB9)

BIT	7	6	5	4	3	2	1	0
Field	MEAS15_PD3_SEL[2:1]		MEAS15_PD2_SEL[2:0]			MEAS15_PD1_SEL[2:0]		
Reset	0x3		0x5			0x4		
Access Type	Write, Read		Write, Read			Write, Read		

MEAS15_PD3_SEL

For details, see the MEAS1_PD3_SEL[2:1] and the MEAS1_PD1_SEL[2:0].

MEAS15_PD2_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS15_PD1_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS15 PD SEL 2 (0xBA)

BIT	7	6	5	4	3	2	1	0
Field	MEAS15_PD6_SEL[2]	MEAS15_PD5_SEL[2:0]			MEAS15_PD4_SEL[2:0]			MEAS15_PD3_SEL[0]
Reset	0	0x0			0x7			0
Access Type	Write, Read	Write, Read			Write, Read			Write, Read

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MEAS15_PD6_SEL

For details, see the MEAS1_PD6_SEL[2] and the MEAS1_PD1_SEL[2:0].

MEAS15_PD5_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS15_PD4_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS15_PD3_SEL

For details, see the MEAS1_PD3_SEL[0] and the MEAS1_PD1_SEL[2:0].

MEAS15 PD SEL 3 (0xBB)

BIT	7	6	5	4	3	2	1	0
Field	MEAS15_PD8_SEL[2:0]			MEAS15_PD7_SEL[2:0]			MEAS15_PD6_SEL[1:0]	
Reset	0x0			0x0			0x0	
Access Type	Write, Read			Write, Read			Write, Read	

MEAS15_PD8_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS15_PD7_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS15_PD6_SEL

For details, see the MEAS1_PD6_SEL[1:0] and the MEAS1_PD1_SEL[2:0].

MEAS16 Selects (0xBC)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS16_AMB	MEAS16_DRVB[2:0]			MEAS16_DRVA[2:0]		
Reset	–	0	0x0			0x0		
Access Type	–	Write, Read	Write, Read			Write, Read		

MEAS16_AMB

For details, see the MEAS1_AMB.

MEAS16_DRVB

For details, see the MEAS1_DRVB[2:0].

MEAS16_DRVA

For details, see the MEAS1_DRVA[2:0].

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MEAS16 Configuration 1 (0xBD)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS16_DAC_LO_NOISE	MEAS16_FILT2_SEL	MEAS16_TINT[1:0]		MEAS16_AVER[2:0]		
Reset	–	0	1	0x3		0x0		
Access Type	–	Write, Read	Write, Read	Write, Read		Write, Read		

MEAS16_DAC_LO_NOISE

For details, see the MEAS1_DAC_LO_NOISE.

MEAS16_FILT2_SEL

For details, see the MEAS1_FILT2_SEL.

MEAS16_TINT

For details, see the MEAS1_TINT.

MEAS16_AVER

For details, see the MEAS1_AVER[2:0].

MEAS16 Configuration 2 (0xBE)

BIT	7	6	5	4	3	2	1	0
Field	MEAS16_SINC3_SEL	MEAS16_FILT_SEL	–	–	MEAS16_PPG4_ADC_RGE	MEAS16_PPG3_ADC_RGE	MEAS16_PPG2_ADC_RGE	MEAS16_PPG1_ADC_RGE
Reset	0	0	–	–	0	0	0	0
Access Type	Write, Read	Write, Read	–	–	Write, Read	Write, Read	Write, Read	Write, Read

MEAS16_SINC3_SEL

For details, see the MEAS1_SINC3_SEL.

MEAS16_FILT_SEL

For details, see the MEAS1_FILT_SEL.

MEAS16_PPG4_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS16_PPG3_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS16_PPG2_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS16_PPG1_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

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MEAS16 Configuration 3 (0xBF)

BIT	7	6	5	4	3	2	1	0
Field	MEAS16_PPG2_DACOFF[3:0]				MEAS16_PPG1_DACOFF[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

MEAS16_PPG2_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS16_PPG1_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS16 Configuration 4 (0xC0)

BIT	7	6	5	4	3	2	1	0
Field	MEAS16_PPG4_DACOFF[3:0]				MEAS16_PPG3_DACOFF[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

MEAS16_PPG4_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS16_PPG3_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS16 Configuration 5 (0xC1)

BIT	7	6	5	4	3	2	1	0
Field	MEAS16_PD_SETLNG[1:0]		MEAS16_LED_SETLNG[1:0]		–	–	MEAS16_LED_RGE[1:0]	
Reset	0x1		0x1		–	–	0x3	
Access Type	Write, Read		Write, Read		–	–	Write, Read	

MEAS16_PD_SETLNG

For details, see the MEAS1_PD_SETLNG[1:0].

MEAS16_LED_SETLNG

For details, see the MEAS1_LED_SETLNG[1:0].

MEAS16_LED_RGE

For details, see the MEAS1_LED_RGE[1:0].

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MEAS16 LEDA Current (0xC2)

BIT	7	6	5	4	3	2	1	0
Field	MEAS16_DRVA_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS16_DRVA_PA

For details, see the MEAS1_DRVA_PA[7:0].

MEAS16 LEDB Current (0xC3)

BIT	7	6	5	4	3	2	1	0
Field	MEAS16_DRVB_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS16_DRVB_PA

For details, see the MEAS1_DRVA_PA[7:0].

MEAS16 PD SEL 1 (0xC4)

BIT	7	6	5	4	3	2	1	0
Field	MEAS16_PD3_SEL[2:1]		MEAS16_PD2_SEL[2:0]			MEAS16_PD1_SEL[2:0]		
Reset	0x3		0x5			0x4		
Access Type	Write, Read		Write, Read			Write, Read		

MEAS16_PD3_SEL

For details, see the MEAS1_PD3_SEL[2:1] and the MEAS1_PD1_SEL[2:0].

MEAS16_PD2_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS16_PD1_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS16 PD SEL 2 (0xC5)

BIT	7	6	5	4	3	2	1	0
Field	MEAS16_PD6_SEL[2]	MEAS16_PD5_SEL[2:0]			MEAS16_PD4_SEL[2:0]			MEAS16_PD3_SEL[0]
Reset	0	0x0			0x7			0
Access Type	Write, Read	Write, Read			Write, Read			Write, Read

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MEAS16_PD6_SEL

For details, see the MEAS1_PD6_SEL[2] and the MEAS1_PD1_SEL[2:0].

MEAS16_PD5_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS16_PD4_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS16_PD3_SEL

For details, see the MEAS1_PD3_SEL[0] and the MEAS1_PD1_SEL[2:0].

MEAS16 PD SEL 3 (0xC6)

BIT	7	6	5	4	3	2	1	0
Field	MEAS16_PD8_SEL[2:0]			MEAS16_PD7_SEL[2:0]			MEAS16_PD6_SEL[1:0]	
Reset	0x0			0x0			0x0	
Access Type	Write, Read			Write, Read			Write, Read	

MEAS16_PD8_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS16_PD7_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS16_PD6_SEL

For details, see the MEAS1_PD6_SEL[1:0] and the MEAS1_PD1_SEL[2:0].

MEAS17 Selects (0xC7)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS17_AMB	MEAS17_DRVB[2:0]			MEAS17_DRVA[2:0]		
Reset	–	0	0x0			0x0		
Access Type	–	Write, Read	Write, Read			Write, Read		

MEAS17_AMB

For details, see the MEAS1_AMB.

MEAS17_DRVB

For details, see the MEAS1_DRVB[2:0].

MEAS17_DRVA

For details, see the MEAS1_DRVA[2:0].

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MEAS17 Configuration 1 (0xC8)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS17_DAC_LO_NOISE	MEAS17_FILT2_SEL	MEAS17_TINT[1:0]		MEAS17_AVER[2:0]		
Reset	–	0	1	0x3		0x0		
Access Type	–	Write, Read	Write, Read	Write, Read		Write, Read		

MEAS17_DAC_LO_NOISE

For details, see the MEAS1_DAC_LO_NOISE.

MEAS17_FILT2_SEL

For details, see the MEAS1_FILT2_SEL.

MEAS17_TINT

For details, see the MEAS1_TINT.

MEAS17_AVER

For details, see the MEAS1_AVER[2:0].

MEAS17 Configuration 2 (0xC9)

BIT	7	6	5	4	3	2	1	0
Field	MEAS17_SINC3_SEL	MEAS17_FILT_SEL	–	–	MEAS17_PPG4_ADC_RGE	MEAS17_PPG3_ADC_RGE	MEAS17_PPG2_ADC_RGE	MEAS17_PPG1_ADC_RGE
Reset	0	0	–	–	0	0	0	0
Access Type	Write, Read	Write, Read	–	–	Write, Read	Write, Read	Write, Read	Write, Read

MEAS17_SINC3_SEL

For details, see the MEAS1_SINC3_SEL.

MEAS17_FILT_SEL

For details, see the MEAS1_FILT_SEL.

MEAS17_PPG4_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS17_PPG3_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS17_PPG2_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS17_PPG1_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

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MEAS17 Configuration 3 (0xCA)

BIT	7	6	5	4	3	2	1	0
Field	MEAS17_PPG2_DACOFF[3:0]				MEAS17_PPG1_DACOFF[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

MEAS17_PPG2_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS17_PPG1_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS17 Configuration 4 (0xCB)

BIT	7	6	5	4	3	2	1	0
Field	MEAS17_PPG4_DACOFF[3:0]				MEAS17_PPG3_DACOFF[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

MEAS17_PPG4_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS17_PPG3_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS17 Configuration 5 (0xCC)

BIT	7	6	5	4	3	2	1	0
Field	MEAS17_PD_SETLNG[1:0]		MEAS17_LED_SETLNG[1:0]		–	–	MEAS17_LED_RGE[1:0]	
Reset	0x1		0x1		–	–	0x3	
Access Type	Write, Read		Write, Read		–	–	Write, Read	

MEAS17_PD_SETLNG

For details, see the MEAS1_PD_SETLNG[1:0].

MEAS17_LED_SETLNG

For details, see the MEAS1_LED_SETLNG[1:0].

MEAS17_LED_RGE

For details, see the MEAS1_LED_RGE[1:0].

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MEAS17 LEDA Current (0xCD)

BIT	7	6	5	4	3	2	1	0
Field	MEAS17_DRVA_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS17_DRVA_PA

For details, see the MEAS1_DRVA_PA[7:0].

MEAS17 LEDB Current (0xCE)

BIT	7	6	5	4	3	2	1	0
Field	MEAS17_DRVB_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS17_DRVB_PA

For details, see the MEAS1_DRVA_PA[7:0].

MEAS17 PD SEL 1 (0xCF)

BIT	7	6	5	4	3	2	1	0
Field	MEAS17_PD3_SEL[2:1]		MEAS17_PD2_SEL[2:0]			MEAS17_PD1_SEL[2:0]		
Reset	0x3		0x5			0x4		
Access Type	Write, Read		Write, Read			Write, Read		

MEAS17_PD3_SEL

For details, see the MEAS1_PD3_SEL[2:1] and the MEAS1_PD1_SEL[2:0].

MEAS17_PD2_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS17_PD1_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS17 PD SEL 2 (0xD0)

BIT	7	6	5	4	3	2	1	0
Field	MEAS17_PD6_SEL[2]	MEAS17_PD5_SEL[2:0]			MEAS17_PD4_SEL[2:0]			MEAS17_PD3_SEL[0]
Reset	0	0x0			0x7			0
Access Type	Write, Read	Write, Read			Write, Read			Write, Read

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MEAS17_PD6_SEL

For details, see the MEAS1_PD6_SEL[2] and the MEAS1_PD1_SEL[2:0].

MEAS17_PD5_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS17_PD4_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS17_PD3_SEL

For details, see the MEAS1_PD3_SEL[0] and the MEAS1_PD1_SEL[2:0].

MEAS17 PD SEL 3 (0xD1)

BIT	7	6	5	4	3	2	1	0
Field	MEAS17_PD8_SEL[2:0]			MEAS17_PD7_SEL[2:0]			MEAS17_PD6_SEL[1:0]	
Reset	0x0			0x0			0x0	
Access Type	Write, Read			Write, Read			Write, Read	

MEAS17_PD8_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS17_PD7_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS17_PD6_SEL

For details, see the MEAS1_PD6_SEL[1:0] and the MEAS1_PD1_SEL[2:0].

MEAS18 Selects (0xD2)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS18_AMB	MEAS18_DRVB[2:0]			MEAS18_DRVA[2:0]		
Reset	–	0	0x0			0x0		
Access Type	–	Write, Read	Write, Read			Write, Read		

MEAS18_AMB

For details, see the MEAS1_AMB.

MEAS18_DRVB

For details, see the MEAS1_DRVB[2:0].

MEAS18_DRVA

For details, see the MEAS1_DRVA[2:0].

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MEAS18 Configuration 1 (0xD3)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS18_DAC_LO_NOISE	MEAS18_FILT2_SEL	MEAS18_TINT[1:0]		MEAS18_AVER[2:0]		
Reset	–	0	1	0x3		0x0		
Access Type	–	Write, Read	Write, Read	Write, Read		Write, Read		

MEAS18_DAC_LO_NOISE

For details, see the MEAS1_DAC_LO_NOISE.

MEAS18_FILT2_SEL

For details, see the MEAS1_FILT2_SEL.

MEAS18_TINT

For details, see the MEAS1_TINT.

MEAS18_AVER

For details, see the MEAS1_AVER[2:0].

MEAS18 Configuration 2 (0xD4)

BIT	7	6	5	4	3	2	1	0
Field	MEAS18_SINC3_SEL	MEAS18_FILT_SEL	–	–	MEAS18_PPG4_ADC_RGE	MEAS18_PPG3_ADC_RGE	MEAS18_PPG2_ADC_RGE	MEAS18_PPG1_ADC_RGE
Reset	0	0	–	–	0	0	0	0
Access Type	Write, Read	Write, Read	–	–	Write, Read	Write, Read	Write, Read	Write, Read

MEAS18_SINC3_SEL

For details, see the MEAS1_SINC3_SEL.

MEAS18_FILT_SEL

For details, see the MEAS1_FILT_SEL.

MEAS18_PPG4_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS18_PPG3_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS18_PPG2_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS18_PPG1_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

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MEAS18 Configuration 3 (0xD5)

BIT	7	6	5	4	3	2	1	0
Field	MEAS18_PPG2_DACOFF[3:0]				MEAS18_PPG1_DACOFF[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

MEAS18_PPG2_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS18_PPG1_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS18 Configuration 4 (0xD6)

BIT	7	6	5	4	3	2	1	0
Field	MEAS18_PPG4_DACOFF[3:0]				MEAS18_PPG3_DACOFF[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

MEAS18_PPG4_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS18_PPG3_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS18 Configuration 5 (0xD7)

BIT	7	6	5	4	3	2	1	0
Field	MEAS18_PD_SETLNG[1:0]		MEAS18_LED_SETLNG[1:0]		–	–	MEAS18_LED_RGE[1:0]	
Reset	0x1		0x1		–	–	0x3	
Access Type	Write, Read		Write, Read		–	–	Write, Read	

MEAS18_PD_SETLNG

For details, see the MEAS1_PD_SETLNG[1:0].

MEAS18_LED_SETLNG

For details, see the MEAS1_LED_SETLNG[1:0].

MEAS18_LED_RGE

For details, see the MEAS1_LED_RGE[1:0].

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MEAS18 LEDA Current (0xD8)

BIT	7	6	5	4	3	2	1	0
Field	MEAS18_DRVA_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS18_DRVA_PA

For details, see the MEAS1_DRVA_PA[7:0].

MEAS18 LEDB Current (0xD9)

BIT	7	6	5	4	3	2	1	0
Field	MEAS18_DRVB_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS18_DRVB_PA

For details, see the MEAS1_DRVA_PA[7:0].

MEAS18 PD SEL 1 (0xDA)

BIT	7	6	5	4	3	2	1	0
Field	MEAS18_PD3_SEL[2:1]		MEAS18_PD2_SEL[2:0]			MEAS18_PD1_SEL[2:0]		
Reset	0x3		0x5			0x4		
Access Type	Write, Read		Write, Read			Write, Read		

MEAS18_PD3_SEL

For details, see the MEAS1_PD3_SEL[2:1] and the MEAS1_PD1_SEL[2:0].

MEAS18_PD2_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS18_PD1_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS18 PD SEL 2 (0xDB)

BIT	7	6	5	4	3	2	1	0
Field	MEAS18_PD6_SEL[2]	MEAS18_PD5_SEL[2:0]			MEAS18_PD4_SEL[2:0]			MEAS18_PD3_SEL[0]
Reset	0	0x0			0x7			0
Access Type	Write, Read	Write, Read			Write, Read			Write, Read

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MEAS18_PD6_SEL

For details, see the MEAS1_PD6_SEL[2] and the MEAS1_PD1_SEL[2:0].

MEAS18_PD5_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS18_PD4_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS18_PD3_SEL

For details, see the MEAS1_PD3_SEL[0] and the MEAS1_PD1_SEL[2:0].

MEAS18 PD SEL 3 (0xDC)

BIT	7	6	5	4	3	2	1	0
Field	MEAS18_PD8_SEL[2:0]			MEAS18_PD7_SEL[2:0]			MEAS18_PD6_SEL[1:0]	
Reset	0x0			0x0			0x0	
Access Type	Write, Read			Write, Read			Write, Read	

MEAS18_PD8_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS18_PD7_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS18_PD6_SEL

For details, see the MEAS1_PD6_SEL[1:0] and the MEAS1_PD1_SEL[2:0].

MEAS19 Selects (0xDD)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS19_AMB	MEAS19_DRVB[2:0]			MEAS19_DRVA[2:0]		
Reset	–	0	0x0			0x0		
Access Type	–	Write, Read	Write, Read			Write, Read		

MEAS19_AMB

For details, see the MEAS1_AMB.

MEAS19_DRVB

For details, see the MEAS1_DRVB[2:0].

MEAS19_DRVA

For details, see the MEAS1_DRVA[2:0].

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MEAS19 Configuration 1 (0xDE)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS19_DAC_LO_NOISE	MEAS19_FILT2_SEL	MEAS19_TINT[1:0]		MEAS19_AVER[2:0]		
Reset	–	0	1	0x3		0x0		
Access Type	–	Write, Read	Write, Read	Write, Read		Write, Read		

MEAS19_DAC_LO_NOISE

For details, see the MEAS1_DAC_LO_NOISE.

MEAS19_FILT2_SEL

For details, see the MEAS1_FILT2_SEL.

MEAS19_TINT

For details, see the MEAS1_TINT.

MEAS19_AVER

For details, see the MEAS1_AVER[2:0].

MEAS19 Configuration 2 (0xDF)

BIT	7	6	5	4	3	2	1	0
Field	MEAS19_SINC3_SEL	MEAS19_FILT_SEL	–	–	MEAS19_PPG4_ADC_RGE	MEAS19_PPG3_ADC_RGE	MEAS19_PPG2_ADC_RGE	MEAS19_PPG1_ADC_RGE
Reset	0	0	–	–	0	0	0	0
Access Type	Write, Read	Write, Read	–	–	Write, Read	Write, Read	Write, Read	Write, Read

MEAS19_SINC3_SEL

For details, see the MEAS1_SINC3_SEL.

MEAS19_FILT_SEL

For details, see the MEAS1_FILT_SEL.

MEAS19_PPG4_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS19_PPG3_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS19_PPG2_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS19_PPG1_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

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MEAS19 Configuration 3 (0xE0)

BIT	7	6	5	4	3	2	1	0
Field	MEAS19_PPG2_DACOFF[3:0]				MEAS19_PPG1_DACOFF[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

MEAS19_PPG2_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS19_PPG1_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS19 Configuration 4 (0xE1)

BIT	7	6	5	4	3	2	1	0
Field	MEAS19_PPG4_DACOFF[3:0]				MEAS19_PPG3_DACOFF[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

MEAS19_PPG4_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS19_PPG3_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS19 Configuration 5 (0xE2)

BIT	7	6	5	4	3	2	1	0
Field	MEAS19_PD_SETLNG[1:0]		MEAS19_LED_SETLNG[1:0]		–	–	MEAS19_LED_RGE[1:0]	
Reset	0x1		0x1		–	–	0x3	
Access Type	Write, Read		Write, Read		–	–	Write, Read	

MEAS19_PD_SETLNG

For details, see the MEAS1_PD_SETLNG[1:0].

MEAS19_LED_SETLNG

For details, see the MEAS1_LED_SETLNG[1:0].

MEAS19_LED_RGE

For details, see the MEAS1_LED_RGE[1:0].

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MEAS19 LEDA Current (0xE3)

BIT	7	6	5	4	3	2	1	0
Field	MEAS19_DRVA_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS19_DRVA_PA

For details, see the MEAS1_DRVA_PA[7:0].

MEAS19 LEDB Current (0xE4)

BIT	7	6	5	4	3	2	1	0
Field	MEAS19_DRVB_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS19_DRVB_PA

For details, see the MEAS1_DRVA_PA[7:0].

MEAS19 PD SEL 1 (0xE5)

BIT	7	6	5	4	3	2	1	0
Field	MEAS19_PD3_SEL[2:1]		MEAS19_PD2_SEL[2:0]			MEAS19_PD1_SEL[2:0]		
Reset	0x3		0x5			0x4		
Access Type	Write, Read		Write, Read			Write, Read		

MEAS19_PD3_SEL

For details, see the MEAS1_PD3_SEL[2:1] and the MEAS1_PD1_SEL[2:0].

MEAS19_PD2_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS19_PD1_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS19 PD SEL 2 (0xE6)

BIT	7	6	5	4	3	2	1	0
Field	MEAS19_PD6_SEL[2]	MEAS19_PD5_SEL[2:0]			MEAS19_PD4_SEL[2:0]			MEAS19_PD3_SEL[0]
Reset	0	0x0			0x7			0
Access Type	Write, Read	Write, Read			Write, Read			Write, Read

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MEAS19_PD6_SEL

For details, see the MEAS1_PD6_SEL[2] and the MEAS1_PD1_SEL[2:0].

MEAS19_PD5_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS19_PD4_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS19_PD3_SEL

For details, see the MEAS1_PD3_SEL[0] and the MEAS1_PD1_SEL[2:0].

MEAS19 PD SEL 3 (0xE7)

BIT	7	6	5	4	3	2	1	0
Field	MEAS19_PD8_SEL[2:0]			MEAS19_PD7_SEL[2:0]			MEAS19_PD6_SEL[1:0]	
Reset	0x0			0x0			0x0	
Access Type	Write, Read			Write, Read			Write, Read	

MEAS19_PD8_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS19_PD7_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS19_PD6_SEL

For details, see the MEAS1_PD6_SEL[1:0] and the MEAS1_PD1_SEL[2:0].

MEAS20 Selects (0xE8)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS20_AMB	MEAS20_DRVB[2:0]			MEAS20_DRVA[2:0]		
Reset	–	0	0x0			0x0		
Access Type	–	Write, Read	Write, Read			Write, Read		

MEAS20_AMB

For details, see the MEAS1_AMB.

MEAS20_DRVB

For details, see the MEAS1_DRVB[2:0].

MEAS20_DRVA

For details, see the MEAS1_DRVA[2:0].

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MEAS20 Configuration 1 (0xE9)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS20_DAC_LO_NOISE	MEAS20_FILT2_SEL	MEAS20_TINT[1:0]		MEAS20_AVER[2:0]		
Reset	–	0	1	0x3		0x0		
Access Type	–	Write, Read	Write, Read	Write, Read		Write, Read		

MEAS20_DAC_LO_NOISE

For details, see the MEAS1_DAC_LO_NOISE.

MEAS20_FILT2_SEL

For details, see the MEAS1_FILT2_SEL.

MEAS20_TINT

For details, see the MEAS1_TINT[1:0].

MEAS20_AVER

For details, see the MEAS1_AVER[2:0].

MEAS20 Configuration 2 (0xEA)

BIT	7	6	5	4	3	2	1	0
Field	MEAS20_SINC3_SEL	MEAS20_FILT_SEL	–	–	MEAS20_PPG4_ADC_RGE	MEAS20_PPG3_ADC_RGE	MEAS20_PPG2_ADC_RGE	MEAS20_PPG1_ADC_RGE
Reset	0	0	–	–	0	0	0	0
Access Type	Write, Read	Write, Read	–	–	Write, Read	Write, Read	Write, Read	Write, Read

MEAS20_SINC3_SEL

For details, see the MEAS1_SINC3_SEL.

MEAS20_FILT_SEL

For details, see the MEAS1_FILT_SEL.

MEAS20_PPG4_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS20_PPG3_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS20_PPG2_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

MEAS20_PPG1_ADC_RGE

For details, see the MEAS1_PPG4_ADC_RGE.

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MEAS20 Configuration 3 (0xEB)

BIT	7	6	5	4	3	2	1	0
Field	MEAS20_PPG2_DACOFF[3:0]				MEAS20_PPG1_DACOFF[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

MEAS20_PPG2_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS20_PPG1_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS20 Configuration 4 (0xEC)

BIT	7	6	5	4	3	2	1	0
Field	MEAS20_PPG4_DACOFF[3:0]				MEAS20_PPG3_DACOFF[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

MEAS20_PPG4_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS20_PPG3_DACOFF

For details, see the MEAS1_PPG2_DACOFF[3:0].

MEAS20 Configuration 5 (0xED)

BIT	7	6	5	4	3	2	1	0
Field	MEAS20_PD_SETLNG[1:0]		MEAS20_LED_SETLNG[1:0]		–	–	MEAS20_LED_RGE[1:0]	
Reset	0x1		0x1		–	–	0x3	
Access Type	Write, Read		Write, Read		–	–	Write, Read	

MEAS20_PD_SETLNG

For details, see the MEAS1_PD_SETLNG[1:0].

MEAS20_LED_SETLNG

For details, see the MEAS1_LED_SETLNG[1:0].

MEAS20_LED_RGE

For details, see the MEAS1_LED_RGE[1:0].

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MEAS20 LEDA Current (0xEE)

BIT	7	6	5	4	3	2	1	0
Field	MEAS20_DRVA_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS20_DRVA_PA

For details, see the MEAS1_DRVA_PA[7:0].

MEAS20 LEDB Current (0xEF)

BIT	7	6	5	4	3	2	1	0
Field	MEAS20_DRVB_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS20_DRVB_PA

For details, see the MEAS1_DRVA_PA[7:0].

MEAS20 PD SEL 1 (0xF0)

BIT	7	6	5	4	3	2	1	0
Field	MEAS20_PD3_SEL[2:1]		MEAS20_PD2_SEL[2:0]			MEAS20_PD1_SEL[2:0]		
Reset	0x3		0x5			0x4		
Access Type	Write, Read		Write, Read			Write, Read		

MEAS20_PD3_SEL

For details, see the MEAS1_PD3_SEL[2:1] and the MEAS1_PD1_SEL[2:0].

MEAS20_PD2_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS20_PD1_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS20 PD SEL 2 (0xF1)

BIT	7	6	5	4	3	2	1	0
Field	MEAS20_PD6_SEL[2]	MEAS20_PD5_SEL[2:0]			MEAS20_PD4_SEL[2:0]			MEAS20_PD3_SEL[0]
Reset	0	0x0			0x7			0
Access Type	Write, Read	Write, Read			Write, Read			Write, Read

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MEAS20_PD6_SEL

For details, see the MEAS1_PD6_SEL[2] and the MEAS1_PD1_SEL[2:0].

MEAS20_PD5_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS20_PD4_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS20_PD3_SEL

For details, see the MEAS1_PD3_SEL[0] and the MEAS1_PD1_SEL[2:0].

MEAS20 PD SEL 3 (0xF2)

BIT	7	6	5	4	3	2	1	0
Field	MEAS20_PD8_SEL[2:0]			MEAS20_PD7_SEL[2:0]			MEAS20_PD6_SEL[1:0]	
Reset	0x0			0x0			0x0	
Access Type	Write, Read			Write, Read			Write, Read	

MEAS20_PD8_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS20_PD7_SEL

For details, see the MEAS1_PD1_SEL[2:0].

MEAS20_PD6_SEL

For details, see the MEAS1_PD6_SEL[1:0] and the MEAS1_PD1_SEL[2:0].

THRESHOLD1 MEAS SEL (0xF3)

BIT	7	6	5	4	3	2	1	0
Field	THRESH1_PPG_SEL[1:0]		–	THRESH1_MEAS_SEL[4:0]				
Reset	0x0		–	0x00				
Access Type	Write, Read		–	Write, Read				

THRESH1_PPG_SEL

THRESH1_PPG_SEL[1:0] sets which optical channel the threshold 1 is applied. If THRESH1_PPG_SEL[1:0] is set to 00, then THRESH1_UPPER and THRESH1_LOWER are applied to optical channel 1. If THRESH1_PPG_SEL[1:0] is set to 01, then THRESH1_UPPER and THRESH1_LOWER are applied to optical channel 2, and so on.

THRESH1_PPG_SEL[1:0]	CHANNEL THAT THRESHOLD1 IS APPLIED
0x0	Optical Channel 1
0x1	Optical Channel 2
0x2	Optical Channel 3
0x3	Optical Channel 4

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THRESH1_MEAS_SEL

THRESH1_MEAS_SEL[4:0] selects which of the MEASx (x = 1 to 20) is used for THRESH1_HILO detect.

For more details, see the Threshold Detect Function section in the Detailed Description.

THRESH1_MEAS_SEL[4:0]	DECODE
0x0	THRESH1_HILO detect is disabled.
0x1	MEAS1 selected.
0x2	MEAS2 selected.
0x3	MEAS3 selected.
0x4	MEAS4 selected.
0x5	MEAS5 selected.
0x6	MEAS6 selected.
0x7	MEAS7 selected.
0x8	MEAS8 selected.
0x9	MEAS9 selected.
0xA	MEAS10 selected.
0xB	MEAS11 selected.
0xC	MEAS12 selected.
0xD	MEAS13 selected.
0xE	MEAS14 selected.
0xF	MEAS15 selected.
0x10	MEAS16 selected.
0x11	MEAS17 selected.
0x12	MEAS18 selected.
0x13	MEAS19 selected.
0x14	MEAS20 selected.
0x15 to 0x1F	THRESH1_HILO detect is disabled.

THRESHOLD2 MEAS SEL (0xF4)

BIT	7	6	5	4	3	2	1	0
Field	THRESH2_PPG_SEL[1:0]		–	THRESH2_MEAS_SEL[4:0]				
Reset	0x0		–	0x00				
Access Type	Write, Read		–	Write, Read				

THRESH2_PPG_SEL

THRESH2_PPG_SEL[1:0] sets which optical channel the threshold 2 is applied. If THRESH2_PPG_SEL[1:0] is set to 00, then THRESH2_UPPER and THRESH2_LOWER are applied to optical channel 1. If THRESH2_PPG_SEL[1:0] is set to 01, then THRESH2_UPPER and THRESH2_LOWER are applied to optical channel 2, and so on.

THRESH2_PPG_SEL[1:0]	CHANNEL THAT THRESHOLD2 IS APPLIED
0x0	Optical Channel 1
0x1	Optical Channel 2
0x2	Optical Channel 3
0x3	Optical Channel 4

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THRESH2_MEAS_SEL

THRESH2_MEAS_SEL[4:0] selects which of the MEASx (x = 1 to 20) is used for THRESH2_HILO detect.

For more details, see the Threshold Detect Function section in the Detailed Description.

THRESH2_MEAS_SEL[4:0]	DECODE
0x0	THRESH1_HILO detect is disabled.
0x1	MEAS1 selected.
0x2	MEAS2 selected.
0x3	MEAS3 selected.
0x4	MEAS4 selected.
0x5	MEAS5 selected.
0x6	MEAS6 selected.
0x7	MEAS7 selected.
0x8	MEAS8 selected.
0x9	MEAS9 selected.
0xA	MEAS10 selected.
0xB	MEAS11 selected.
0xC	MEAS12 selected.
0xD	MEAS13 selected.
0xE	MEAS14 selected.
0xF	MEAS15 selected.
0x10	MEAS16 selected.
0x11	MEAS17 selected.
0x12	MEAS18 selected.
0x13	MEAS19 selected.
0x14	MEAS20 selected.
0x15 to 0x1F	THRESH1_HILO detect is disabled.

THRESHOLD HYST (0xF5)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	TIME_HYST[1:0]		LEVEL_HYST[2:0]		
Reset	–	–	–	0x0		0x0		
Access Type	–	–	–	Write, Read		Write, Read		

TIME_HYST

Time hysteresis sets the number of samples that the ambient light corrected exposure signal is above the THRESHOLDx_UPPER or is below THRESHOLDx_LOWER before the threshold interrupt is set. This value is in ADC counts and is applied at ±½*LEVEL_HYST around the THRESHOLDx_UPPER and THRESHOLDx_LOWER. Specifically, in order for an interrupt to be generated from the threshold function, an ambient light corrected exposure must transition above the THRESHOLDx_UPPER + ½ x LEVEL_HYST and stay above THRESHOLDx_UPPER - ½ x LEVEL_HYST for TIME_HYST samples or transition below THRESHOLDx_LOWER - ½ x LEVEL_HYST and stay below THRESHOLDx_LOWER + ½ x LEVEL_HYST for TIME_HYST samples. TIME_HYST parameter applies to both instances of threshold interrupts.

TIME_HYST	NUMBER OF SAMPLES BEFORE INTERRUPT IS SET

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0x0	0, Time Hysteresis Disabled
0x1	2 Samples
0x2	4 Samples
0x3	8 Samples

NOTE: When using External Frame Trigger Input mode for synchronization, the Time Hysteresis field must be set to Zero.

When SYNC_MODE[7:6](0x0D) = 0x1, write TIME_HYST[4:3](0xF5) = 0b00.

LEVEL_HYST

Level hysteresis sets the amount of ambient light corrected exposure hysteresis to apply to both instances of the threshold function. This value is in ADC counts and is applied at ±½ x LEVEL_HYST around the THRESHOLDx_UPPER and THRESHOLDx_LOWER. Specifically, in order for an interrupt to be generated from the threshold function, an ambient light corrected exposure must transition above the THRESHOLDx_UPPER + ½ x LEVEL_HYST and stay above THRESHOLDx_UPPER - ½ x LEVEL_HYST for TIME_HYST samples or transition below THRESHOLDx_LOWER - ½ x LEVEL_HYST and stay below THRESHOLDx_LOWER + ½ x LEVEL_HYST for TIME_HYST samples. LEVEL_HYST parameter applies to both instances of threshold interrupts.

Level_HYST[2:0]	MAGNITUDE OF HYSTERISIS (LSBs)
0x0	0, Disable Level Hysteresis
0x1	2
0x2	4
0x3	8
0x4	16
0x5	32
0x6	64
0x7	128

PPG HI THRESHOLD1 (0xF6)

BIT	7	6	5	4	3	2	1	0
Field	THRESHOLD1_UPPER[7:0]							
Reset	0xFF							
Access Type	Write, Read							

THRESHOLD1_UPPER

Upper threshold for instance 1. Each LSB of the threshold represents 2048 LSBs of the ambient light corrected exposure code.

It is important to program the THRESHOLD1_UPPER to be greater than the THRESHOLD1_LOWER. Otherwise, the interrupt behavior is undefined.

THRESHOLD1_UPPER[7:0]	AMBIENT LIGHT CORRECTED EXPOSURE SIGNAL
0x00	0, upper threshold is disabled
0x01	2048
0x02	4096
0x03	6144
•	•
•	•

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THRESHOLD1_UPPER[7:0]	AMBIENT LIGHT CORRECTED EXPOSURE SIGNAL
•	•
0xFD	518144
0xFE	520192
0xFF	522240

PPG LO THRESHOLD1 (0xF7)

BIT	7	6	5	4	3	2	1	0
Field	THRESHOLD1_LOWER[7:0]							
Reset	0x00							
Access Type	Write, Read							

THRESHOLD1_LOWER

Lower threshold for instance 1. Each LSB of the threshold represents 2048 LSBs of the ambient light corrected exposure code.

It is important to program the THRESHOLD1_UPPER to be greater than the THRESHOLD1_LOWER. Otherwise, the interrupt behavior is undefined.

THRESHOLD1_LOWER	AMBIENT LIGHT CORRECTED EXPOSURE SIGNAL
0x00	0, lower threshold is disabled
0x01	2048
0x02	4096
0x03	6144
•	•
•	•
•	•
0xFD	518144
0xFE	520192
0xFF	522240

PPG HI THRESHOLD2 (0xF8)

BIT	7	6	5	4	3	2	1	0
Field	THRESHOLD2_UPPER[7:0]							
Reset	0xFF							
Access Type	Write, Read							

THRESHOLD2_UPPER

Upper threshold for instance 2. Each LSB of the threshold represents 2048 LSBs of the ambient light corrected exposure code.

It is important to program the THRESHOLD2_UPPER to be greater than the THRESHOLD2_LOWER. Otherwise, the interrupt behavior is undefined.

For the values, see the THRESHOLD1_UPPER[7:0] (register address 0xF6) table.

THRESHOLD2_UPPER	AMBIENT LIGHT CORRECTED EXPOSURE SIGNAL

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0x00	0, upper threshold is disabled
0x01	2048
0x02	4096
0x03	6144
•	•
•	•
•	•
0xFD	518144
0xFE	520192
0xFF	522240

PPG LO THRESHOLD2 (0xF9)

BIT	7	6	5	4	3	2	1	0
Field	THRESHOLD2_LOWER[7:0]							
Reset	0x00							
Access Type	Write, Read							

THRESHOLD2_LOWER

Lower threshold for instance 2. Each LSB of the threshold represents 2048 LSBs of the ambient light corrected exposure code.

It is important to program the THRESHOLD2_UPPER to be greater than the THRESHOLD2_LOWER. Otherwise, the interrupt behavior is undefined.

For the values, see the THRESHOLD1_LOWER[7:0] (register address 0xF7) table.

THRESHOLD2_LOWER	AMBIENT LIGHT CORRECTED EXPOSURE SIGNAL
0x00	0, lower threshold is disabled
0x01	2048
0x02	4096
0x03	6144
•	•
•	•
•	•
0xFD	518144
0xFE	520192
0xFF	522240

Interrupt1 Enable 1 (0xFA)

BIT	7	6	5	4	3	2	1	0
Field	A_FULL_EN1	FRAME_RDY_EN1	FIFO_DATA_RDY_EN1	ALC_OVF_EN1	EXP_OVF_EN1	THRESH2_HILO_EN1	THRESH1_HILO_EN1	LED_TX_EN1
Reset	0	0	0	0	0	0	0	0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

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A_FULL_EN1

Enables the A_FULL status bit to be output to the INT1 output pin.

FRAME_RDY_EN1

Enables the FRAME_RDY status bit to be output to the INT1 output pin.

FIFO_DATA_RDY_EN1

Enables the FIFO_DATA_RDY status bit to be output to the INT1 output pin.

ALC_OVF_EN1

Enables the ALC_OVF status bit to be output to the INT1 output pin.

EXP_OVF_EN1

Enables the EXP_OVF status bit to be output to the INT1 output pin.

THRESH2_HILO_EN1

Enables the THRESH2_HILO status bit to be output to the INT1 output pin.

THRESH1_HILO_EN1

Enables the THRESH1_HILO status bit to be output to the INT1 output pin.

LED_TX_EN1

Enables the LED_TX_EN to be output to the INT1 output pin. LED_TX_EN is asserted 500ns before any of the 6 LED Driver pins, LEDn_DRV (n = 1 to 6) gets asserted. This feature can be used in combination with the MAX20345 boost converter to switch it from a fully "off" state to a fully "on" state, thus reducing the boost quiescent power and the effects of boost ripple on the MAX86177.

The application should not set any of the other bits in the Interrupt 1 Enable Registers when the LED_TX_EN1 is set to 1.

Interrupt1 Enable 2 (0xFB)

BIT	7	6	5	4	3	2	1	0
Field	INVALID_CFG_EN1	–	LED6_COMPB_EN1	LED5_COMPB_EN1	LED4_COMPB_EN1	LED3_COMPB_EN1	LED2_COMPB_EN1	LED1_COMPB_EN1
Reset	0	–	0	0	0	0	0	0
Access Type	Write, Read	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

INVALID_CFG_EN1

Enables the INVALID_CFG status bit to be output to the INT1 output pin.

LED6_COMPB_EN1

Enables the LED6_COMPB status bit to be output to the INT1 output pin.

LED5_COMPB_EN1

Enables the LED5_COMPB status bit to be output to the INT1 output pin.

LED4_COMPB_EN1

Enables the LED4_COMPB status bit to be output to the INT1 output pin.

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LED3_COMPB_EN1

Enables the LED3_COMPB status bit to be output to the INT1 output pin.

LED2_COMPB_EN1

Enables the LED2_COMPB status bit to be output to the INT1 output pin.

LED1_COMPB_EN1

Enables the LED1_COMPB status bit to be output to the INT1 output pin.

Interrupt2 Enable 1 (0xFC)

BIT	7	6	5	4	3	2	1	0
Field	A_FULL_EN2	FRAME_RDY_EN2	FIFO_DATA_RDY_EN2	ALC_OVF_EN2	EXP_OVF_EN2	THRESH2_HILO_EN2	THRESH1_HILO_EN2	LED_TX_EN2
Reset	0	0	0	0	0	0	0	0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

A_FULL_EN2

Enables the A_FULL status bit to be output to the INT2 output pin.

FRAME_RDY_EN2

Enables the FRAME_RDY status bit to be output to the INT2 output pin.

FIFO_DATA_RDY_EN2

Enables the FIFO_DATA_RDY status bit to be output to the INT2 output pin.

ALC_OVF_EN2

Enables the ALC_OVF status bit to be output to the INT2 output pin.

EXP_OVF_EN2

Enables the EXP_OVF status bit to be output to the INT2 output pin.

THRESH2_HILO_EN2

Enables the THRESH2_HILO status bit to be output to the INT2 output pin.

THRESH1_HILO_EN2

Enables the THRESH1_HILO status bit to be output to the INT2 output pin.

LED_TX_EN2

Enables the LED_TX_EN to be output to the INT2 output pin. LED_TX_EN is asserted 500ns before any of the 6 LED Driver pins, LEDn_DRV (n = 1 to 6) gets asserted. This feature can be used in combination with the MAX20345 boost converter to switch it from a fully "off" state to a fully "on" state, thus reducing the boost quiescent power and the effects of boost ripple on the MAX86177.

The application should not set any of the other bits in the Interrupt 2 Enable Registers when the LED_TX_EN2 is set to 1.

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Interrupt2 Enable 2 (0xFD)

BIT	7	6	5	4	3	2	1	0
Field	INVALID_CFG_EN2	–	LED6_COMPB_EN2	LED5_COMPB_EN2	LED4_COMPB_EN2	LED3_COMPB_EN2	LED2_COMPB_EN2	LED1_COMPB_EN2
Reset	0	–	0	0	0	0	0	0
Access Type	Write, Read	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

INVALID_CFG_EN2

Enables the INVALID_CFG status bit to be output to the INT2 output pin.

LED6_COMPB_EN2

Enables the LED6_COMPB status bit to be output to the INT2 output pin.

LED5_COMPB_EN2

Enables the LED5_COMPB status bit to be output to the INT2 output pin.

LED4_COMPB_EN2

Enables the LED4_COMPB status bit to be output to the INT2 output pin.

LED3_COMPB_EN2

Enables the LED3_COMPB status bit to be output to the INT2 output pin.

LED2_COMPB_EN2

Enables the LED2_COMPB status bit to be output to the INT2 output pin.

LED1_COMPB_EN2

Enables the LED1_COMPB status bit to be output to the INT2 output pin.

Part ID (0xFF)

BIT	7	6	5	4	3	2	1	0
Field	PART_ID[7:0]							
Reset	0x46							
Access Type	Read Only							

PART_ID

This register stores the part identifier for the chip.

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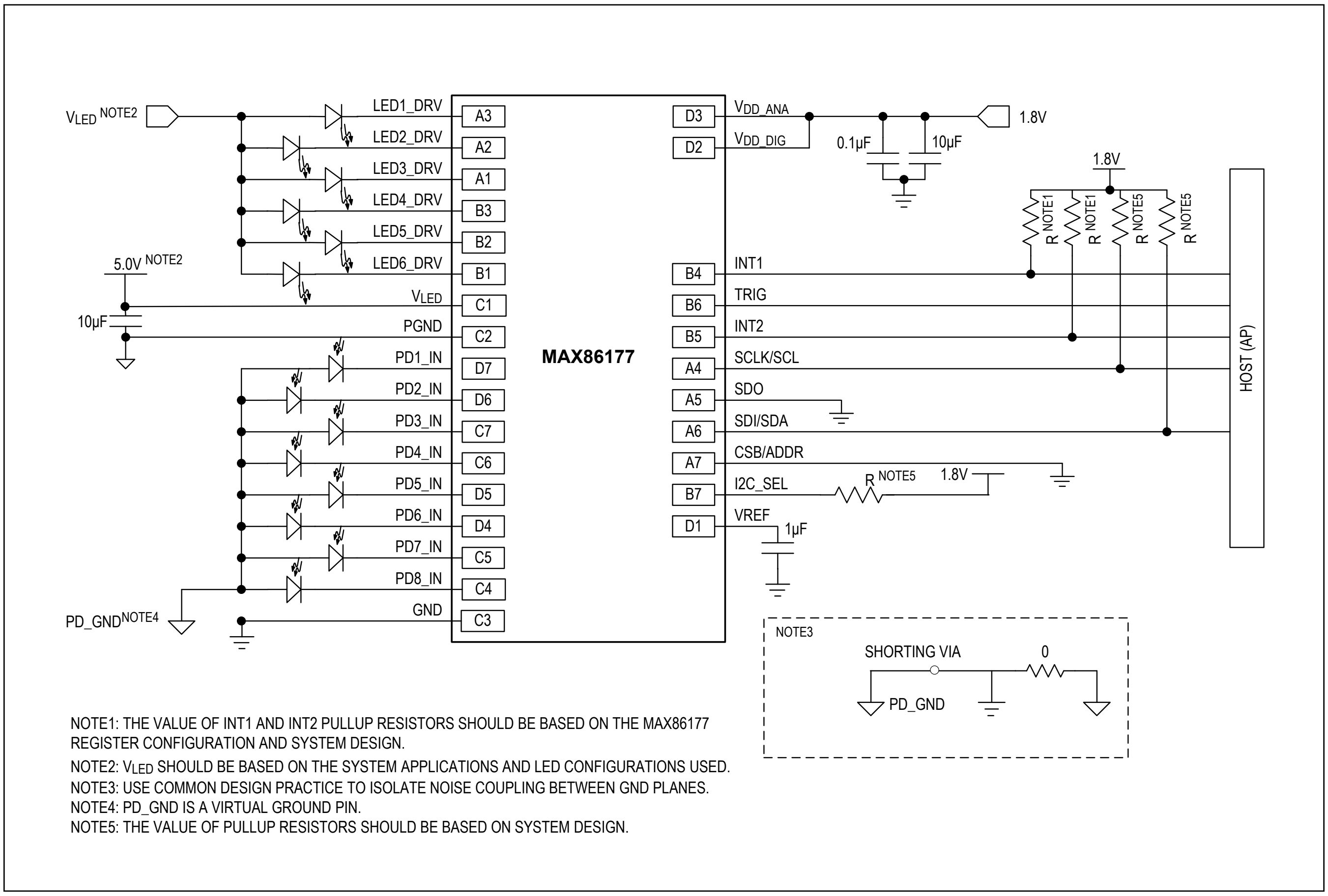
Typical Application Circuits

I2C Mode



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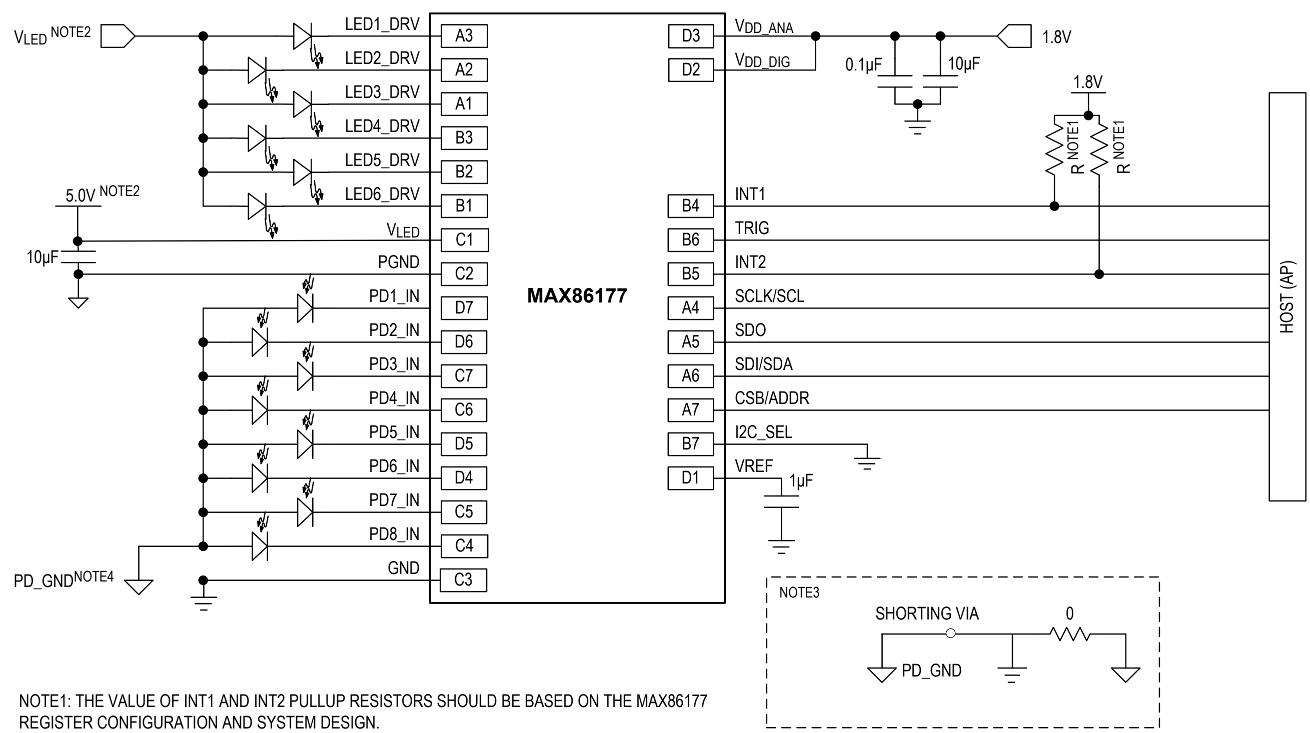
Typical Application Circuits (continued)

SPI Mode



NOTE1: THE VALUE OF INT1 AND INT2 PULLUP RESISTORS SHOULD BE BASED ON THE MAX86177 REGISTER CONFIGURATION AND SYSTEM DESIGN.
NOTE2: VLED SHOULD BE BASED ON THE SYSTEM APPLICATIONS AND LED CONFIGURATIONS USED.
NOTE3: USE COMMON DESIGN PRACTICE TO ISOLATE NOISE COUPLING BETWEEN GND PLANES.
NOTE4: PD_GND IS A VIRTUAL GROUND PIN

Ordering Information

PART NUMBER	TEMP.RANGE	BUMP
MAX86177ENI+	-40°C to +85°C	28 WLP
MAX86177ENI+T	-40°C to +85°C	28 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/21	Release for Market Intro	—
1	6/23	Updated TOC 2, Pin Description, Optical Transmitter Overview, Optical Receiver Overview, Photodiode Biasing, Measurement Configuration and Timing, Frame with One Measurement Only, Frame with All Twenty Measurements Enabled, On-Chip Averaging, Measurement Averaging, Ambient-Light Cancellation, ADC Decimation Filter, SYNC_MODE = 0x1 External Frame Trigger Input Mode, FIFO Description, FIFO Configuration Registers, Threshold Detect Function, Detailed SPI Timing, Single-Word SPI Register Read/Write Transaction, SPI FIFO Burst Mode Read Transaction, I2C-,Compatible and SMBus-Compatible Serial Interface, Target Address, START and STOP Conditions, Acknowledge Bit, I2C Write Data Format, I2C Read Data Format, PCB Layout Guidelines, and Register Map	14, 17, 19, 20–24, 26–29, 35–38, 40, 41, 43, 66–160

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