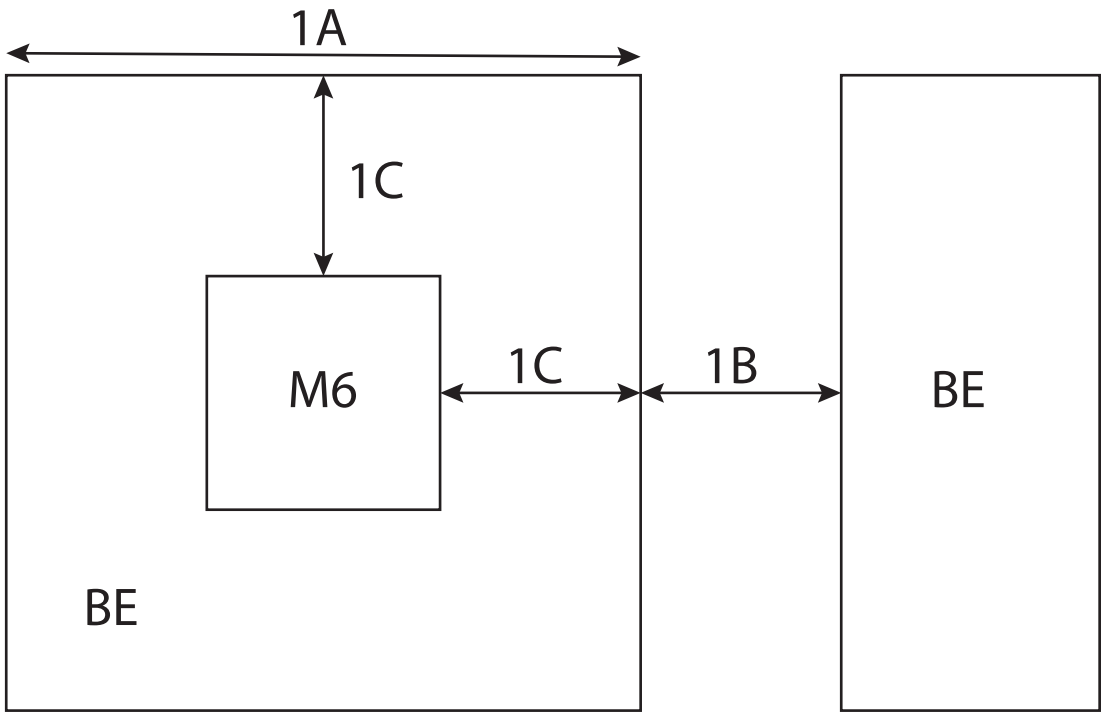
Design Rules Manual RRAM_CMOS_DK

Version 1.1

Content

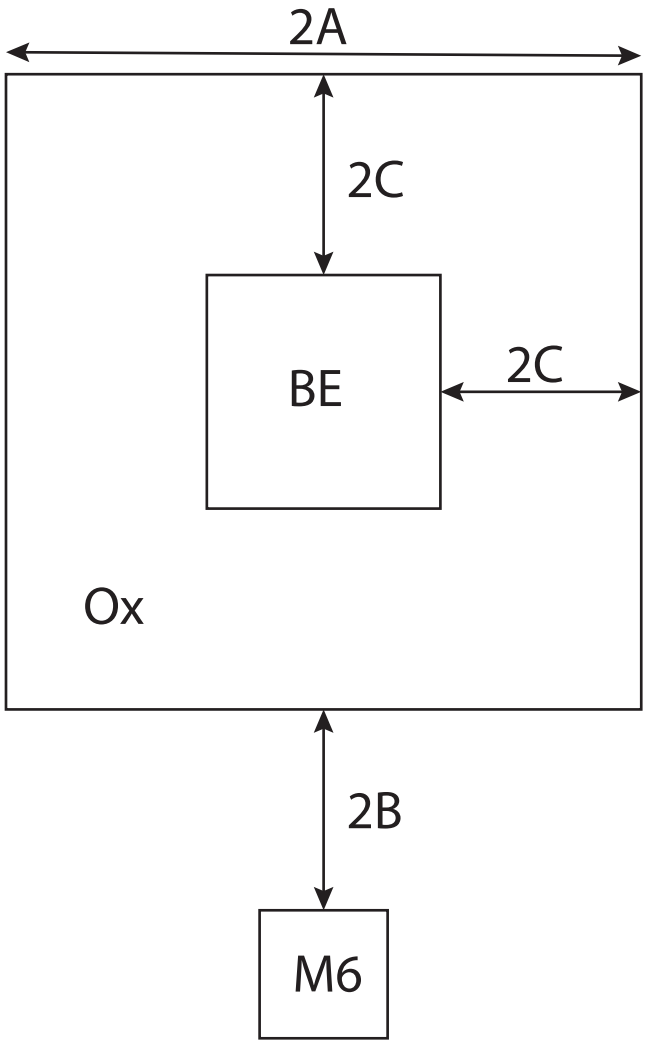
1. Layer BottomElectrode

	(unit : µm)
1A. Minimum BE width	1
1B. Minimum BE to BE	1
1C. Minimum BE layer enclosure of M6	1



2. Layer MetalOxide

	(unit : µm)
2A. Minimum Ox width	1
2B. Minimum Ox to M6	1
2C. Minimum Ox layer enclosure of BE	1



3. Layer TopElectrode

	(unit : µm)
3A. Minimum TE width	1
3B. Minimum TE to TE	1
3C. Minimum TE layer enclosure of Ox	1
3D. Minimum TE layer enclosure of M6	1
3E. Minimum TE to external M6	2