SKY130_UUOPENFPGA_CC_HD_INVMUX2_1

Cell Library: sky130_uuopenfpga_cc_hd
Process: TT
Voltage: 1.80
Temp: 25.00

Footprint

Cell Name	Area
sky130_uuopenfpga_cc_hd_invmux2_1	15.01440

Pin Capacitance Information

Cell Name	Pin Cap(pf)						Max Cap(pf)
	Q1	**Q2**	**S0**	**S0B**	**S1**	**S1B**	**Z**
sky130_uuopenfpga_cc_hd_invmux2_1	0.00261	0.00256	0.00139	0.00147	0.00129	0.00152	0.21844

Leakage Information

Cell Name	Leakage(nW)		
	Min.	**Avg**	**Max.**
sky130_uuopenfpga_cc_hd_invmux2_1	0.01636	23848.70000	238510.00000

Delay Information

Delay(ns) to Z rising :

Cell Name	Timing Arc(Dir)	Delay(ns)		
		First	**Mid**	**Last**
sky130_uuopenfpga_cc_hd_invmux2_1	**Q1->Z (FR)**	0.04964	0.44438	2.52612
	Q2->Z (FR)	0.04963	0.44451	2.52653
	S0->Z (FR)	0.00637	0.07894	0.89486
	S0->Z (RR)	0.01696	0.39469	2.38455
	S0B->Z (RR)	0.00637	0.07894	0.89486
	S0B->Z (FR)	0.01696	0.39469	2.38455
	S1->Z (FR)	0.00635	0.07894	0.89485
	S1->Z (RR)	0.01771	0.39569	2.38589
	S1B->Z (RR)	0.00635	0.07894	0.89485
	S1B->Z (FR)	0.01771	0.39569	2.38589

Delay(ns) to Z falling :

Cell Name	Timing Arc(Dir)	Delay(ns)		
		First	Mid	Last
sky130_uuopenfpga_cc_hd_invmux2_1	Q1->Z (RF)	0.03398	0.28451	1.67750
	Q2->Z (RF)	0.03398	0.28465	1.67822
	S0->Z (FF)	0.00651	0.07898	0.89489
	S0->Z (RF)	0.01407	0.26292	1.68862
	S0B->Z (RF)	0.00651	0.07898	0.89489
	S0B->Z (FF)	0.01407	0.26292	1.68862
	S1->Z (FF)	0.00652	0.07897	0.89488
	S1->Z (RF)	0.01309	0.26207	1.68993
	S1B->Z (RF)	0.00652	0.07897	0.89488
	S1B->Z (FF)	0.01309	0.26207	1.68993

Power Information

Internal switching power(pJ) to Z rising :

Cell Name	Input	Power(pJ)		
		first	mid	last
sky130_uuopenfpga_cc_hd_invmux2_1	Q1	0.01510	0.01462	0.01421
	Q2	0.01489	0.01440	0.01401
	S0	0.00535	0.00494	0.00416
	S0B	0.00535	0.00494	0.00416
	S1	0.00535	0.00488	0.00422
	S1B	0.00535	0.00488	0.00422

Internal switching power(pJ) to Z falling :

Cell Name	Input	Power(pJ)		
		first	mid	last
sky130_uuopenfpga_cc_hd_invmux2_1	Q1	0.00222	0.00199	0.00340
	Q2	0.00244	0.00222	0.00363
	S0	0.00300	0.00300	0.00300
	S0B	0.00300	0.00300	0.00300
	S1	0.00298	0.00297	0.00298
	S1B	0.00298	0.00297	0.00298

Passive power(pJ) for Q1 rising (conditional):

Cell Name	When	Power(pJ)		
		first	mid	last
sky130_uuopenfpga_cc_hd_invmux2_1	(Q2 * !S0 * S0B * S1 * !S1B * !Z) + (Q2 * !S0 * S0B * !S1 * S1B) + (!Q2 * !S0 * S0B * S1 * !S1B * Z) + (!Q2 * !S0 * S0B * !S1 * S1B)	0.00000	0.00000	0.00247

Passive power(pJ) for Q1 falling (conditional):

Cell Name	When	Power(pJ)		
		first	mid	last
sky130_uuopenfpga_cc_hd_invmux2_1	(Q2 * !S0 * S0B * S1 * !S1B * !Z) + (Q2 * !S0 * S0B * !S1 * S1B) + (!Q2 * !S0 * S0B * S1 * !S1B * Z) + (!Q2 * !S0 * S0B * !S1 * S1B)	0.00821	0.00795	0.01223

Passive power(pJ) for Q2 rising (conditional):

Cell Name	When	Power(pJ)		
		first	mid	last
sky130_uuopenfpga_cc_hd_invmux2_1	(Q1 * S0 * !S0B * !S1 * S1B * !Z) + (Q1 * !S0 * S0B * !S1 * S1B) + (!Q1 * S0 * !S0B * !S1 * S1B * Z) + (!Q1 * !S0 * S0B * !S1 * S1B)	0.00000	0.00000	0.00273

Passive power(pJ) for Q2 falling (conditional):

Cell Name	When	Power(pJ)		
		first	mid	last
sky130_uuopenfpga_cc_hd_invmux2_1	(Q1 * S0 * !S0B * !S1 * S1B * !Z) + (Q1 * !S0 * S0B * !S1 * S1B) + (!Q1 * S0 * !S0B * !S1 * S1B * Z) + (!Q1 * !S0 * S0B * !S1 * S1B)	0.00799	0.00773	0.01201