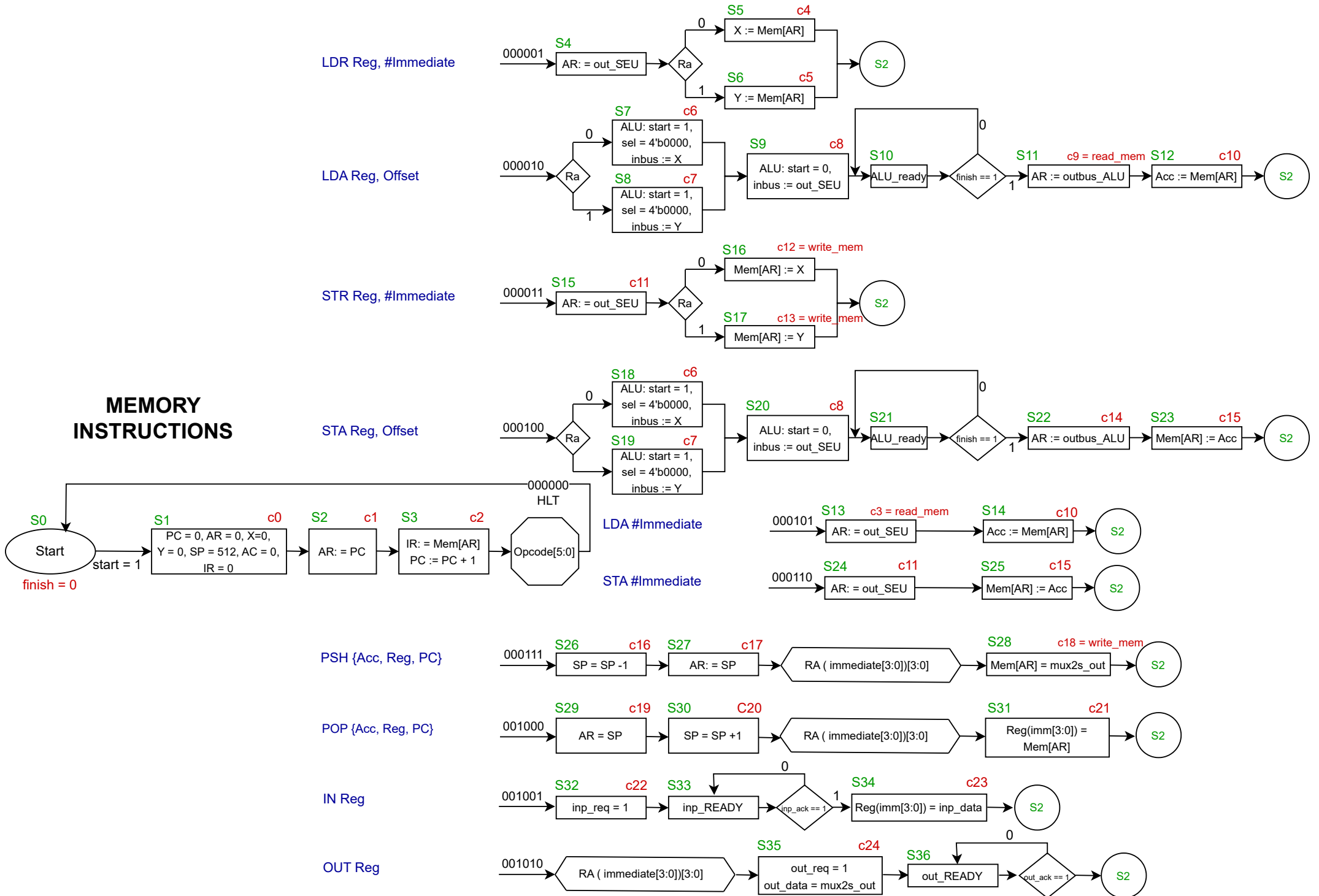
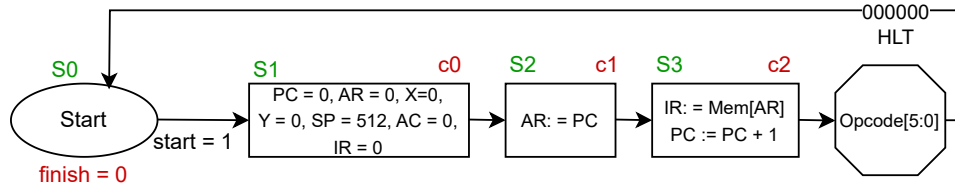


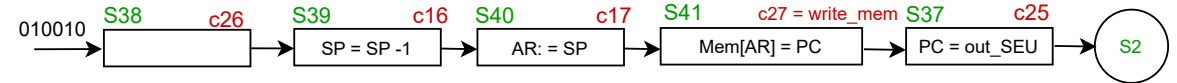
MEMORY INSTRUCTIONS



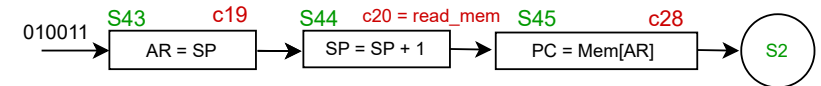
BRANCH INSTRUCTIONS



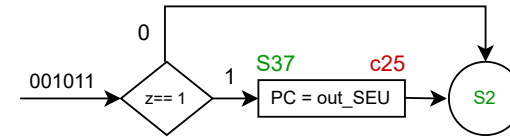
JMP



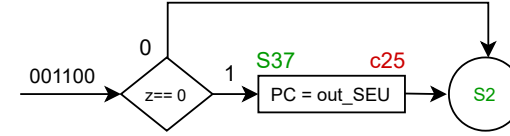
RET



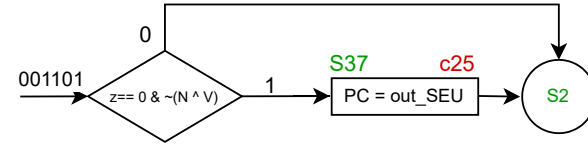
BEQ



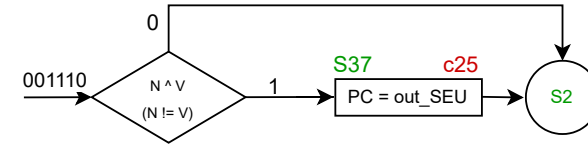
BNE



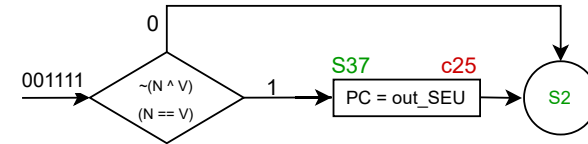
BGT



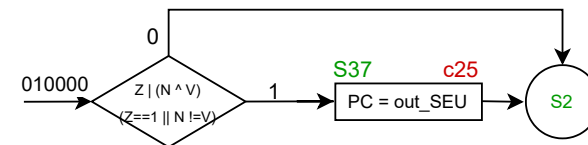
BLT



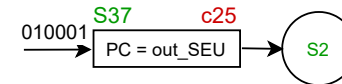
BGE



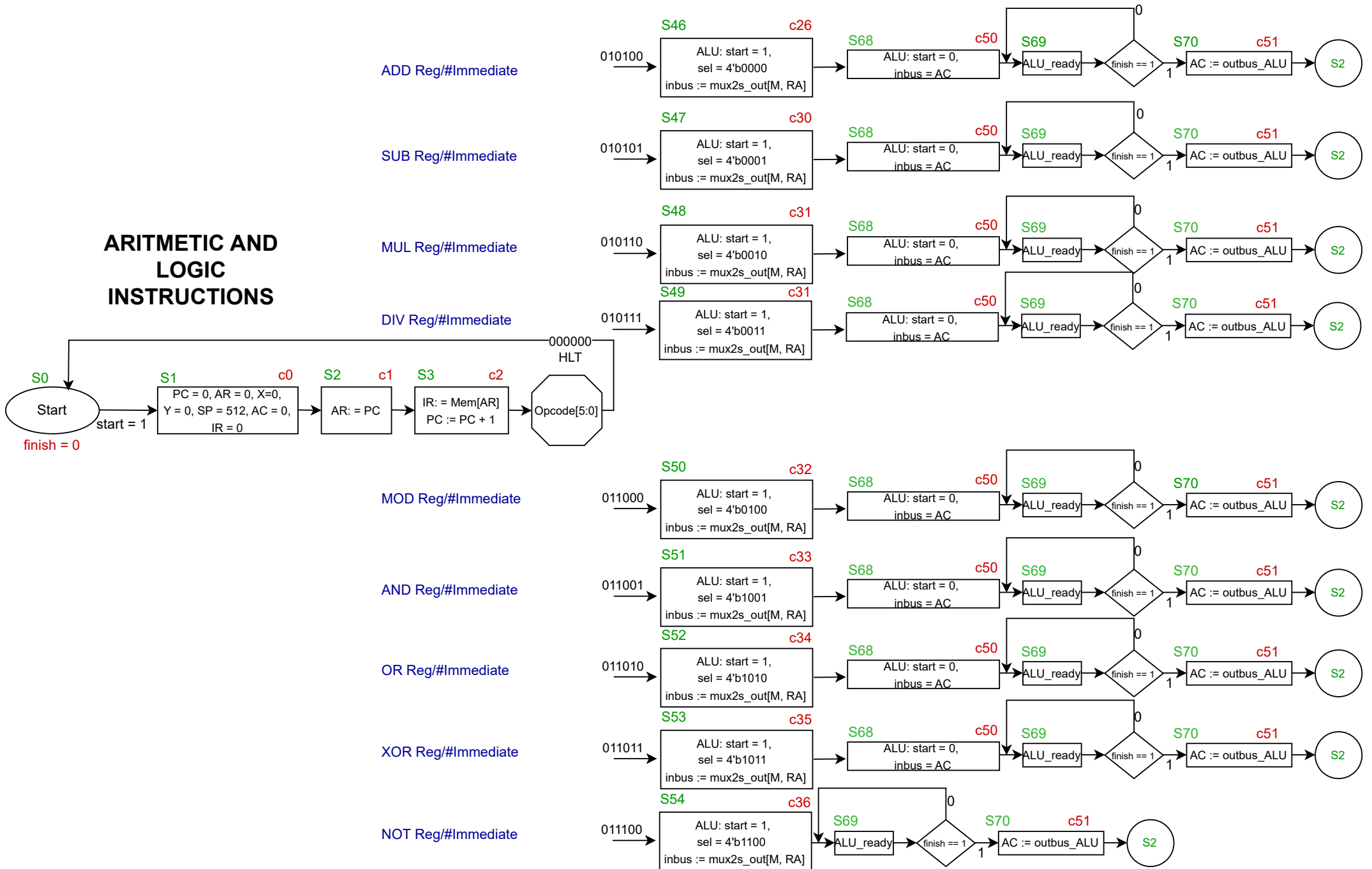
BLE



BRA



ARITMETIC AND LOGIC INSTRUCTIONS



ARITMETIC AND LOGIC INSTRUCTIONS

ADD #Address

SUB #Address

MUL #Address

DIV #Address

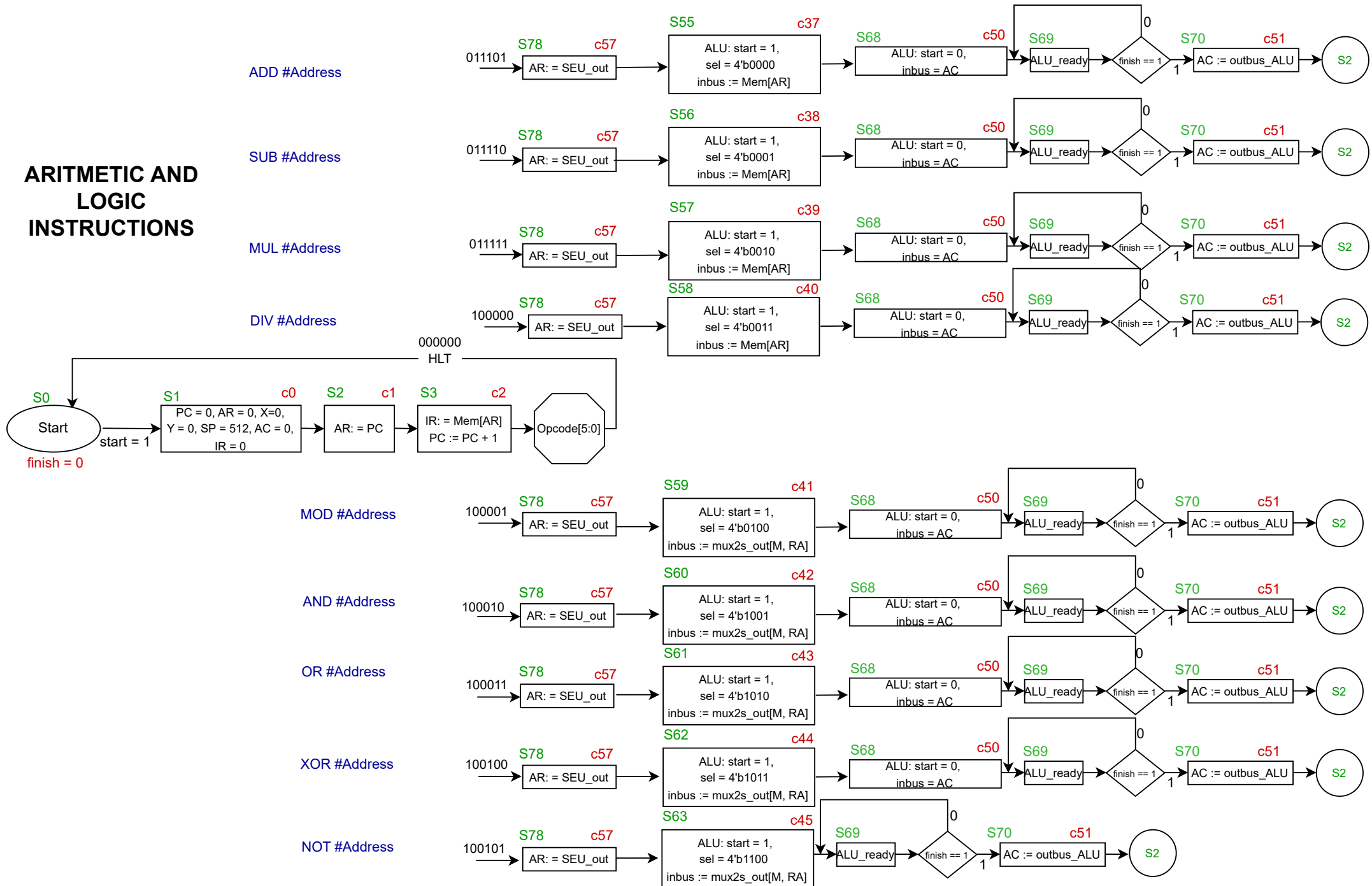
MOD #Address

AND #Address

OR #Address

XOR #Address

NOT #Address



ARITMETIC AND LOGIC INSTRUCTIONS

LSR #Immediate

LSL #Immediate

RSR #Immediate

RSL #Immediate

CMP Reg, Reg

TST Reg, Reg

MOV Reg, Reg

MOV Reg, #Immediate

