Chapter 6 Sequential Building Blocks

N-bit Register

Data input : N-bit vector $\vec{D} = d_{n-1} \cdots d_1 d_0$

Data output : N-bit vector $\vec{Q} = q_{N-1} \cdots q_1 q_0$

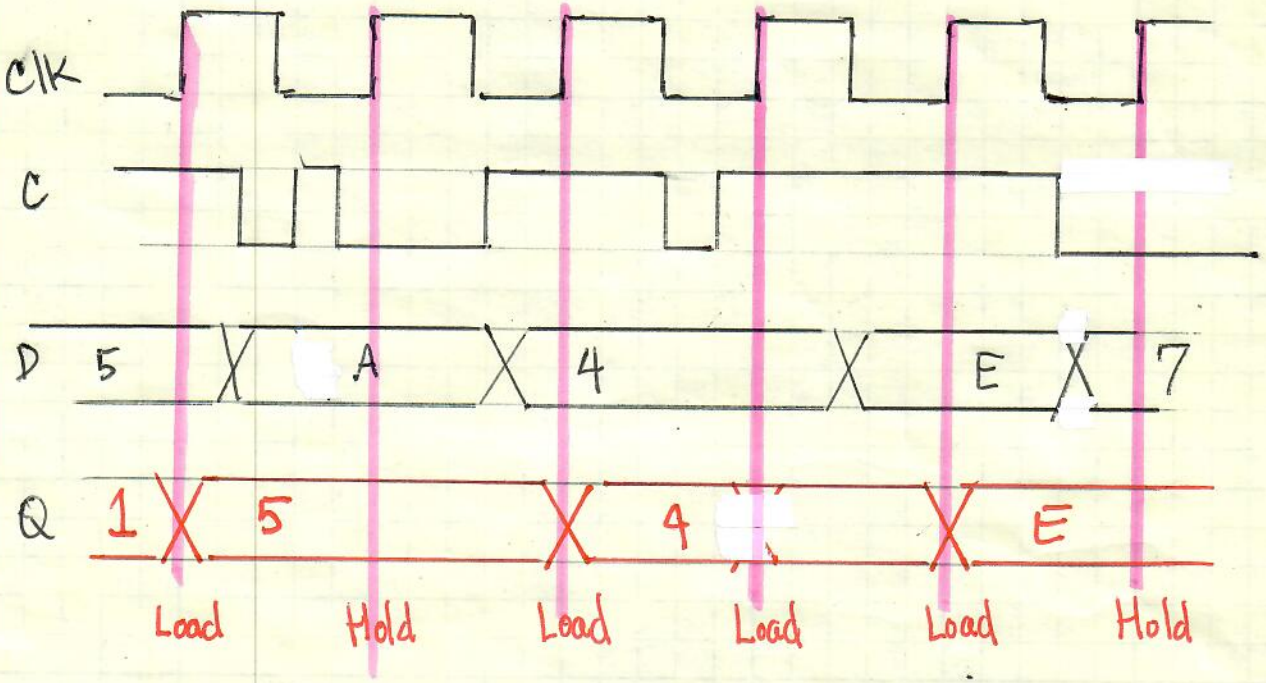
Control : 1-bit C

Status : None

Other : clk, reset

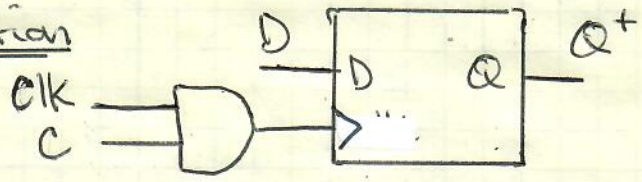
Behavior

reset	clk	C	D	Q^+	Note
0	X	X	X	0	
1	0, 1, ↓	X	X	Q	
1	↑	0	X	Q	Hold
1	↑	1	D	D	Load



Internal organization

Wrong Solution

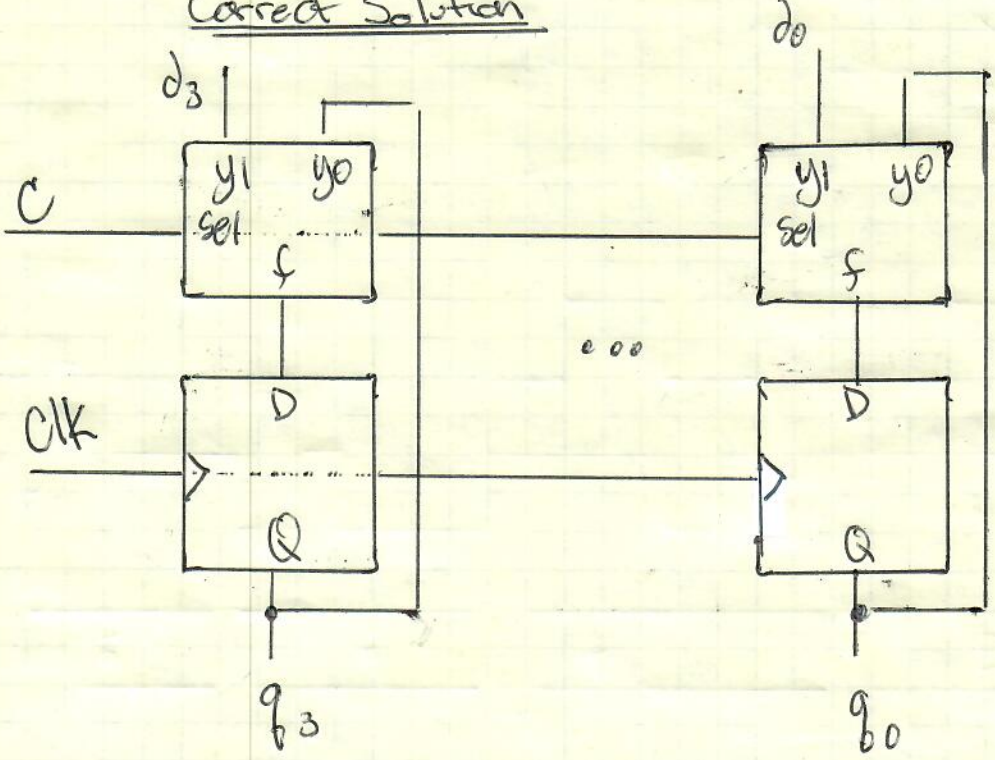


Because you can get a positive edge when

clk = 1 C ↑

Introduces delay in clk net causing skew

Correct Solution



When C = 1 d_i passed to D input & loaded on next clk

C = 0 q_i passed to D input & loaded on next clk