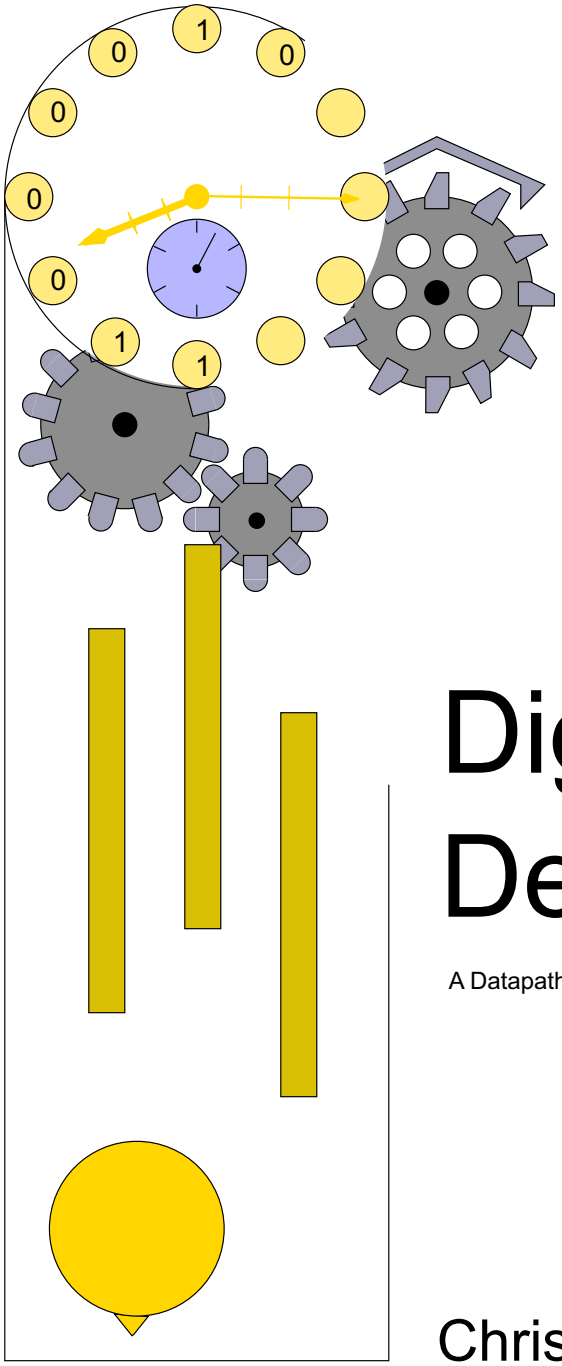

Digital Design

A Datapath and Control Approach

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This document was prepared with LaTeX.

Contents

List of Processes

List of Basic Building Blocks

Chapter 0

Why?

Welcome to Introduction to Digital Design - A Datapath and Control Approach. You might be tempted to ask "Why bother writing yet another digital design text?" The assumption being that this text is going to cover the same ground as a typical digital design text. And yes, to some degree it will, but more importantly it will not. *This text presents a systematic approach to the design process for digital circuits that will enable you to design sophisticated digital systems.* I consider a digital design sophisticated when it needs to be described algorithmically.

After going through this text and laboratories my goal is that you should be able to use 100% of the material you learned to design a digital systems that in Figure 0.1.

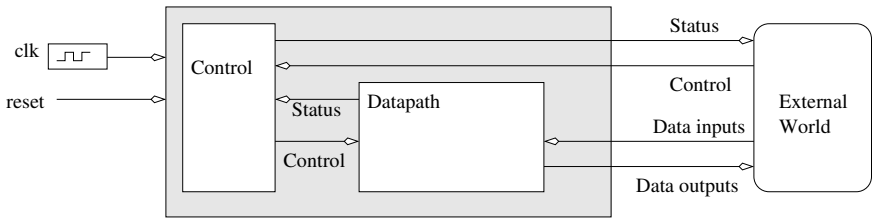

Figure 0.1: An abstract digital system constructed from a datapath and a control unit.

The datapath and control framework classifies the inputs and outputs of every digital logic building block as either **Data inputs**, **Data output**, **Control inputs**, **Status output** (the two special signals, **clk** and **reset** sit outside this classification). Under this framework, the datapath performs all data manipulations and the control unit sequences the control inputs for datapath. The datapath is built from combinational and sequential building blocks like multiplexers and counters. The control unit is a finite state machine.

Class Organization

I wrote the text, homework and laboratory exercises for a 4-credit course delivery. The example timeline shown in Table 0.1 assumes 3 50-minute lectures per week and 1 2/3-hour laboratory a week.

Laboratory

While it is expected that students finish the laboratory during the scheduled time, frequently students will need additional time to complete work, so accommodations need to be in-place for them to access the hardware and software outside of course hours. I expect that my students will need to work about 4-hours a week outside of class.

0.1 Example Timeline

Table 0.1: The labs in this example timeline are shown the earliest possible to insure that the prerequisite skills have been covered or 3 lecture sessions have passed since the last lecture.

Session	Topic	Assignment	Reading
1	Course Intro, Binary numbering, Hexadecimal		1.1 – 1.3
2	Binary Addition		1.4
3	Logic gates / Circuit to Symbolic / Circuit to Truth Table		2.1, 2.21, 2.2.2
4	Symbolic to Truth Table / Symbolic to Circuit	HW#1 Due	2.2.3, 2.2.4
5	Symbolic to Verilog		Supplemental
Lab #1	Introduction to CAD tools and Verilog		
6	Symbolic to Symbolic		2.2.5
7	Symbolic to Symbolic		2.2.5
8	Truth Table to Symbolic SOP and POS	HW#2 Due	2.2.6, 2.2.7, 2.3
Lab #2	Hexadecimal to 7-segment Converter	Lab #1 Due	
9	Karnaugh Maps, 3 variables		3.1
10	Combinational Logic with Verilog		Supplemental
11	Karnaugh Maps, 4 and 5 variables	HW#3 Due	3.2, 3.3
Lab #3	Rock Paper Scissors	Lab #2 Due	
12	Don't cares		3.5
13	SOP and POS in Karnaugh maps		
14	Exam Review	HW#4 Due	3.6
Lab #4	Guessing Game	Lab #3 Due	
15	Exam I		
16	Decoder / Multiplexers		4.1, 4.2
17	2's complement		1.5
18	Adders	HW#5 Due	4.3
19	Adder Subtractor		4.4
Lab #5	Guessing Game with Hints	Lab #4 Due	
20	Comparator		4.5
21	Wire Logic / Combinations		4.7, 4.8
22	SR Latch	HW#6 Due	5.5
23	Basic memory elements – timing		5.1
24	Basic memory elements – practical considerations		5.7
Lab #6	Decimal Calculator	Lab #5 Due	
25	Register	HW#7 Due	6.1
26	Shift Registers		6.2

Session	Topic	Assignment	Reading
27	Counter		6.3
Lab #7	1 Dimensional Cellular Automata	Lab #6 Due	6.3
28	RAM		6.4
29	Register Transfer		6.5
30	Exam Review	HW#8 Due	Supplemental
Lab #8	Mod 10 Counter	Lab #7 Due	
31	Exam II		
32	Sequential Design – Traffic Light Controller		7.4
33	Sequential Design – Verilog		Supplemental
Lab #9	Stopwatch Datapath	Lab #8 Due	
34	Sequential Design – Timing		7.6
35	Sequential Design – Vending Machine	HW#9 Due	7.5
Lab#10	Stopwatch Control	Lab #9 Due	
36	Datapath and Control Theory		8.1, 8.2, 8.3
37	Datapath and Control Theory		8.1, 8.2, 8.3
38	Datapath and Control Practice	HW#10 Due	8.4, 8.5
Lab#11	Stopwatch – Datapath and Control	Lab #10	
39	Datapath and Control Practice		8.4, 8.5
40	Datapath and Control Timing		8.4, 8.5
41	Datapath and Control Practice		8.7
	Lab wrap-up	Lab #11 Due	
42	Exam Review	HW#11 Due	Supplemental
	Exam III		

Appendix A

74LS00 Data Sheets

Since the device documentation for the TI chips is covered by TI's copyright it was decided to leave these pages out of this text. The documents discussed in the text can be found onilne at:
http://focus.ti.com/lit/ds/symlink/sn74ls00.pdf