

CMPEN 271 – Fall 2008

Exam 2

Name:

PSU ID:

D	Q+	T	Q+	S	R	Q+	J	K	Q+
0	0	0	Q	0	0	Q	0	0	Q
0	0	0	Q	0	1	0	0	1	0
1	1	1	Q'	1	0	1	1	0	1
				1	1	x	1	1	Q'

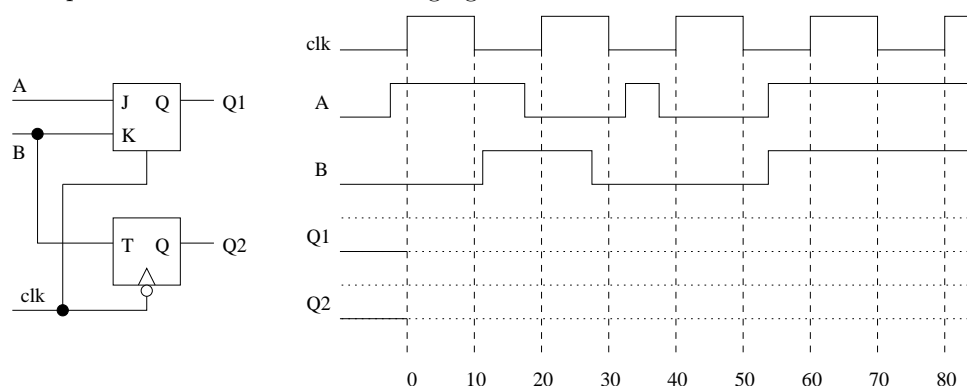
- (1 pt.) Assuming a word size of 5 bits, interpret 11010 as a 2's complement number.
a) -24 b) -12 c) -6 d) -2 e) None of the above.
- (1 pt.) Assuming a word size of 4 bits, determine the 2's complement representation of -5.
a) 1011 b) 1101 c) 1100 d) 1001 e) None of the above.
- (2 pt.) How many AND gates are in a 4:16 decoder?
a) 4 b) 8 c) 16 d) 32 e) None of the above.
- (2 pt.) How many inputs do the AND gates in a 16:1 mux have?
a) 2 b) 4 c) 8 d) 16 e) None of the above.
- (1 pt.) How many 4:1 muxes are needed to construct a 8x4x1 mux?
a) 4 b) 8 c) 12 d) 32 e) None of the above.
- (2 pt.) How many 2:1 muxes are in an 8-bit register?
a) 2 b) 3 c) 4 d) 8 e) 64
- (1 pt.) How many address lines does a 256kx32 RAM have?
a) 32 b) 19 c) 18 d) 16 e) 15

Questions 8-10 concern the construction of a bit-slice of a comparator. The questions will ask you to complete the entries in the truth table below denoted by a , b , and c .

G_{in}	L_{in}	E_{in}	x	y	G_{out}	L_{out}	E_{out}
0	0	0	1	0	a		
0	0	1	1	0		b	
1	0	1	1	0			c

8. (1 pt.) What is the value of a ?
a) 0 b) 1 c) x
9. (1 pt.) What is the value of b ?
a) 0 b) 1 c) x
10. (1 pt.) What is the value of c ?
a) 0 b) 1 c) x

For questions 11-14 use the following figure



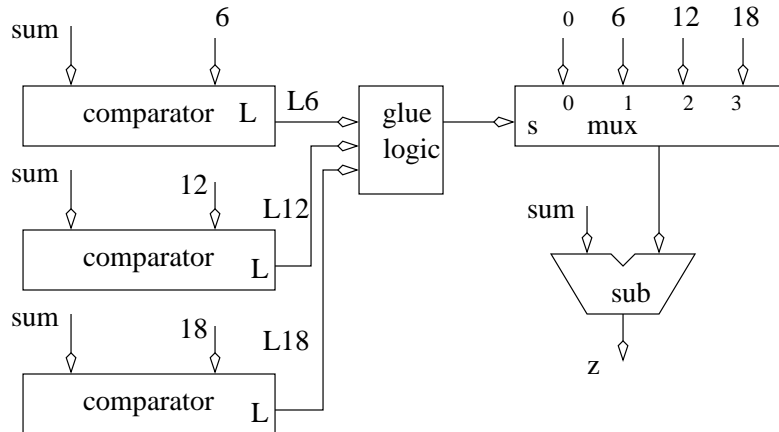
11. (1 pt.) What is the value of Q1 at time 45
a) 0 b) 1 c) toggling
12. (1 pt.) What is the value of Q1 at time 65
a) 0 b) 1 c) toggling
13. (1 pt.) What is the value of Q2 at time 25
a) 0 b) 1 c) toggling
14. (1 pt.) What is the value of Q2 at time 75
a) 0 b) 1 c) toggling

You have a digital design which calls for a circuit which performs the following task (written as a C if/then statement). You have decided on the architecture. Its your job to design to complete the truth table for the glue-logic box (only an arbitrary portion of the complete truth table is shown). I would recommend drawing a number line and putting the values of L6, L12, and L18 on it.

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if      (sum < 6)  z = sum
else if (sum < 12) z = sum-6
else if (sum < 18) z = sum-12
else      z = sum-18

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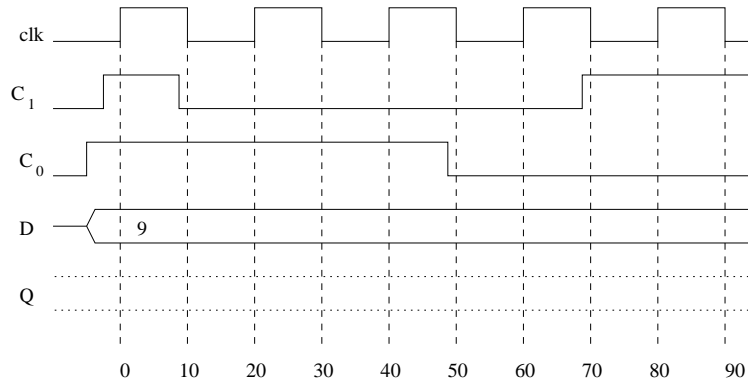


L6	L12	L18	select
0	0	0	a
0	1	1	b
1	0	1	c

15. **(1 pt.)**What is the (decimal) value of a in the truth table?
 - a) 0
 - b) 1
 - c) 2
 - d) 3
 - e) x
16. **(1 pt.)**What is the (decimal) value of b in the truth table?
 - a) 0
 - b) 1
 - c) 2
 - d) 3
 - e) x
17. **(1 pt.)**What is the (decimal) value of c in the truth table?
 - a) 0
 - b) 1
 - c) 2
 - d) 3
 - e) x

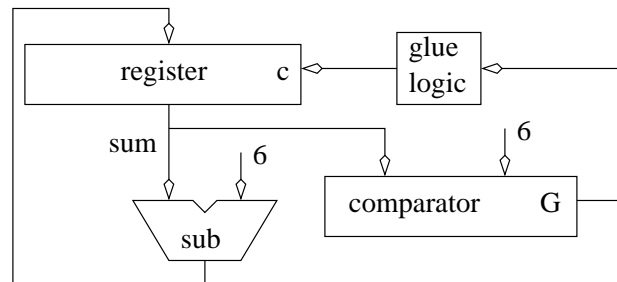
For questions 18,19 assume that a 4-bit (circular) shift register has the following truth table. Complete the timing diagram below.

clk	C_1C_0	D	Q^+
0,1,↓	xx	x	Q
↑	00	x	Q
↑	01	x	$Q \gg 1$ (CSR)
↑	10	x	$Q \ll 1$ (CSL)
↑	11	D	D



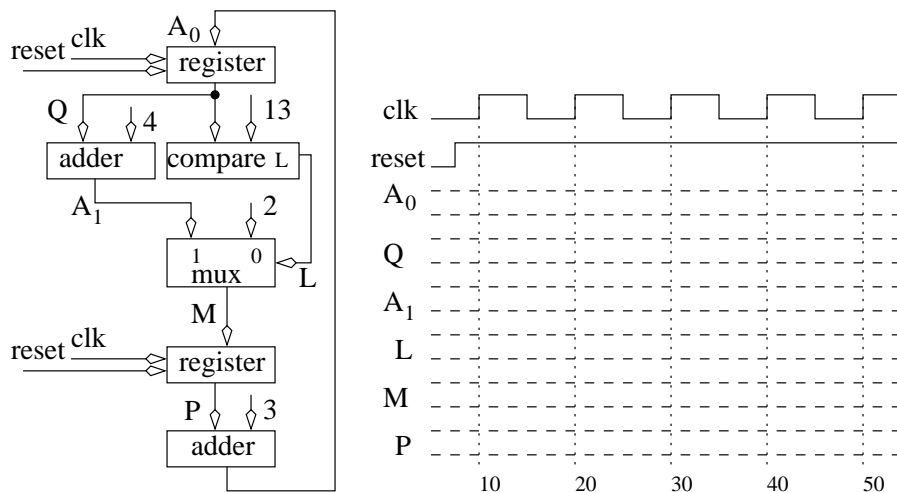
18. (1 pt.) What is the value of Q at time 55?
- a) 0110 b) 0010 c) 0100 d) 1110 e) none of the above
19. (1 pt.) What is the value of Q at time 90?
- a) 0001 b) 1100 c) 0100 d) 1110 e) none of the above
20. (2 pt.) You have a digital design which calls for a circuit which performs the following task. You have decided on the architecture shown to the right. Its your job to design the contents of the glue-logic box. Note, a register holds its value when the control input is 0 and loads its input when the control input is 1.

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while (sum > 6) sum -= 6;
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- a) $c=0$ b) $c=1$ c) $c=G$ d) $c=G'$ e) none of the above.

For problems 21-25 use the following figure and timing diagram. You should assume that all the devices process 5-bits data values.



21. (2 pt.) What is the value of P at time 15?
a) 0 b) 3 c) 4 d) 6 e) 11
22. (2 pt.) What is the value of A_0 at time 25?
a) 3 b) 5 c) 7 d) 8 e) 10
23. (1 pt.) What is the value of A_1 at time 35?
a) 8 b) 11 c) 14 d) 15 e) 18
24. (1 pt.) What is the value of Q at time 45?
a) 5 b) 7 c) 11 d) 13 e) 14
25. (1 pt.) What is the value of M at time 55?
a) 2 b) 5 c) 7 d) 8 e) 9