CMPEN 271

Exam 3 Fall 2012

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Name: Student ID:

1. **(3 pts.)** Determine the SOP_{min} realizations for F(A,B,C,D)=Σm(0,2,4,6,7,13,15).

$AB\backslash CD$	00	01	11	10
00				
01				
11				
10				

   a) A'C'D' + A'CD' + BCD + ABD
   b) A'D' + BCD + ABD
   c) AD' + B'D + A'C'D
   d) (A'+D)(B+D')(A+C+D')
   e) None of the above

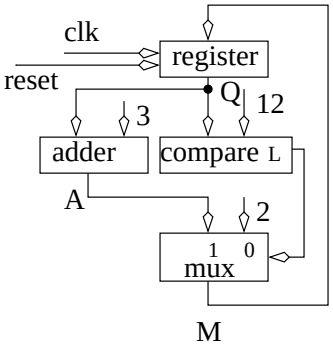
2. **(3 pts.)** The output of a sequential circuit is fundamentally different than a combinational circuit because the sequential circuits output is a function of the?

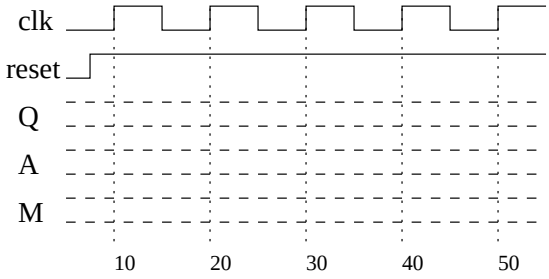
   a) State b) Input c) Output d) MIE's

3. **(2 pts.)** You are told to implement a 3 bit counter using the ones hot encoding of states. Each state represents the current count value. How many flip flops will the counter require?

   a) 3 b) 4 c) 7 d) 8 e) 16

For problems 4-7 use the following figure and timing diagram. You should assume that all the devices process 5-bits data values.





4. **(2 pts.)**What is the value of A at time 25?
   a) 0 b) 2 c) 3 d) 6 e) 9

5. **(2 pts.)**What is the value of Q at time 35?
   a) 0 b) 2 c) 3 d) 6 e) 9

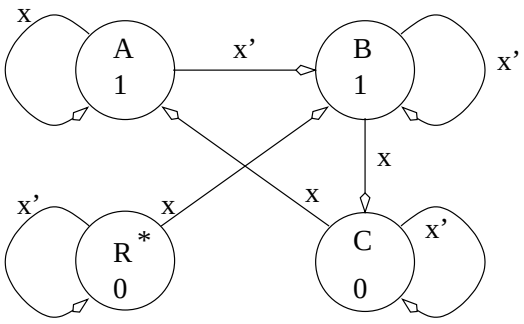
6. **(2 pts.)**What is the value of M at time 45?
   a) 2 b) 5 c) 9 d) 12 e) 15

7. **(2 pts.)**What is the value of A at time 45?
   a) 2 b) 5 c) 9 d) 12 e) 15

Questions 8-11 concern the FSM realization of the state diagram given below. Assume a ones hot encoding of the states. The input is X and the output Z. Let D_A be the input to the flip flop representing state A. Let Q_A be the output from the flip flop representing state A. Apply the preceding definitions to $D_B, Q_B, D_C, Q_C, D_R, Q_R$.

8. **(2 pts.)** How many flip flops are required to realize this FSM?
   a) 1 b) 2 c) 3 d) 4 e) 5

9. **(3 pts.)** What is the memory input equation for flip flop A?
   a) 1
   b) 0
   c) $X'Q_B$
   d) $XQ_A + XQ_C$
   e) None of the above.



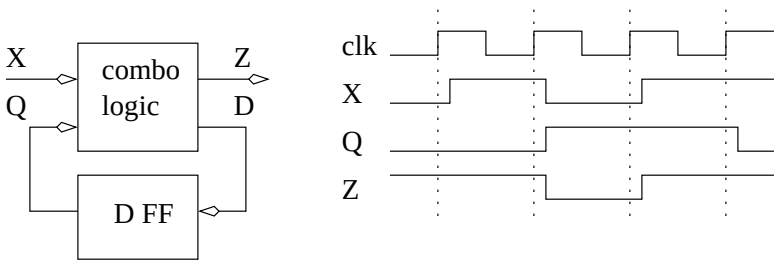
10. **(3 pts.)** What is the memory input equation for flip flop R?

    a) 1
    b) 0
    c) $XQ_B + X'Q_C$
    d) Q_R
    e) None of the above.

11. **(3 pts.)** What is the equation for Z?

    a) 0
    b) 1
    c) $Q_R + Q_C$
    d) $XQ_R + XQ_C + XQ_B + XQ_A$
    e) None of the above.

Questions 12 and 13 are based on the figure below of a FSM constructed from 1 D flip flop and some combinational logic. The timing diagram to the right shows the response of the circuit to an input sequence X applied to it. The timing diagram shows small propagation delays. From the timing diagram you are to infer the contents of the combinational logic box.



12. **(2 pts.)** Which of the following describes D?

$Q\backslash x$	0	1
0		
1		

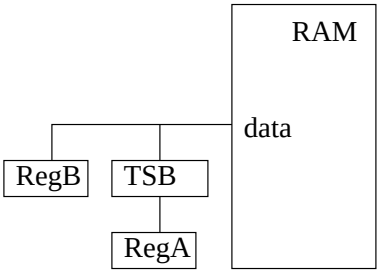
    a) $D = Q'$
    b) $D = X'Q$
    c) $D = X' + Q$
    d) $D = XQ' + X'Q$
    e) D Cannot be determined from given information.

13. **(2 pts.)** Which of the following describes Z?

$Q\backslash x$	0	1
0		
1		

    a) $Z = Q$
    b) $Z = X'Q$
    c) $Z = X + Q'$
    d) $Z = X'Q + XQ'$
    e) Z Cannot be determined from given information.

The following circuit is used to read and write a RAM. Consult it for questions 14-16. Note, this question requires you to determine the direction of data flow in the circuit, hence arrows are not shown on the data line. In addition you should not infer anything from the position of the data lines incident to the registers.



14. **(3 pts.)** Which register does the RAM read data from?

    a) RegA b) RegB

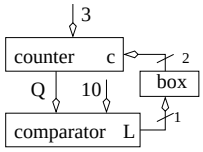
15. **(3 pts.)** For which operation does the TSB tristate (open circuit) its output?

    a) RAM Read b) RAM Write

16. **(3 pts.)** The address lines (not shown in the schematic) will need to have a TSB as well.

    a) True b) False

17. **(3 pts.)** What is the logic inside `box` in order to make the count sequence on Q go from 3 to 11 (inclusive of both) over and over. Use the truth table for the counter given below.

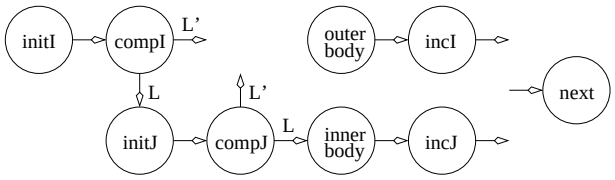


    a) $c_1 = L'$ $c_0 = 0$
    b) $c_1 = L'$ $c_0 = 1$
    c) $c_1 = L$ $c_0 = 0$
    d) $c_1 = L$ $c_0 = 1$
    e) None of the above

clk	C_1C_0	D	Q^+
0,1,↓	xx	x	Q
↑	00	x	Q
↑	01	x	Q+1
↑	10	x	Q-1
↑	11	D	D

Questions 18-21 concern themselves with the problem of implementing a doubly nested for loops. The algorithm follows.

```
for(i=0; i<A; i++) {
    for(j=0; j<B; j++) {
        inner_body;
    }
    outer_body;
}
next
```



Part of the state diagram for the FSM is already drawn. Answer the questions in order to help me complete it.

18. **(1 pt.)** Which state does the L' arc from `compI` go to?

    a) `outer_body`
    b) `incI`
    c) `inner_body`
    d) `next`
    e) None of the above.

19. **(1 pt.)** Which state does the L' arc from `compJ` go to?

    a) `outer_body`
    b) `incJ`
    c) `incI`
    d) `next`
    e) None of the above.

20. **(1 pt.)** Which state does the arc from `incI` go to?

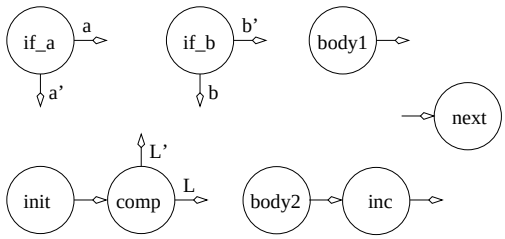
    a) `compI`
    b) `initJ`
    c) `compJ`
    d) `next`
    e) None of the above.

21. **(1 pt.)** Which state does the arc from `incJ` go to?

    a) `compI`
    b) `initJ`
    c) `inner_body`
    d) `next`
    e) None of the above.

Questions 22-25 concern themselves with the problem of implementing the following algorithm. Note that `a` and `b` are status bits, from comparators, which are either true or false. The output of the for loop comparator is `L`.

```
if (a) {
    if (b) {
        body1; }
    for(i=0; i<N; i++) {
        body2;         }  }
next
```



Part of the state diagram for the FSM is already drawn. Answer the questions in order to help me complete it.

22. **(1 pt.)** Which state does the `a'` arc from `if_a` go to?

    a) `if_b`
    b) `body1`
    c) `init`
    d) `next`
    e) None of the above.

23. **(1 pt.)** Which state does the `b` arc from `if_b` go to?

    a) `body1`
    b) `init`
    c) `comp`
    d) `next`
    e) None of the above.

24. **(1 pt.)** Which state does the `b'` arc from `if_b` go to?

    a) `body1`
    b) `init`
    c) `comp`
    d) `next`
    e) None of the above.

25. **(1 pt.)** Which state does the arc leaving `body1` go to?

    a) `if_b`
    b) `init`
    c) `comp`
    d) `next`
    e) None of the above.

26. **(1 pt.)** Don't cares are not used as control inputs on sequential circuits because.

    a) A sequential circuit will remember a wrong control input.

    b) It would agitate the staple monkey.

    c) FSM are built from combination logic and flip flops.

    d) When a sequential circuit loads a value its control input is active.

    e) None of the above.

27. **(1 pt.)** The output of a mux feeds a register. The FSM tells the register to hold. What is true.

    a) The input of the register cannot change.

    b) The control input of the mux is a don't care.

    c) The output of the register is being feed into the mux.

    d) The output of the register cannot be used during that clock cycle.

    e) None of the above.

28. **(1 pt.)** In a complete 2-line handshake, how many total transitions are their on the 2 control lines (ACK and REQ)? A line is said to make a transition when it changes its logic level.

    a) 2

    b) 3

    c) 4

    d) 5

    e) None of the above.

29. **(3 pts.)** A FSM has an input called `button` which is the connected to a push button. When pressed the button outputs a 0, otherwise it outputs a 1. While the button is pressed we want the FSM to stay in state `wait` and increment a counter (via the control word). How should the self arc to state `wait` be labeled?

    a) `button'`

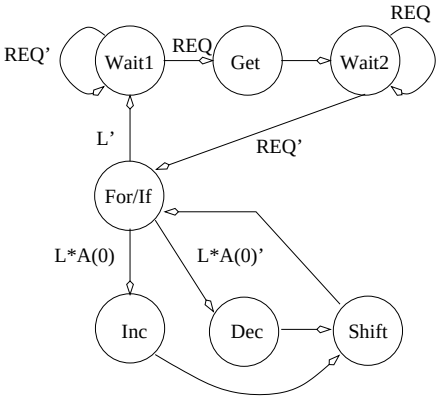
    b) `button`

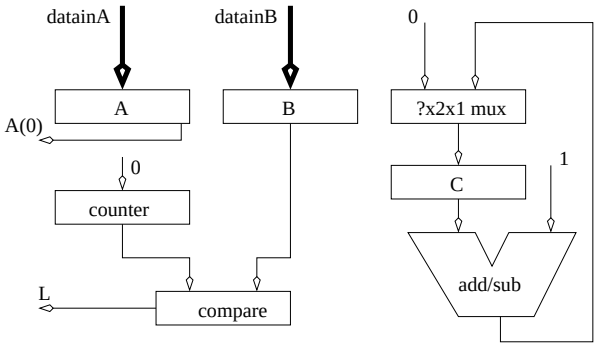
    c) There is no self arc to/from `wait`

    d) None of the above

Questions 30-52 **(1 pt. each)** This question deals with the construction of a digital circuit to accomplish the task specified by the following algorithm. A(0) refers to the LSB of A. A>> 1 refers to A shifted right 1 bit.

```
while(1) {
    ACK = 0;
    while(REQ == 0);              // If the control bit equals 0 or 00  mark A
    A = datainA;                  // If the control bit equals 01       mark B
    B = datainB;                  // If the control bit equals 10       mark C
    ACK = 1;                      // If the control bit equals 1 or 11  mark D
    while (REQ == 1);             // If the control bit is a don't care mark E
    ACK = 0;
    C = 0;
    for (i=0; i<B; i++) {
        if (A(0) == 1) then
            C = C + 1;
        else
            C = C - 1;
        A = A >> 1;
}   }
```





State	ACK	A	B	C	Mux	count	Add/Sub
	0	00 hold	0 hold	0 hold	0 pass 0	00 hold	0 add
	1	01 SR	1 load	1 load	1 pass C±1	01 down	1 sub
		10 SL				10 up	
		11 load				11 load	

Wait1	30						
Get	31	32	33	34			35
Wait2	36	37			38	39	
For/If							
Inc		40		41	42		43
Dec	44			45	46		47
Shift		48	49	50	51		52

Questions 53-56 are based on the datapath and control shown on the previous page.

53. **(2 pts.)** How many bits are in the status word?

a) 1 b) 2 c) 3 d) 5 e) 9

54. **(2 pts.)** How many bits are in the control word?

a) 2 b) 3 c) 5 d) 7 e) 9

55. **(3 pts.)** What is the Memory Input Equation for the For/If flip flop; assume a ones-hot encoding?

a) $D_{\text{For/If}} = Q_{\text{Wait1}} * L' + Q_{\text{Inc}} * L * A(0) + Q_{\text{Dec}} * L * A(0)'$

b) $Q_{\text{For/If}} = D_{\text{Wait1}} * L' + D_{\text{Inc}} * L * A(0) + D_{\text{Dec}} * L * A(0)'$

c) $D_{\text{For/If}} = Q_{\text{Wait2}} * REQ' + Q_{\text{Shift}}$

d) $Q_{\text{For/If}} = D_{\text{Wait2}} * REQ' + D_{\text{Shift}}$

e) None of the above.

56. **(2 pts.)** Which of the following is the circuit playing in the two-line handshake?

a) Active Producer

b) Active Consumer

c) Passive Producer

d) Passive Consumer

In order to assure the continued success of the Behrend ECE program, I would appreciate your evaluation of whether or not this course met its learning objectives. All answers will be kept anonymous and will be used for the future improvement of this course and the entire ECE program. Please record your answers on the SCANTRON form. Thanks for your help.

		Strongly Disagree A	Disagree B	Neutral C	Agree D	Strongly Agree E
57.	I understand how to convert numbers from one base to another and how to add and subtract numbers represented in binary and 2's complement form.					
58.	I understand how to convert between a truth table, a circuit diagram, boolean expression and a word statement.					
59.	I understand how to simplify logic expression into SOP or POS minimal form with or without don't cares.					
60.	I understand how to use ESPRESSO to minimize combinational logic functions.					
61.	I understand how adders, comparators, multiplexers and decoders are built and how they operate.					
62.	I understand how D,T,SR,JK, latches, clock latches and flip flops are supposed to operate.					
63.	I understand how registers, shift registers, counters, tri-state logic and RAMs are built and how they should operate.					
64.	I understand how to design Finite State Machines using a dense or Ones Hot encoding.					
65.	I understand how to implement complex digital systems using the datapath and control design approach.					