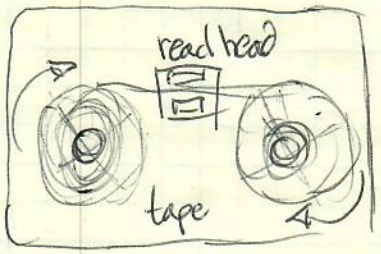
Random Access Memories (RAM) Use Verilog

The "random" in RAM is a reference to the access time to retrieve a byte at a random location (address). being indepent of bytes location. First mass storage devices were tape drives. The time to access a byte depends on the physical distance between the current read location & the bytes location.



Types: Volatile / Non-Volatile — Power Removed
Static / Dynamic — Refreshing
Serial / Parallel — Moving bits in/out

NxM RAM

Data in : $\log_2(N)$-bit address $\vec{A}$
M^2-bit bi-directional $\vec{D}$
Data out :
Control : R/$\overline{W}$ & CS
States : None
Behavior :

A	CS	R/$\overline{W}$	$\vec{D}$	Note
x	0	x	Z	hi impedance
A	1	0	M[A]=D	write
A	1	1	D=M[A]	read

RAM is collection of bits stored in words

8x4 RAM

Address	Contents
000	0110
001	1010
010	1101
011	0010
100	1000
101	0001
110	1101
111	1111

M[010] contains 1101

To read data

1. Assert $\vec{A}$, CS=1, R/$\bar{W}$ = 1
2. Wait
3. Read $\vec{D}$

To write data

1. Assert $\vec{A}$ $\vec{D}$
2. Assert CS=1 R/$\bar{W}$=0
3. Wait

Size prefix		
	2^{10}	1 kB
	2^{20}	1 MB
	2^{30}	1 GB
	2^{40}	1 TB
	2^{50}	1 PB ?

How many address bits for 2GB memory?

$2 * 1GB = 2^{31}$ bytes 31-bits

How many address bits for 512kB Memory?

$512 * 1kB = 2^{19}$ bytes 19-bits

Random Access Memory (RAM)

- Word: set of bits that can be simultaneously manipulated.
- RAM is a collection of words, each stored at a unique address that can be retrieved (read) or overwritten (write).

N×M RAM

data in: $\log_2(N)$ bit address $\vec{A}$

data: M-bit bidirectional data $\vec{D}$

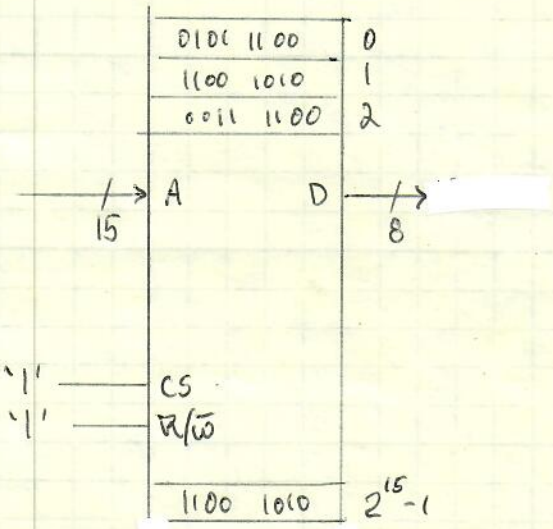
control: 1 bit $R/\bar{W}$, $\overline{CS}$

status: None

Behavior:

$\vec{A}$	$\overline{CS}$	$R/\bar{W}$	$\vec{D}$	
X	0	X	Z	
A	1	0	M[A] = D	write
A	1	1	M[A]	read

Example 32K × 8 RAM $32K = 2^{15}$ words each 8 bits



Size

1K	2^{10}
1M	2^{20}
1G	2^{30}
1T	2^{40}

$2^N K = 2^N \cdot 2^{10} = 2^{10+N}$