Final Exam Review

Exam: Monday May 4th 10:15 - 12:15
Show up to Zoom lecture @ 10 am - 10:15

Practice: Retake Exam 2 up to 2 times for make-up credit on Exam 2.

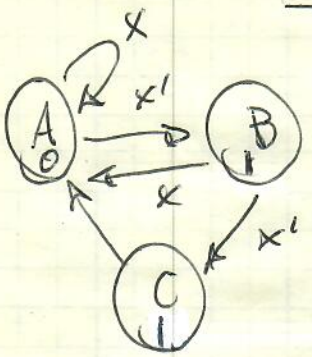
Quiz: 15% will be allocated to other HW, Labs, X1, X2 and final 3% each

Content:

- Kmap
- Glue logic
- BBB timing
- Algorithm → SD
- SD → MIE, OE
- Algorithm + SD + DP → Control Word
- Verilog

L.P.T. Some problems may have several associated questions. In these cases the problem statement will be repeated. Be on the look out for this and use Canvas navigation to look @ next question.

State Diagram has output in state



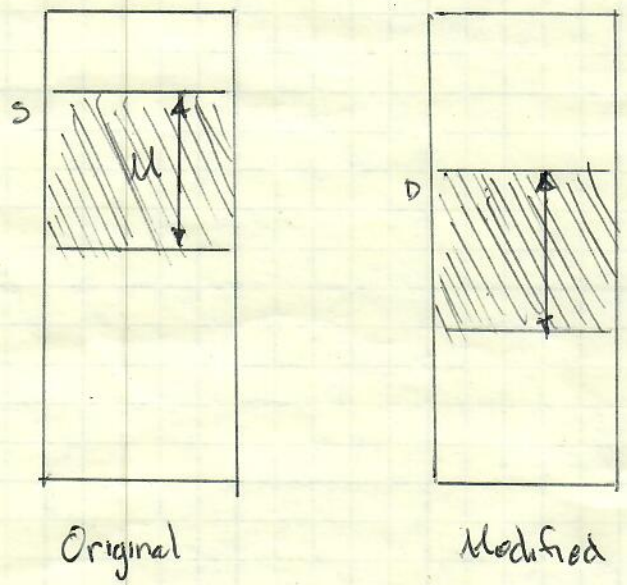
$D_A = XQ_A + XQ_B + Q_C$

$D_B = X'Q_A +$

$D_C = X'Q_B$

$Z = Q_B + Q_C$

Move M words from address S (source) to address D (destination)
Assume S<D

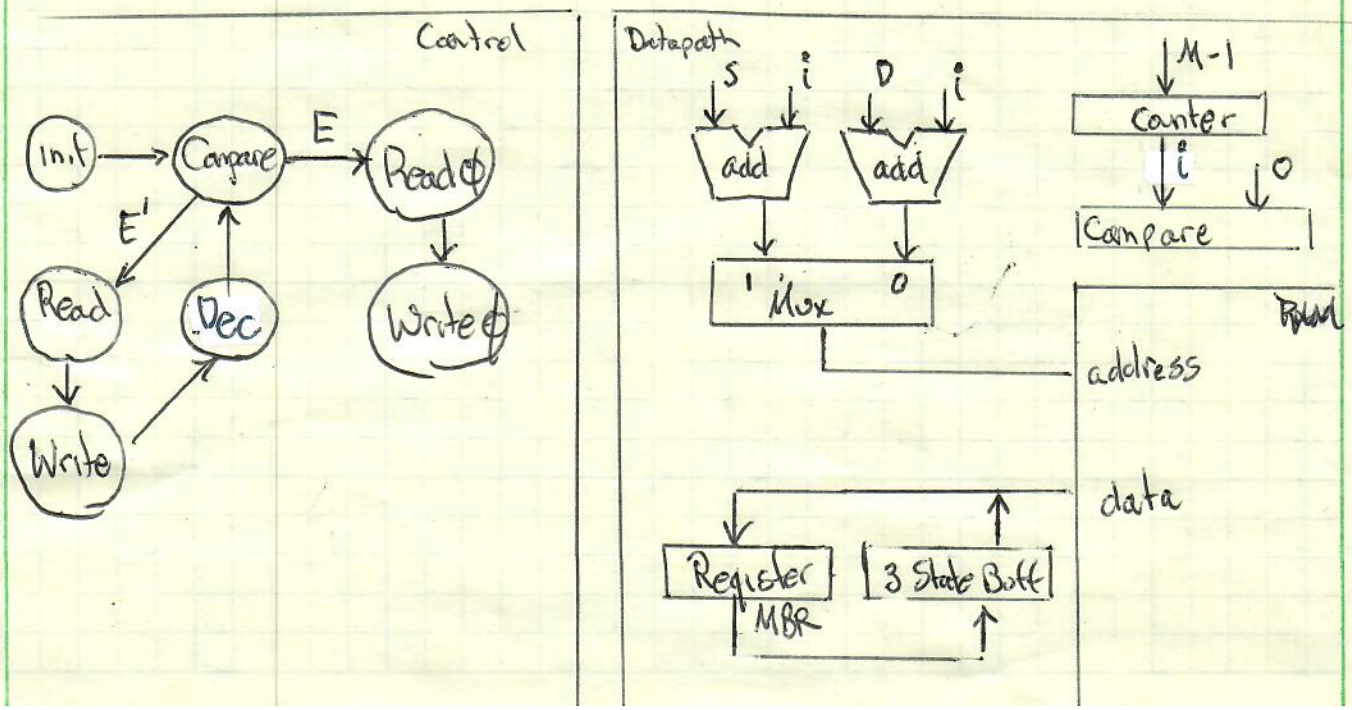


Yes the source block and destination block may overlap.

Solution move last word in source block first, then work towards first word. By the time D block overlaps S block, the overwritten word will already have been moved.

Algorithm:

```
for (i=M-1; i!=0; i--) {
    MBR = RAM[S+i]
    RAM[D+i] = MBR;
}
MBR = RAM[S];
RAM[D] = MBR;
```



Control word table

	Counter 00 hold 01 up 10 down 11 load	Mux 0 Dti 1 Sti	MBR 0 hold 1 load	3 State 0 Z 1 MBR	CS 0 1	RE 0 1	WE 0 1
Init	11				0		
Compare					0		
Read		1	1	0	1	1	
Write		0	0	1	1		1
Dec	10				0		
Readϕ		1	1	0	1	1	
Writeϕ		0	0	1	1		1