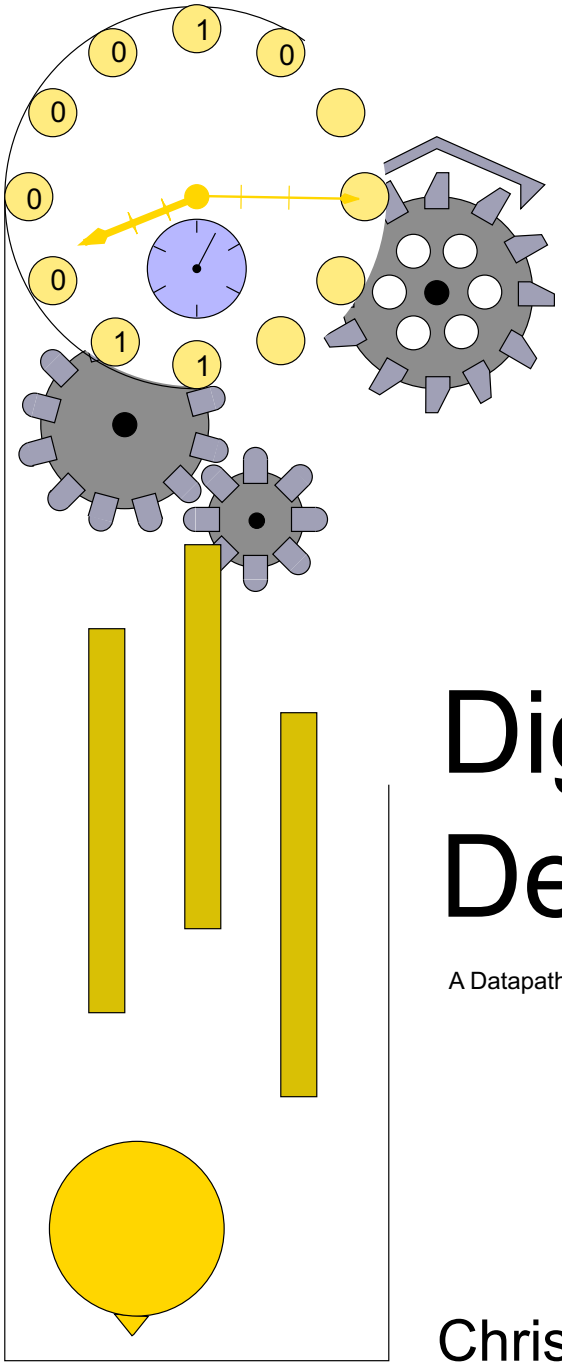


Digital Design

A Datapath and Control Approach

Chris Coulston

October 2, 2024

Contents

Chapter 1

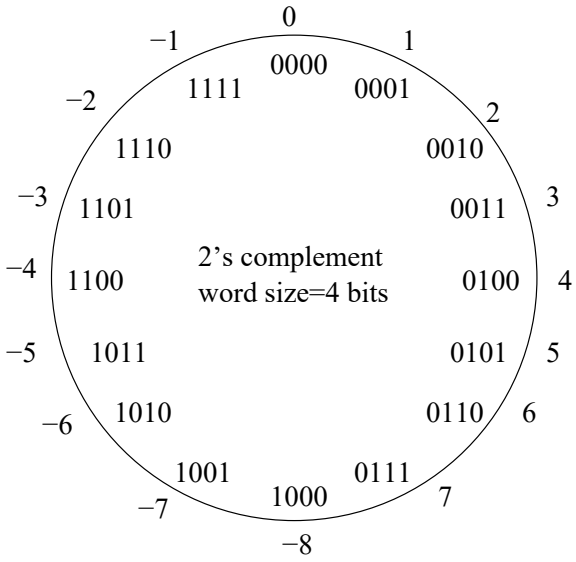
Numbering Systems

Helpfull Stuff

Decimal	Binary	Hexadecimal
0	0000	0
1	0001	1
2	0010	2
3	0011	3
4		4
5	0101	5
6		6
7		7
8	1000	8
9		9
10	1010	A
11		B
12	1100	C
13	1101	D
14		E
15	1111	F

i	0	1	2	3	4	5	6	7	8	9
2^i	1	2	4	8	16	32	64	128	256	512

$1110101011_2 =$
$1 * 2^9 + 1 * 2^8 + 1 * 2^7 + 0 * 2^6 + 1 * 2^5 + 0 * 2^4 + 1 * 2^3 + 0 * 2^2 + 1 * 2^1 + 1 * 2^0 =$
$2^8(0 * 2^3 + 0 * 2^2 + 1 * 2^1 + 1 * 2^0) + 2^4(1 * 2^3 + 0 * 2^2 + 1 * 2^1 + 0 * 2^0) + 2^0 * (1 * 2^3 + 0 * 2^2 + 1 * 2^1 + 1 * 2^0) =$
$2^8(0011_2) + 2^4(1010_2) + 2^0(1011_2) =$
$2^{4*2}(0011_2) + 2^{4*1}(1010_2) + 2^{4*0}(1011_2) =$
$16^2(0011_2) + 16^1(1010_2) + 16^0 * (1011_2) =$
$16^2(3) + 16^1(A) + 16^0 * (B) =$
$3AB_{16}$



Chapter 2

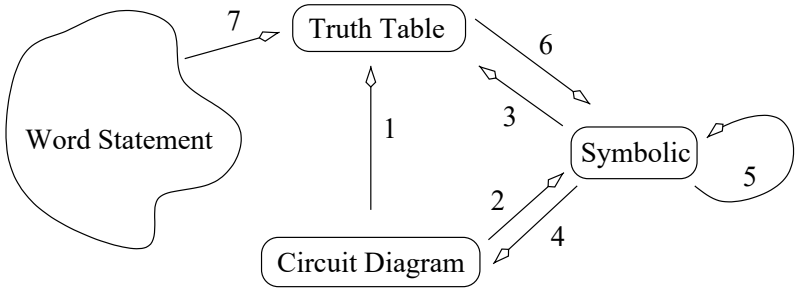
Representations of Logical Functions

2.1 Helpfull Stuff

A	B	A*B
0	0	0
0	1	0
1	0	0
1	1	1

A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

A	A'
0	1
1	0



	Regular Algebra	Boolean Algebra
Performed First	Parenthesis	Parenthesis
	Exponents	Not
	multiplication/division	And
Performed Last	addition/subtraction	Or

Axiom	Primary	Dual
1.	x+0=x	x*1=x
2.	x+1=1	x*0=0
3.	x+x=x	x*x=x
4.	x"=x	
5.	x+x'=1	x*x'=0
6.	x+y=y+x	x*y=y*x
7.	x+(y+z)=(x+y)+z	x*(y*z)=(x*y)*z
8.	x*(y+z)=x*y+x*z	x+(y*z)=(x+y)*(x+z)
9.	(x+y)'=x'*y'	(x*y)'=x'+y'

2.2 Definitions

Define each of the following. Some of the definitions should use terms you've defined.

Minterm

Maxterm

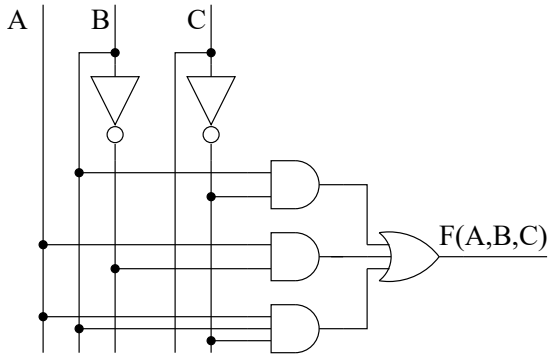
Minterm Trick

Expansion Trick

2.3 Problems

Solve the following problems in the space provided.

1. Given the circuit diagram below, produce the corresponding truth table.



A	B	C	F(A,B,C)
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

2. Given the symbolic expression below, produce the corresponding circuit diagram.

   F(A,B,C)=AB'+A(B'+C)

3. Given the symbolic expression below, produce the corresponding circuit diagram.

   F(A,B,C,D)=A(BC+A(C'+D)')' + B'CD'

4. Given the symbolic expression below, produce the corresponding truth table.

   F(A,B,C) = AB'+A(B'+C)

A	B	C			F(A,B,C)
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

5. Given the symbolic expression below, produce the corresponding truth table.

   F(A,B,C,D)=A(BC+A(C'+D)')' + B'CD'

A	B	C	D						F(A,B,C,D)
0	0	0	0						
0	0	0	1						
0	0	1	0						
0	0	1	1						
0	1	0	0						
0	1	0	1						
0	1	1	0						
0	1	1	1						
1	0	0	0						
1	0	0	1						
1	0	1	0						
1	0	1	1						
1	1	0	0						
1	1	0	1						
1	1	1	0						
1	1	1	1						

6. Given the truth table below, produce the corresponding symbolic expression.

A	B	C	F(A,B,C)	minterm	maxterm
0	0	0	0		
0	0	1	1		
0	1	0	1		
0	1	1	1		
1	0	0	1		
1	0	1	0		
1	1	0	0		
1	1	1	1		

7. Given the word state below, produce the corresponding truth table. Design a circuit with two 2-bit inputs called $A = a_1a_0$ and $B = b_1b_0$ The single bit output F should equal 1 when A+B > 6, otherwise F should equal 0.

a_1	a_0	b_1	b_0	A	B	$F(a_1, a_0, b_1, b_0)$
0	0	0	0			
0	0	0	1			
0	0	1	0			
0	0	1	1			
0	1	0	0			
0	1	0	1			
0	1	1	0			
0	1	1	1			
1	0	0	0			
1	0	0	1			
1	0	1	0			
1	0	1	1			
1	1	0	0			
1	1	0	1			
1	1	1	0			
1	1	1	1			

Chapter 3

Minimization of Logical Functions

Definitions

Simplification Trick

Problems

Simplify Utilize the simplification trick.

A	B	C	F	G	H
0	0	0	1	0	1
0	0	1	1	1	1
0	1	0	0	0	0
0	1	1	0	0	0
1	0	0	0	0	0
1	0	1	0	1	1
1	1	0	0	0	0
1	1	1	0	0	0

F(A,B,C)=
G(A,B,C)=
H(A,B,C)=

Kmap 3 variable Solve each kmap.

A	B	C	F	G	H	I	J	K	L	M
0	0	0	0	0	0	1	1	1	1	0
0	0	1	0	0	1	1	0	1	1	0
0	1	0	0	1	0	0	1	1	0	0
0	1	1	1	1	1	0	0	0	1	0
1	0	0	1	0	0	0	1	0	1	0
1	0	1	1	0	1	1	1	1	1	0
1	1	0	0	0	0	0	0	1	0	0
1	1	1	0	1	1	1	0	1	1	0

A \ BC	00	01	11	10
0				
1				

F

A \ BC	00	01	11	10
0				
1				

G

A \ BC	00	01	11	10
0				
1				

H

A \ BC	00	01	11	10
0				
1				

I

A \ BC	00	01	11	10
0				
1				

J

A \ BC	00	01	11	10
0				
1				

K

A \ BC	00	01	11	10
0				
1				

L

A \ BC	00	01	11	10
0				
1				

M

Minimize Determine the SOP $_{\min}$ for the following functions.

F(A,B,C)=A'BC' + A'BC + AB'C' + AB'C

G(A,B,C)=A'B' + AB'C' + AC

H(A,B,C)=B+AB'C + B'C'

I(A,B,C)=A(B+C')+A'B'C'

A \ BC	00	01	11	10
0				
1				

F

A \ BC	00	01	11	10
0				
1				

G

A \ BC	00	01	11	10
0				
1				

H

A \ BC	00	01	11	10
0				
1				

I

Minimize Determine the SOP $_{\min}$ realization

$F(A,B,C,D) = \sum m(0,1,4,5,8,9)$

$G(A,B,C,D) = \sum m(0,5,7,10,11,14,15)$

$H(A,B,C,D) = \sum m(0,2,3,5,6,7,8,10,11,14,15)$

$I(A,B,C,D) = \sum m(1,4,6,9,11,12,14,15)$

AB\CD	00	01	11	10
00				
01				
11				
10				

F

AB\CD	00	01	11	10
00				
01				
11				
10				

G

AB\CD	00	01	11	10
00				
01				
11				
10				

H

AB\CD	00	01	11	10
00				
01				
11				
10				

I

Minimize Determine the SOP $_{\min}$ for the following functions.

$F(A,B,C,D,E) = \sum m(0,1,2,5,7,8,10,15,16,18,23,24,26,28,29,31)$
$G(A,B,C,D,E) = \sum m(0,2,4,6,7,8,9,15,16,18,20,21,22,24,25,29)$

BC\DE	00	01	11	10
00				
01				
11				
10				

A=0

BC\DE	00	01	11	10
00				
01				
11				
10				

A=1

F(A,B,C,D,E)=

BC\DE	00	01	11	10
00				
01				
11				
10				

A=0

BC\DE	00	01	11	10
00				
01				
11				
10				

A=1

G(A,B,C,D,E)=

Minmize Determine the SOP $_{\min}$ reaization of the following functions.

$F(A,B,C,D) = \sum m(0,1,5,14,15) + \sum d(4,13)$
$G(A,B,C,D) = \sum m(0,6,7,9,10,12) + \sum d(2,4,8,13)$

AB\CD	00	01	11	10
00				
01				
11				
10				

F

AB\CD	00	01	11	10
00				
01				
11				
10				

G

Chapter 4

Combinational Logic Building Blocks

Helpfull Stuff

The following is a list of the devices covered in this chapter.

Nomenclature:	N:M decoder
Data Input:	1-bit D
Data Output:	M-bit vector $y = y_{M-1} \dots y_1 y_0$
Control:	N-bit vector $s = s_{N-1} \dots s_1 s_0$
Status:	none
Behavior:	$y_s = D$ all other outputs equal 0

Nomenclature:	N:1 multiplexer
Data Input:	M-bit vector $y = y_{M-1} \dots y_1 y_0$
Data Output:	1-bit F
Control:	$log_2(N)$-bit vector $s = s_{log_2(N)} \dots s_1 s_0$
Status:	none
Behavior:	$F = y_s$

Nomenclature:	N-bit adder subtractor
Data Input:	two N-bit vectors A and B
Data Output:	N-bit vector s
Control:	1-bit c
Status:	1-bit ovf
Behavior:	if c=0 then $s = A + B$ else $s = A - B$

Nomenclature:	N-bit comparator
Data Input:	two N-bit vectors X and Y
Data Output:	none
Control:	none
Status:	1-bit G, L, E
Behavior:	

cond	E	L	G
$X = Y$	1	0	0
$X < Y$	0	1	0
$X > Y$	0	0	1

Definitions

Data in

Control

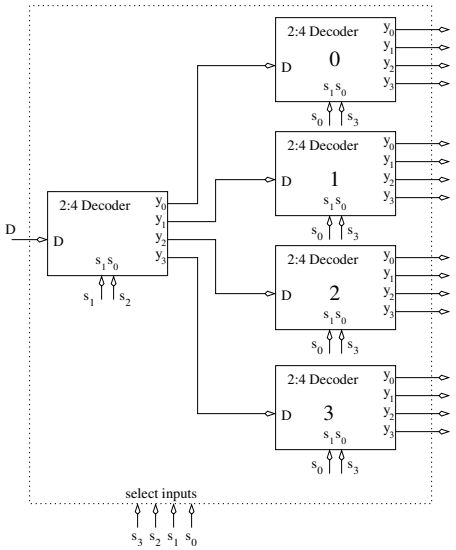
Data out

Status

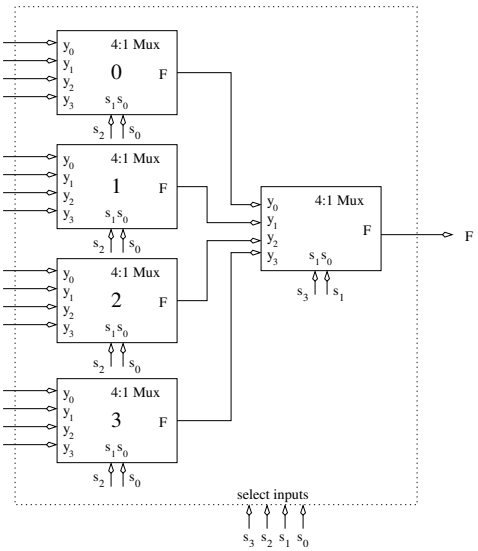
Problems

Here are a couple of problems to work on.

Label the outputs of the decoder.



Label the inputs of the mux.



Build the circuit. `if (Y<4) then X=2 else X=3`

Build the circuit. `if (Y>=4) then X=Y+2 else X=Y+3`

Build the circuit. `if (Y+1>15) then X=2 else X=3`