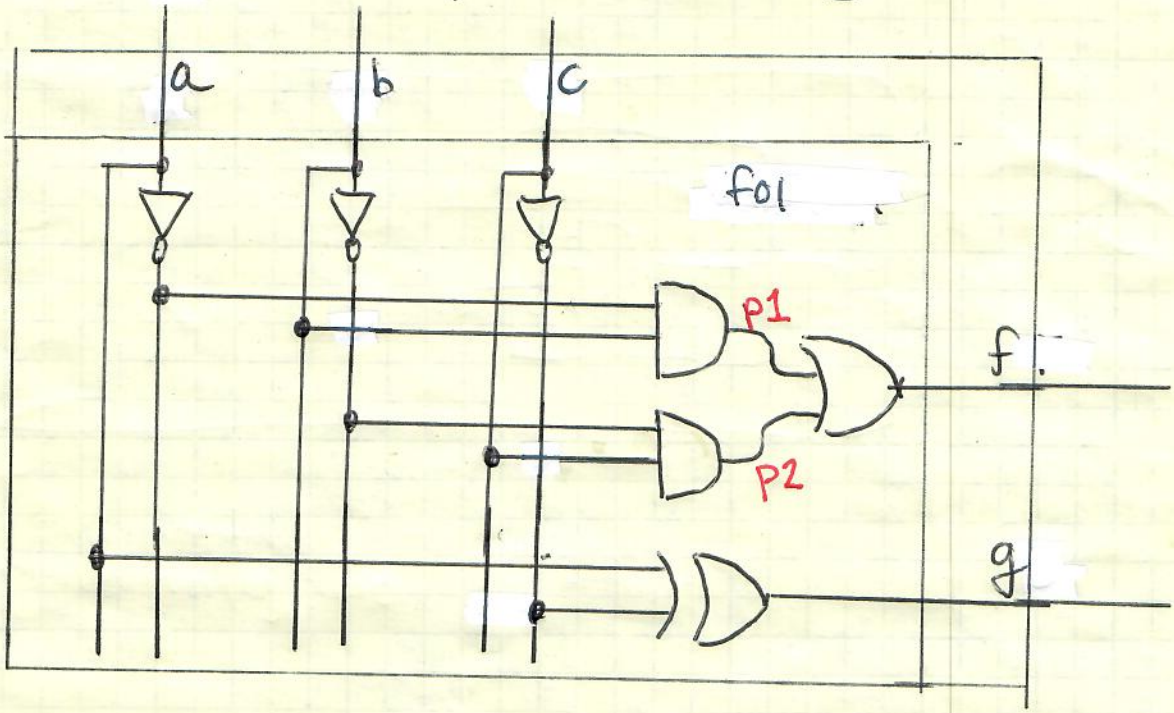
⑤ Circuit Diagram → Verilog



every input and output from module

```
module f01 (a, b, c, f, g);
    input wire a, b, c;
    output wire f, g;

    wire p1, p2;

    assign p1 = ~a & b;
    assign p2 = ~b & c;
    assign f = p1 | p2;
    assign g = a ^ ~c;

endmodule
```

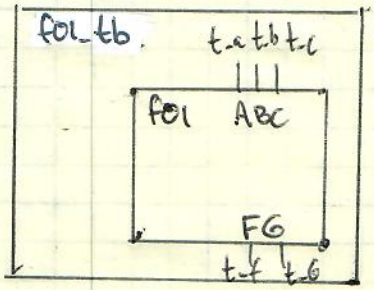
begins and ends inside module

Concurrent
Continous

Changing order will not change behavior

A wire should be on the LHS of exactly 1 assign

To check your Verilog code you will put it inside a testbench. A testbench is Verilog module constructed to apply inputs to a Verilog module called the unit under test (uut).

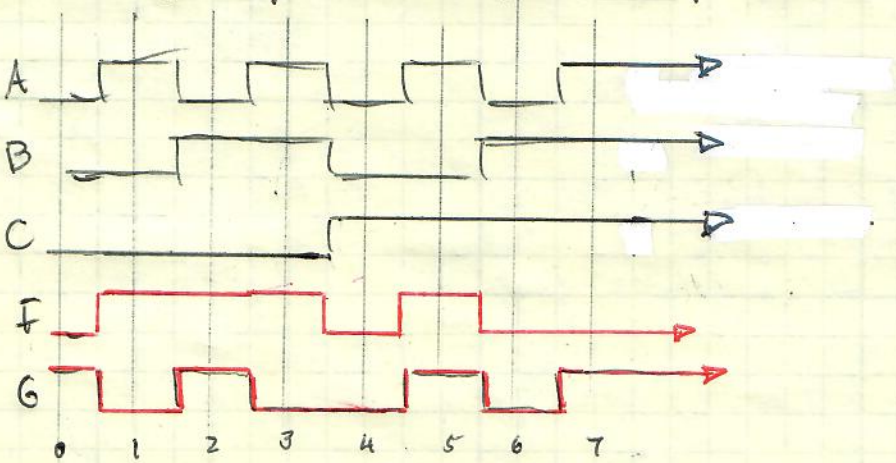


The testbench has 2 main parts

- module instantiation
- Stimulus vector definition

You the simulate the testbench to check your Verilog code.

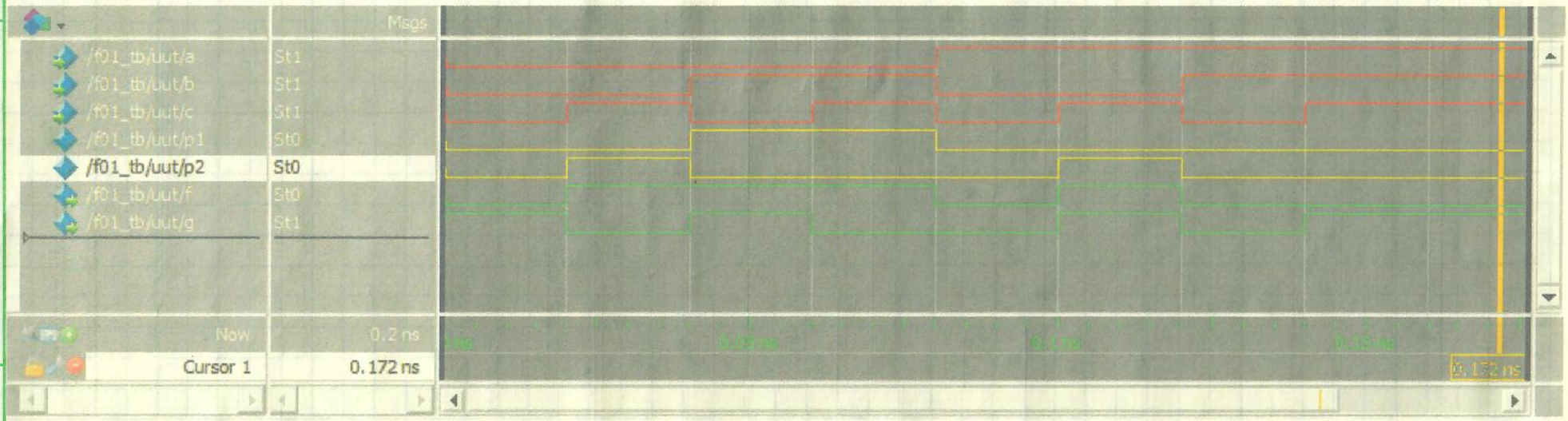
The simulation will generate a timing diagram
A timing diagram is a plot of logic level vs time



A	B	C	F	G
0	0	0	0	1
0	0	1	1	0
0	1	0	1	1
0	1	1	1	0
1	0	0	0	0
1	0	1	1	1
1	1	0	0	0
1	1	1	0	1

$F = a'b + b'c$

$G = a \oplus \sim c$


Msgs
/f01_tb/uut/a
/f01_tb/uut/b
/f01_tb/uut/c
/f01_tb/uut/p1
/f01_tb/uut/p2
/f01_tb/uut/f
/f01_tb/uut/g
St1
St1
St1
St0
St0
St0
St1
Now
0.2 ns
Cursor 1
0.172 ns