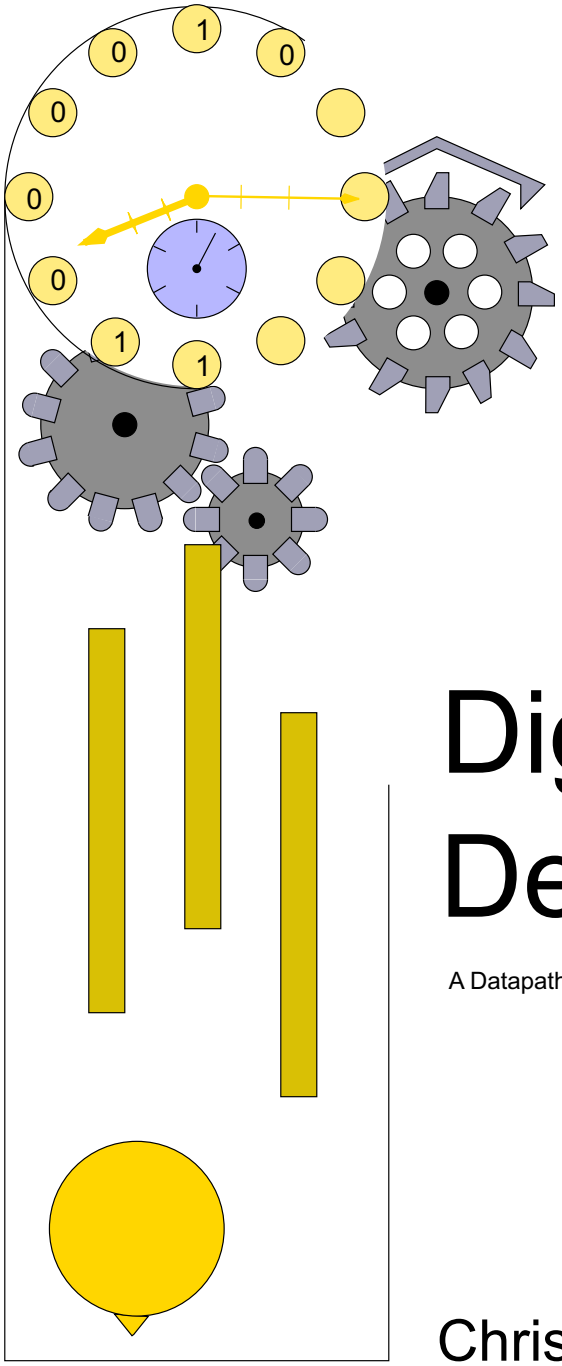


Digital Design

A Datapath and Control Approach

Chris Coulston

September 27, 2024

This document was prepared with LaTeX.

Contents

Chapter 1

Numbering Systems

1.1 Exercises

1. **(1 pt. each)** Syllabus:

   a) What is the late penalty for homework?
   There is a 33% deduction per day.

   b) True or False: Calculators can be used during exams.
   You cannot use calculators at my exams.

   c) True of False: University ID is required during exams.
   I check ID at the exams. After I learn your names its not such a big deal, but bring it to be safe.

   d) What is my thesis regarding grades?

   e) Bob L. Student has the following grades. Determine his final overall course percentage and grade.

Component	Percentage
Homework	60%
Exam 1	90%
Exam 2	80%
Final	70%

Component	*Percentage*	*Weight*
Homework	60%	*60*0.35 = 21*
Exam 1	90%	*90*0.20 = 18*
Exam 2	80%	*80*0.20 = 16*
Final	70%	*70*0.25 = 17.5*
Total	72.5%	*C*

   f) How should you prepare for the 43^{rd} lecture?
   Look over homework problem 8.10, page 165

2. **(1 pt. each)** Convert the following numbers to decimal. Show work, or receive 1/2 credit.

   a) 100_2 $100_2 = 2^2 = 4_{10}$

   b) 1000_2 $1000_2 = 2^3 = 8_{10}$

   c) 10000_2 $10000_2 = 2^4 = 16_{10}$

   d) 100000_2 $100000_2 = 2^5 = 32_{10}$

   e) 111111_2 $111111_2 = 2^5 + 2^4 + 2^3 + 2^2 + 2^1 + 2^0 = 63_{10}$

   f) 1000100101000101_2 $1000100101000101_2 = 2^{15} + 2^{11} + 2^8 + 2^6 + 2^5 + 2^0 = 35141_{10}$

   g) $3EA_{16}$ $3EA_{16} = 001111101010 = 2^9 + 2^8 + 2^7 + 2^6 + 2^5 + 2^3 + 2^1 = 1002_{10}$

3. **(1 pt. each)** Convert the following number to binary. Show work, or receive 1/2 credit.

   a) 44_{16} $44_{16} = 01000100_2$

   b) 44_{10} $44_{10} = 32 + 8 = 2^5 + 2^3 = 101100_2$

   c) 1023_{10} $1023_{10} = 512 + 256 + 128 + 64 + 32 + 16 + 8 + 4 + 2 + 1 = 2^9 + 2^8 + 2^7 + 2^6 + 2^5 + 2^4 + 2^3 + 2^2 + 2^1 + 2^0 = 1111111111_2$

4. **(1 pt. each)** Convert the following number to hex. Show work, or receive 1/2 credit.

   a) 101011101_2 $101011101_2 = 15D_{16}$

   b) 77_{10} $77_{10} = 64 + 8 + 4 + 1 = 2^6 + 2^3 + 2^2 + 2^0 = 1001101_2 = 4D_{16}$

5. **(2 pts. each)** Toughies:

   a) Convert 123_5 to base-12 $123_5 = 1 * 5^2 + 2 * 5^1 + 3 * 5^0 = 25 + 10 + 3 = 38_{10} = 3 * 12^1 + 2 * 12^0 = 32_{12}$

   b) Convert 789_{12} to base-5 $789_{12} = 7*12^2+8*12^1+9*12^0 = 1008+96+9 = 1113_{10} = 1 * 5^4 + 3 * 5^3 + 4 * 5^2 + 2 * 5^1 + 3 * 5^0 = 13423_5$

   c) What is the largest base-10 quantity that can be represented using 5 digits in base 12?

   $BBBBB_{12} = 11 * 12^4 + 11 * 12^3 + 11 * 12^2 + 11 * 12^1 + 11 * 12^0 = 248831_{10}$

6. **(1 pt. each)** Perform the following additions, assume a word size of four bits. Determine if overflow occurs.

   a) $0110_2 + 0101_2$ *0110 + 0101 = 1011*

   b) $0010_2 + 0110_2$ *0010 + 0110 = 1000*

   c) $0111_2 + 0011_2$ *0111 + 0011 = 1010*

   d) $0010_2 + 0101_2$ *0010 + 0101 = 0111*

   e) $0010_2 + 1010_2$ *0010 + 1010 = 1100*

   f) $0101_2 + 1011_2$ *0101 + 1011 = 10000 overflow*

   g) $0011_2 + 1001_2$ *0011 + 1001 = 1100*

Chapter 2

Representations of Logical Functions

2.1 Exercises

1. **(2 pts. each)** Given: $F(A,B,C,D) = (AB' + (C + (AD)')(BD))'$

   a) Determine the truth table for $F(A,B,C,D)$

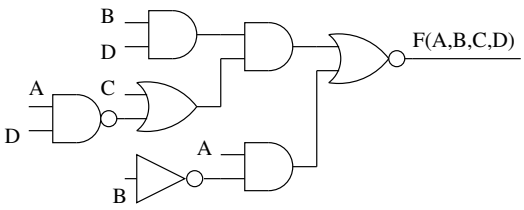
   Solution

   Let T3 = C+(AD)'
   T4 = BD
   *T1 = AB' T5 = T3 * T4*

A	*B*	*C*	*D*	*AB'*	*(AD)'*	*C+(AD)'*	*BD*	*T3*T4*	*T1+T5*	*F*
0	*0*	*0*	*0*	*0*	*1*	*1*	*0*	*0*	*0*	*1*
0	*0*	*0*	*1*	*0*	*1*	*1*	*0*	*0*	*0*	*1*
0	*0*	*1*	*0*	*0*	*1*	*1*	*0*	*0*	*0*	*1*
0	*0*	*1*	*1*	*0*	*1*	*1*	*0*	*0*	*0*	*1*
0	*1*	*0*	*0*	*0*	*1*	*1*	*0*	*0*	*0*	*1*
0	*1*	*0*	*1*	*0*	*1*	*1*	*1*	*1*	*1*	*0*
0	*1*	*1*	*0*	*0*	*1*	*1*	*0*	*0*	*0*	*1*
0	*1*	*1*	*1*	*0*	*1*	*1*	*1*	*1*	*1*	*0*
1	*0*	*0*	*0*	*1*	*1*	*1*	*0*	*0*	*1*	*0*
1	*0*	*0*	*1*	*1*	*0*	*0*	*0*	*0*	*1*	*0*
1	*0*	*1*	*0*	*1*	*1*	*1*	*0*	*0*	*1*	*0*
1	*0*	*1*	*1*	*1*	*0*	*1*	*0*	*0*	*1*	*0*
1	*1*	*0*	*0*	*0*	*1*	*1*	*0*	*0*	*0*	*1*
1	*1*	*0*	*1*	*0*	*0*	*0*	*1*	*0*	*0*	*1*
1	*1*	*1*	*0*	*0*	*1*	*1*	*0*	*0*	*0*	*1*
1	*1*	*1*	*1*	*0*	*0*	*1*	*1*	*1*	*1*	*0*

   b) Draw a schematic of the logic circuit which realizes F as shown, i.e. do not use Boolean Algebra on F.

   Solution



2. **(2 pts. each)** For the circuit in Figure 2.1

   a) Write a Boolean expression for the function.
   Solution *F(A,B,C,D) = (AB+C)D'+ABD'*

   b) Draw the truth table for the function.
   Solution

A	B	C	D	AB+C	(AB+C)D'	ABD'	F
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	1	0	0	1
0	0	1	1	1	1	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	1	0	0
1	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0
1	0	1	0	1	0	0	1
1	0	1	1	1	1	0	0
1	1	0	0	1	0	1	1
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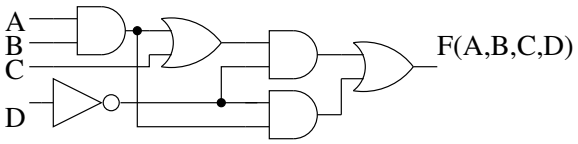


Figure 2.1: The circuit for Problems 2 and 3.

3. **(2 pts. each)** For the functions F,G,H,I defined by the truth table shown below:

   a) Determine the canonical SOP and POS realization for F, G, H, I.

   Solution

   F(A,B,C) = (A+B+C)(A+B'+C')(A'+B+C')(A'+B'+C) = A'B'C + A'BC' + AB'C' + ABC

   G(A,B,C) = (A'+B+C)(A'+B'+C') =
   A'B'C' + A'B'C + A'BC' + A'BC + AB'C + ABC'

   H(A,B,C) = (A+B'+C)(A+B'+C')(A'+B+C)(A'+B+C')(A'+B'+C') =
   A'B'C' + A'B'C + ABC'

   I(A,B,C) = (A+B+C)(A+B'+C)(A'+B+C)(A'+B'+C) =
   A'B'C + A'BC + AB'C + ABC

   b) Draw the circuit diagram for the canonical SOP and POS realization.

   Solution

Treat each output independently of the other. For example when working with function I, cover up the columns F, G and H.

A	B	C	F	G	H	I
0	0	0	0	1	1	0
0	0	1	1	1	1	1
0	1	0	1	1	0	0
0	1	1	0	1	0	1
1	0	0	1	0	0	0
1	0	1	0	1	0	1
1	1	0	0	1	1	0
1	1	1	1	0	0	1

4. **(2 pts. each)** Prove the validity of the following statements using the laws of Boolean Algebra. For each step of the proof, identify which law was used.

   a) $X'Y' + XY + X'Y = X' + Y$

   Solution

   X'Y' + XY + X'Y = *3D*
   X'Y' + X'Y + XY+ X'Y = *8*
   X'(Y' + Y)+ Y(X+ X')Y= *5*
   X' + Y *QED*

   b) $(X + Y')X'Y' = X'Y'$

   Solution

   (X+Y')X'Y' = *8*
   XX'Y + X'Y'Y' = *5D*
   0+X'Y'= *1*
   X'Y' *QED*

   c) $(X + Y)(X' + Z) = XZ + X'Y$

   Solution

   (X+Y)(X'+Z) = *8*
   (X+Y)X' + (X+Y)Z = *8*
   XX' + YX' + XZ + YZ = *1D,5*
   YX' + XZ + YZ(X+X') = *8*
   YX' + XZ + XYZ + X'YZ = *6*
   X'Y + X'YZ + XZ + XYZ = *1D, 8*
   X'Y(1+Z) + XZ(1+Y) = *2, 1D*
   X'Y + XZ *QED*

   d) $X'Y' + (X + Y)Z = X'Y' + Z$

   Solution

   X'Y' + (X+Y)Z = *8*
   X'Y' + XZ + YZ = *1D,5*
   X'Y'(Z+Z') + XZ + YZ(X+X') =* *8*
   X'Y'Z' + X'Y'Z + XZ + XYZ + X'YZ = *3*
   X'Y'Z' + X'Y'Z + X'Y'Z + XZ + XYZ + X'YZ = *8*
   X'Y'(Z+Z') + XZ(1+Y) + X'Z(Y'+Y) = *5,1D*
   X'Y' + XZ + X'Z = *8*
   X'Y' + Z(X+X') = *5, 1D*
   X'Y' + Z *QED*

e) $A'C + BC + AB = A'C + AB$

Solution

A'C + BC+AB =	*1D, 5*
A'C + (A+A')BC + AB(C+C')	*8*
A'C + ABC + A'BC + ABC + ABC'=	*3*
A'C + A'BC + ABC + ABC'=	*8*
A'C(1+B) + AB(C+C')=	*5, 1D*
A'C + AB	*QED*

f) $A(B + C) = AB + AB'C$

Solution

AB+AB'C=	*1D,5*
AB(C+C') + AB'C=	*8*
ABC+ABC'+AB'C=	*3*
ABC + ABC + ABC' + AB'C=	*6*
ABC + ABC' + ABC + AB'C=	*8*
AB(C+C'+C) + AB'C =	*8*
AB + AB'C=	*QED*

g) $(A + B + C)(A + B + C')(A' + B + C')(A' + B' + C') = (A + B)(A' + C')$

Solution

(A+B+C)(A+B+C')(A'B+C')(A'+B'+C')=	*4*
((A+B+C)(A+B+C')(A'B+C')(A'+B'+C'))"=	*9D*
(A'B'C + A'B'C' + AB'C + ABC)'=	*8*
(A'B'(C+C') + AC(B'+B))'=	*5, 1D*
(A'B' + AC)'=	*9*
(A+B)(A'+C')=	*QED*

5. **(4 pts.)** Design a circuit called MUX2. MUX2 has three bits of input S, y_0, y_1 and one bit of output F. If $S = 0$, then $F = y_0$; else if $S = 1$, then $F = y_1$.

a) Write down the truth table for the MUX2 function.

Solution

S	*y0*	*y1*	*F*
0	*0*	*0*	*0*
0	*0*	*1*	*0*
0	*1*	*0*	*1*
0	*1*	*1*	*1*
1	*0*	*0*	*0*
1	*0*	*1*	*1*
1	*1*	*0*	*0*
1	*1*	*1*	*1*

b) Determine the canonical SOP realization for MUX2; do not simplify.

Solution *F = S'y0y1' + S'y0y1 + Sy0'y1 + Sy0y1*

6. **(6 pts.)** Design a circuit called MUX4. MUX4 has six bits of input $S_1S_0, y_0, y_1, y_2, y_3$ and one bit of output F.
If $S_1S_0 = 00$ then $F = y_0$
else if $S_1S_0 = 01$ then $F = y_1$
else if $S_1S_0 = 10$ then $F = y_2$

else if $S_1S_0 = 11$ then $F = y_3$
Without writing down the truth table determine a SOP expression to realize F by listing all possible inputs which will cause F to equal 1. Then try to simplify your expression using Boolean Algebra.

Solution

The output F only equals one in the following cases.

S1=0 S0=0 and y0=1

S1=0 S0=1 and y1=1

S1=1 S0=0 and y2=1

S1=1 S0=1 and y3=1

With this information we can form four product terms, one for each input, that equal 1 only for that input. ORing together these product terms will give us the solution to the problem.

$F = S_1'S_0'y_0 + S_1'S_0y_1 + S_1S_0'y_2 + S_1S_0y_3$

7. **(4 pts.)** Design a logic circuit called MAJ which has three inputs A, B, C and one output Z. The output equals 1 when a majority of the inputs are equal to 1, otherwise the output is 0.

   a) Write the truth table for the MAJ function.

   Solution

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

   b) Determine the canonical SOP realization for the MAJ function, do not simplify.

   Solution *F = A'BC + AB'C+ABC'+ABC*

8. **(4 pts.)** Let X and Y each be 2-bit signals whose elements are x_1x_0 and y_1y_0 respectively. Determine the $\sum m$ and $\prod M$ expression for a circuit whose 1-bit output z is defined by the following statement.

```
if (X == Y) then z = 1 else z =0
```

Solution

a_1	a_0	b_1	b_0	A	B	z
0	0	0	0	0	0	1
0	0	0	1	0	1	0
0	0	1	0	0	2	0
0	0	1	1	0	3	0
0	1	0	0	1	0	0
0	1	0	1	1	1	1
0	1	1	0	1	2	0
0	1	1	1	1	3	0
1	0	0	0	2	0	0
1	0	0	1	2	1	0
1	0	1	0	2	2	1
1	0	1	1	2	3	0
1	1	0	0	3	0	1
1	1	0	1	3	1	0
1	1	1	0	3	2	0
1	1	1	1	3	3	1

Yielding

$z = \sum m(0, 5, 10, 15) = \prod M(1, 2, 3, 4, 6, 7, 8, 9, 11, 12, 13, 14)$

9. **(4 pts.)** Let X and Y each be 2-bit signals whose elements are x_1x_0 and y_1y_0, respectively. Determine the $\sum m$ and $\prod M$ expressions for a circuit whose 1-bit output z is defined by the following statement.

```
if (X + Y > 3) then z = 0 else z =1
```

Solution

a_1	a_0	b_1	b_0	A	B	z
0	0	0	0	0	0	1
0	0	0	1	0	1	1
0	0	1	0	0	2	1
0	0	1	1	0	3	1
0	1	0	0	1	0	1
0	1	0	1	1	1	1
0	1	1	0	1	2	1
0	1	1	1	1	3	0
1	0	0	0	2	0	1
1	0	0	1	2	1	1
1	0	1	0	2	2	0
1	0	1	1	2	3	0
1	1	0	0	3	0	1
1	1	0	1	3	1	0
1	1	1	0	3	2	0
1	1	1	1	3	3	0

Leading to the answer $z = \sum m(0, 1, 2, 3.4, 5, 6, 8, 12) = \prod M(7, 9, 10, 11, 13, 14, 15)$

10. **(3 pts.)** Determine the canonical SOP and POS expression for $F(A, B, C) = \prod M(0, 1, 4, 5)$ Hint, compose the truth table for F.

    Solution

    F(A,B,C)=A'BC' + A'BC +ABC' +ABC
    F(A,B,C)=(A+B+C)(A+B+C')(A'+B+C)(A'+B+C')

11. **(3 pts.)** Determine the canonical SOP and POS expression for $F(A, B, C, D) = \sum m(0, 4, 12, 15)$ Hint, write out the truth table for F.

    Solution

    F(A,B,C)=A'B'C'D' + A'BC'D' + ABC'D' + ABCD
    F(A,B,C)=(A+B+C+D')(A+B+C'+D)(A+B+C'+D') (A+B'+C+D')(A+B'+C'+D)
    (A+B'+C'+D')(A'+B+C+D)(A'+B+C+D') (A'+B+C'+D)(A'+B+C'+D')(A'+B'+C+D')
    (A'+B'+C'+D)

12. **(4 pts.)** For the function $F(A, B, C) = BC + AB'C'$, draw a timing diagram for an input sequence that follows the same order as the rows of the truth table. Assume a propagation delay for NOT, AND and OR gate are all 10nS.

    Solution *skipped for now*

13. **(4 pts.)** Complete the timing diagram in Figure 2.2 for the functions $F(A, B, C) = AB' + BC + ABC'$ and $G(A, B, C) = (A + B')C + (BC')'$

    Solution

14. **(16 pts.)** Design a circuit to control the water pump of a washing machine. The pump will not pump water if

    The lid is closed and the cycle is not fill

    The cycle is fill and the detergent level is empty

    The detergent is not empty and the lid is open

    The variables for this problem are:

    L = lid is closed

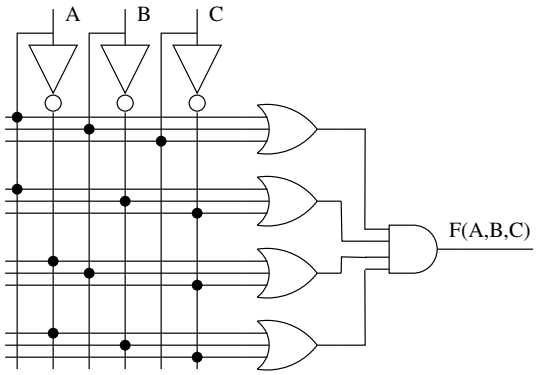
    C = cycle is fill

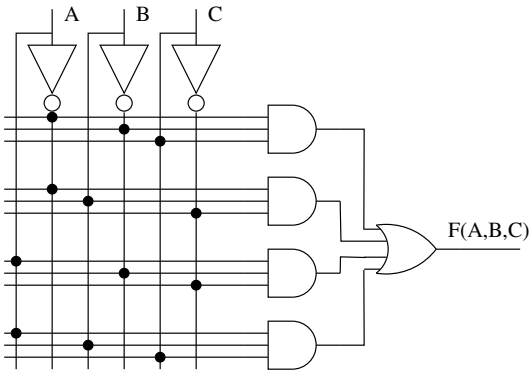
    D = detergent is empty

    P = pump will pump water

    Create a truth table which describes when the pump will not pump water. Call this output P'. Determine the canonical SOP expression for P'. Use this canonical SOP expression to generate a circuit diagram for P. This can be done by inserting an inverter onto the output of the circuit.

    Take the P' column from truth table and invert all the entries to generate a new output column called P (because the negation of P' is P). Determine the canonical SOP realization for P using this new column.


A
B
C
F(A,B,C)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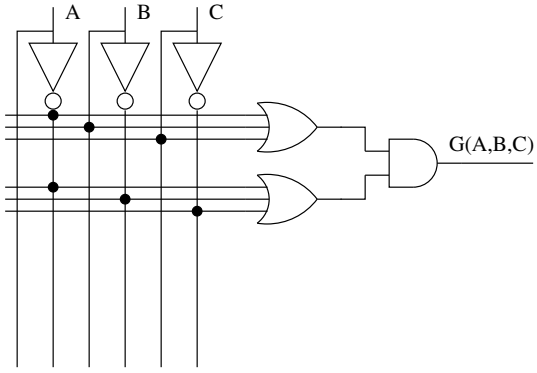
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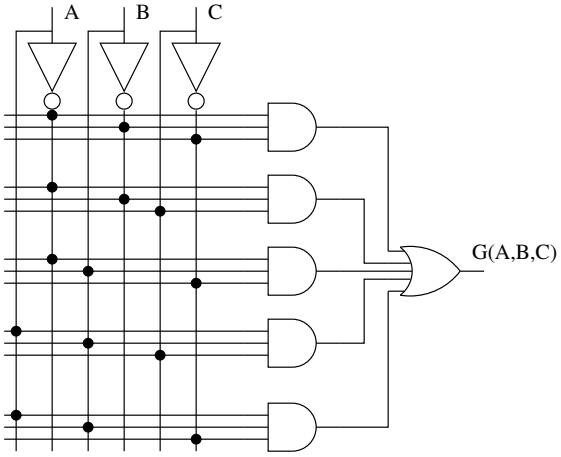
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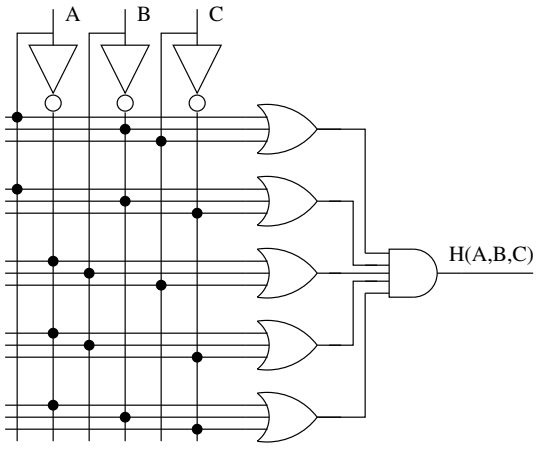
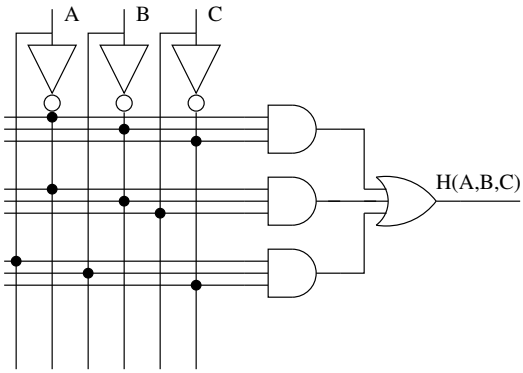
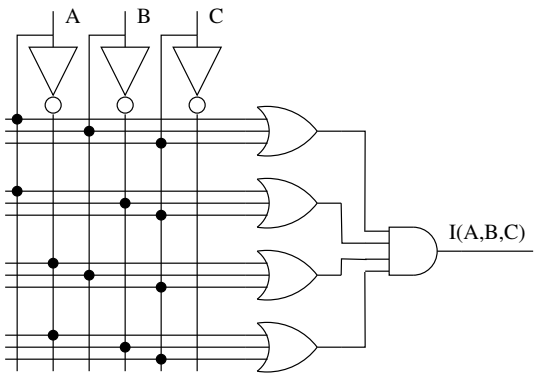
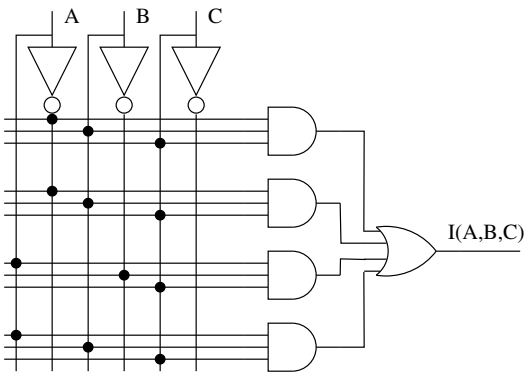

A
B
C
H(A,B,C)


A
B
C
H(A,B,C)


A
B
C
I(A,B,C)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B
C
I(A,B,C)

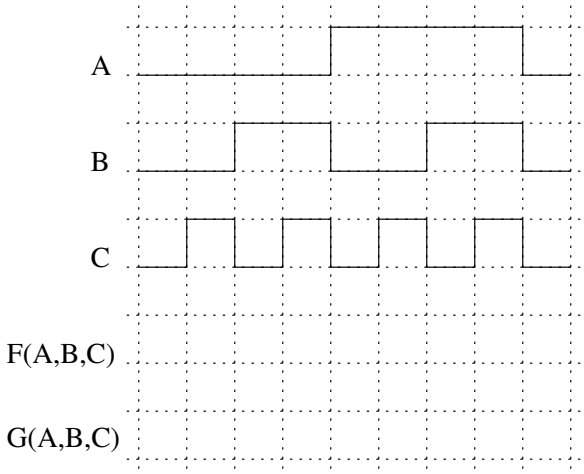

Figure 2.2: The timing diagram for two functions, F and G.