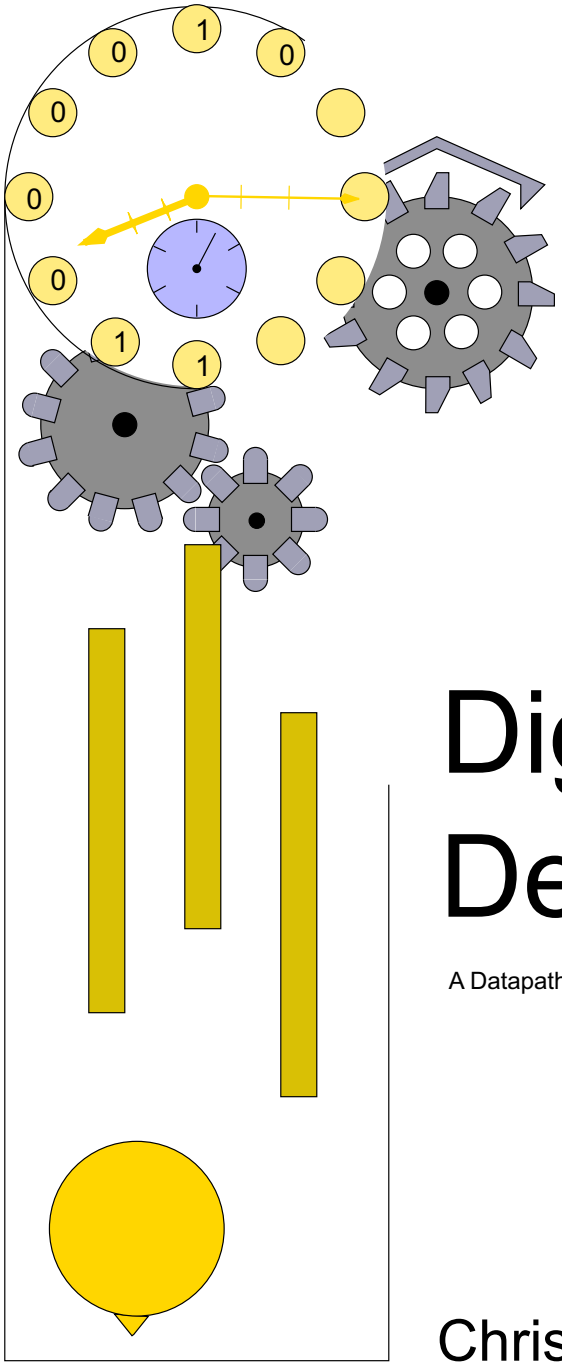

Digital Design

A Datapath and Control Approach

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This document was prepared with LaTeX.

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List of Processes

List of Basic Building Blocks

Chapter 0

Why?

Welcome to Introduction to Digital Design - A Datapath and Control Approach. You might be tempted to ask "Why bother writing yet another digital design text?" The assumption being that this text is going to cover the same ground as a typical digital design text. And yes, to some degree it will, but more importantly it will not. *This text presents a systematic approach to the design process for digital circuits that will enable you to design sophisticated digital systems.* I consider a digital design sophisticated when it needs to be described algorithmically.

After going through this text and laboratories the goal is for you to be able to use all of the material you learned to design a digital systems that in Figure 0.1.

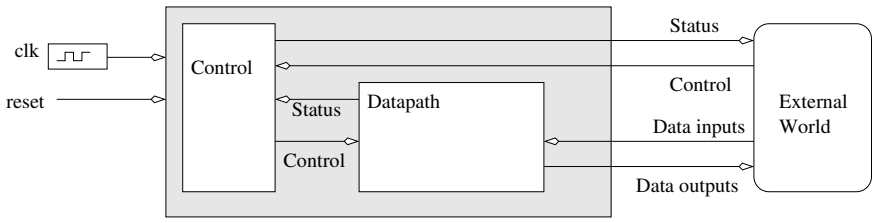

Figure 0.1: An abstract digital system constructed from a datapath and a control unit.

The datapath and control framework classifies the inputs and outputs of every digital logic building block as either **Data inputs**, **Data output**, **Control inputs**, **Status output** (the two special signals, **clk** and **reset** sit outside this classification). Under this framework, the datapath performs all data manipulations and the control unit sequences the control inputs for datapath. The datapath is built from combinational and sequential building blocks like multiplexers and counters. The control unit is a finite state machine.

Class Organization

The text, homework and laboratory are intended for a 4-credit course. The example timeline shown in Table 0.1 assumes 3 50-minute lectures per week and one 2 or 3 hour laboratory a week.

Laboratory

While it is expected that students finish the laboratory during the scheduled time, frequently students will need additional time to complete work, so accommodations need to be in-place for them to access the hardware and software outside of course hours. I expect that my students will need to work about 4-hours a week outside of class.

0.1 Example Timeline

Table 0.1: The labs in this example timeline are shown the earliest possible to insure that the prerequisite skills have been covered or 3 lecture sessions have passed since the last lecture.

Session	Topic	Assignment	Reading
1	Course Intro, Binary numbering, Hexadecimal	1.1 – 1.3	
2	Binary Addition	1.4	
3	Logic gates / Circuit to Symbolic / Circuit to Truth Table	2.1, 2.21, 2.2.2	
4	Symbolic to Truth Table / Symbolic to Circuit	2.2.3, 2.2.4	
5	Symbolic to Verilog	Supplemental	
Lab #1	Introduction to CAD tools and Verilog		
6	Symbolic to Symbolic	2.2.5	
7	Symbolic to Symbolic	2.2.5	
8	Truth Table to Symbolic SOP and POS	2.2.6, 2.2.7, 2.3	
Lab #2	Hexadecimal to 7-segment Converter		
9	Karnaugh Maps, 3 variables	3.1	
10	Combinational Logic with Verilog	Supplemental	
11	Karnaugh Maps, 4 and 5 variables	3.2, 3.3	
Lab #3	Rock Paper Scissors		
12	Don't cares	3.5	
13	SOP and POS in Karnaugh maps		
14	Exam Review	3.6	
Lab #4	Guessing Game		
15	Exam I		
16	Decoder / Multiplexers	4.1, 4.2	
17	2's complement	1.5	
18	Adders	4.3	
19	Adder Subtractor	4.4	
Lab #5	Guessing Game with Hints		
20	Comparator	4.5	
21	Wire Logic / Combinations	4.7, 4.8	
22	SR Latch e	5.5	
23	Basic memory elements – timing	5.1	
24	Basic memory elements – practical considerations	5.7	
Lab #6	Decimal Calculator		
25	Register	6.1	
26	Shift Registers	6.2	

Session	Topic	Reading	
27	Counter	6.3	
Lab #7	1 Dimensional Cellular Automata	6.3	
28	RAM	6.4	
29	Register Transfer	6.5	
30	Exam Review	Supplemental	
Lab #8	Mod 10 Counter		
31	Exam II		
32	Sequential Design – Traffic Light Controller	7.4	
33	Sequential Design – Verilog	Supplemental	
Lab #9	Stopwatch Datapath		
34	Sequential Design – Timing	7.6	
35	Sequential Design – Vending Machine	7.5	
Lab#10	Stopwatch Control		
36	Datapath and Control Theory	8.1, 8.2, 8.3	
37	Datapath and Control Theory	8.1, 8.2, 8.3	
38	Datapath and Control Practice	8.4, 8.5	
Lab#11	Stopwatch – Datapath and Control		
39	Datapath and Control Practice	8.4, 8.5	
40	Datapath and Control Timing	8.4, 8.5	
41	Datapath and Control Practice	8.7	
	Lab wrap-up		
42	Exam Review	Supplemental	
	Exam III		

Contributing to this work

An important feature of this text is the ability for others to contribute to its ongoing improvement. At present the text lacks HDL material and would benefit from a unit on FPGA architectures. There are countless ways that you can improve this text. If you are interested in contributing, reach out to coulston@mines.edu and I can arrange to make a branch of the text repository. I'd enjoy working with others and sharing perspectives.

Appendix A

74LS00 Data Sheets

Since the device documentation for the TI chips is covered by TI's copyright it was decided to leave these pages out of this text. The documents discussed in the text can be found onilne at:
http://focus.ti.com/lit/ds/symlink/sn74ls00.pdf