$D_{S25} = Q_{LR} \cdot timer$

$D_{L6} = Q_{L6} \cdot timer' + Q_{S25}$

$D_{S5} = Q_{L6} \cdot timer$

$D_{LY} = Q_{LY} \cdot timer' + Q_{S5}$

$D_{S30} = Q_{LY} \cdot timer$

$Z_{RED} = Q_{LR} + Q_{S25}$

$Z_{YELLOW} = Q_{LY} + Q_{S30}$

$Z_{Green} = Q_{L6} + Q_{S5}$

$Z_{C2} = Q_{S30}$

$Z_{C1} = Q_{S5}$

$Z_{C0} = Q_{25}$

Verilog

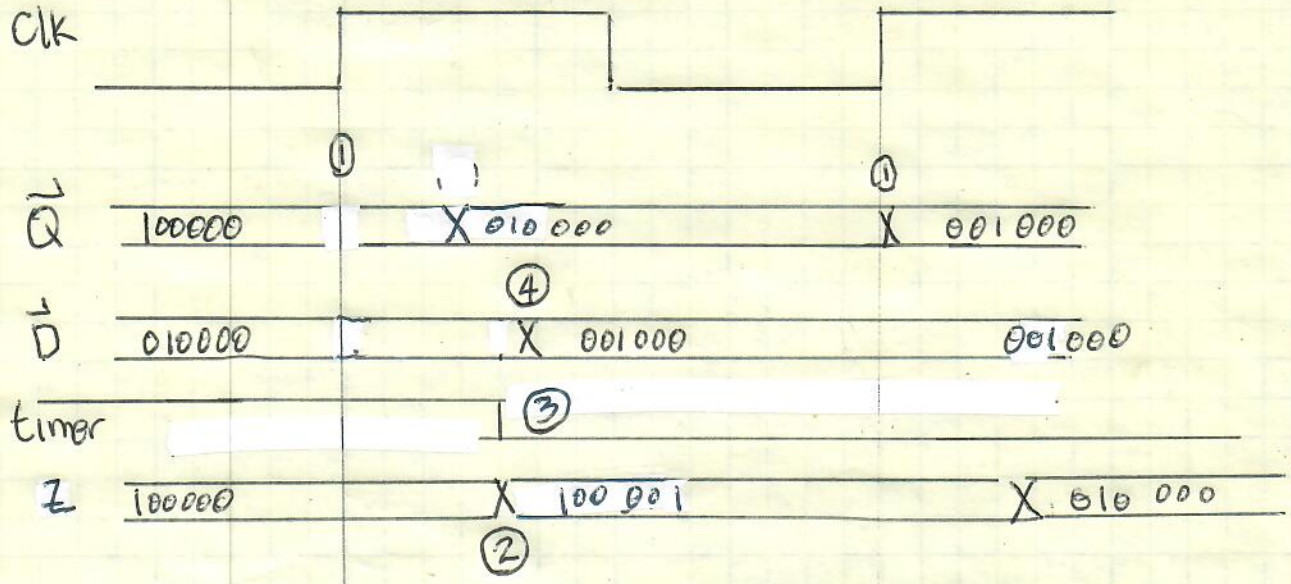
```
module trafficLight Controller (clk, reset, cw, sw)
  :
// Next state logic - MIE
always @(state)
begin
  case (state)

    LGT_RED:
    begin
        if (timer = 1'b1)  nextstate = SET_25;
        else               nextstate = LGT_RED;
    end

    SET_25:                nextstate = LGT_GREEN;
      :
    default:               nextstate = LGT_RED;
```

Timing in a FSM

Apply inputs observe outputs

On circuit
On state diagram

Start @ positive edge of clk



State	LR	S25	LG
next state	S25	LG	LG

Minimum Period $T_p(FF) + T(combo) + T_{so}(FF)$