Shift register

Before going into the mechanics of shift registers behavior & construction, let's consider why shifting bits is useful.

Given $\vec{X} = X_3 X_2 X_1 X_0$

The value of $\vec{x}$ (interpreted as binary number)

$value(\vec{x}) = X_3 2^3 + X_2 2^2 + X_1 2^1 + X_0 2^0$

Shift $\vec{X}$ left by 1 bit $X_3 X_2 X_1 X_0 0$

Find: $value(\vec{x} << 1) = X_3 2^4 + X_2 2^3 + X_1 2^2 + X_0 2^1$

$= 2(X_3 2^3 + X_2 2^2 + X_1 2^1 + X_0 2^0)$

$= 2\vec{x}$

Summary: Shift $\vec{x}$ left multiplies interpretation by 2
Shift $\vec{x}$ right divides interpretation by 2

Types of Shifts

Given $\vec{x} = X_3 X_2 X_1 X_0$

	Left	Right
Logical	$X_2 X_1 X_0 0$	$0 X_3 X_2 X_1$
Arithmetic	$X_2 X_1 X_0 0$	$X_3 X_3 X_2 X_1$
Circular	$X_2 X_1 X_0 X_3$	$X_0 X_3 X_2 X_1$

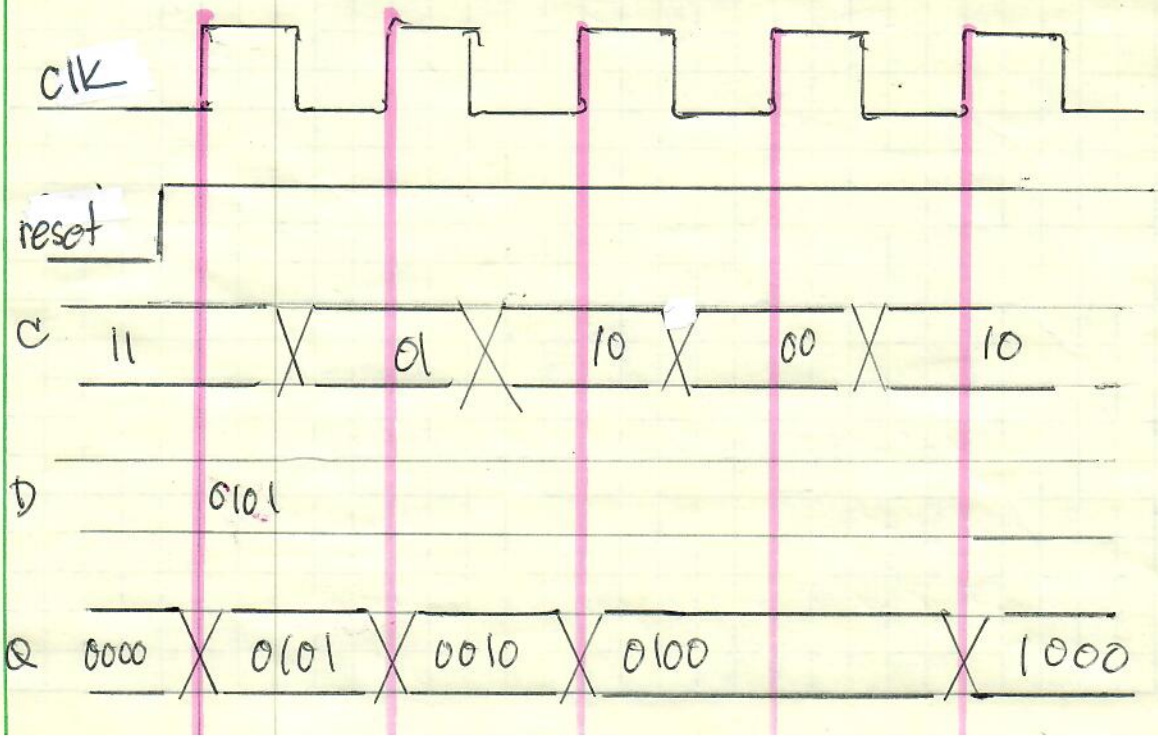
logical shift

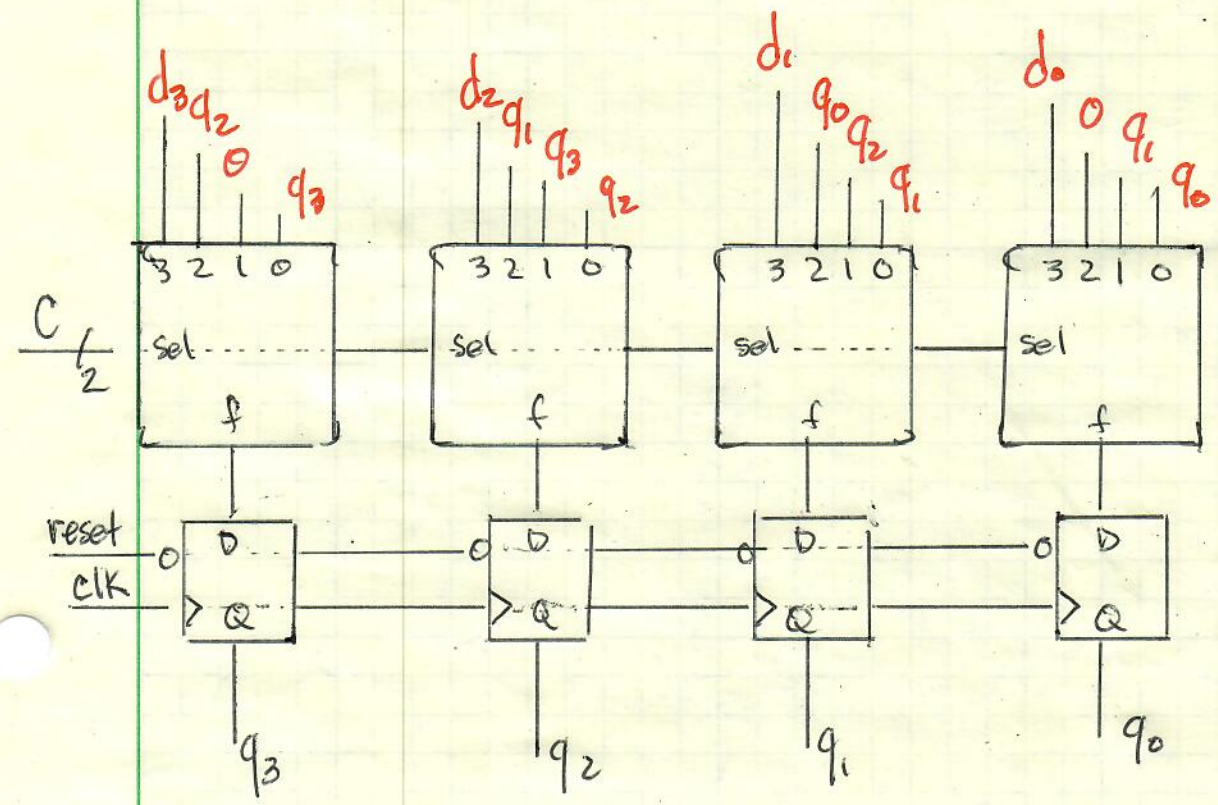
N-bit register w/ parallel load

Data in	N-bit vector $\vec{D} = d_{N-1} \cdots d_1 d_0$
Data out	N-bit vector $\vec{Q} = q_{N-1} \cdots q_1 q_0$
Control	2-bit $\vec{C} = c_1 c_0$
Status	None
Behavior	

reset	clk	C	D	Q^+	Note
0	x	x	x	$\vec{0}$	Reset
1	0, 1, ↓	x	x	Q	
1	↑	00	x	Q	Hold
1	↑	01	x	Q>>1	Right
1	↑	10	x	Q<<1	Left
1	↑	11	D	D	Load

4-bit




d_3 q_2 0 q_3
d_2 q_1 q_3 q_2
d_1 q_0 q_2 q_1
d_0 0 q_1 q_0
3 2 1 0
sel
f
C
$\frac{f}{2}$
reset
clk
D
Q
q_3
q_2
q_1
q_0