Digital Design Numbering Systems Positional Numbering Systems Base 10 - Decimal Base 2 - Binary Base 16 - Hexadecimal Between Bases Word Size 2's Complement Representation of Logical Function Elementary Logical Functions Analyzing a word statement for a logic function Creating a truth table description for a logic function Creating a symbolic form for a logic function Creating a circuit diagram for a logic function Creating Hardware Description Language statements for a logic function Conversion between two different representations of a logic function Describing a functions with multiple outputs Timing Diagrams Logic Minimization Karnaugh Maps (Kmaps) Kmaps for circuits with multiple outputs Kmaps to find POSmin Using logic minimization software to describe a logic function Combination Logic Building Blocks Decoder Multiplexers Adders Comparators Wire Logic Designing glue logic to interface building blocks Analyzing a circuit with a combination of building blocks Arithmetic Statements Conditional Statements Basic Memory Element Behavior Characteristics Timing of basic memory element Asynchronous set reset Sequential Logic Building Blocks Analysis, design and use of a register in a digital design Shift Register Counter Static RAM Design a circuit that performs register transfer Finite State Machines Hardware organization of a finite state machine State diagram for a finite state machine One's Hot Encoding Design Using a timing diagram to specify or verify the proper operation of a Finite State Machine Datapath and Control Datapath and Control Architecture Algorithmic Language Design a control word table and spcify the control word values for every state. Design Using a timing for a datapath and control circuit to specify or verify proper operation..

Verilog Writing concurrent signal assignment statements for a logic function Writing a Verilog statement using primitive logic operations Writing a Verilog statement using an Always/Case statement Writing a Verilog statement using an Always/CaseZ statement Creating a Verilog statement that uses vectors Analyzing and designing a Verilog testbench Definition and instantiation of Verilog generic modules Definition of Verilog modules Instantiation of Verilog Modules Definition of Finite State Machines in Verilog Hardware and Software Specifics Creating a simulation timing diagram for a module Creating a pin assignment for a module Creating a Do file to automate waveform setup Synthesizing a module on the FPGA development board