* When analyzing combinations of sequential & combinational logic

① Look at reset signal & reset output of any sequential element to $\vec{0}$.

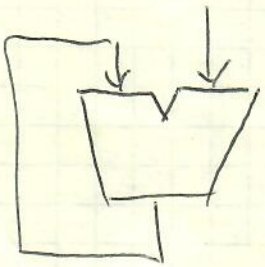
② After clk ↑ edge allow sequential element outputs to propagate through combinational elements. Stop @ sequential inputs.

③ At clk ↑ edge allow sequential devices to update their state.

⓪ Identify combinational & sequential elements

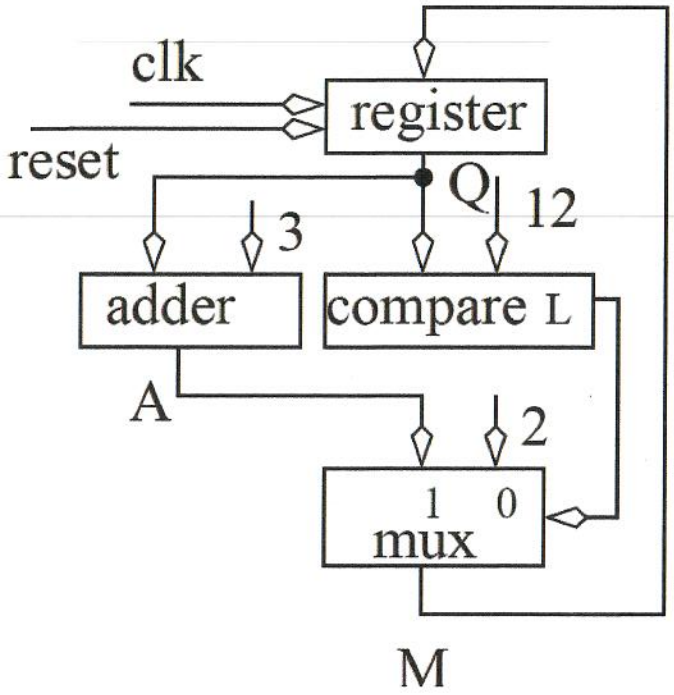
I'll never give you combinational logic circuits that have unpredictable outputs.

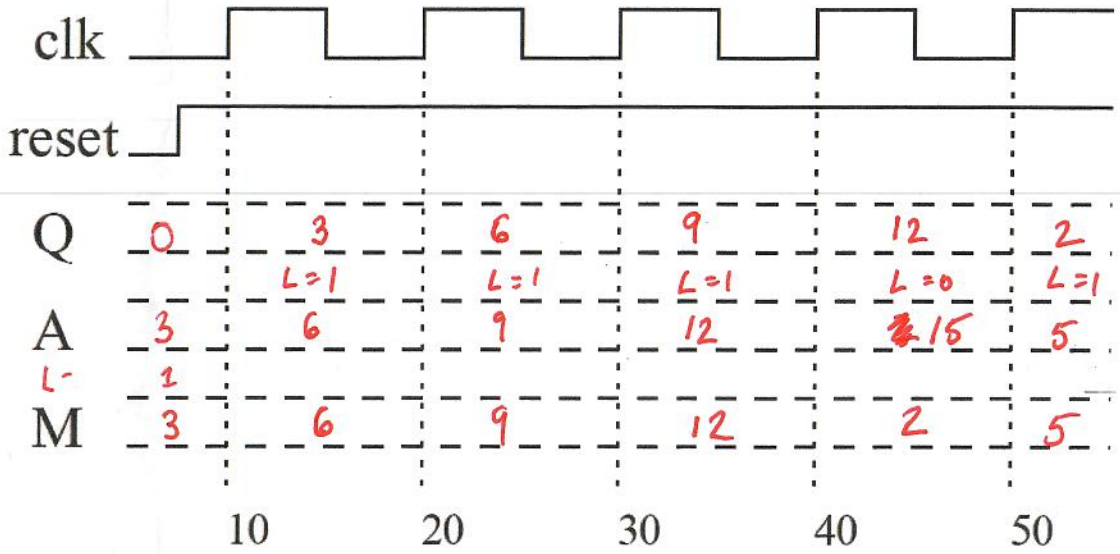
Eg. of a race



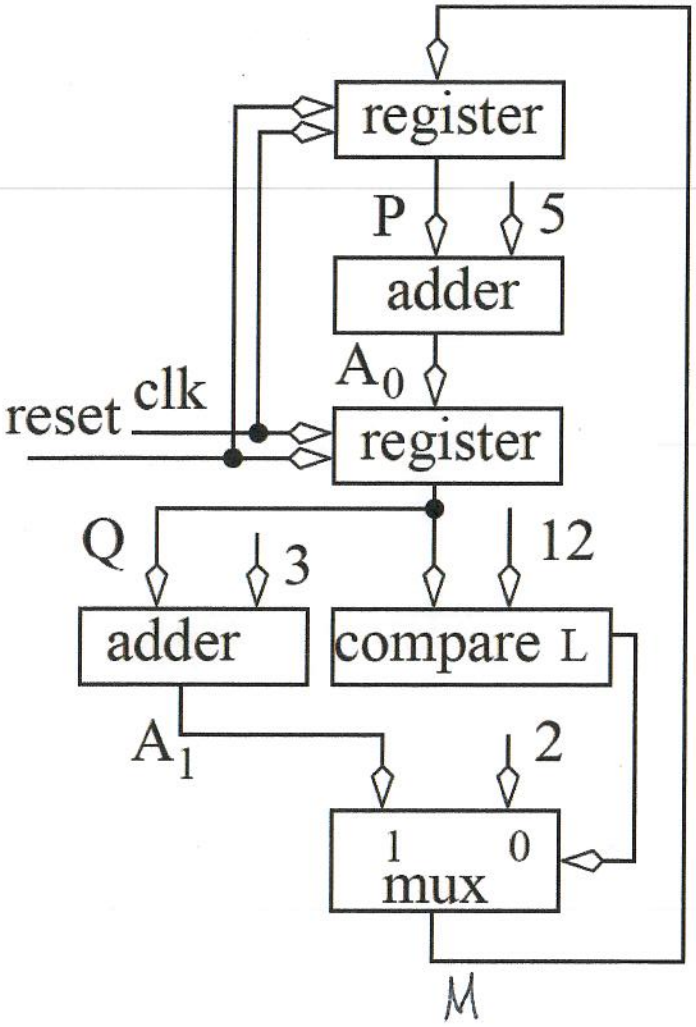
Do timing diagrams from workbook or a handout

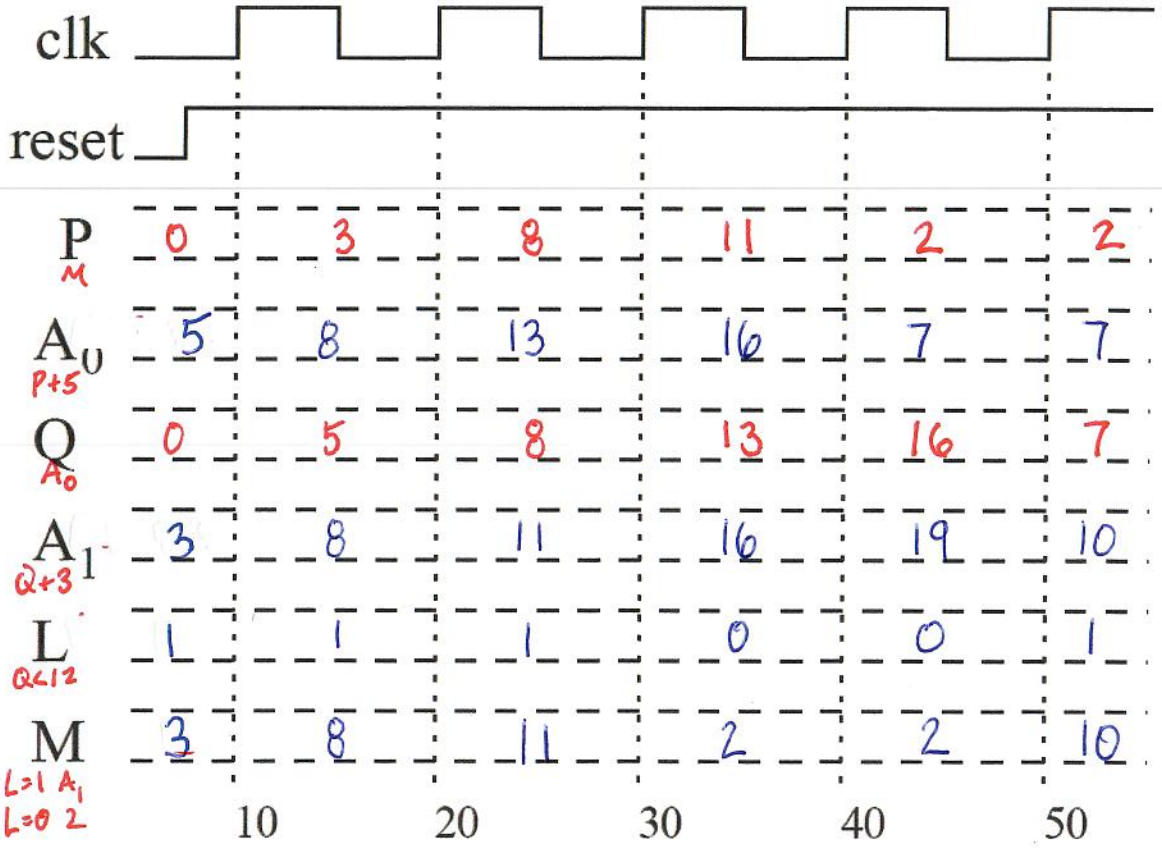
Example #1


clk
register
reset
Q
12
3
adder
compare L
A
2
1 0
mux
M


clk
reset
Q
A
L
M
0
3
6
9
12
2
L=1
L=1
L=1
L=0
L=1
3
6
9
12
15
5
1
3
6
9
12
2
5
10
20
30
40
50

Example #2





Red register

Blue combinational