EENG 284 – Spring 2024
Exam 2

Name: Key CWID:

Clearly circle your answer to each question.

1. **(3 pts.)** Assuming a word size of 5 bits, interpret 10110 as a 2's complement number.
   a) -9 b) -10 c) -5 d) 22 e) None of the above.

   01001 + 1 = 01010 = 10

2. **(3 pts.)** Assuming a word size of 5 bits, determine the 2's complement representation of -9.
   a) 11011 b) 10111 c) 10110 d) 11001 e) None of the above.

   9 = 01001, 10110 + 1 = 10111

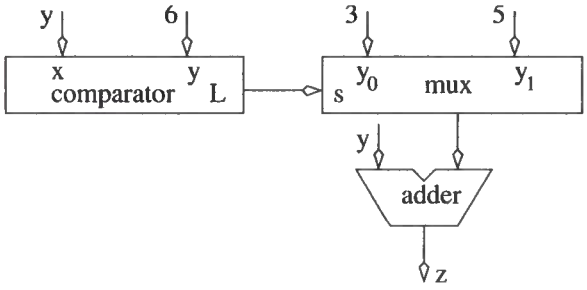
3. **(3 pts.)** How many inputs do the AND gates in a 5:32 decoder have?
   a) 5 b) 6 c) 31 d) 32 e) None of the above.

   minterm + data in

4. **(3 pts.)** How many 2:1 muxes does it take to build a 32:1 mux?
   a) 3 b) 7 c) 15 d) 31 e) None of the above.

   16+8+4+2+1

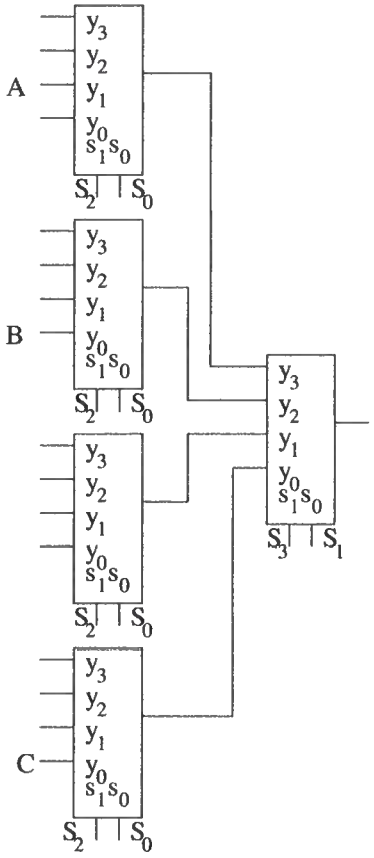
5. **(5 pts.)** Which line of pseudo-code is equivalent to the following piece of hardware.



if (y<6) z = y+5
else z = y+3

   a) `if (6 < Y) then Z = X+3 else Z = Y+5;`
   b) `if (6 < Y) then Z = Y+5 else Z = Y+3;`
   c) `if (Y < 6) then Z = X+3 else Z = Y+5;`
   d) `if (Y < 6) then Z = Y+5 else Z = Y+3;`

You are given the following 16:1 multiplexer built from 4:1 multiplexers. Unfortunately, the select lines were connected in a most unusual fashion. Its your job to label each input with the index which selects it. Most of the inputs have been omitted for clarity.



	S_2S_0	S_3S_1	$S_3S_2S_1S_0$	
A	01	11	1011	11
B	00	10	1000	8
C	00	00	0000	0

6. **(3 pts.)** What is the value of the input labeled A?

   a) y_7 b) y_{11} c) y_{13} d) y_{14} e) None of the above

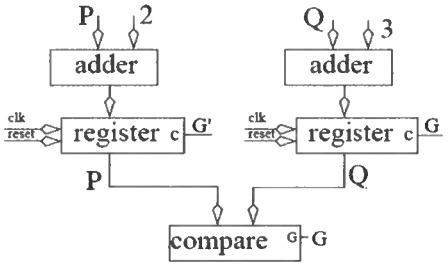
7. **(3 pts.)** What is the value of the input labeled B?

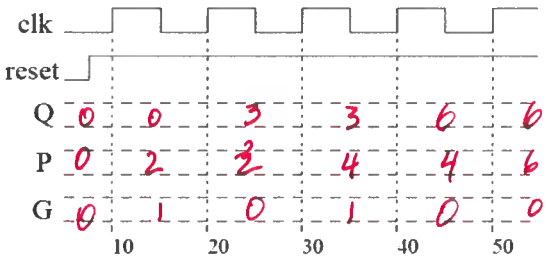
   a) y_1 b) y_2 c) y_4 d) y_8 e) None of the above

8. **(3 pts.)** What is the value of the input labeled C?

   a) y_0 b) y_{10} c) y_{11} d) y_{12} e) None of the above

For the following problems use the circuit and timing diagram. The "c" input of the register's is the control input. Note one of the control inputs is G' i(the negation of G) while the other is G.





9. **(4 pts.)**What is the value of P at time 15?
   a) 0 b) 2 c) 4 d) 6 e) none of the above

10. **(4 pts.)**What is the value of Q at time 25?
    a) 0 b) 3 c) 6 d) 9 e) none of the above

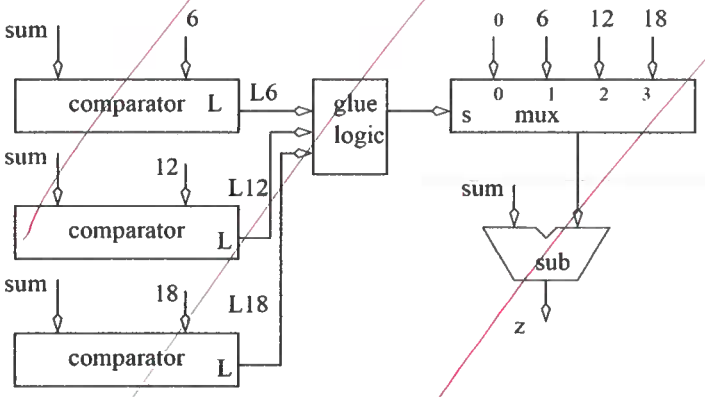
11. **(4 pts.)**What is the value of ~~Y~~ at time 35?
    a) 0 b) 1 c) none of the above

12. **(4 pts.)**What is the value of P at time 45?
    a) 0 b) 2 c) 4 d) 6 e) none of the above

You have a digital design which calls for a circuit which performs the following task (written as a C if/then statement).

```
if      (sum < 6)  z = sum-18
else if (sum > 12) z = sum-12
else if (sum > 18) z = sum-6
else               z = sum
```

To do this, you have decided on the following architecture.



It's your job to design to complete the truth table for the the `glue logic` box. Show you can do this by completing the following three rows.

L6	L12	L18	select
1	1	1	a
0	1	1	b
1	0	1	c

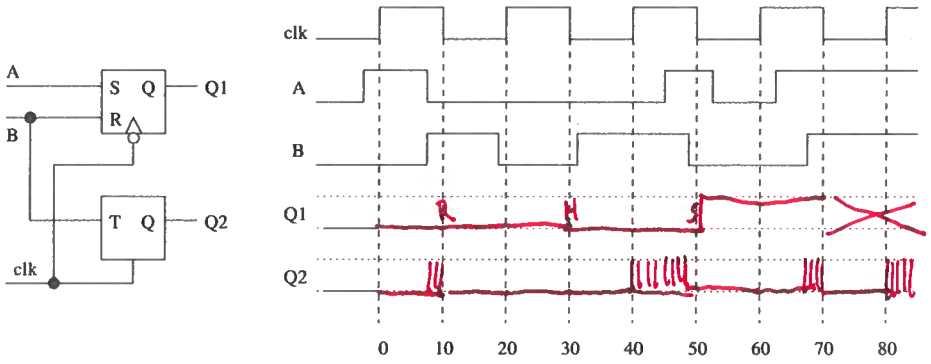
13. **(3 pts.)**What is the (decimal) value of a in the truth table?
    a) 0 b) 1 c) 2 d) 3 e) x

14. **(3 pts.)**What is the (decimal) value of b in the truth table?
    a) 0 b) 1 c) 2 d) 3 e) x

15. **(3 pts.)**What is the (decimal) value of c in the truth table?
    a) 0 b) 1 c) 2 d) 3 e) x

Not graded

Assume that initial value of Q is 0 (as shown in the figure), and that the outputs, after a period of rapid toggling, end-up at 0.



16. **(3 pts.)** What is the value of Q1 at time 25
    a) 0 b) 1 c) toggling d) unknown

17. **(3 pts.)** What is the value of Q1 at time 35
    a) 0 b) 1 c) toggling d) unknown

18. **(3 pts.)** What is the value of Q1 at time 65
    a) 0 b) 1 c) toggling d) unknown

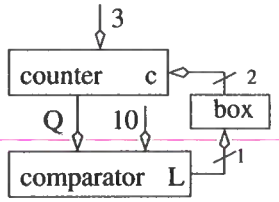
19. **(3 pts.)** What is the value of Q2 at time 25
    a) 0 b) 1 c) toggling d) unknown

20. **(3 pts.)** What is the value of Q2 at time 45
    a) 0 b) 1 c) toggling d) unknown

For the following problems use the following state table for the counter.

clk	C_1C_0	D	Q^+	Note
0,1,↓	xx	x	Q	No clk edge
↑	00	x	Q	Hold
↑	01	x	Q+1	Count up mod 2^N
↑	10	x	Q-1	Count down mod 2^N
↑	11	D	D	Parallel load

21. **(3 pts.)**What is the logic inside box in order to make the count sequence on Q go from 3 to 10 (inclusive of both) over and over.

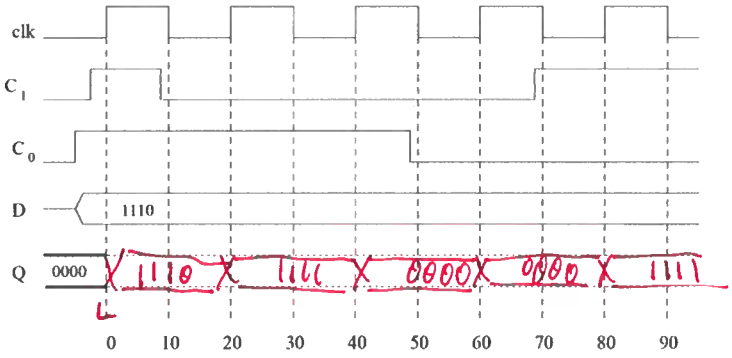


3 9 10
L 01 10 10
count up up load
01 11

a) $c_1 = L'$ $c_0 = 0$
b) $c_1 = L'$ $c_0 = 1$
c) $c_1 = L$ $c_0 = 0$
d) $c_1 = L$ $c_0 = 1$
e) None of the above

$C_1 = L'$
$C_0 = 1$

Use the timing diagram below as the input to a 4-bit counter with the state table given above. Determine the output sequence Q to answer the questions below.



22. **(3 pt.)**What is the value of Q at time 15?
a) 0000 b) 0001 c) 1110 d) 1111 e) None of the above

23. **(3 pt.)**What is the value of Q at time 65?
a) 0000 b) 0001 c) 1110 d) 1111 e) None of the above

24. **(3 pt.)**What is the value of Q at time 85?
a) 0000 b) 0001 c) 1110 d) 1111 e) None of the above