CSE 271 – Fall 2004

Exam 2

Name: SSN:

D	Q+
0	0
1	1

T	Q+
0	Q
1	Q'

S	R	Q+
0	0	Q
0	1	0
1	0	1
1	1	x

J	K	Q+
0	0	Q
0	1	0
1	0	1
1	1	Q'

All counter in this exam are 4-bits wide and have the following behavior.

clk	C_1C_0	D	Q^+
0,1,↓	xx	x	Q
↑	00	x	Q
↑	01	x	Q+1
↑	10	x	Q-1
↑	11	D	D

All shift registers in this exam are 4-bits wide and have the following behavior.

clk	C_1C_0	D	Q^+	comment
0,1,↓	xx	x	Q	hold
↑	00	x	Q	hold
↑	01	x	Q>>1	shift right
↑	10	x	Q<<1	shift left
↑	11	D	D	parallel load

1. **(1 pt.)** Assuming a word size of 5 bits, interpret 10101 as a 2's complement number.

   a) -21 b) -11 c) -10 d) -5 e) None of the above

2. **(1 pt.)** Assuming a word size of 5 bits, determine the 2's complement representation of -12.

   a) 10100 b) 11100 c) 10011 d) 10010 e) None of the above

3. **(1 pt.)**How many OR gates are there inside a 3:8 decoder?

   a) 1 b) 3 c) 8 d) 16 e) None of the above

4. **(1 pt.)**How many inputs do the AND gates inside a 3:8 decoder have?

   a) 1 b) 3 c) 4 d) 8 e) None of the above

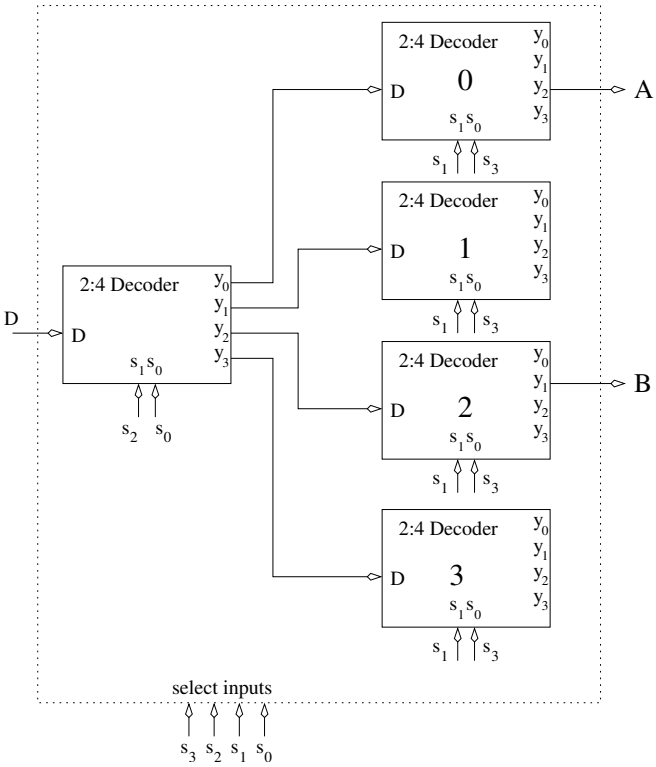
5. **(1 pt.)** How many AND gates are there in an 8:1 mux?

   a) 1 b) 2 c) 3 d) 8 e) None of the above

6. **(1 pt.)** How many 2:1 muxes are needed to construct a 64x1 mux?

   a) 31 b) 32 c) 63 d) 64 e) None of the above

You are given the following 4:16 decoder built from 2:4 decoders. Unfortunately, the student who built it wired the select lines in a most unusual fashion. Its your job to label each output with the index which selects it. Most of the outputs have been omitted for clarity.



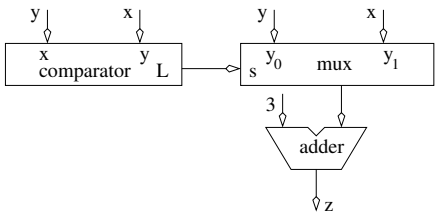
7. **(1 pt.)** What is the value of the output labeled A?

   a) y_1 b) y_2 c) y_4 d) y_8 e) None of the above

8. **(1 pt.)** What is the value of the output labeled B?

   a) y_1 b) y_6 c) y_9 d) y_{12} e) None of the above

9. **(2 pt.)** Which line of pseudo-code best characterizes the following piece of hardware.



a) `if (X < Y) then Z = X+3 else Z = Y+3;`

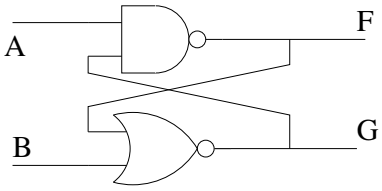
b) `if (X < Y) then Z = Y+3 else Z = X+3;`

c) `if (X > Y) then Z = X+3 else Z = Y+3;`

d) `if (X > Y) then Z = Y+3 else Z = X+3;`

e) None of the above

For questions 10-11 you are to complete the state table for the following circuit.



10. **(1 pt.)** What does G^+ equal for (A,B)=(0,0)?

a) 0 b) 1 c) F d) F' e) illegal

11. **(1 pt.)** What does F^+ equal for (A,B)=(1,1)?

a) 0 b) 1 c) F d) F' e) illegal

12. **(2 pt.)**What is the logic inside `box` in order to make the count sequence on Q go from 3 to 10 (inclusive of both) over and over.

a) $c_1 = L'$ $c_0 = 0$

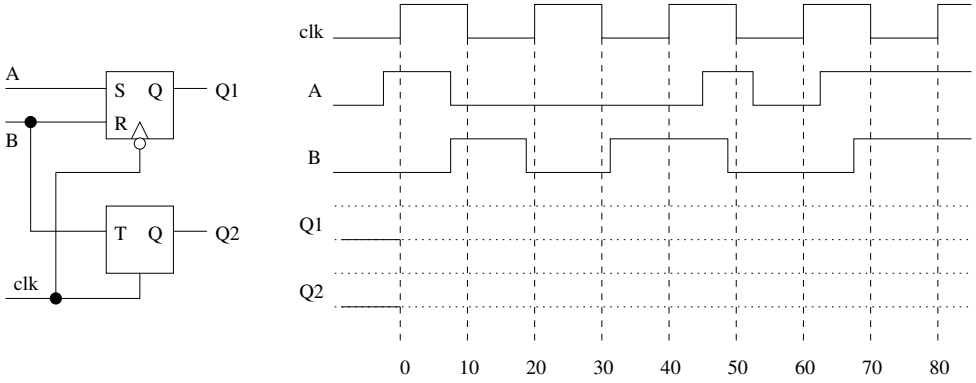
b) $c_1 = L'$ $c_0 = 1$

c) $c_1 = L$ $c_0 = 0$

d) $c_1 = L$ $c_0 = 1$

e) None of the above

For questions 13-16 use the circuit and timing diagram show below. If necessary, you can assume that Q settles to 0 after a period of rapid toggling.



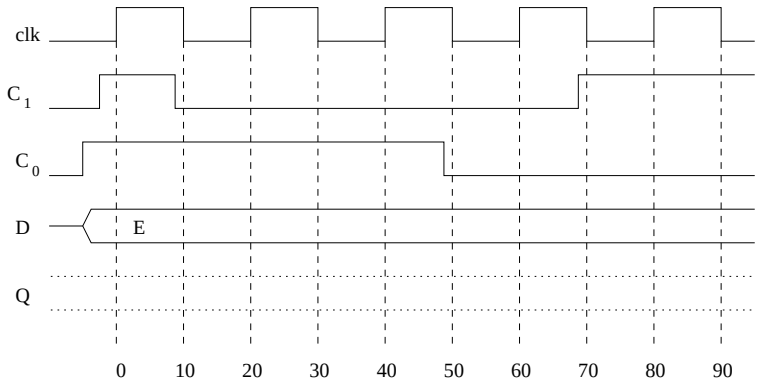
13. **(1 pt.)** What is the value of Q_1 at time=25nS?
    a) 0 b) 1 c) Toggling rapidly d) Unknown

14. **(1 pt.)** What is the value of Q_1 at time=75nS?
    a) 0 b) 1 c) Toggling rapidly d) Unknown

15. **(1 pt.)** What is the value of Q_2 at time=15nS?
    a) 0 b) 1 c) Toggling rapidly d) Unknown

16. **(1 pt.)** What is the value of Q_2 at time=45nS?
    a) 0 b) 1 c) Toggling rapidly d) Unknown

For problems 17-19 use the timing diagram below as the input to a counter. Determine the output sequence Q to answer the questions below.


clk
C 1
C 0
D
E
Q
0
10
20
30
40
50
60
70
80
90

17. **(1 pt.)**What is the value of Q at time 15?

a) 0000 b) 0001 c) 1110 d) 1111 e) None of the above

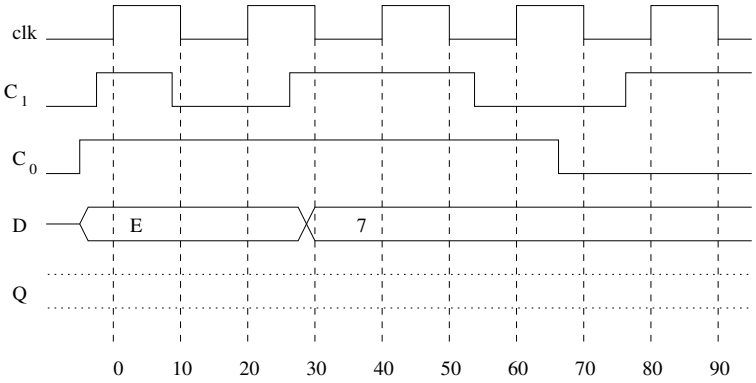
18. **(1 pt.)**What is the value of Q at time 65?

a) 0000 b) 0001 c) 1110 d) 1111 e) None of the above

19. **(1 pt.)**What is the value of Q at time 85?

a) 0000 b) 0001 c) 1110 d) 1111 e) None of the above

For problems 20-22 use the timing diagram below as the input to a arithmetic shift register. Determine the output sequence Q to answer the questions below.



20. **(1 pt.)**What is the value of Q at time 25?

a) 0000 b) 0111 c) 1110 d) 1111 e) None of the above

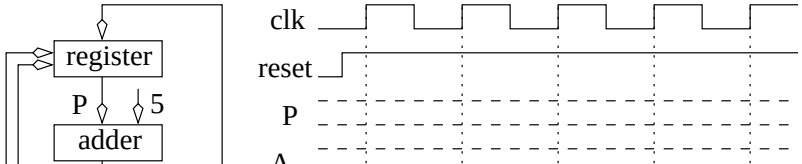
21. **(1 pt.)**What is the value of Q at time 65?

a) 0000 b) 0111 c) 0110 d) 1110 e) None of the above

22. **(1 pt.)**What is the value of Q at time 85?

a) 0000 b) 0111 c) 0110 d) 1110 e) None of the above

For problems 23-27 use the following figure and timing diagram. You should assume that all the devices process 5-bits data values.


register
P
5
adder
clk
reset
P

23. **(2 pt.)**What is the value of P at time 15?

a) 0 b) 2 c) 3 d) 5 e) 8

24. **(2 pt.)**What is the value of A_0 at time 25?

a) 7 b) 8 c) 11 d) 13 e) 16

25. **(2 pt.)**What is the value of Q at time 35?

a) 7 b) 8 c) 11 d) 13 e) 16

26. **(2 pt.)**What is the value of A_1 at time 45?

a) 8 b) 10 c) 13 d) 16 e) 19

27. **(2 pt.)**What is the value of M at time 55?

a) 2 b) 8 c) 10 d) 11 e) 12