外文文献译文

设计(论文)题目: 电子密码锁的设计

专业与班级: 测控技术与仪器 0602 班

学生姓名: 于良

指导教师: 周彬

2007 年 3 月 18 日

Introduction of AT89C51

Description:

The AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4K bytes of Flash programmable and erasable read only memory (PEROM). The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry-standard MCS-51 instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the ATMEL Co.'s AT89C51 is a powerful microcomputer which provides a highly-flexible and cost-effective solution to many embedded control applications.

Features:

·Compatible with instruction set of MCS-51 products

·4K bytes of in-system reprogrammable Flash memory

·Endurance: 1000 write/erase cycles

·Data retention time: 10 years

·Fully static operation: 0 Hz to 24 MHz

·Three-level program memory lock

·128×8-bit internal RAM

·32 programmable I/O lines

·Two 16-bit Timer/Counters

·Six interrupt source

·Programmable serial channel

·Low-power idle and Power-down modes

·On-chip oscillator and clock circuitry

·Full-duplex UART serial port interrupt line

·Dual Data Pointer Register

Function Characteristic Description:

The AT89C51 provides the following standard features: 4K bytes of Flash memory, 128 bytes of RAM, 32 I/O lines, two 16-bit timer/counters, a five vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator and clock circuitry. In addition, the AT89C51 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port and

interrupt system to continue functioning. The Power-down Mode saves the RAM contents but freezes the oscillator disabling all other chip functions until the next hardware reset.

The 8051 microcontroller is an industry standard architecture that has broad acceptance, wide-ranging applications and development tools available. There are numerous commercial vendors that supply this controller or have it integrated into some type of system-on-a-chip structure. Both MRC and IAμE chose this device to demonstrate two distinctly different technologies for hardening. The MRC example of this is to use temporal latches that require specific timing to ensure that single event effects are minimized. The IAμE technology uses ultra low power, and layout and architecture HBD design rules to achieve their results. These are fundamentally different than the approach by Aeroflex-United Technologies Microelectronics Center (UTMC), the commercial vendor of a radiation– hardened 8051, that built their 8051 microcontroller using radiation hardened processes. This broad range of technology within one device structure makes the 8051an ideal vehicle for performing this technology evaluation

Pin Description:

·VCC: Supply voltage

·GND: Ground

·Port 0: Port 0 is an 8-bit open-drain bi-directional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high impedance inputs.

Port 0 may also be configured to be the multiplexed low order address/bus during accesses to external program and data memory. In this mode P0 has internal pull ups.

Port 0 also receives the code bytes during Flash programming, and outputs the code bytes during program verification. External pull ups are required during program verification.

·Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pull ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins they are pulled high by the internal pull ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (IIL) because of the internal pull ups.

Port 1 also receives the low-order address bytes during Flash programming and verification.

·Port 2: Port 2 is an 8-bit bi-directional I/O port with internal pull ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins they are pulled high by the internal pull ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (IIL) because of the internal pull ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory which uses 16-bit addresses (MOVX @ DPTR). In this application, it uses strong internal pull ups when emitting 1s. During accesses to external data memory which uses 8-bit addresses (MOVX @ RI). Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

·Port 3: Port 3 is an 8-bit bi-directional I/O port with internal pullups.The Port 3 output buffers can sink/source four TTL inputs. When the P3 I write "1" after, they are internal pull-up is high, and used as input. As input, due to the external pull-down for the low, P3 port output current (ILL) This is due to pull-up's sake.

Port 3 also serves the functions of various special features of the AT89C51 as listed below:

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{\text{INT0}}$ (external interrupt 0)
P3.3	$\overline{\text{INT1}}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{\text{WR}}$ (external data memory write strobe)
P3.7	$\overline{\text{RD}}$ (external data memory read strobe)

Port 3 also receives some control signals for Flash programming and verification.

·RST: Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

·ALE/$\overline{PROG}$: Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming. In normal operation ALE is emitted at a

constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

· $\overline{PSEN}$：Program Store Enable is the read strobe to external program memory. When the AT89C51 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

·/ EA /VPP：External Access Enable. EA must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, EA will be internally latched on reset. EA should be strapped to VCC for internal program executions. When / EA to maintain low, then during this period the external program memory (0000H-FFFFH), regardless of whether an internal program memory.

This pin also receives the 12-volt programming enable voltage (VPP) during Flash programming, for parts that require 12-volt VPP.

·XTAL1：Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

·XTAL2：Output from the inverting oscillator amplifier.

·Ready/ $\overline{BUSY}$: The progress of byte programming can also be monitored by the RDY/ $\overline{BSY}$ output signal. P3.4 is pulled low after ALE goes high during programming to indicate BUSY. P3.4 is pulled high again when programming is done to indicate READY.

Oscillator Characteristics：

XTAL1 and XTAL2 respectively, reverse amplifier input and output. The reverse amplifier can be configured as on-chip oscillator. Shi Jing oscillation and ceramic oscillation can be used. If using an external clock source drive the device, XTAL2 should not take. More than input to the internal clock signal through a two-way flip-flop, so the external clock signal pulse width without any request, but must ensure that the high-low pulse width requirements.

Clock Oscillator：

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator. Either a quartz crystal or ceramic resonator may be used.

To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven.

There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide by two flip trigger, but minimum and maximum voltage high and low time specifications must be observed.

Idle Mode：

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

It should be noted that when idle is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

Power-down Mode:

In the power-down mode, the oscillator is stopped, and the instruction that invokes power-down is the last instruction executed. The on-chip RAM and special function registers retain their values until the power-down mode is terminated. The only exit from power-down is a hardware reset. Reset redefines the special function registers but does not change the on-chip RAM. The reset should not be activated before VCC is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Program Memory Lock Bits:

On the chip are three lock bits which can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the table below.

Lock Bit Protection Modes

Program Lock Bits				
	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash is disabled
3	P	P	U	Same as mode 2, also verify is disabled
4	P	P	P	Same as mode 3, also external execution is disabled

When lock bit 1 is programmed, the logic level at the EA pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value, and holds that value until reset is activated. It is necessary that the latched value of EA be in agreement with the current logic level at that pin in order for the device to function properly.

Programming the Flash:

The AT89C51 is normally shipped with the on-chip Flash memory array in the erased state (that is, contents = FFH) and ready to be programmed. The programming interface accepts either a high-voltage (12-volt) or a low-voltage (VCC) program enable signal. The low-voltage programming mode provides a convenient way to program the AT89C51 inside the user's system, while the high-voltage programming mode is compatible with conventional third party Flash or EPROM programmers.The AT89C51 is shipped with either the high-voltage or low-voltage programming mode enabled.

The AT89C51 code memory array is programmed byte-by-byte in either programming mode. To program any nonblank byte in the on-chip Flash memory, the entire memory must be erased using the chip erase mode.

Programming Algorithm:

Before programming the AT89C51, the address, data and control signals should be set up according to the Flash programming mode table .To program the AT89C51, take the following steps:

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise EA/VPP to 12V for the high-voltage programming mode.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits.

The byte-write cycle is self-timed and typically takes no more than 1.5ms.

Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

Data Polling:

The AT89C51 features Data Polling to indicate the end of a write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written datum on PO.7. Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. Data polling may begin any time after a write cycle has been initiated.

Program Verify:

If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The lock bits cannot be verified directly. Verification of the lock bits is achieved by observing that their features are enabled.

Chip Erase:

The whole array and three lock-bit PEROM electrical erase control signals through the right combination and maintain ALE pin is low 10ms to complete. Cleaning operation in the chip, code arrays were all written "1" and in any non-empty memory byte has been programmed to repeat the past, the operation must be executed. In addition, AT89C51 with steady-state logic, and can be in the low to zero frequency under the conditions of static logic, and supports two software selectable power-down mode. In idle mode, CPU stop working. But the RAM, timers, counters, serial port and interrupt system are still working. In the power-down mode, to save the contents of RAM and a freeze oscillator, to prohibit the use of other chip functions until the next until a hardware reset.

Reading the Signature Bytes:

The signature bytes are read by the same procedure as a normal verification of locations 030H, 031H, and 032H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows:

(030H) = 1EH indicates manufactured by ATMEL

(031H) = 51H indicates AT89C51 single-chip

(032H) = FFH indicates 12V programming

(032H) = 05H indicates 5V programming

Programming Interface:

Every code byte in the Flash array can be written and the entire array can be

erased by using the appropriate combination of control signals. The write operation cycle is self timed and once initiated, will automatically time itself to completion.

Watchdog (WDT) circuit:

Watchdog (WDT) reset circuit is to achieve the main functionality. When the MCU is running an infinite loop occurs when the watchdog (WDT) can play a protection circuit to achieve reduction effect.

摘自: http：//www.docin.com/p-35268283.html

AT89C51 的介绍

描述：

AT89C51 是一个低电压，高性能 CMOS8 位单片机带有 4K 字节的可反复擦写的程序存储器（PENROM）。和 128 字节的存取数据存储器（RAM），这种器件采用 ATMEL 公司的高密度、不容易丢失存储技术生产，并且能够与 MCS-51 系列的单片机兼容。片内含有 8 位中央处理器和闪烁存储单元，功能强大 AT89C51 单片机可为您提供许多高性价比的应用场合，可灵活应用于各种控制领域。

主要性能参数：

- 与 MCS-51 产品指令系统完全兼容
- 4K 字节可重擦写 Flash 闪速存储器
- 1000 次擦写周期
- 数据保留时间：10 年
- 全静态操作：0Hz—24MHz
- 三级加密程序存储器
- 128×8 字节内部 RAM
- 32 个可编程 I/O 口线
- 2 个 16 位定时/计数器
- 6 个中断源
- 可编程串行 UART 通道
- 低功耗空闲和掉电模式
- 片内振荡器和时钟电路
- 全双工 UART 串行中断口线
- 双数据寄存器指针

功能特性概述：

AT89C51 提供以下标准功能：4K 字节 Flash 闪速存储器，128 字节内部 RAM，32 个 I/O 口线，两个 16 位定时/计数器，一个 5 向量两级中断结构，一个全双工串行通信口，片内振荡器及时钟电路。同时，AT89C51 可降至 0Hz 的静态逻辑操作，并支持两种软件可选的节电工作模式。空闲方式停止 CPU 的工作，但允许 RAM，定时/计数器。串行通信口及中断系统继续工作。掉电方式保存 RAM 中的内容，但振荡器停止工作并禁止其它所有部件工作直到下一个硬件复位。

AT89C51 单片机是一个行业标准架构，被广泛接受和应用，并作为一种开发工具。有许多工业供应商，他们供应这种控制器或把这种控制器集成到某种类型的系统芯片的结构。医学研究理事会和高级微电子研究所都选择这个设备，但他们论证的是两种截然不同固化工艺。医学研究理事会的实例是使用时间锁存，需

要具体时间以确保单粒子效应减少到最低限度。高级微电子研究所采用超低功耗，以及布局和建筑固化工艺的设计原则来实现其结果。这些是与 Aeroflex 联合技术微电子中心（ UTMC ）完全不同的方法 ，抗辐射固化的 AT89C51 的工业供应商，利用抗辐射固化进程研制自己的 AT89C51 单片机。

引脚功能说明：

• V_{CC}：电源电压

• GND：地

• P0 口：P0 口是一组 8 位漏极开路型双向 I/O 口，也即地址/数据总线复用口。作为输出口用时，每位能吸收电流的方式驱动 8 个 TTL 逻辑门电路，对端口写“1”可作为高阻抗输入端用。

在访问外部数据存储器或程序存储器时，这组口线分时转换地址（低 8 位）和数据总线复用，在访问期间即或内部上拉电阻。

在 Flash 编程时，P0 口接收指令字节，而在程序校验时，输出指令字节，校验时，要求外接上拉电阻。

• P1 口：P1 是一个带有内部上拉电阻的 8 位双向 I/O 口，P1 的输出缓冲级可驱动（吸收或输出电流）4 个 TTL 逻辑门电路。对端口写“1”，通过内部的上拉电阻把端口拉到高电平，此时可作输入口。作输入口使用时，因为内部存在上拉电阻，某个引脚被外部信号拉低时会输出一个电流（I_{IL}）。

Flash 编程和程序校验期间，P1 接收低 8 位地址。

• P2 口：P2 是一个带有内部上拉电阻的 8 位双向 I/O 口，P2 的输出缓冲级可驱动（吸收或输出电流）4 个 TTL 逻辑门电路。对端口写“1”，通过内部的上拉电阻把端口拉到高电平，此时可作输入口。作输入口使用时，因为内部存在上拉电阻，某个引脚被外部信号拉低时会输出一个电流（I_{IL}）。

在访问外部程序存储器或 16 位地址的外部数据存储器(例如执行 MOVX@DPTR 指令）时，P2 口送出高 8 位地址数据。在访问 8 位地址的外部数据存储器（如执行 MOVX@RI 指令）时，P2 口线上的内容在整个访问期间不改变。

Flash 编程或检验时，P2 亦接收高位地址和其它控制信号。

• P3 口：P3 口是一组带有内部电阻的 8 位双向 I/O 口，P3 口输出缓冲故可驱动 4 个 TTL 电路。当 P3 口写入“1”后，它们被内部上拉为高电平，并用作输入。作为输入，由于外部下拉为低电平，P3 口将输出电流（ILL）这是由于上拉的缘故。

P3 口除了作为一般的 I/O 口外，更重要的用途是它的第二功能，如表 1 所示：

表 1 P3 口第二功能

端口引脚	第二功能
P3.0	RXD
P3.1	TXD
P3.2	INT0
P3.3	INT1
P3.4	T0
P3.5	T1
P3.6	WR
P3.7	RD

P3 口还接收一些用于闪烁存储器编程和程序校验的控制信号。

• RET：复位输入。当振荡器工作时，RET 引脚出现两个机器周期以上高电平将使单片机复位。

• ALE/$\overline{PROG}$：当访问外部程序存储器或数据存储器时，ALE（地址锁存允许）输出脉冲用于锁存地址的低 8 位字节。对 Flash 存储器编程期间，该引脚还用于输入编程脉冲（$\overline{PROG}$）。即使不访问外部存储器，ALE 仍以时钟振荡频率的 1/6 输出固定的正脉冲信号，因此它可对外输出时钟或用于定时目的。要注意的是：每当访问外部数据存储器时将跳过一个 ALE 脉冲。

如有必要，可通过对特殊功能寄存器（SFR）区中的 8EH 单元的 D0 位置位，可禁止 ALE 操作。该位置位后，只有一条 MOVX 和 MOVC 指令 ALE 才会被激活。此外，该引脚会被微弱拉高，单片机执行外部程序时，应设置 ALE 无效。

• $\overline{PSEN}$：程序储存允许（$\overline{PSEN}$）输出是外部程序存储器的读选通信号，当 AT89C51 由外部程序存储器取指令（或数据）时，每个机器周期两次 $\overline{PSEN}$ 有效，即输出两个脉冲。在此期间，当访问外部数据存储器，这两次有效的 $\overline{PSEN}$ 信号不出现。

$\overline{EA}$/VPP：外部访问允许。欲使 CPU 仅访问外部程序存储器（地址为 0000H—FFFFH），$\overline{EA}$ 端必须保持低电平（接地）。需注意的是：如果加密位 LB1 被编程，复位时内部会锁存 EA 端状态。如 $\overline{EA}$ 端为高电平（接 VCC 端），CPU 则执行内部程序存储器中的指令。当 $\overline{EA}$ 保持低电平时，则在此期间外部程序存储器（0000H-FFFFH），不管是否有内部程序存储器。

Flash 存储器编程时，该引脚加上+12V 的编程允许电源 V_{PP}，当然这必须是该器件是使用 12V 编程电压 V_{PP}。

XTAL1：振荡器反相放大器及内部时钟发生器的输入端。

XTAL2：振荡器反相放大器的输出端。

Ready/$\overline{BUSY}$：字节编程的进度可通过 RDY/$\overline{BSY}$ 输出信号监测，编程期间，ALE 变为高电平“H”后 P3.4（RDY/$\overline{BSY}$）端电平被拉低，表示正在编程状态（忙状态）。编程完成后，P3.4 变为高电平表示准备就绪状态。

振荡器特性：

XTAL1 和 XTAL2 分别为反向放大器的输入和输出。该反向放大器可以配置为片内振荡器。石晶振荡和陶瓷振荡均可采用。如采用外部时钟源驱动器件，XTAL2 应不接。有余输入至内部时钟信号要通过一个二分频触发器，因此对外部时钟信号的脉宽无任何要求，但必须保证脉冲的高低电平要求的宽度。

时钟振荡器：

AT89C51 中有一个用于构成内部振荡器的高增益反相放大器，引脚 XTAL1 和 XTAL2 分别是该放大器的输入端和输出端。这个放大器与作为反馈元件的片外石英晶体 或陶瓷谐振器一起构成自激振荡器。

用户也可以采用外部时钟。这种情况下，外部时钟脉冲接到 XTAL1 端，即内部时钟发生器的输入端，XTAL2 则悬空。

由于外部时钟信号是通过一个 2 分频触发器后作为内部时钟信号的，所以对外部时钟信号的占空比没有特殊要求，但最小高电平持续时间和最大的低电平持续时间应符合产品技术条件的要求。

空闲节电模式：

在空闲工作模式状态，CPU 保持睡眠状态而所有片内的外设仍保持激活状态，这种方式由软件产生。此时，片内 RAM 和所有特殊功能寄存器的内容保持不变。空闲模式可由任何允许的中断请求或硬件复位终止。

通过硬件复位也可将空闲工作模式终止。需要注意的是：当由硬件复位来终止空闲工作模式时，CPU 通常是从激活空闲模式那条指令的下一条指令开始继续执行程序的，要完成内部复位操作，硬件复位脉冲要保持两个机器周期有效，在这种情况下，内部禁止 CPU 访问片内 RAM，而允许访问其它端口。为了避免可能对端口产生意外写入，激活空闲模式的那条指令后一条指令不应是一条对端口或外部存储器的写入指令。

掉电模式：

在掉电模式下，振荡器停止工作，进入掉电模式的指令是最后一条被执行的指令，片内 RAM 和特殊功能寄存器的内容在终止掉电模式前被冻结。退出掉电模式的唯一方法是硬件复位，复位后将重新定义全部特殊功能寄存器但不改变 RAM 中的内容，在 V_{CC} 恢复到正常工作电平前，复位应无效，且必须保持一定时间以

使振荡器重启动并稳定工作。

程序存储器的加密：

AT89C51 可使用对芯片上的三个加密位 LB1，LB2，LB3 进行编程（P）或不编程（U）得到如表 2 所示的功能：

表 2 程序加密位及保护类型

程序加密位				保护类型
				没有程序保护功能
				禁止从外部程序存储器中执行 MOVC 指令读取内部程序存储器的内容
				除上表功能外，还禁止程序校验
				除以上功能外，同时禁止外部执行

当加密位 LB1 被编程时，在复位期间，EA 端的逻辑电平被采样并锁存，如果单片机上电后一直没有复位，则锁存起的初始值是一个随机数，且这个随机数会一直保存到真正复位为止。为使单片机能正常工作，被锁存的 EA 电平值必须与该引脚当前的逻辑电平一致。此外，加密位只能通过整片擦除的方法清除。

Flash 闪速存储器的编程：

AT89C51 单片机内部有 4K 字节的 Flash PEROM，这个 Flash 存储阵列出厂时已处于擦除状态（即所有存储单元的内容均为 FFH），用户随时可对其进行编程。编程接口可接收高电压（+12V）或低电压（V_{CC}）的允许编程信号。低电压编程模式适合于用户在线编程系统，而高电压编程模式可与通用 EPROM 编程器兼容。

AT89C51 的程序存储器阵列是采用字节写入方式编程的，每次写入一个字节，要对整个芯片内的 PEROM 程序存储器写入一个非空字节，必须使用片擦除的方式将整个存储器的内容清除。

编程方法：

编程前，须根据表设置好地址、数据及控制信号。AT89C51 编程方法如下：

1、在地址线上加上要编程单元的地址信号。

2、在数据线上加上要写入的数据字节。

3、激活相应的控制信号。

4、在高电压编程方式时，将 EA/V_{PP} 端加上+12V 编程电压。

5、每对 Flash 存储阵列写入一个字节或每写入一个程序加密位，加上一个 ALE/$\overline{PROG}$ 编程脉冲。改变编程单元的地址和写入的数据，重复 1—5 步骤，直到全部文件编程结束。每个字节写入周期是自身定时的，通常约为 1.5ms。

数据查询：

AT89C51 单片机用数据查询方式来检测一个写周期是否结束，在一个写周期中，如需读取最后写入的那个字节，则读出的数据最高位是原来写入字节最高位的反码。写周期完成后，有效的数据就会出现在所有输出端上，此时，可进入下一个字节的写周期，写周期开始后，可在任意时刻进行数据查询。

程序校验：

如果加密位 LB1、LB2 没有进行编程，则代码数据可通过地址和数据线读回原编写的数据。加密位不可直接校验，加密位的校验可通过对存储器的校验和写入状态来验证。

芯片擦除：

整个 PEROM 阵列和三个锁定位的电擦除可通过正确的控制信号组合，并保持 ALE 管脚处于低电平 10ms 来完成。在芯片擦操作中，代码阵列全被写“1”且在任何非空存储字节被重复编程以前，该操作必须被执行。

此外，AT89C51 设有稳态逻辑，可以在低到零频率的条件下静态逻辑，支持两种软件可选的掉电模式。在闲置模式下，CPU 停止工作。但 RAM，定时器，计数器，串口和中断系统仍在工作。在掉电模式下，保存 RAM 的内容并且冻结振荡器，禁止所用其他芯片功能，直到下一个硬件复位为止。

读片内签名字节：

读签名字节的过程和单元 030H、031H 及 032H 的正常校验相仿，只需将 P3.6 和 P3.7 保持低电平，返回值意义如下：

(030H)=1EH 声明产品由 ATMEL 公司制造

(031H)=51H 声明为 AT89C51 单片机

(032H)=FFH 声明为 12V 编程电压

(032H)=05H 声明为 5V 编程电压

编程接口：

采用控制信号的正确组合可对 Flash 闪速存储阵列中的每一代码字节进行写入和存储器的整片擦除，写操作周期是自身定时的，初始化后它将自动定时到操作完成。

看门狗（WDT）电路：

看门狗（WDT）电路的主要是实现复位功能。当单片机运行出现死循环时，看门狗（WDT）电路可以起保护功能,实现复位作用。

指导教师评阅意见

指导教师签字：

年　　月　　日