Lab 3 – Timing Optimizations

Optimization 1:

Figure 1 - Summary of Paths

	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	-5.583	fifo:fifo_|altsyncram:ram_rtl_0|...|ram_block1a0~portb_address_reg0	mult_out[9][0]	clk	clk	4.000	-0.394	8.945
2	-5.583	fifo:fifo_|altsyncram:ram_rtl_0|...|ram_block1a0~portb_address_reg0	mult_out[9][1]	clk	clk	4.000	-0.394	8.945
3	-5.583	fifo:fifo_|altsyncram:ram_rtl_0|...|ram_block1a0~portb_address_reg0	mult_out[9][2]	clk	clk	4.000	-0.394	8.945
4	-5.583	fifo:fifo_|altsyncram:ram_rtl_0|...|ram_block1a0~portb_address_reg0	mult_out[9][3]	clk	clk	4.000	-0.394	8.945
5	-5.583	fifo:fifo_|altsyncram:ram_rtl_0|...|ram_block1a0~portb_address_reg0	mult_out[9][4]	clk	clk	4.000	-0.394	8.945
6	-5.583	fifo:fifo_|altsyncram:ram_rtl_0|...|ram_block1a0~portb_address_reg0	mult_out[9][5]	clk	clk	4.000	-0.394	8.945
7	-5.583	fifo:fifo_|altsyncram:ram_rtl_0|...|ram_block1a0~portb_address_reg0	mult_out[9][6]	clk	clk	4.000	-0.394	8.945
8	-5.583	fifo:fifo_|altsyncram:ram_rtl_0|...|ram_block1a0~portb_address_reg0	mult_out[9][7]	clk	clk	4.000	-0.394	8.945
9	-5.583	fifo:fifo_|altsyncram:ram_rtl_0|...|ram_block1a0~portb_address_reg0	mult_out[8][0]	clk	clk	4.000	-0.394	8.945
10	-5.583	fifo:fifo_|altsyncram:ram_rtl_0|...|ram_block1a0~portb_address_reg0	mult_out[8][1]	clk	clk	4.000	-0.394	8.945
11	-5.583	fifo:fifo_|altsyncram:ram_rtl_0|...|ram_block1a0~portb_address_reg0	mult_out[8][2]	clk	clk	4.000	-0.394	8.945
12	-5.583	fifo:fifo_|altsyncram:ram_rtl_0|...|ram_block1a0~portb_address_reg0	mult_out[8][3]	clk	clk	4.000	-0.394	8.945
13	-5.583	fifo:fifo_|altsyncram:ram_rtl_0|...|ram_block1a0~portb_address_reg0	mult_out[8][4]	clk	clk	4.000	-0.394	8.945
14	-5.583	fifo:fifo_|altsyncram:ram_rtl_0|...|ram_block1a0~portb_address_reg0	mult_out[8][5]	clk	clk	4.000	-0.394	8.945
15	-5.583	fifo:fifo_|altsyncram:ram_rtl_0|...|ram_block1a0~portb_address_reg0	mult_out[8][6]	clk	clk	4.000	-0.394	8.945
16	-5.583	fifo:fifo_|altsyncram:ram_rtl_0|...|ram_block1a0~portb_address_reg0	mult_out[8][7]	clk	clk	4.000	-0.394	8.945

Critical Path: FIFO -> mult_out

Figure 2 - Statistics showing Cell Data as 68% of the delay

Property	Value	Count	Total Delay	% of Total	Min	M
Arrival Path						
Clock						
IC		3	1.311	42	0.000	0.94
Cell		3	1.805	58	0.000	1.01
Data						
IC		4	2.522	28	0.000	1.16
Cell		5	6.116	68	0.047	3.07
uTco		1	0.307	3	0.307	0.30
Required Path						
Clock						
IC		3	1.590	59	0.000	1.23
Cell		3	1.111	41	0.000	0.79

Figure 3 - Data Arrival Path Showing dataout[17] with 3.076 delay

Data Arrival Path

Total	Incr	RF	Type	ano	Location	Element
6.022	2.599	RR	CELL	2	M9K_X26_Y9_N0	fifo_|ram_rtl_0|auto_generated|ram_block1a0|portbdataout[2]
7.184	1.162	RR	IC	1	LCCOMB_X22_Y9_N28	fifo_|ram~8|datad
7.381	0.197	RR	CELL	1	LCCOMB_X22_Y9_N28	fifo_|ram~8|combout
7.605	0.224	RR	IC	1	LCCOMB_X22_Y9_N14	fifo_|ram~9|datad
7.802	0.197	RR	CELL	16	LCCOMB_X22_Y9_N14	fifo_|ram~9|combout
8.938	1.136	RR	IC	1	DSPMULT_X21_Y8_N0	Mult9|auto_generated|mac_mult1|datab[4]
12.014	3.076	RR	CELL	8	DSPMULT_X21_Y8_N0	Mult9|auto_generated|mac_mult1|dataout[17]
12.014	0.000	RR	IC	1	DSPOUT_X21_Y8_N2	Mult9|auto_generated|mac_out2|dataa[3]
12.061	0.047	RR	CELL	1	DSPOUT_X21_Y8_N2	mult_out[9][0]

- Can infer the longest path of 3.076 is talking about the output data from the multiplier
- Can infer it is talking about the FIFO read data coming into the multiplier and the output from the multiplier.

After Optimization:

	Fmax	Restricted Fmax	Clock Name	Note
1	120.19 MHz	120.19 MHz	clk	

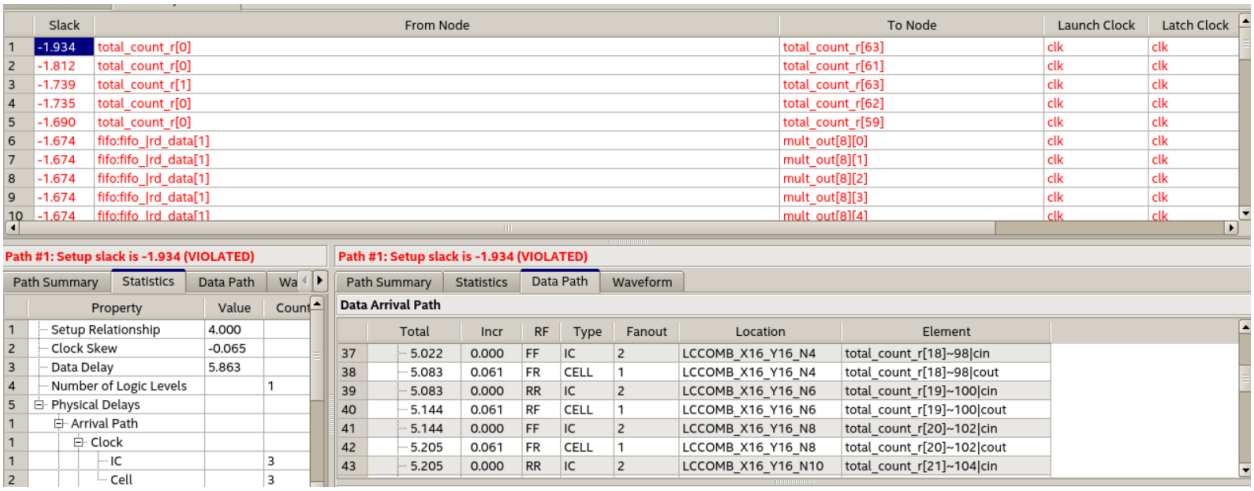
- The same paths still had the worst slack, so I registered the rd_data output which increased the clock again.

After optimization:

	Fmax	Restricted Fmax	Clock Name	Note
1	168.52 MHz	168.52 MHz	clk	

Optimization 2:

Figure 4 - Summary of Paths and Statistics for Optimization 3



	Slack	From Node	To Node	Launch Clock	Latch Clock
1	-1.934	total_count_r[0]	total_count_r[63]	clk	clk
2	-1.812	total_count_r[0]	total_count_r[61]	clk	clk
3	-1.739	total_count_r[1]	total_count_r[63]	clk	clk
4	-1.735	total_count_r[0]	total_count_r[62]	clk	clk
5	-1.690	total_count_r[0]	total_count_r[59]	clk	clk
6	-1.674	fifo:fifo_|rd_data[1]	mult_out[8][0]	clk	clk
7	-1.674	fifo:fifo_|rd_data[1]	mult_out[8][1]	clk	clk
8	-1.674	fifo:fifo_|rd_data[1]	mult_out[8][2]	clk	clk
9	-1.674	fifo:fifo_|rd_data[1]	mult_out[8][3]	clk	clk
10	-1.674	fifo:fifo_|rd_data[1]	mult_out[8][4]	clk	clk

Path #1: Setup slack is -1.934 (VIOLATED)

Path Summary | Statistics | Data Path | Wa

	Property	Value	Count
1	Setup Relationship	4.000	
2	Clock Skew	-0.065	
3	Data Delay	5.863	
4	Number of Logic Levels		1
5	Physical Delays		
1	Arrival Path		
1	Clock		
1	IC		3
2	Cell		3

Path #1: Setup slack is -1.934 (VIOLATED)

Path Summary | Statistics | Data Path | Waveform

Data Arrival Path

	Total	Incr	RF	Type	Fanout	Location	Element
37	5.022	0.000	FF	IC	2	LCCOMB_X16_Y16_N4	total_count_r[18]~98|cin
38	5.083	0.061	FR	CELL	1	LCCOMB_X16_Y16_N4	total_count_r[18]~98|cout
39	5.083	0.000	RR	IC	2	LCCOMB_X16_Y16_N6	total_count_r[19]~100|cin
40	5.144	0.061	RF	CELL	1	LCCOMB_X16_Y16_N6	total_count_r[19]~100|cout
41	5.144	0.000	FF	IC	2	LCCOMB_X16_Y16_N8	total_count_r[20]~102|cin
42	5.205	0.061	FR	CELL	1	LCCOMB_X16_Y16_N8	total_count_r[20]~102|cout
43	5.205	0.000	RR	IC	2	LCCOMB_X16_Y16_N10	total_count_r[21]~104|cin

Critical Path:

- total_count_r -> total_count_r
- Since this signal only gets updated occasionally, it is considered a multicycle path.

Code Changed:

```
set_multicycle_path -setup -end -from [get_keepers {total_count_r*}] -to [get_keepers {total_count_r*}] 2
set_multicycle_path -hold -end -from [get_keepers {total_count_r*}] -to [get_keepers {total_count_r*}] 1
```

After Optimization:

Fmax	Restricted Fmax	Clock Name	Note
175.28 MHz	175.28 MHz	clk	

Optimization 3:

Summary of Paths and Statistics for Optimization 4

	Slack	From Node	To Node	Launch Clock	Latch Clock
1	-1.705	fifo:fifo_|rd_data[5]	mult_out[5][0]	clk	clk
2	-1.705	fifo:fifo_|rd_data[5]	mult_out[5][1]	clk	clk
3	-1.705	fifo:fifo_|rd_data[5]	mult_out[5][2]	clk	clk
4	-1.705	fifo:fifo_|rd_data[5]	mult_out[5][3]	clk	clk
5	-1.705	fifo:fifo_|rd_data[5]	mult_out[5][4]	clk	clk
6	-1.705	fifo:fifo_|rd_data[5]	mult_out[5][5]	clk	clk
7	-1.705	fifo:fifo_|rd_data[5]	mult_out[5][6]	clk	clk
8	-1.705	fifo:fifo_|rd_data[5]	mult_out[5][7]	clk	clk
9	-1.705	fifo:fifo_|rd_data[5]	mult_out[4][0]	clk	clk
10	-1.705	fifo:fifo_|rd_data[5]	mult_out[4][1]	clk	clk

Path #1: Setup slack is -1.705 (VIOLATED)

Path Summary | Statistics | Data Path | Wa

	Property	Value	Count
1	Setup Relationship	4.000	
2	Clock Skew	-0.387	
3	Data Delay	5.074	
4	Number of Logic Levels		1
5	Physical Delays		
1	Arrival Path		
1	Clock		
1	IC		3
2	Cell		3

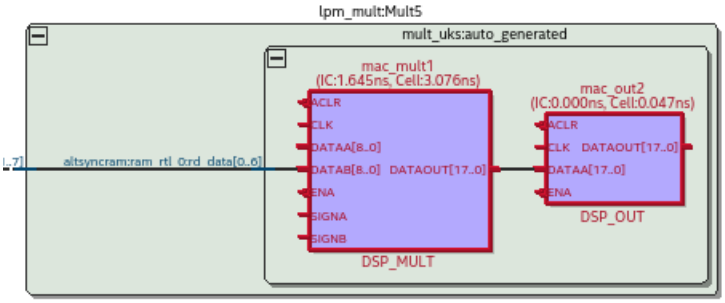
Path #1: Setup slack is -1.705 (VIOLATED)

Path Summary | Statistics | Data Path | Waveform

Data Arrival Path

	Total	Incr	RF	Type	Fanout	Location	Element
3	8.183	5.074					data path
1	3.369	0.260		uTco	1	M9K_X26_Y7_N0	fifo:fifo_|rd_data[5]
2	3.415	0.046	RR	CELL	16	M9K_X26_Y7_N0	fifo_|ram_rtl_0|auto_generated|ram_block1a0|portbdataout[5]
3	5.060	1.645	RR	IC	1	DSPMULT_X21_Y9_N1	Mult5|auto_generated|mac_mult1|datab[7]
4	8.136	3.076	RR	CELL	8	DSPMULT_X21_Y9_N1	Mult5|auto_generated|mac_mult1|dataout[17]
5	8.136	0.000	RR	IC	1	DSPOUT_X21_Y9_N3	Mult5|auto_generated|mac_out2|dataa[3]
6	8.183	0.047	RR	CELL	1	DSPOUT_X21_Y9_N3	mult_out[5][0]

Figure 5 - Path of Longest Slack



Critical Path: IC and CELL of multiply.

Code Changed:

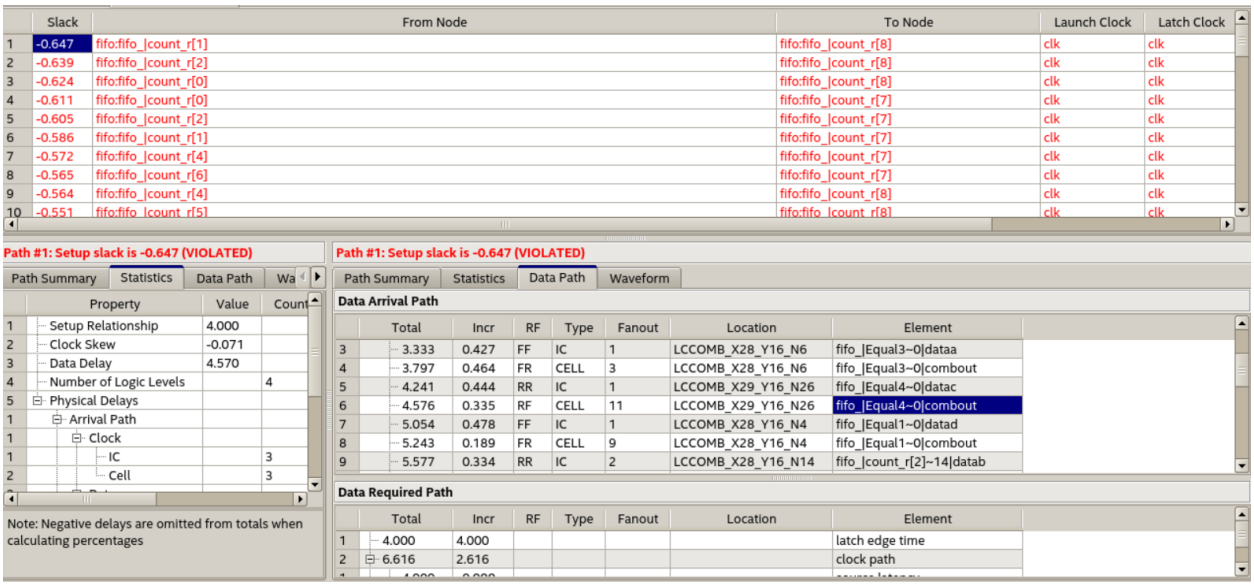
- Registered the fifo_rd_data signal

After Optimization:

	Fmax	Restricted Fmax	Clock Name	Note
1	215.19 MHz	210.04 MHz	clk	lim...in)

Optimization 4:

Summary of Paths and Statistics for Optimization 5



	Slack	From Node	To Node	Launch Clock	Latch Clock
1	-0.647	fifo:fifo_|count_r[1]	fifo:fifo_|count_r[8]	clk	clk
2	-0.639	fifo:fifo_|count_r[2]	fifo:fifo_|count_r[8]	clk	clk
3	-0.624	fifo:fifo_|count_r[0]	fifo:fifo_|count_r[8]	clk	clk
4	-0.611	fifo:fifo_|count_r[0]	fifo:fifo_|count_r[7]	clk	clk
5	-0.605	fifo:fifo_|count_r[2]	fifo:fifo_|count_r[7]	clk	clk
6	-0.586	fifo:fifo_|count_r[1]	fifo:fifo_|count_r[7]	clk	clk
7	-0.572	fifo:fifo_|count_r[4]	fifo:fifo_|count_r[7]	clk	clk
8	-0.565	fifo:fifo_|count_r[6]	fifo:fifo_|count_r[7]	clk	clk
9	-0.564	fifo:fifo_|count_r[4]	fifo:fifo_|count_r[8]	clk	clk
10	-0.551	fifo:fifo_|count_r[5]	fifo:fifo_|count_r[8]	clk	clk

Path #1: Setup slack is -0.647 (VIOLATED)

Path Summary | Statistics | Data Path | Wa

	Property	Value	Count
1	Setup Relationship	4.000	
2	Clock Skew	-0.071	
3	Data Delay	4.570	
4	Number of Logic Levels		4
5	Physical Delays		
1	Arrival Path		
1	Clock		
1	IC		3
2	Cell		3

Note: Negative delays are omitted from totals when calculating percentages

Path #1: Setup slack is -0.647 (VIOLATED)

Path Summary | Statistics | Data Path | Waveform

Data Arrival Path

	Total	Incr	RF	Type	Fanout	Location	Element
3	3.333	0.427	FF	IC	1	LCCOMB_X28_Y16_N6	fifo_|Equal3~0|dataa
4	3.797	0.464	FR	CELL	3	LCCOMB_X28_Y16_N6	fifo_|Equal3~0|combout
5	4.241	0.444	RR	IC	1	LCCOMB_X29_Y16_N26	fifo_|Equal4~0|datac
6	4.576	0.335	RF	CELL	11	LCCOMB_X29_Y16_N26	fifo_|Equal4~0|combout
7	5.054	0.478	FF	IC	1	LCCOMB_X28_Y16_N4	fifo_|Equal1~0|datad
8	5.243	0.189	FR	CELL	9	LCCOMB_X28_Y16_N4	fifo_|Equal1~0|combout
9	5.577	0.334	RR	IC	2	LCCOMB_X28_Y16_N14	fifo_|count_r[2]~14|datab

Data Required Path

	Total	Incr	RF	Type	Fanout	Location	Element
1	4.000	4.000					latch edge time
2	6.616	2.616					clock path

Critical Path:

- Count_r

Code Changed:

- Removed one bit from count_r, used the almost full signal instead of FULL, removed the rd_en, since valid_rd is only based on !empty

After Optimization:

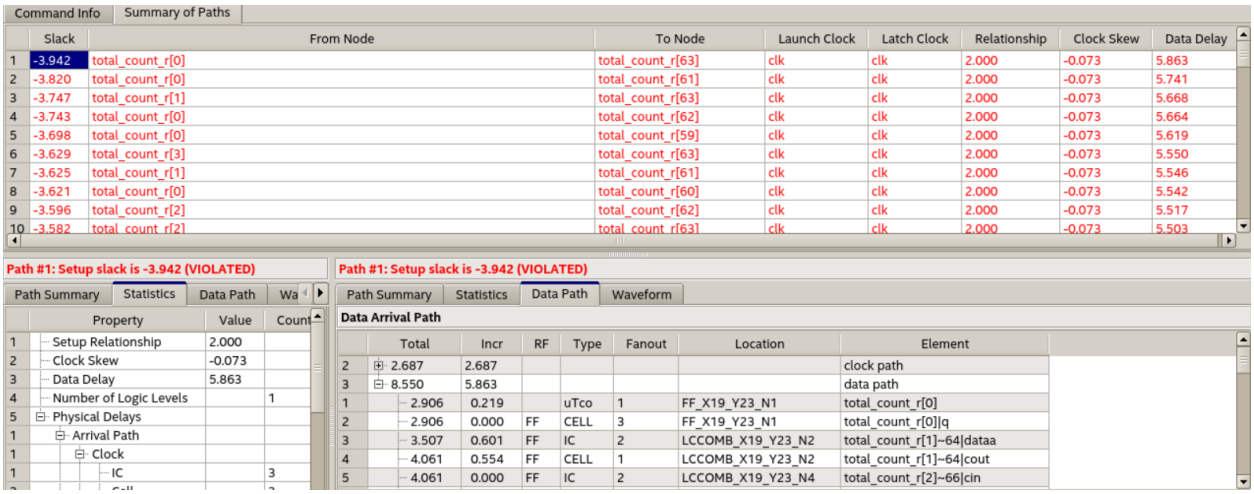
	Fmax
1	242.31 MHz

Optimization 5:

Summary of Paths and Statistics for Optimization 6

```
create_clock -name {clk} -period 2.000 -waveform { 0.000 2.000 } [get_ports {clk}]
```

Applied faster clock constraint



Command Info | Summary of Paths

	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	-3.942	total_count_r[0]	total_count_r[63]	clk	clk	2.000	-0.073	5.863
2	-3.820	total_count_r[0]	total_count_r[61]	clk	clk	2.000	-0.073	5.741
3	-3.747	total_count_r[1]	total_count_r[63]	clk	clk	2.000	-0.073	5.668
4	-3.743	total_count_r[0]	total_count_r[62]	clk	clk	2.000	-0.073	5.664
5	-3.698	total_count_r[0]	total_count_r[59]	clk	clk	2.000	-0.073	5.619
6	-3.629	total_count_r[3]	total_count_r[63]	clk	clk	2.000	-0.073	5.550
7	-3.625	total_count_r[1]	total_count_r[61]	clk	clk	2.000	-0.073	5.546
8	-3.621	total_count_r[0]	total_count_r[60]	clk	clk	2.000	-0.073	5.542
9	-3.596	total_count_r[2]	total_count_r[62]	clk	clk	2.000	-0.073	5.517
10	-3.582	total_count_r[2]	total_count_r[63]	clk	clk	2.000	-0.073	5.503

Path #1: Setup slack is -3.942 (VIOLATED)

Path Summary | Statistics | Data Path | Wa

	Property	Value	Count
1	Setup Relationship	2.000	
2	Clock Skew	-0.073	
3	Data Delay	5.863	
4	Number of Logic Levels		1
5	Physical Delays		
1	Arrival Path		
1	Clock		
1	IC		3

Path #1: Setup slack is -3.942 (VIOLATED)

Path Summary | Statistics | Data Path | Waveform

Data Arrival Path

	Total	Incr	RF	Type	Fanout	Location	Element
2	2.687	2.687					clock path
3	8.550	5.863					data path
1	2.906	0.219		uTco	1	FF_X19_Y23_N1	total_count_r[0]
2	2.906	0.000	FF	CELL	3	FF_X19_Y23_N1	total_count_r[0]|q
3	3.507	0.601	FF	IC	2	LCCOMB_X19_Y23_N2	total_count_r[1]~64|dataa
4	4.061	0.554	FF	CELL	1	LCCOMB_X19_Y23_N2	total_count_r[1]~64|cout
5	4.061	0.000	FF	IC	2	LCCOMB_X19_Y23_N4	total_count_r[2]~66|cin

Critical Path:

- Total_count_r

Code Changed:

- Increased the multicycle clock path by 1 temporarily to find more bottlenecks

List of Code Changes

1. Got rid of read during write behavior and optimized the counter
2. Registered the rd_data output
3. Set up multicycle paths