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Report – Lab 1

Figure 1 - FSMD 1-Process Modelsim, showing no errors

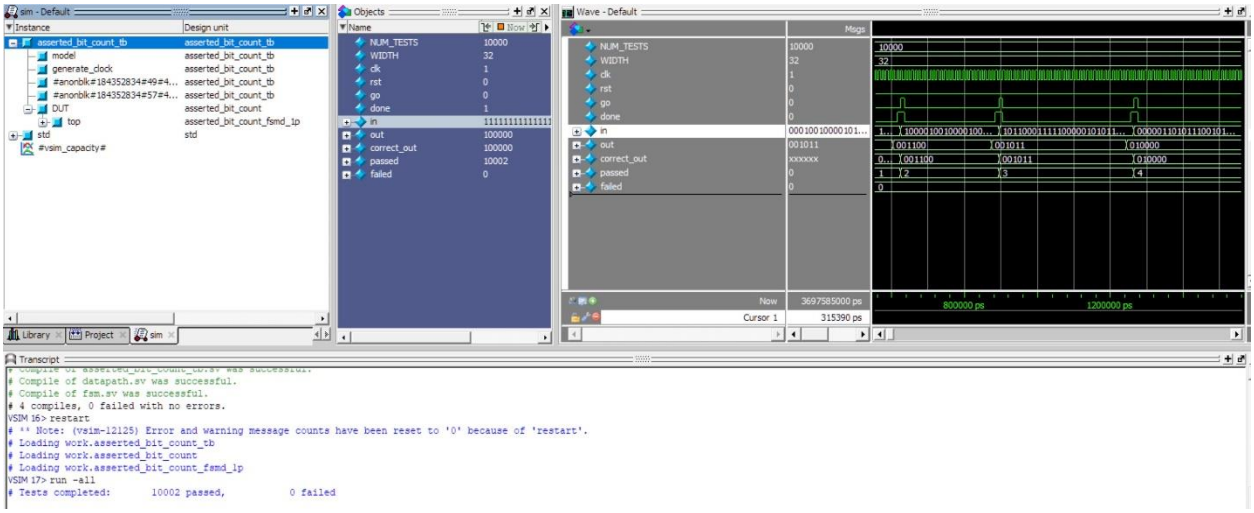


Figure 2 - FSMD 2-Process Modelsim, showing no errors

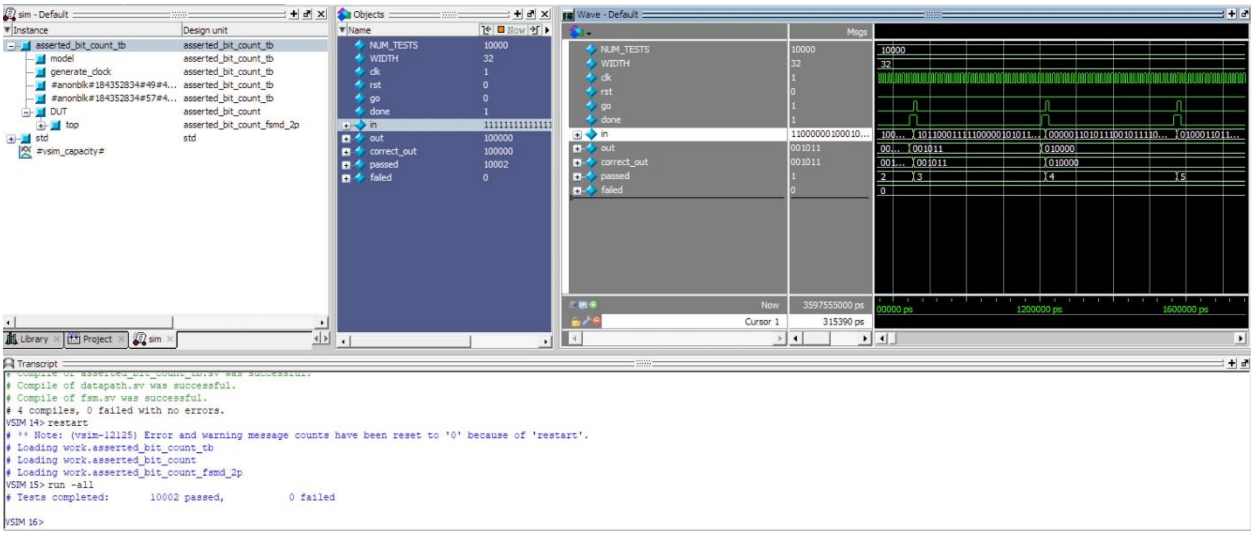


Figure 3 - FSM + D Modelsim, showing no errors

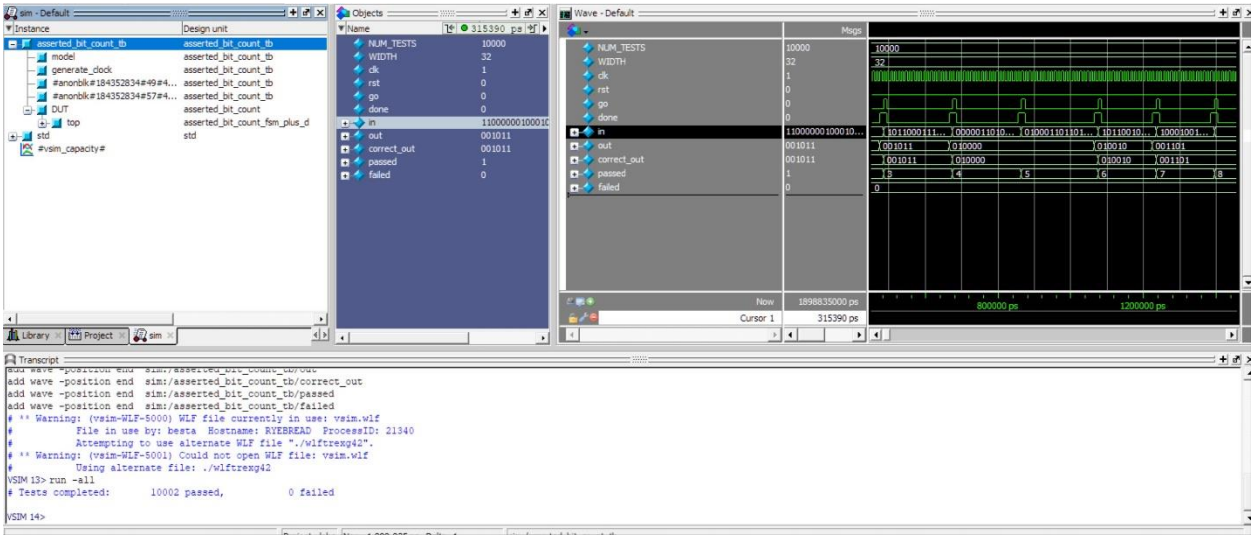


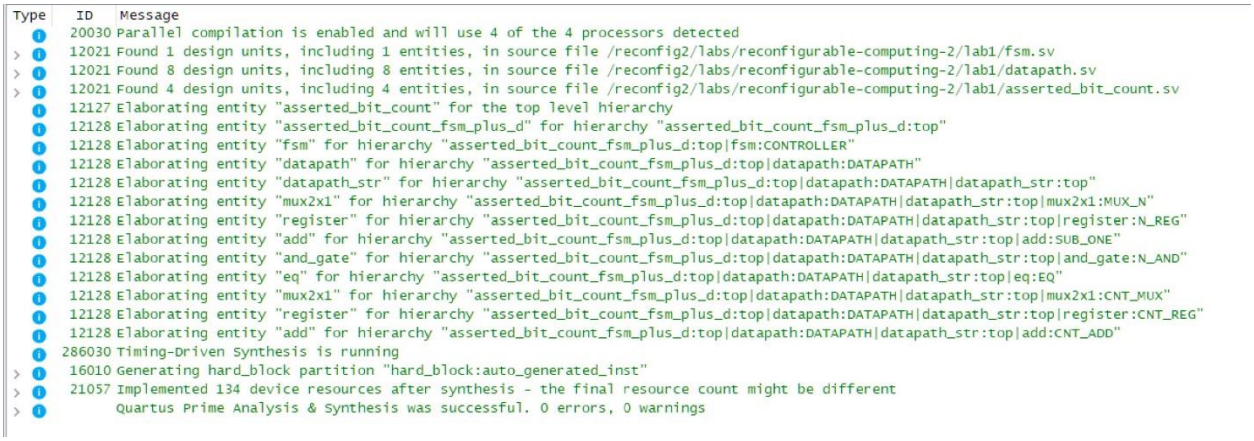
Figure 4 - FSM 1-Process Quartus, showing no errors

Type	ID	Message
		Running Quartus Prime Analysis & Synthesis
		Command: quartus_map --read_settings_files=on --write_settings_files=off lab1 -c lab1
	20030	Parallel compilation is enabled and will use 4 of the 4 processors detected
	12021	Found 1 design units, including 1 entities, in source file /reconfig2/labs/reconfigurable-computing-2/lab1/fsm.sv
	12021	Found 8 design units, including 8 entities, in source file /reconfig2/labs/reconfigurable-computing-2/lab1/datapath.sv
	12021	Found 4 design units, including 4 entities, in source file /reconfig2/labs/reconfigurable-computing-2/lab1/asserted_bit_count.sv
	12127	Elaborating entity "asserted_bit_count" for the top level hierarchy
	12128	Elaborating entity "asserted_bit_count_fsmd_1p" for hierarchy "asserted_bit_count_fsmd_1p:top"
	286030	Timing-Driven Synthesis is running
	16010	Generating hard_block partition "hard_block:auto_generated_inst"
	21057	Implemented 151 device resources after synthesis - the final resource count might be different
		Quartus Prime Analysis & Synthesis was successful. 0 errors, 0 warnings

Figure 5 - FSM 2-Process Quartus, showing no errors

Type	ID	Message
		Command: quartus_map --read_settings_files=on --write_settings_files=off lab1 -c lab1
	20030	Parallel compilation is enabled and will use 4 of the 4 processors detected
	12021	Found 1 design units, including 1 entities, in source file /reconfig2/labs/reconfigurable-computing-2/lab1/fsm.sv
	12021	Found 8 design units, including 8 entities, in source file /reconfig2/labs/reconfigurable-computing-2/lab1/datapath.sv
	12021	Found 4 design units, including 4 entities, in source file /reconfig2/labs/reconfigurable-computing-2/lab1/asserted_bit_count.sv
	12127	Elaborating entity "asserted_bit_count" for the top level hierarchy
	12128	Elaborating entity "asserted_bit_count_fsmd_2p" for hierarchy "asserted_bit_count_fsmd_2p:top"
	286030	Timing-Driven Synthesis is running
	144001	Generated suppressed messages file C:/reconfig2_quartus/labs/lab1/output_files/lab1.map.smsg
	16010	Generating hard_block partition "hard_block:auto_generated_inst"
	21057	Implemented 147 device resources after synthesis - the final resource count might be different
		Quartus Prime Analysis & Synthesis was successful. 0 errors, 0 warnings

Figure 6 - FSM + D Quartus, showing no errors



Type	ID	Message
ℹ	20030	Parallel compilation is enabled and will use 4 of the 4 processors detected
ℹ	12021	Found 1 design units, including 1 entities, in source file /reconfig2/labs/reconfigurable-computing-2/lab1/fsm.sv
ℹ	12021	Found 8 design units, including 8 entities, in source file /reconfig2/labs/reconfigurable-computing-2/lab1/datapath.sv
ℹ	12021	Found 4 design units, including 4 entities, in source file /reconfig2/labs/reconfigurable-computing-2/lab1/asserted_bit_count.sv
ℹ	12127	Elaborating entity "asserted_bit_count" for the top level hierarchy
ℹ	12128	Elaborating entity "asserted_bit_count_fsm_plus_d" for hierarchy "asserted_bit_count_fsm_plus_d:top"
ℹ	12128	Elaborating entity "fsm" for hierarchy "asserted_bit_count_fsm_plus_d:top|fsm:CONTROLLER"
ℹ	12128	Elaborating entity "datapath" for hierarchy "asserted_bit_count_fsm_plus_d:top|datapath:DATAPATH"
ℹ	12128	Elaborating entity "datapath_str" for hierarchy "asserted_bit_count_fsm_plus_d:top|datapath:DATAPATH|datapath_str:top"
ℹ	12128	Elaborating entity "mux2x1" for hierarchy "asserted_bit_count_fsm_plus_d:top|datapath:DATAPATH|datapath_str:top|mux2x1:MUX_N"
ℹ	12128	Elaborating entity "register" for hierarchy "asserted_bit_count_fsm_plus_d:top|datapath:DATAPATH|datapath_str:top|register:N_REG"
ℹ	12128	Elaborating entity "add" for hierarchy "asserted_bit_count_fsm_plus_d:top|datapath:DATAPATH|datapath_str:top|add:SUB_ONE"
ℹ	12128	Elaborating entity "and_gate" for hierarchy "asserted_bit_count_fsm_plus_d:top|datapath:DATAPATH|datapath_str:top|and_gate:N_AND"
ℹ	12128	Elaborating entity "eq" for hierarchy "asserted_bit_count_fsm_plus_d:top|datapath:DATAPATH|datapath_str:top|eq:EQ"
ℹ	12128	Elaborating entity "mux2x1" for hierarchy "asserted_bit_count_fsm_plus_d:top|datapath:DATAPATH|datapath_str:top|mux2x1:CNT_MUX"
ℹ	12128	Elaborating entity "register" for hierarchy "asserted_bit_count_fsm_plus_d:top|datapath:DATAPATH|datapath_str:top|register:CNT_REG"
ℹ	12128	Elaborating entity "add" for hierarchy "asserted_bit_count_fsm_plus_d:top|datapath:DATAPATH|datapath_str:top|add:CNT_ADD"
ℹ	286030	Timing-Driven Synthesis is running
ℹ	16010	Generating hard_block partition "hard_block:auto_generated_inst"
ℹ	21057	Implemented 134 device resources after synthesis - the final resource count might be different
ℹ		Quartus Prime Analysis & Synthesis was successful. 0 errors, 0 warnings

Figure 7 - Datapath Schematic