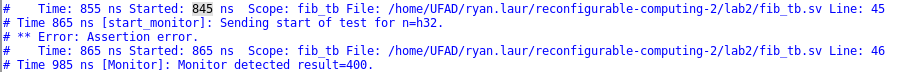
When circuit is restarted, go = ‘1’ and done = ‘1’ (cond) done should be cleared on cycle following assertion of go



Timeline

Description automatically generated

Done is cleared two cycles after go was asserted



A picture containing timeline

Description automatically generated