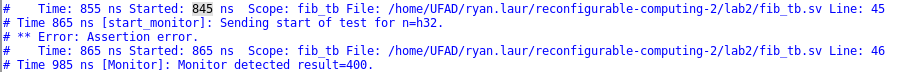
When circuit is restarted, go = ‘1’ and done = ‘1’ (cond) done should be cleared on cycle following assertion of go



Timeline

Description automatically generated

Done is cleared two cycles after go was asserted



A picture containing timeline

Description automatically generated

Infinite Loop for n = 0x3F (max number)

Graphical user interface, application, Word

Description automatically generated

Result Changes when done is asserted

Graphical user interface, application

Description automatically generated

I\_r, x\_r, and y\_r signals from the module were monitored after a check\_for\_done, and compared with the variables used in the theoretical fibonnaci algorithm. The check failed, showing values that are less than the true values, which means the computation is ending before it is truly finished due to changes in input ‘n’.

Graphical user interface

Description automatically generated

X\_r and y\_r full\_add\_r are truncated compared to what they should be. Therefore, the overflow will be incorrect

Text

Description automatically generated