Lab 3 – Timing Optimizations

# Optimization 1:

Figure 1 - Summary of Paths

Table

Description automatically generated with medium confidence

Critical Path: FIFO -> mult\_out

Figure 2 - Statistics showing Cell Data as 68% of the delay

Application, table, Excel

Description automatically generated

Figure 3 - Data Arrival Path Showing dataout[17] with 3.076 delay

Table

Description automatically generated

* Can infer the longest path of 3.076 is talking about the output data from the multiplier
* Can infer it is talking about the FIFO read data coming into the multiplier and the output from the multiplier.

After Optimization:

Table

Description automatically generated

* The same paths still had the worst slack, so I registered the rd\_data output which increased the clock again.

After optimization:

Table

Description automatically generated

# Optimization 2:

Figure 4 - Summary of Paths and Statistics for Optimization 3

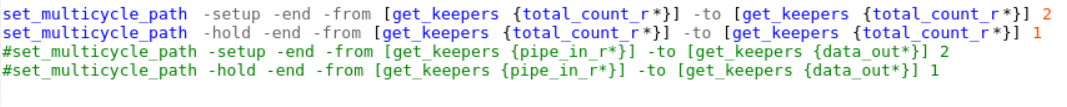
Table

Description automatically generated

### Critical Path:

* total\_count\_r -> total\_count\_r
* Since this signal only gets updated occasionally, it is considered a multicycle path.

### Code Changed:



After Optimization:

Table

Description automatically generated

# Optimization 3:

Summary of Paths and Statistics for Optimization 4

Table

Description automatically generated

Figure 5 - Path of Longest Slack

Diagram, schematic

Description automatically generated

Critical Path: IC and CELL of multiply.

### Code Changed:

* Registered the fifo\_rd\_data signal

After Optimization:

Table

Description automatically generated

# Optimization 4:

Summary of Paths and Statistics for Optimization 5

Graphical user interface, application, table

Description automatically generated

### Critical Path:

* Count\_r

### Code Changed:

* Removed one bit from count\_r, used the almost full signal instead of FULL, removed the rd\_en, since valid\_rd is only based on !empty

After Optimization:

A picture containing table

Description automatically generated

# Optimization 5:

Summary of Paths and Statistics for Optimization 6



Applied faster clock constraint

Graphical user interface, application, table, Excel

Description automatically generated

### Critical Path:

* Total\_count\_r

### Code Changed:

* Increased the multicycle clock path by 1 temporarily to find more bottlenecks

# List of Code Changes

1. Got rid of read during write behavior and optimized the counter
2. Registered the rd\_data output
3. Set up multicycle paths