UNIT-5 & UNIT-6

Objective type question and answer

1. Which of the following is page fault?
   a. Page fault occurs when a program accesses a page of another program
   b. Page fault occurs when a program accesses a page in main memory
   c. Page fault occurs when there is an error in particular page
   d. Page fault occurs when a program accesses a page which is not present in main memory

   Ans: - d
2. Which of the following statements regarding a computer's primary memory is true?
   1. Data loss occurs in the main memory when the power is turned off.
   2. It is faster than secondary memory.
   3. User written program get stored in main memory for use in future
   4. it consists both RAM and ROM
      a. 1 and 2
      b. 1 and 3
      c. 1, 2 and 4
      d. All are correct

   Answer: c
3. Which of the following is correct about the An Auxiliary memory?
   1. the lowest-cost
   2. highest data storing capacity
   3. slowest data transfer speed
   4. small access time

4. Which of the following statements concerning cache memory is true?
   a. Data is briefly stored in cache memory.
   b. It contains the information and program that must be executed quickly.
   c. It requires a shorter access time than RAM does.
   d. All are correct

   Answer: d
5. What does DRAM stand for?
   a. Dynamic Read Access Memory
   b. Digital Random Access Memory
   c. Dynamic Random Access Memory
   d. Dynamic Read Allocation Memory

   Ans: -c
6. Which of the following is correct about the An Auxiliary memory?
   1. the lowest-cost
   2. highest data storing capacity
   3. slowest data transfer speed
   4. small access time
      1. 1 and 2

2. 1 and 3
3. 1,2 and 3
4. All of these

Ans: - 3

7. Which algorithm chooses the oldest page whenever the page required to be replaced?
   a. first in first out algorithm
   b. additional reference bit algorithm
   c. least recently used algorithm
   d. counting based page replacement algorithm
   Ans: - a
8. Cache memory acts between
   (A) CPU and RAM (B) RAM and ROM (C) CPU and Hard Disk (D) None of these
   Ans: A
9. Write Through technique is used in which memory for updating the data
   (A) Virtual memory
   (B) Main memory
   (C) Auxiliary memory
   (D) Cache memory
   Ans: D
10. Generally Dynamic RAM is used as main memory in a computer system as it
    (A) Consumes less power
    (B) has higher speed
    (C) has lower cell density
    (D) needs refreshing circuitry
    Ans: B
11. If the main memory is of 8K bytes and the cache memory is of 2K words. It uses associative mapping. Then each word of cache memory shall be
    (A) 11 bits (B) 21 bits (C) 16 bits (D) 20 bits

    Ans: -c

12. Cache memory works on the principle of(A) Locality of data (B) Locality of memory(C) Locality of reference (D) Locality of reference & memory
    Ans: C
13. The main memory in a Personal Computer (PC) is made of(A) cache memory. (B) static RAM(C) Dynamic Ram (D) both (A) and (B).
    Ans: D
14. What characteristic of RAM memory makes it not suitable for permanent storage? (A) too slow (B) unreliable (C) it is volatile (D) too bulky
    Ans: C
15. What is the series in memory hierarchy from top to bottom?
    (A) Cache memory (B) USB (C) Registers (D) Magnetic Disc
    a. C,A,B,D
    b. C,A,D,B
    c. A,C,D,B
    d. A,C,B,D

    Ans:-a

16. Which of the following is not the part of hardware implementation of Addition and Subtraction:
    a. Parallel subtractor
    b. Parallel adder
    c. Mode of control
    d. Complementor

    Ans:-a
17. In _____ mapping, the data can be mapped in a fixed line in the Cache Memory.
    a) Associative b) Direct c) Set Associative d) Indirect
    Ans:-b
18. Generally Dynamic RAM is used as main memory in a computer system as it (A) Consumes less power (B) has higher speed (C) has lower cell density (D) needs refreshing circuitary
    Ans: B
19. Memory unit accessed by content is called (A) Read only memory (B) Programmable Memory (C) Virtual Memory (D) Associative Memory
    Ans: D
20. Which of the following is correct about the Associative Memory: -
    1. Accessed by content
    2. Uses to search pattern
    3. Uses hardware circuits
    4. Less costly

    a. 1,2
    b. 1,2,3
    c. 1,4
    d. All of these

    Ans:-b
21. For a 3 page frame the following is the reference string:
    7,0,1,2,0,3,0,4,2,3,0,3,2,1,2,0,1
    How many page faults does the LRU algorithm produce?
    a. 10
    b. 11
    c. 12
    d. 15

    Ans:-b
22. For a 3 page frame the following is the reference string:
    7,0,1,2,0,3,0,4,2,3,0,3,2,1,2,0,1,7
    How many page hits does the **optimal** algorithm produce?
    a. 10
    b. 7
    c. 9
    d. 8

Ans- c

23. Subtraction in computers is carried out by -

    a. 1's complement
    b. 2's complement

c. 3's complement
d. 9's complement

Ans:-b

24. Fage Faults related to optmal, decoder lines, memory
25. Which of the following memory unit communicates directly with the CPU?
    a. Auxiliary memory
    b. Main memory
    c. Secondary memory
    d. None of the above

    Ans: b
26. Which of the following techniques used for the page replacement: -
    1. LRU
    2. FIFO
    3. Direct mapping
    4. Associative mapping

    a. 1 only
    b. 1 and 2
    c. 3 and 4
    d. All of these

    Ans:- b

27. In which of the following the performance of cache memory is best?
    a. No. of hits =10, No. of miss =20
    b. No. of hits =20, No. of miss =50
    c. No. of hits =7, No. of miss =10
    d. No. of hits =50, No. of miss =125

    Ans: -c
28. In which of the following the performance of cache memory is best?
    a. No. of hits =5, No. of miss =6
    b. No. of hits =20, No. of miss =50
    c. No. of hits =7, No. of miss =14
    d. No. of hits =50, No. of miss =125

    Ans: -a

29. The multiplication of 110101 * 101010 is performed. What is a general term use for 110101?
    a. Dividend
    b. Quotient
    c. Multiplicand

d. Multiplier

Ans: - c

30. The result obtained on binary multiplication of 1101 * 0101 is……
    a. 1000001
    b. 1000011
    c. 1100001
    d. 1010011

Ans: a

31. What do you call the intermediate terms in binary multiplication?
    a. Multipliers
    b. Mid term
    c. Partial products
    d. Multiplicand

Ans: c

32. For Qn Qn+1 =10 which operation get performed in booth multiplication algorithm?
    a. Addition of AC& BR
    b. Subtraction of AC & BR
    c. Multination
    d. None of these

    Ans: b

33. Which shift operation is used inn booth multiplication
    a. ASHR
    b. ASHL
    c. SHR
    d. SHL

Ans: a

34. In booth multiplication algorithm, arithmetic shifting performed on?
    a. E AC & QR
    b. AC & QR
    c. BR & QR
    d. AC & BR

    Ans: - b

35. If the multiplicand B is 10101001 and multiplier Q is 11111010, then how many add operation are performed in multiplication process to reach final product?
    a. 8
    b. 7
    c. 6

d. 5

Ans: - d

36. The address of a terminal connected to a data communication processor consists of three digits of the 10 numerals. The total number of address is equal to the size of a main memory in bytes. If a Ram size is 128 bytes, then how many minimum numbers of Ram is required to design the memory?
    a. 8
    b. 9
    c. 10
    d. 6

    Ans: - a

37. The address of a terminal connected to a data communication processor consists of two letters of the alphabet or a letter and one of the 10 numerals. The total number of addresses is equal to the size of a main memory in bytes. If a Ram size is 128 bytes, then how many minimum numbers of Ram is required to design the memory?
    a. 8
    b. 16
    c. 32
    d. 4

    Ans: - b

38. Consider a memory system with cache- access time of 100 n sec and a memory access time is 1200 n sec. If the effective time is 20% greater than the ache access time, what is the hit ratio(H)?
    a. 119/120
    b. 180/190
    c. 118/120
    d. 108/110

    Ans :- c

39. In Add and Subtract Operation algorithm E= 0 represents that:-
    a. A>B
    b. A<B
    c. A=B
    d. All of these

    Ans:- b

40. How many 128 x 8 RAM chips are needed to provide a memory capacity or 2048 bytes?
    a. 12
    b. 13

c. 14
d. 16

Ans: -d

41. How many 128 x 8 RAM chips are needed to provide a memory capacity or 1024 bytes?
    a. 64
    b. 8
    c. 32
    d. 16

    Ans: - b

42. How many 128 x 8 RAM chips are needed to provide a memory capacity or 4096 bytes?
    a. 64
    b. 32
    c. 8
    d. 16

    Ans; -b

43. A 128 x 8 RAM chips are used to provide a memory capacity or 4096 bytes. How many lines must be decoded for chip select in decoder?
    a. 2
    b. 3
    c. 4
    d. 5

    Ans: - d

Mathematical questions: -

44. Consider a direct mapped cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Number of bits in tag is:-
45. Consider a direct mapped cache of size 8 KB with block size 1 KB. There are 4 bits in the tag. Size of main memory is:-
    a. 128 KB
    b. 64 KB
    c. 256 KB
    d. 32 KB
    Ans :- a
46. In cache direct mapping, the address of CPU gets divided into which two parts?
    a. Index, Code

b. Sequence, Tag
c. Index, Tag
d. None of above

Ans: - c

47. Computer memory used as backup storage is called_____.
    a. cache memory
    b. virtual memory
    c. auxiliary memory
    d. main memory

    Ans: -c

48. The magnetic disk's surface is divided into a number of invisible concentric circles called:
    a. Drives
    b. Tracks
    c. Spindle
    d. Sectors

    Ans: - b

49. The smallest physical storage unit on the magnetic disk is called: -
    a. Drives
    b. Tracks
    c. Spindle
    d. Sectors

    Ans: - d

50. Consider a direct mapped cache of size 8 KB with block size 4 bytes. The CPU generates 16-bit address. The no. of bits required for cache indexing (Line bits) and bits respectively: -
    a. 3,11
    b. 4,10
    c. 5,9
    d. 6,10

    Ans:- a

51. Consider a direct mapped cache of size 4 KB with block size 4 bytes. The CPU generates 16-bit address. The no. of bits required for cache indexing (Line bits) and bits respectively: -
    a. 3,11
    b. 4,10
    c. 5,9
    d. 6,10

    Ans:-b

52. Consider a direct mapped cache of size 2 KB with block size 4 bytes. The CPU generates 16-bit address. The no. of bits required for cache indexing (Line bits) and bits respectively: -
    a. 3,11
    b. 4,10
    c. 5,9
    d. 6,10

Ans: - c

53. The disk platters mounted on a spindle and the heads mounted on a disk arm are together known as _____

a) Read-disk assemblies

b) Head–disk assemblies

c) Head-write assemblies

d) Read-read assemblies

Ans: - b

54. A computer system has a cache with cache access time 20ns, hit ratio of 80% and average memory access time of 36ns. The access time for physical memory is ……. ns?
    a. 100
    b. 120
    c. 80
    d. 50

Ans: - a

55. If the size of a main memory (in KB) is given by the value of the postfix expression 4 7 2 1 + – *?. If a Ram size is 256*8, then how many minimum numbers of Ram is required to design the memory?

    a. 64
    b. 128
    c. 32
    d. 256

Ans: -64

56. If the size of a main memory (in KB) is given by the value of the postfix expression (4 7 2 1 + – *?). If a Ram size is 64*8, then how many minimum numbers of Ram is required to design the memory?

    a. 64
    b. 128
    c. 32
    d. 256

Ans:-d

57. For Qn Qn+1 =01 which operation get performed in booth multiplication algorithm?
    a. Addition of AC& BR
    b. Subtraction of AC & BR
    c. Multination

d. None of these

Ans: - a

58. In Add and Subtract Operation algorithm E= 1 represents that:-
    a. A>B
    b. A<B
    c. A=B
    d. None of these

    Ans: - d

59. Each stage in pipelining should be completed within _____ cycle.
    a. 1
    b. 2
    c. 3
    d. 4

    Ans: - a

60. The pipeline included in the RISC processor has ....stages?
    a. 4
    b. 6
    c. 5
    d. 16

    Ans:- c

61. Pipelining is a ----------technique?
    a. Serial operation
    b. Parallel operation
    c. Scalar operation
    d. Superscalar operation

    Ans:- b

62. A 4-stage pipeline has the stage delays as 150, 120, 160 and 140 nanoseconds respectively. Registers that are used between the stages have a delay of 5 nanoseconds each. Assuming constant clocking rate, the total time taken to process 1000 data items on this pipeline will be
    a. 120.4 microseconds
    b. 160.5 microseconds
    c. 165.5 microseconds
    d. 590.0 microseconds

Solution: -

Delay between each stage is 5 ns.

Total delay for 1st data item = 165*4
= 660
For 1000 data items,
first data will take 660 ns to complete and
rest 999 data will take max of all the stages
that is 160 ns + 5 ns register delay
Total Delay = 660 + 999*165 ns
which is equal to 165.5 microsecond.
Note: time taken in pipelining process (tp) = 1x k x t + (n-1)x t ; where t is the time taken in one clock pulse.

63. Consider a non-pipelined processor with a clock rate of 2.5 gigahertz and average cycles per instruction of four. The same processor is upgraded to a pipelined processor with five stages; but due to the internal pipeline delay, the clock speed is reduced to 2 gigahertz. Assume that there are no stalls in the pipeline. The speed up achieved in this pipelined processor is _____. [Gate-2015]
    A. 3.2
    B. 3.0
    C. 2.2
    D. 2.0

    Ans:- b