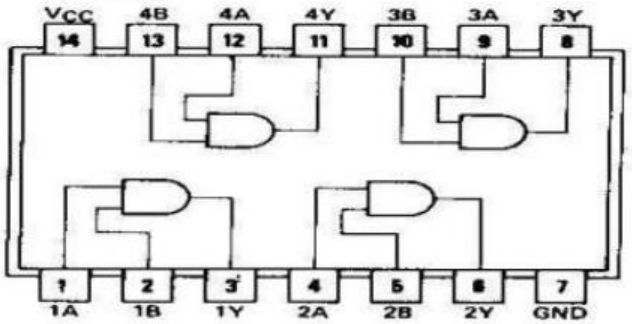
DIGITAL ELECTRONICS LABORATORY ECE-279

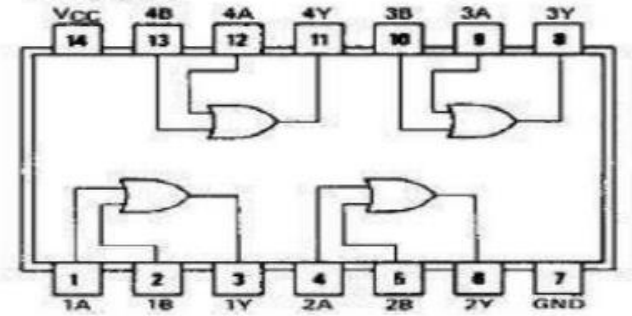
EXPERIMENT :- 6

To analyse and implement Boolean expression using basic logic (AND, OR, NOT, NAND, NOR, XOR, XNOR

7408



7432



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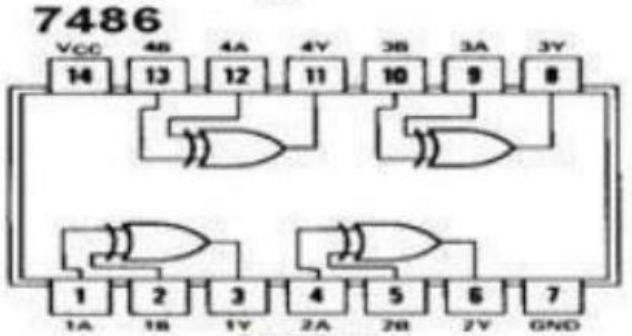

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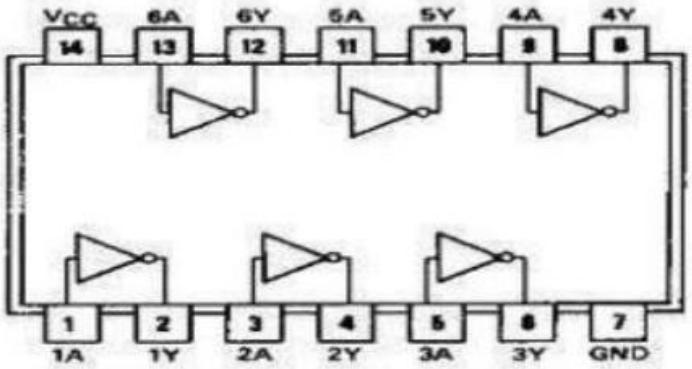

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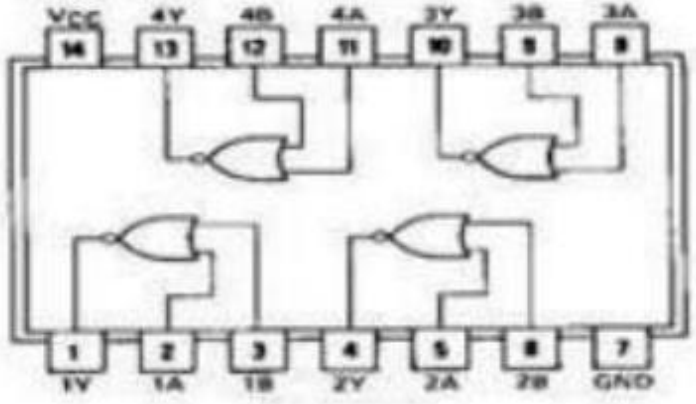

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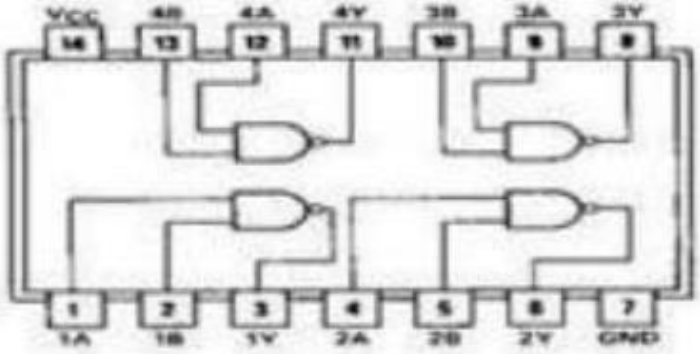
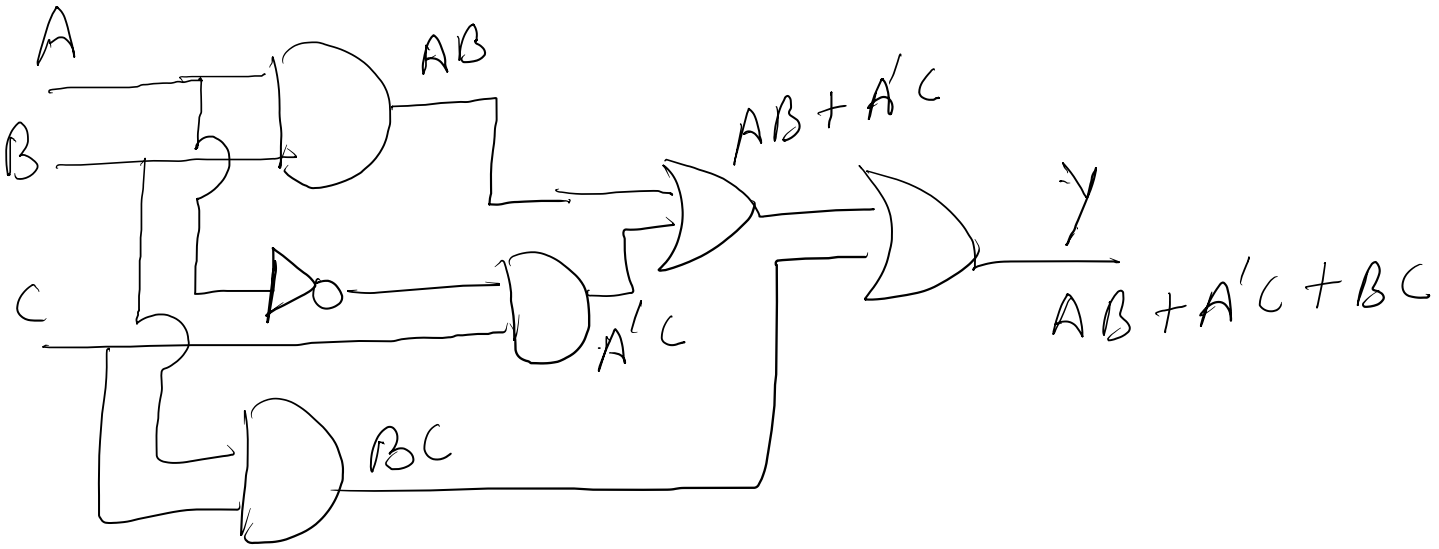


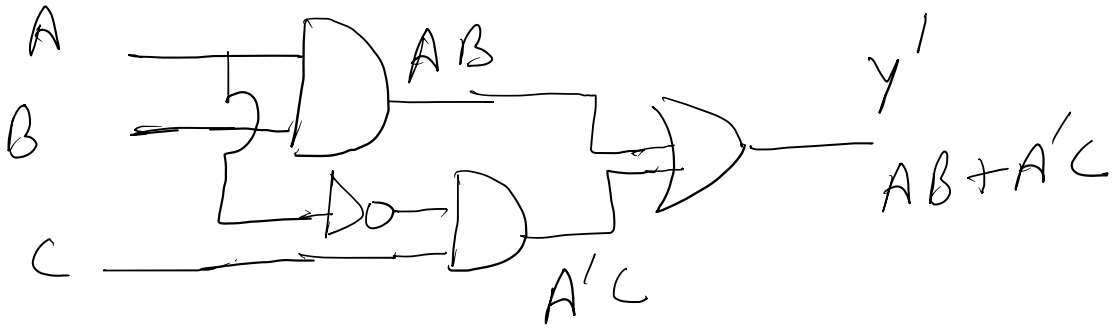
Implement boolean equation

AB+A'C+BC= AB+ A'C

L.H.S



R.H.S

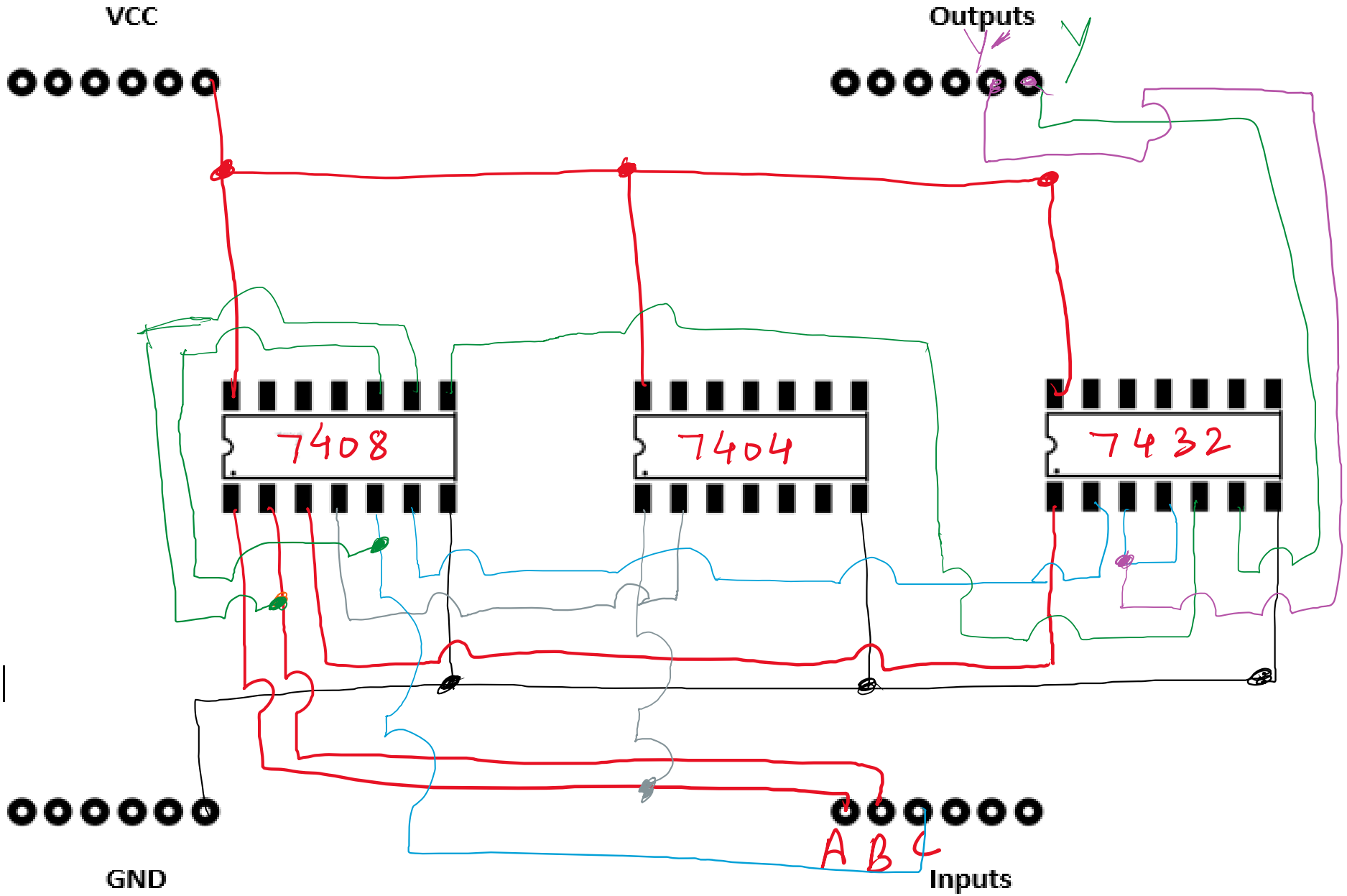


Truth Table

A	B	C	A’	AB	A’C	BC	Y’=AB+ A’C	Y=AB+A’C +BC
0	0	0	1	0	0	0	0	0
0	0	1	1	0	1	0	1	1
0	1	0	1	0	0	0	0	0
0	1	1	1	0	1	1	1	1
1	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0
1	1	0	0	1	0	0	1	1
1	1	1	0	1	0	1	1	1

Implement boolean equation

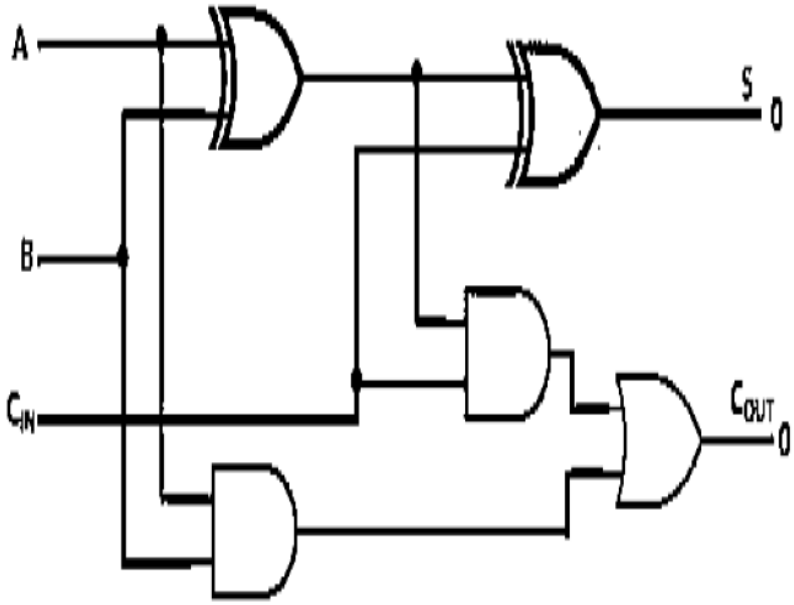
AB+A'C+BC= AB+ A'C



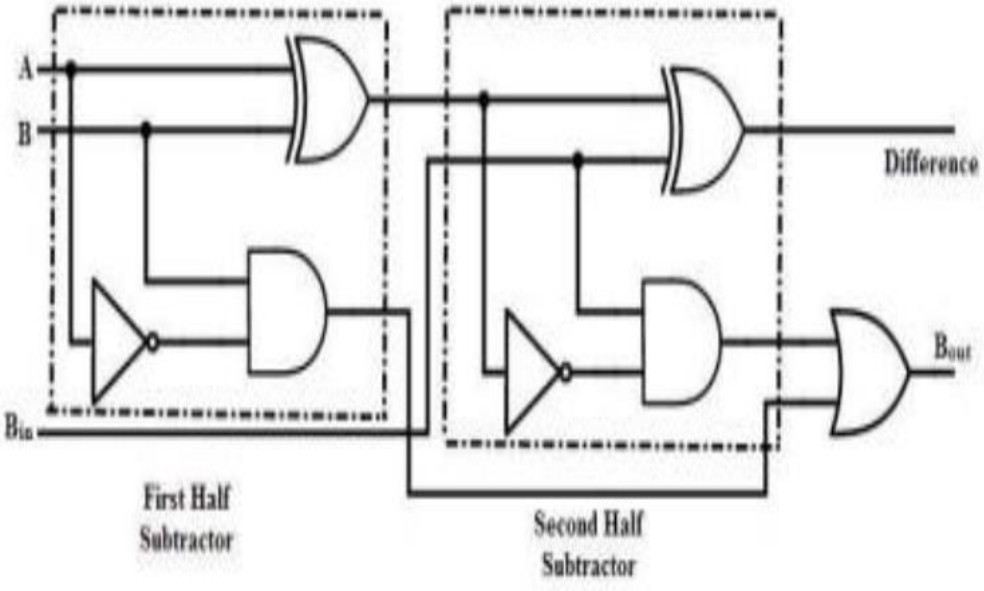
EXPERIMENT :- 7

To design a circuit for full Adder and full Subtractor using XOR and basic gates

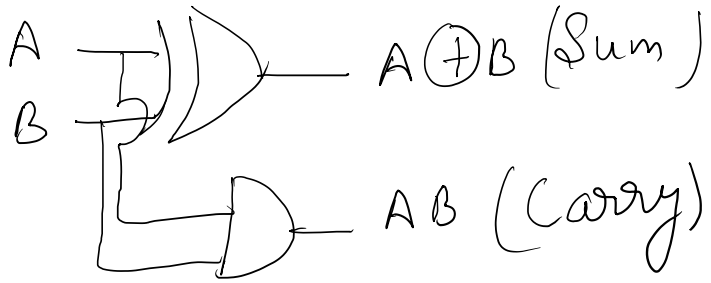
1). Full Adder using two half adders



2). Full Subtractor using two half subtractor

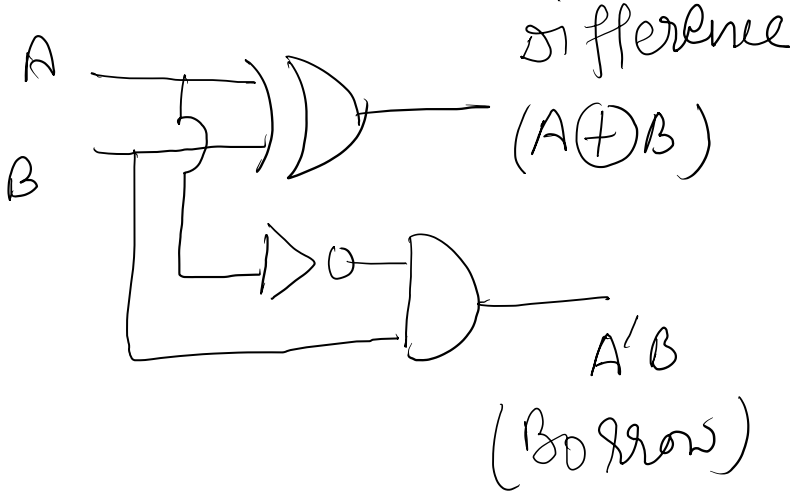


HALF ADDER →



A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Half Subtractor →



A	B	Diff.	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Full Adder

Sum → $\bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$

$= C(\bar{A}\bar{B} + AB) + \bar{C}(\bar{A}B + A\bar{B})$

$= C(\overline{A \oplus B}) + \bar{C}(A \oplus B)$

$= A \oplus B \oplus C$

carry → $\bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$

$= C(\bar{A}B + A\bar{B}) + AB(\bar{C} + C)$ $\quad (\because \bar{C} + C = 1)$

$= C(A \oplus B) + AB$

Full Subtractor

Difference $\Rightarrow$ $\bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$

$\Rightarrow C(\bar{A}\bar{B} + AB) + \bar{C}(\bar{A}B + A\bar{B})$

$\Rightarrow C(\overline{A \oplus B}) + \bar{C}(A \oplus B)$

$\Rightarrow A \oplus B \oplus C$

Borrow $\rightarrow$ $\bar{A}\bar{B}C + \bar{A}B\bar{C} + \bar{A}BC + ABC$

$\Rightarrow C(\bar{A}\bar{B} + AB) + \bar{A}B(\bar{C} + C)$ $(\because \bar{C} + C = 1)$

$\Rightarrow C(\overline{A + B}) + \bar{A}B(1)$

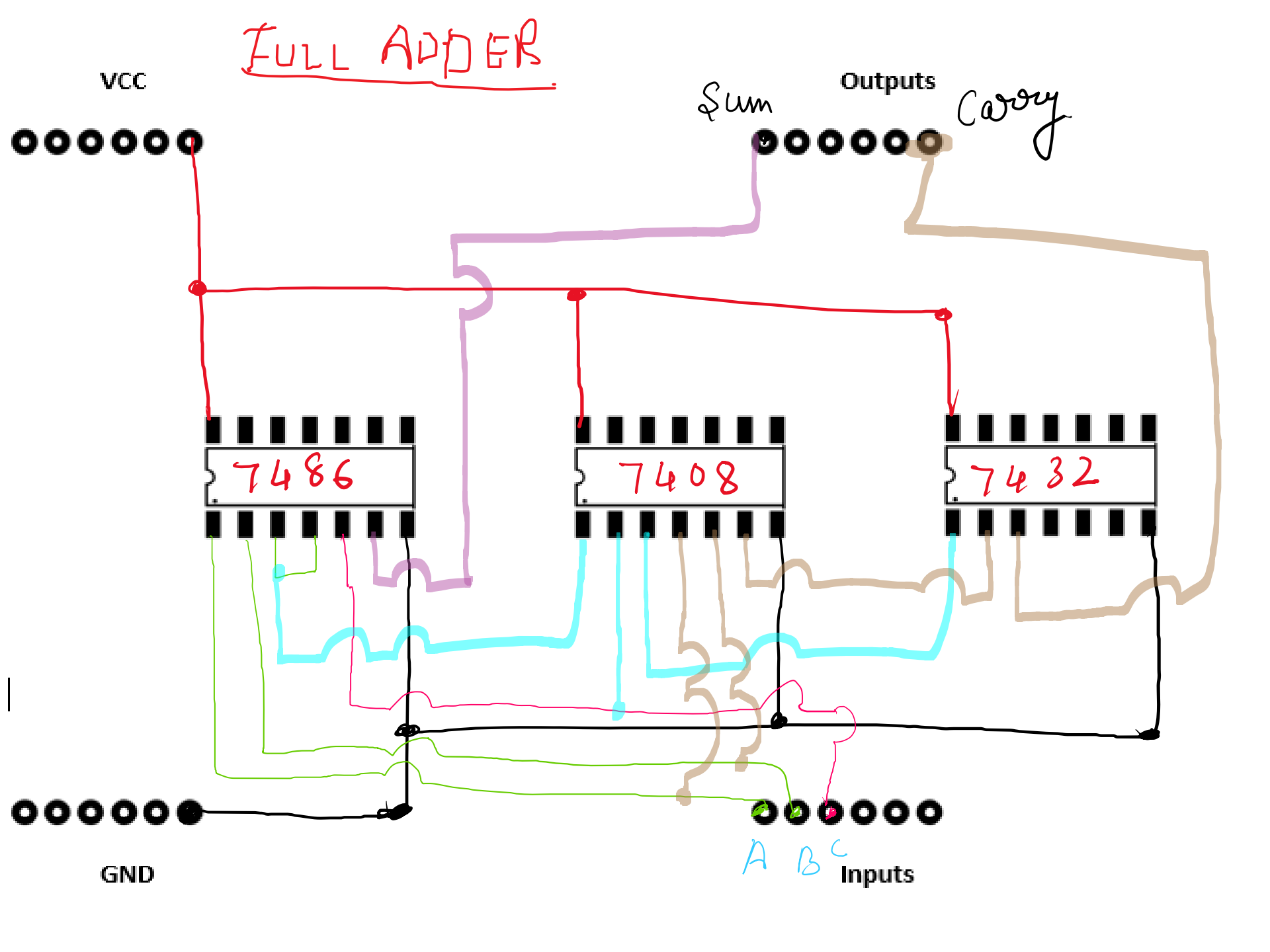
$= C \cdot (\overline{A + B}) + \bar{A}B$

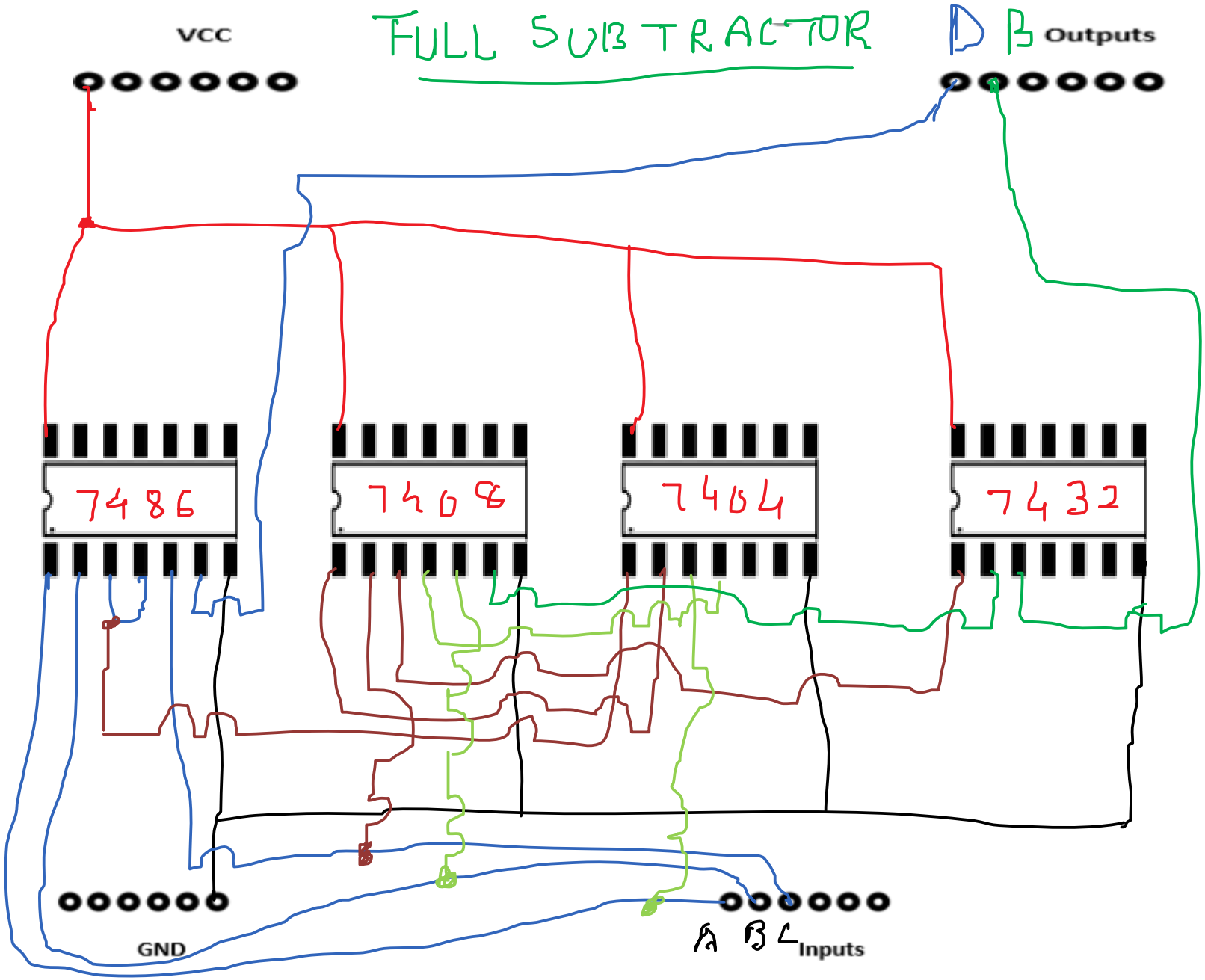
Full Adder truth table

A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Full Subtractor truth table

A	B	C	Diff.	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

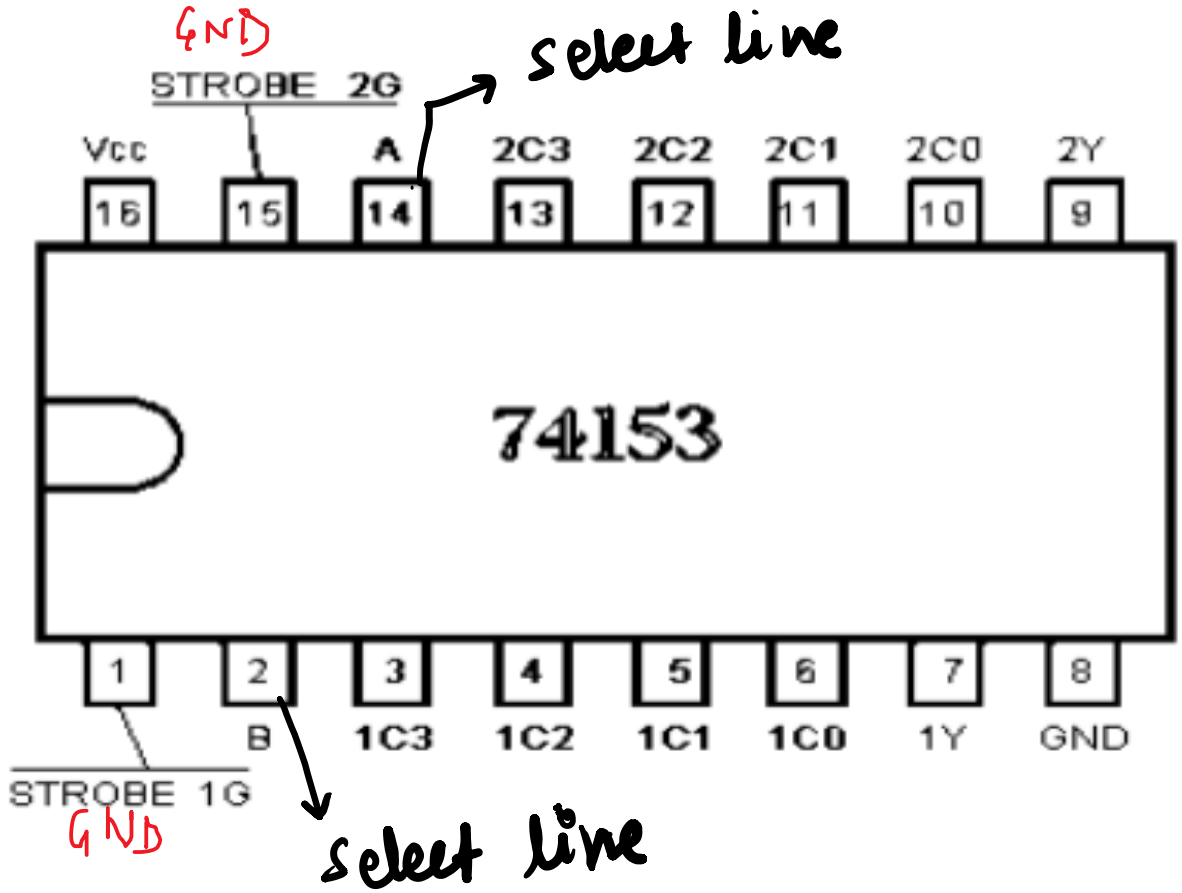

FULL ADDER
VCC
Outputs
Sum
Carry
7486
7408
7432
GND
A B C
Inputs


FULL SUBTRACTOR
VCC
D B Outputs
7486
7408
7404
7432
GND
A B C Inputs

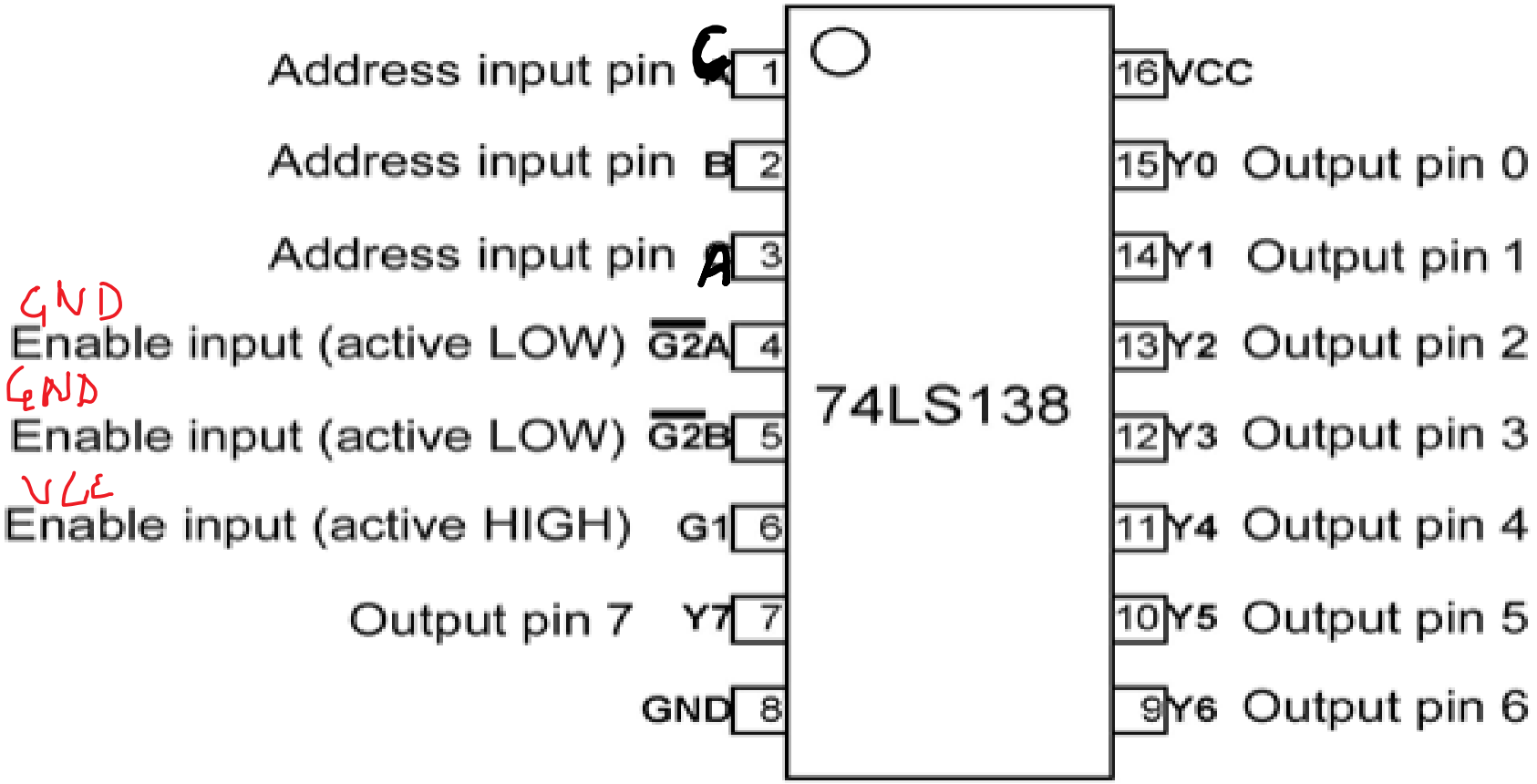
EXPERIMENT :- 8

1. **Aim: To design a circuit to implement Boolean functions using Multiplexers.**
2. **Aim: To design a circuit to implement Boolean functions using Decoders.**

MULTIPLEXER IC

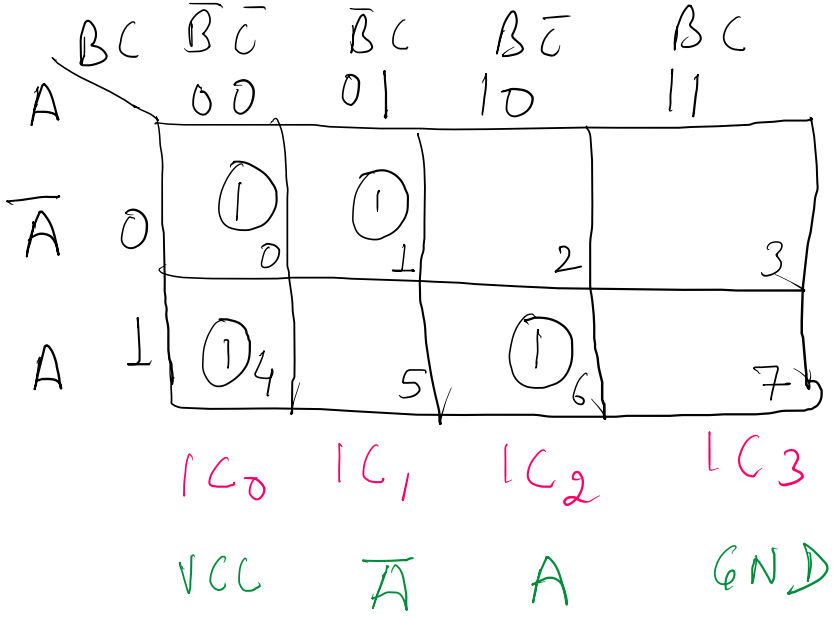


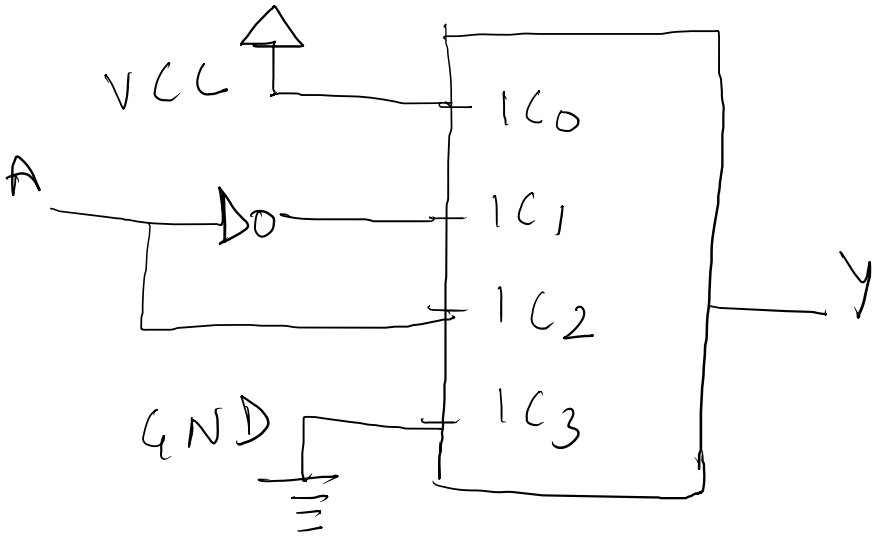
3:8 DECODER IC



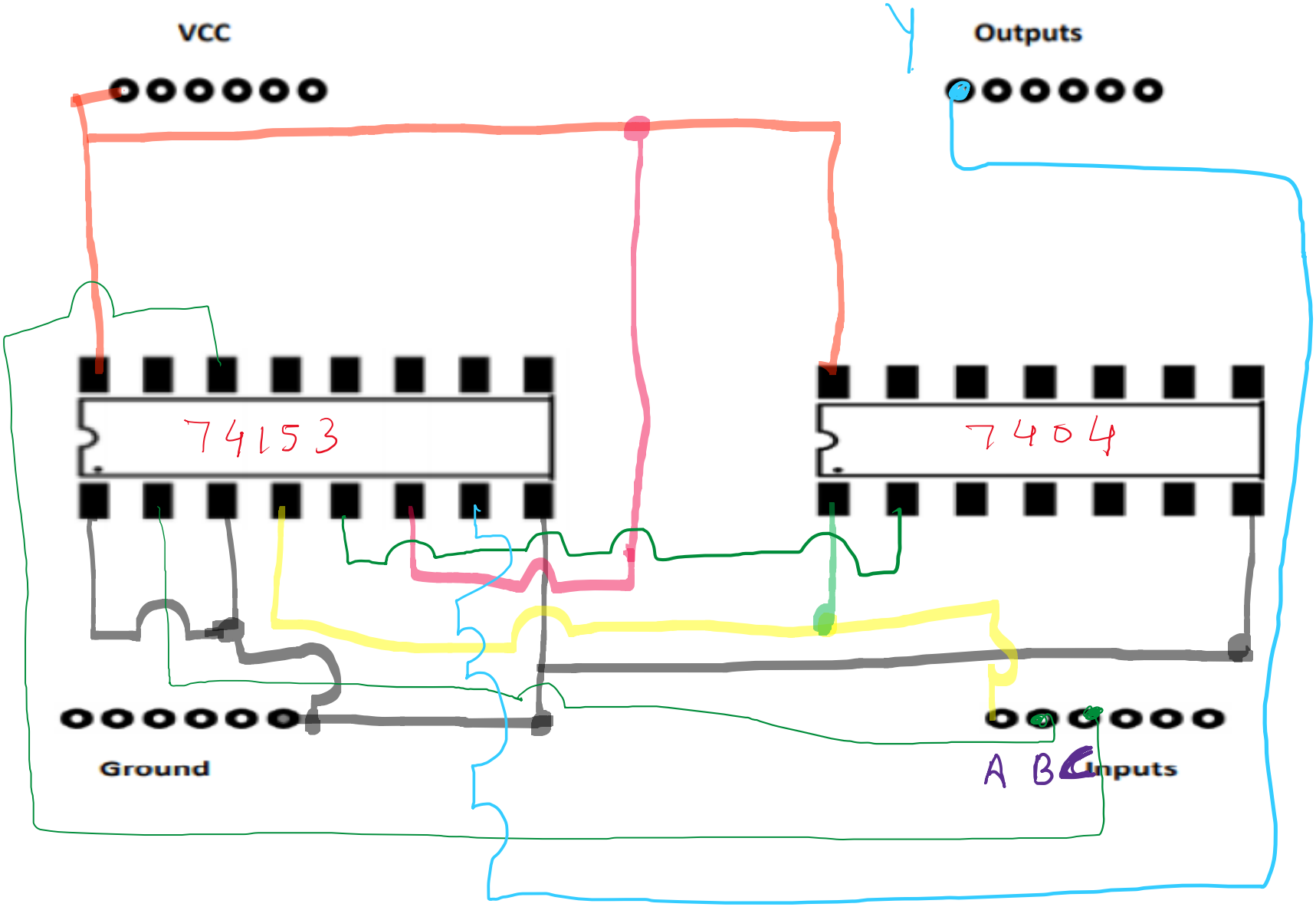
Multiplexer → $\Sigma m(0,1,4,6)$ (select line BC)

mux mapping →





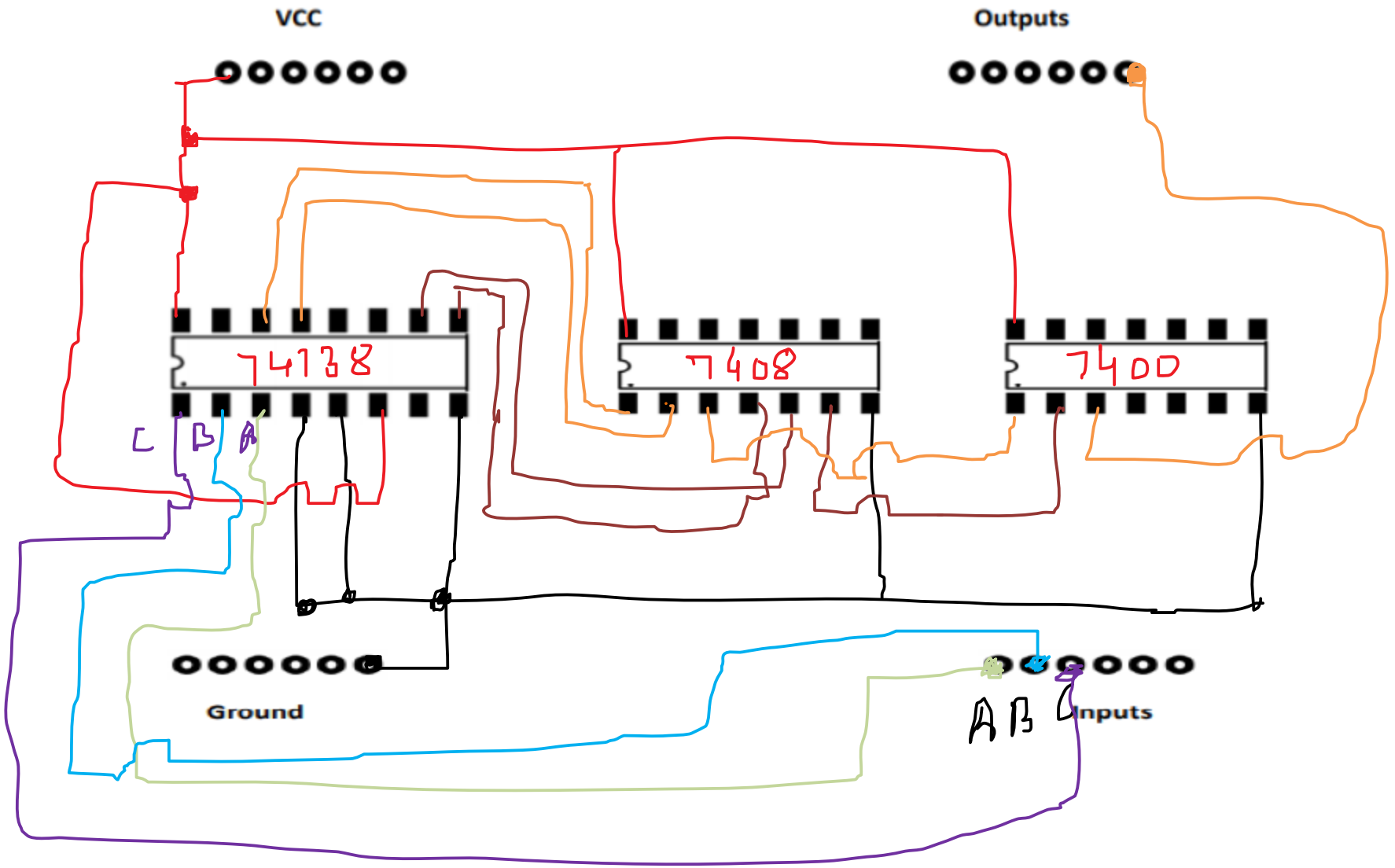
4:1 MUX → $\sum m(0,1,4,6)$ select line BC



$\Sigma m(0,1,4,6)$ (4:1 MUX)

ABC	O/P
000	1
001	1
010	0
011	0
100	1
101	0
110	1
111	0

3:8 Decoder → Im (1,2,5,6)



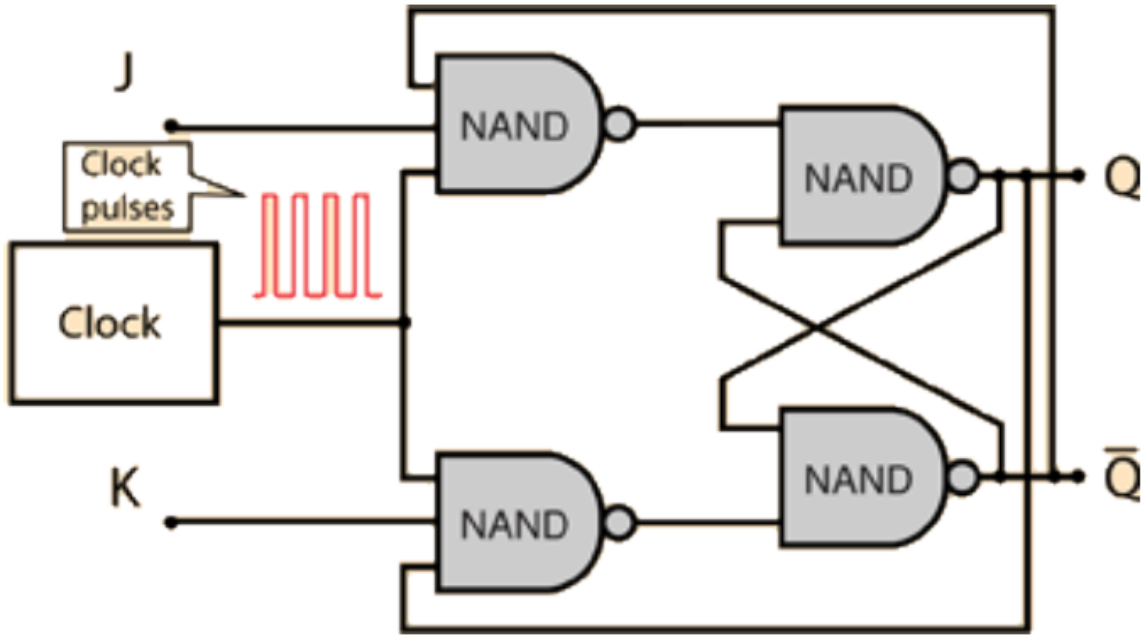
$\Sigma m(1, 2, 5, 6)$, 3:8 Decoder

ABC	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
000	0	0	0	0	0	0	0	0
001	0	1	0	0	0	0	0	0
010	0	0	1	0	0	0	0	0
011	0	0	0	0	0	0	0	0
100	0	0	0	0	0	0	0	0
101	0	0	0	0	0	1	0	0
110	0	0	0	0	0	0	1	0
111	0	0	0	0	0	0	0	0

Experiment-9

Understanding the sequential logic by implementing the flip flop with the help of logic gates

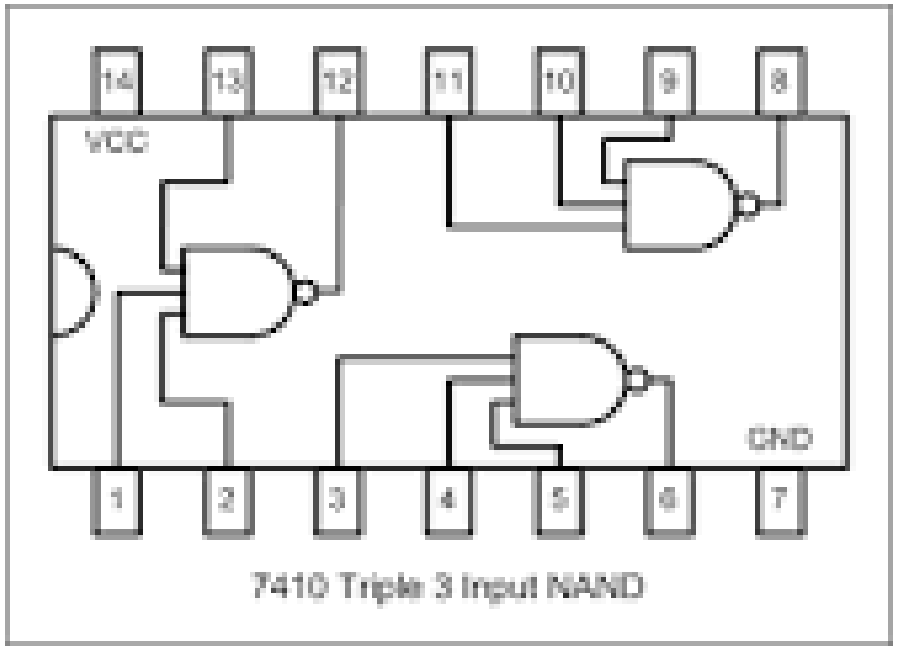
J-K flip-flop

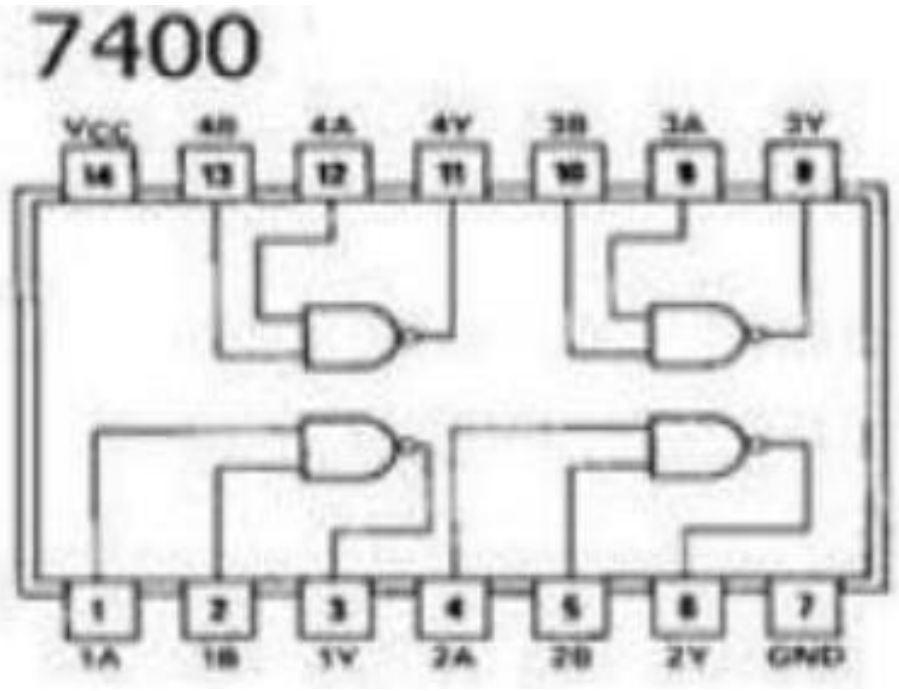


J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	$\overline{Q}$ (t)

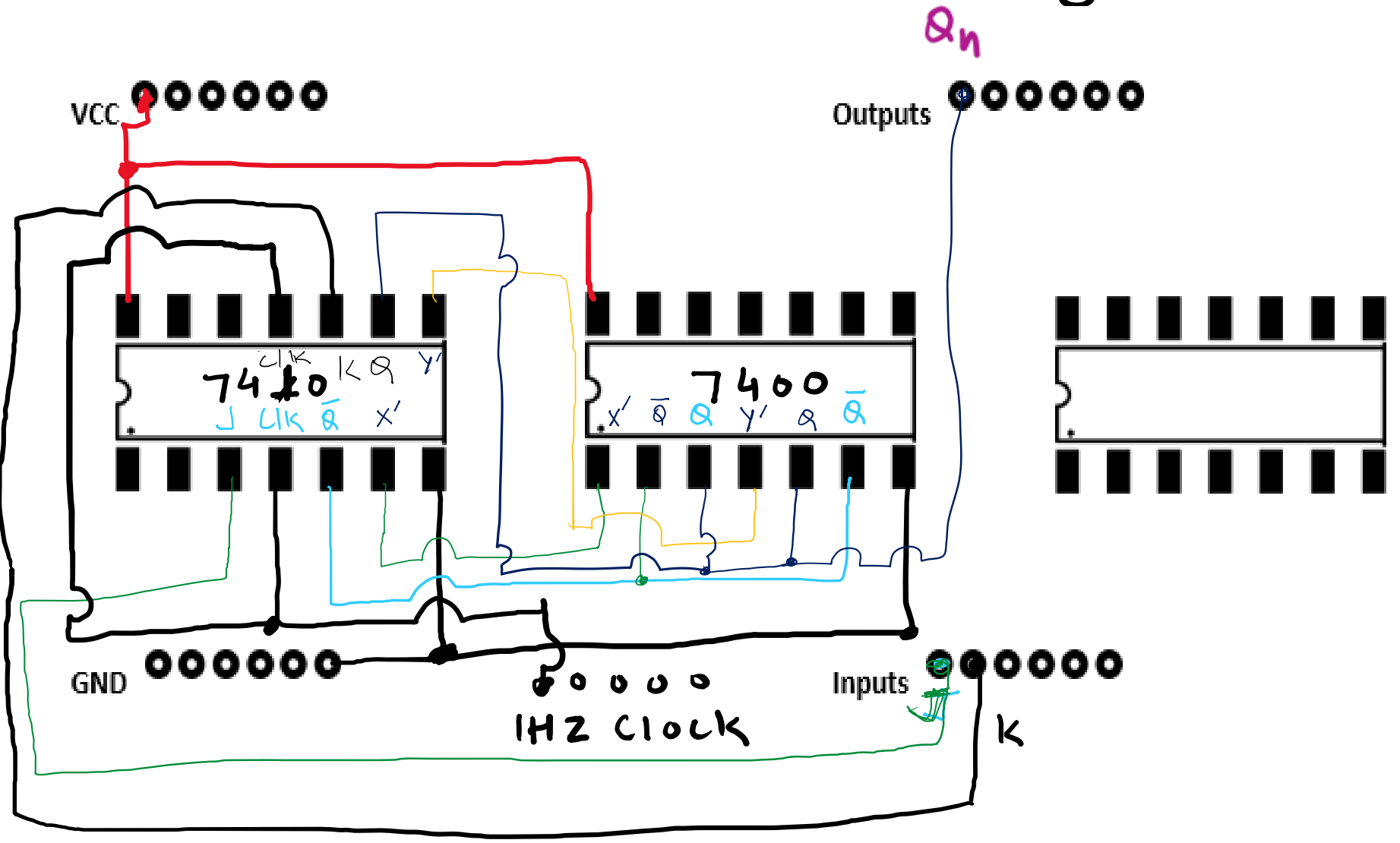
Pin Diagram

7410



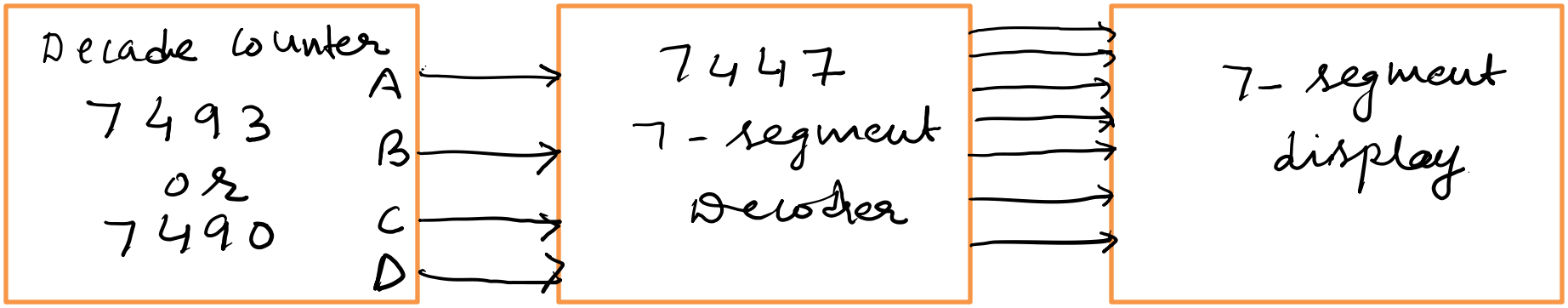


Virtual bread board diagram

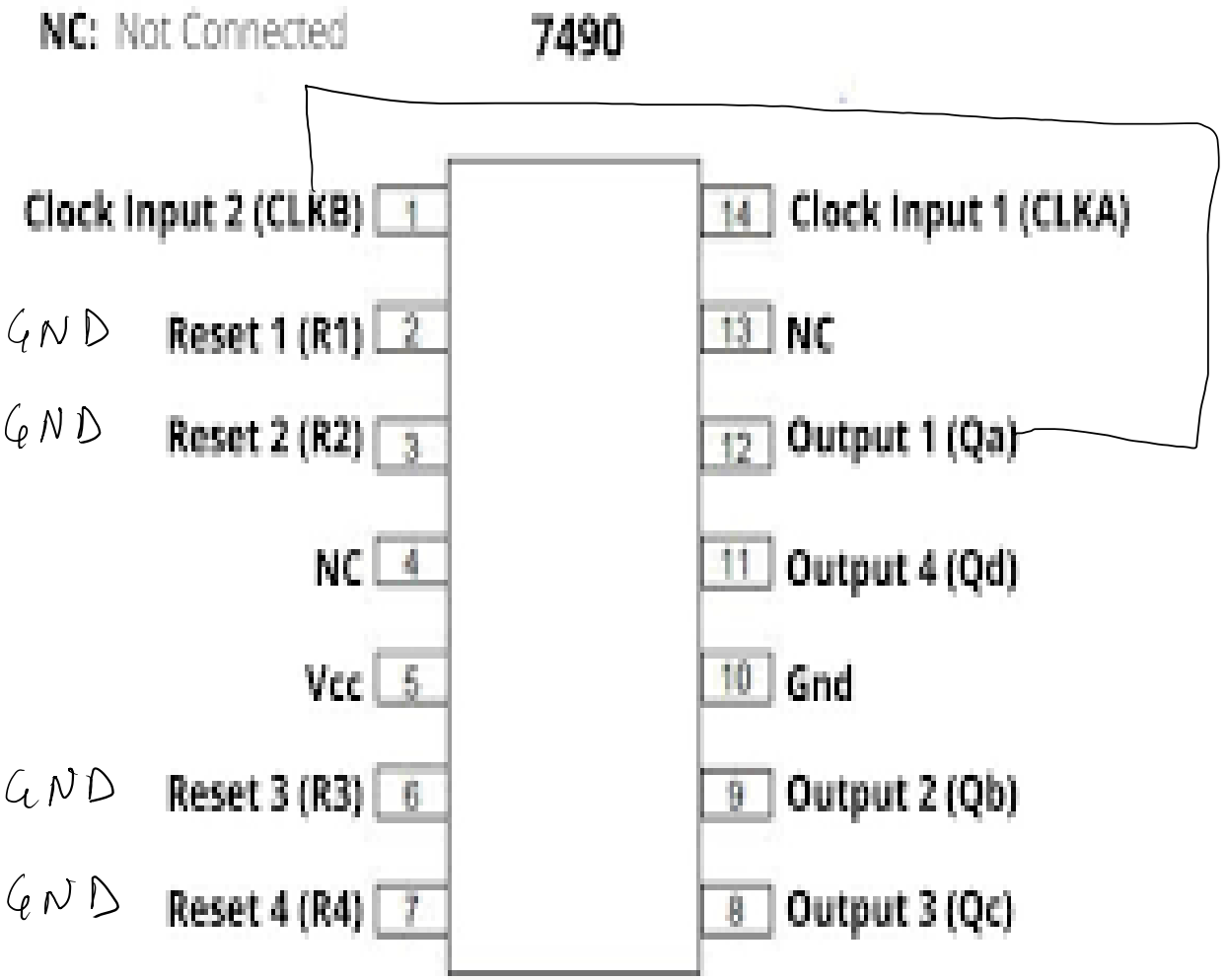


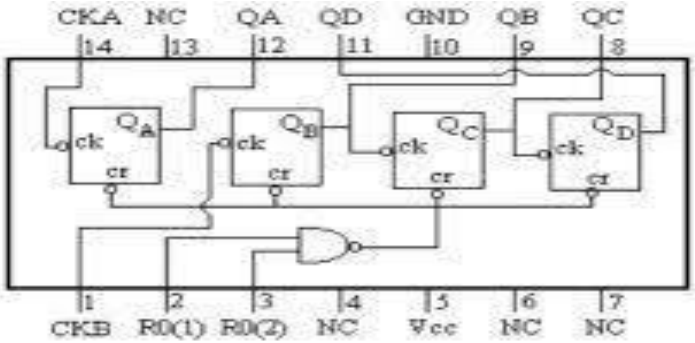
Experiment 10

To visualize the output of decade counter on seven segment display



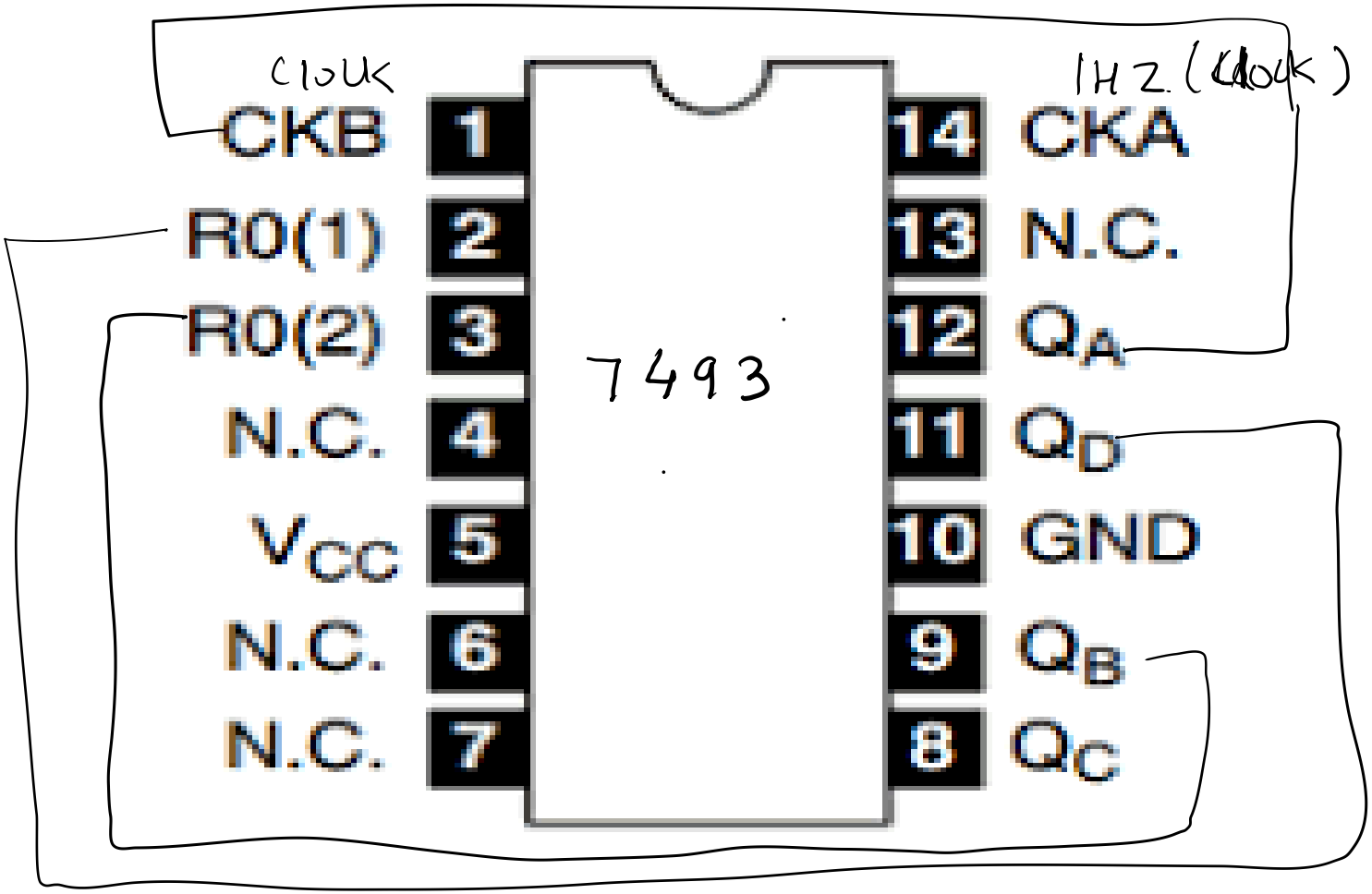
Pin Configuration



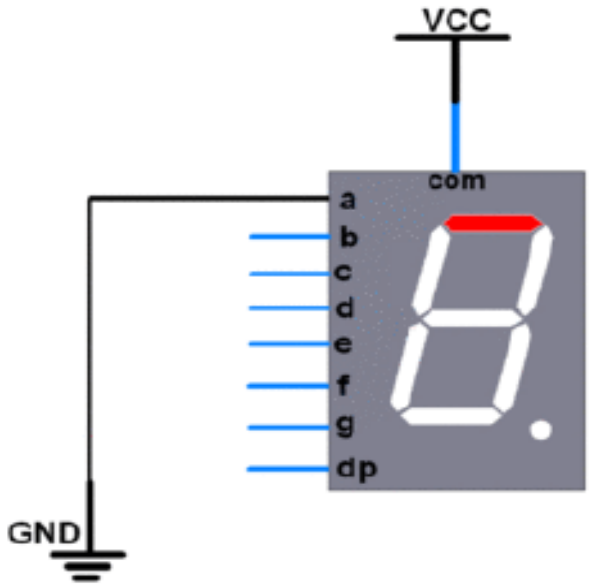


Pin Configuration

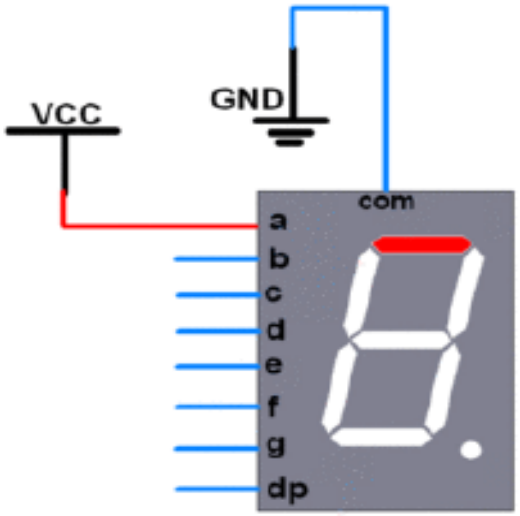
nnection Diagram



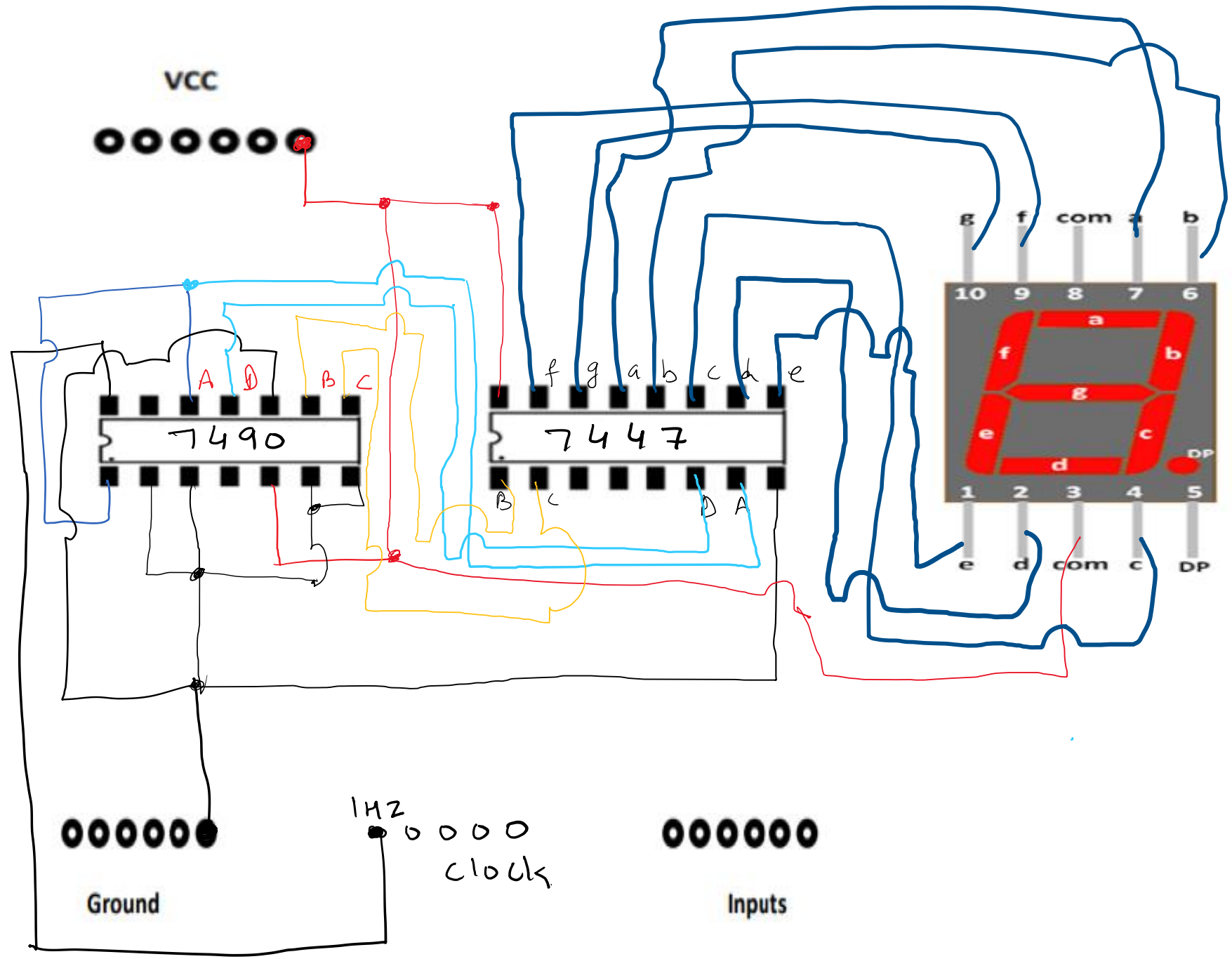
Testing of 7 segment display

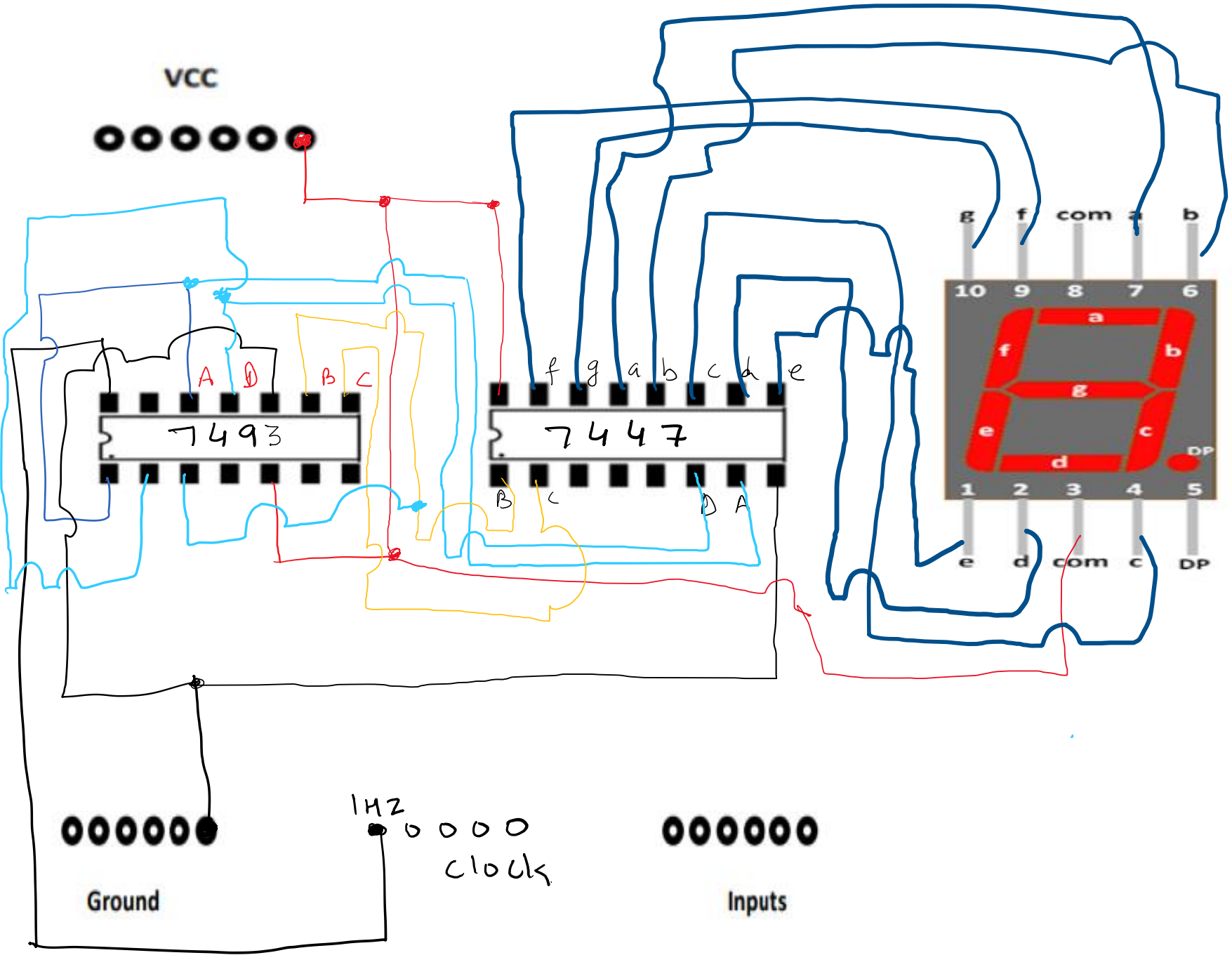


Common Anode



Common Cathode


VCC
7490
7447
A
D
B
C
f g a b c d e
B
C
D
A
g f com a b
10 9 8 7 6
a
f
b
g
e
c
d
DP
1 2 3 4 5
e d com c DP
1HZ
clock
Ground
Inputs


VCC
7493
7447
A
D
B
C
f
g
a
b
c
d
e
g
f
com
a
b
10
9
8
7
6
1
2
3
4
5
e
d
com
c
DP
1HZ
clock
Ground
Inputs