1. Which of the following is incorrect about GPU
   A. GPU is similar to CPU
   B. GPU has large number of cores for faster processing
   C. GPU has big cache, few threads
   D. GPU mainly rely on multi-threading

2. In multiprocessor, graceful degradation is
   A. Ability to continue working even if one processor fail
   B. Ability to continue working even if Shared Memory fail
   C. both A and B
   D. none of the above

3. The bus-based multiprocessors are

   (a) without cache

   (b) with cache

   (c) with cache and private memory

   A. only a and b

   B. only b & c

   C. only a and c

   D. a, b and c are correct

4. Which of the following is not an example of the Physical forms available for interconnection network in a multiprocessor

A. Time shared common bus

B. Frequency shared common bus

C. Cross bar Switch

D. Multiport Memory

5. Which of the following statements is/are correct

(A) Multiprocessor has separate memory and single CPU

(B) Multiprocessor has shared Memory with multiple CPUs

(C) The CPUs in Multiprocessor can have master-slave relationship only

   A. Only A is correct

   B. Only B is correct

   C. B & C are correct

   D. A, B are correct

6. Which of the following is not correct about ARM processor

A . Low power consumption

B . Complex Circuit

C. It can't be used in Windows

D. Scheduling instructions is difficult

7. Memory Hierarchy in terms of access speed is

A. Cache> Main Memory>Register

B. Register> Cache> Main Memory

C. Register> Main Memory Cache

D. Main Memory>Register> Cache

8. Which of the following is not an example of the Physical forms available for interconnection network in a multiprocessor

A. Time shared common bus

B. Frequency shared common bus

C. Cross bar Switch

D. Multiport Memory

9. Parallel Processing is applicable at

A. Job level only

B. task level only

C. instruction level only

D. All of the above

10. Which of the following is not an example of shared memory multiprocessor models

A. UMA

B. NUMA

C. PUMA

D. COMA

11. In a associative Memory, the smallest unit cell C has

A. J-K Flip flop

B. D flip flop

C. S-R flip flop

D. T flip flop

12. The bus-based multiprocessors are

(a) without cache

(b) with cache

(c) with cache and private memory

A. only a and b

B. only b & c

C. only a and c

D. a, b and c are correct

13. Which of the following memory is also known as content addressable memory

A. Virtual Memory

B. Auxiliary Memory

C. Cache Memory

D. Associative Memory

14. _mapping stores both address and the content of the memory word

A. Direct Mapping

B. Associative Mapping

C. Set associative mapping

D. None of the above

15. Hit Ratio is associated with

A. Cache Memory

B. Virtual Memory

C. Associative Memory

D. Main Memory

16. Tracks and sectors are associated with

A. Magnetic tapes

B. Magnetic Drives

C. Pen Drives

D. All of the above

17. Hardware organization of Content Addressable Memory includes

A. Argument register only

B. Key register

C. Match register

D. All of the above

18. Associative mapping procedure is related to

A. Cache Memory

B. Virtual Memory

C. Associative memory

D. Auxiliary Memory

19. Which of the following is a replacement algorithm used for page replacement

A. Least Recently Used

B. Least Recently Utilized

C. Least Recurrently Used

D. Last Recently Used

20. Address space and Memory space is associated with which of the memory types

A. Cache Memory

B. Content Addressable Memory CAM

C. Virtual Memory

D. Auxiliary Memory

21. Consider the following statements

a) FIFO replacement policy is easy to implement

b) In FIFO, under certain circumstances pages are removed and loaded from memory too frequently

A. Only A is correct

B. Only B is correct

C. Both A and B are correct

D. None of the above

22. If in a associative memory, Argument register A = 110111000 and Key register K=000111000 then the correct content in the match register M from the following will be

A. 110000111

B. 101111011

C. 101110111

D. 111101111

23. Which of the following is NOT an example of Input-output command

A. Control

A or D not confirm

B. Status

C. Data

D. all of the above

24. Which of the following is an example of Output device

A. Card Puncher

B. Card Reader

C. Optical Mark Reader

D. Bar Code Reader

25. MUX can be used to design

A. Adders only

B. Fundamental Gates only

C. Universal Gates only

D. All of the above

26. To perform a logical AND operation, which of the following symbol is used

A. <

B. >

C. ^

D. +

27. In a asynchronous Data transfer

a) Internal timing in CPU and interface is dependent

b) It requires control signals be transmitted to indicate the time of data being transmitted

A. Only A is correct

B. Only B is correct

C. Both A and B are correct

D. None of the above

28. Which of the following is incorrect about Input-Output Interface

A. It decodes the device address

B. It decodes the Command (Operations)

C. Provides Signal for D. Peripheral Controller

D. none of the above

29. Input-Output Interface resolves the difference between

A. CPU and Memory

B. Computer and Peripheral Devices

C. Memory and Peripheral Devices

D. None of the above

30. Input-output Interface includes

A. Timing and control Unit

B. Control and Status register

C. Port registers

D. All of the above

31. Which of the following statements is/are correct

A) Isolated I/O is more efficient than the Memory mapped 1/0

B) Memory mapped I/O has increased memory due to addition of I/O

A. Only A is correct

B. Only B is correct

C. Both A and B are correct

D. None of the above

32. In programmed I/O method,

a) CPU stays in loop until the I/O unit indicated that it is ready for the data transfer

b) It is a time consuming process

A. Only A is correct

B. Only B is correct

C. Both A and B are correct

D. None of the above

33. Which of the following is/are correct

A) In programmed I/O, CPU stays in a program loop until the I/O unit indicate that it is ready for data transfer

B) The problem mentioned above can be solved by using Interrupts

A. Only A is correct

B. Only B is correct

C. Both A and B are correct

D. None of them is correct

34. Consider the following statements

i. Memory mapped I/O is less efficient than Isolated 1/0

ii. Memory mapped I/O is larger in size than Isolated 1/0

A. Only i is correct

B. only ii is correct

C.both i and ii are correct

D.None of the above

35. Memory mapped I/O has

A. Increased addressing memory due to the memory mapped I/0

B. decreased addressing memo due to the memory mapped I/0

C. Separate control line

D. none of the above

36. Isolated input-output has

A. common address and control bus but separate data bus

B. common address and data bus but separate control bus

C. common control and data bus but address control bus

D. common address, data and control bus

37. Which of the following is a NOT feature of RISC computers

A. Few instructions

B. Few addressing modes

C. variable length instruction

D. hardwired control unit

38. Which of the following is correct about CISC computers

A. the instructions acts indirectly on memory address

B. machine instructions are designed to match high level language

C. both A and B

D. none of the above

39. What will the output of the given instruction: ADD R1, R2

A. Add the content of R1 and R2 and move the result to R2

B. Add the content of R1 and R2 and move the result to R1

C. Add the content of R1 and R2 and move the result to Accumulator

D. None of the above

40. Which of the following is a zero address instruction

A. LOAD A

B. PUSH A

C. MOV R1, A

D. ADD R1, A

41. Which of the following is incorrect about the control unit

A. Control unit can be hardwired or programmed

B. Hardwired controls provides faster mode of operation

C. programmed controls are difficult to be modify

D. Hardwired control used combinational and sequential circuits

42.In a basic computer, the PC is of bits

A. 12

B. 8

C. 16

D. 10

43. If the Instruction register IR = 7800, AR=123, DR= F800 then the type of instruction will be

A. Direct memory reference

B. indirect memory reference

C. register reference

D. Input/output

44. In a basic computer, the machine instruction is executed in following manner

A. decode, fetch, execute

B. fetch, execute, decode

C. fetch, decode, execute

D. any of the above sequence

45. Which of the following forms the part of instruction set completeness

A. functional instruction

B. control instruction

C. transfer instruction

D. all of the above

46. Selective set operation can be executed by using.

A. OR gate

B. AND gate

C. NOT gate

D. none of the above

47. To design a arithmetic circuit which can perform 7 different arithmetic operation is used

A. Encoder

B. Multiplexer

C. Decoder

D. Demultiplexer

48. Pipelining increases of the processor

A. Storage

B. Latency

C. predictivity

D. Throughput

49. Index hold and Tag field is associated with which of the mapping technique in cache memory

A. Direct Mapping

B. Associative Mapping

C. Set-associative Mapping

D. Upset-associative Mapping

50. Hardware organization of Content Addressable Memory includes

A. Argument register only

B. Key register

C. Match register

D. All of the above

51. SR Flip Flop produces invalid output for input

A. S=0, R=0

B. S=0, R=1

C. S=1, R=0

D. S=1, R=1

52. Toggle condition in flip flop consider as

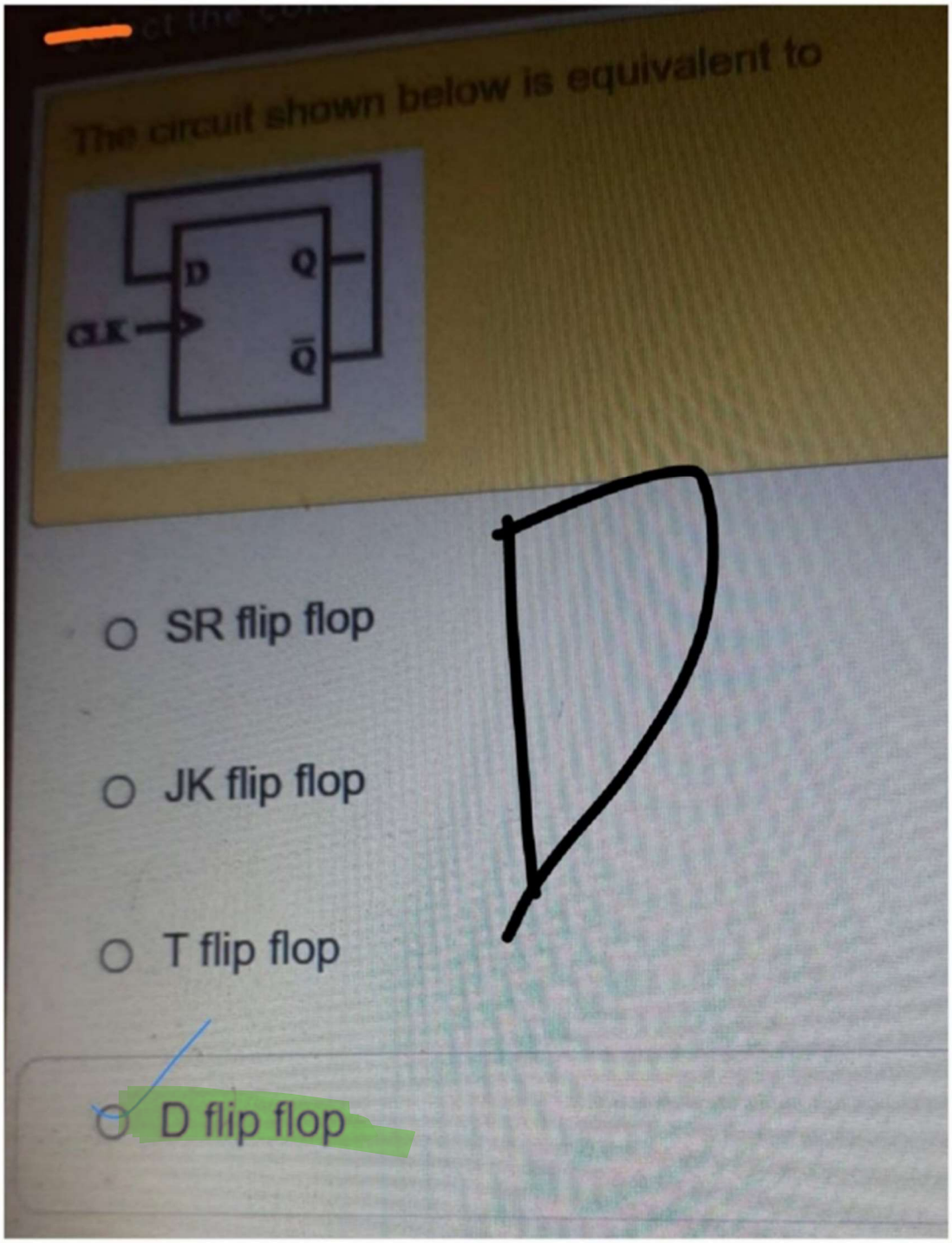
A. next state same as previous state

B. next state delayed version of previous state

C. next state shifted version of previous state

D. next state is compliment of previous state

53.



54. in programmable logic devices connection are made by means of

A. Glue

B. Foam

C. Fuse

D. Wire

55. Which of the following memory is also known as content addressable memory

A. Virtual Memory

B. Auxiliary Memory

C. Cache Memory

D. Associative Memory

56. The difference between half adder and full adder is

A. Half adder has two inputs while full adder has three inputs

B.Half adder has three inputs while full adder two inputs

C. Half adder has two outputs while full adder has tree outputs

D. Half adder has three outputs while full adder has two outputs

57. Which of the following is correct about Multiplexer

A. It is a data converter

B. It can be represented as 4:1 MUX

C. Both A and B

D. None of the above

58. Data transfer to and from peripheral can be handled using

A. Programmed I/O only

B. Interrupt-Initiated I/O only

C. Direct Memory Access (DMA)

D. All of the above

59. To design a 1024 x 8 RAM using 128 x 8 RAM, how many such chips are required

A. 4

B. 6

C. 8

D. 10

60. Which of the following is an example of a Peripheral Device

A. CPU

B. Memory

C. Input/Output

D. All of the above