

OPERATIONAL AMPLIFIER

- K. GURU GOVIND

→ Operational Amplifier :-

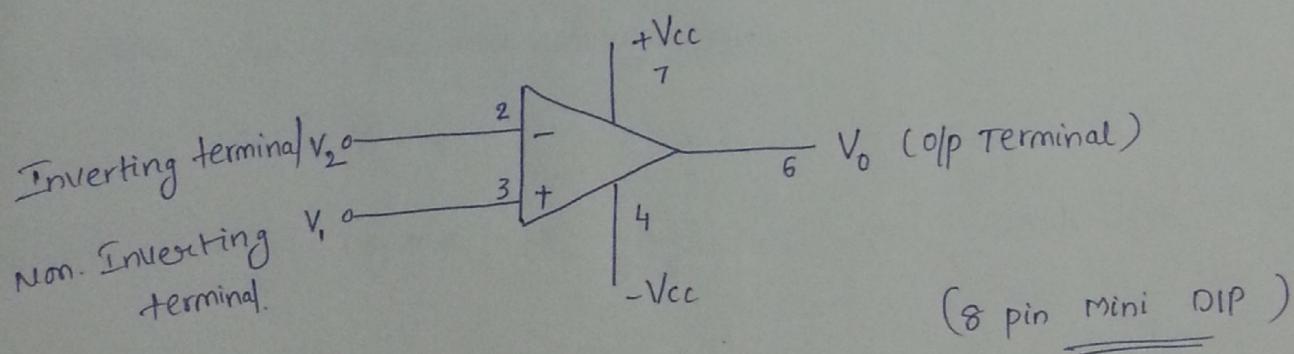
operational amplifier basically a device where a no. of differential Amplifier stages are connected in series and the overall gain of the op-Amp is made high.

- op-Amp has very high input impedance in the order of $M\Omega$.
- output impedance of op-Amp is very less than 100Ω .
- op-Amp is basically in many applications Eg. Mathematical operations in Analog i.e Summation, Subtraction, integration, differentiation etc.. Above operations effectively. That is why the op-Amp can perform above operations effectively. That is why the Amplifier is known as operational Amplifier.

→ Typical Applications of op-Amp are

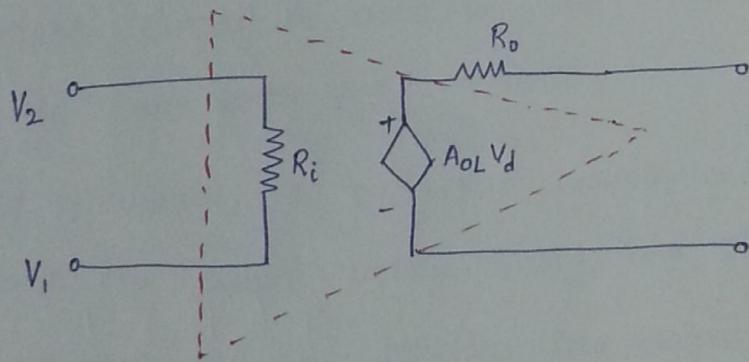
- i) to provide Voltage Amplification changes
- ii) oscillators
- iii) Filter Circuits
- iv) Instrumentation Circuits.

→ Circuit symbol of op-Amp with power supplies :-



Characteristics of ideal op-Amp:-

- i) Input Resistance $R_i = \infty$
- ii) Output Resistance $R_o = 0$
- iii) Voltage gain (A) = ∞
- iv) Band width = ∞ .
- v) perfect balance i.e $V_o = 0$ when $V_1 = V_2$
- vi) Op-Amp characteristics do not drift with temperature.
→ An ideal op-Amp draws no current at both input terminals because of high input resistance. (∞)
→ Since Gain is ∞ , The voltage between inverting and non-inverting terminals should be zero. i.e $V_d = V_1 - V_2 = 0$.
→ Above properties can never be realized practically. Therefore practical op-Amp equivalent circuit is given by



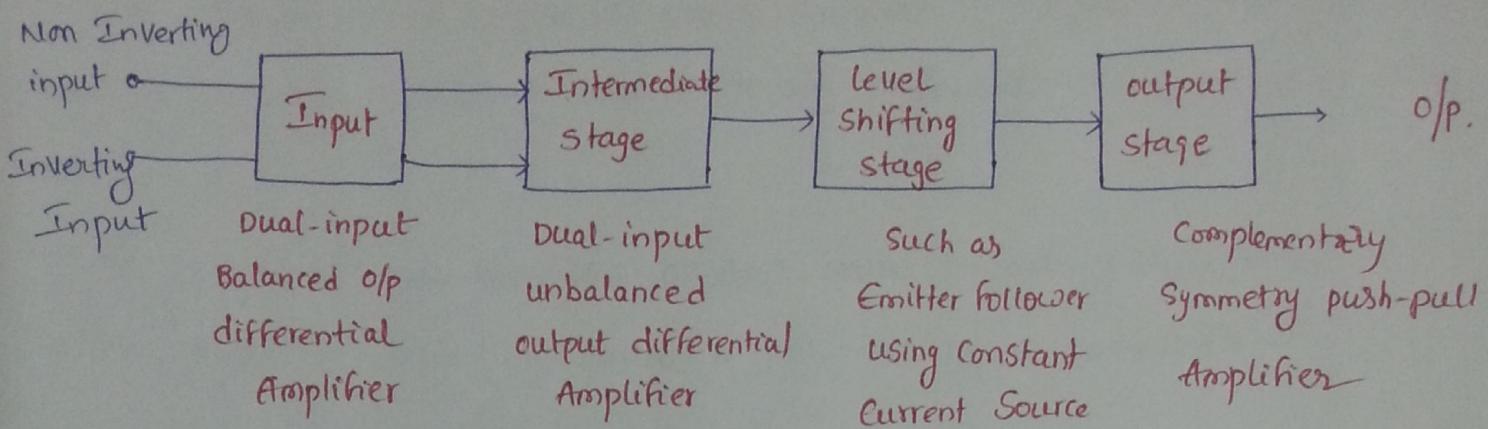
$$\begin{aligned}V_o &= AOL \cdot V_d \\&= AOL(V_1 - V_2)\end{aligned}$$

where AOL = open loop voltage gain.

$$V_d = V_1 - V_2$$

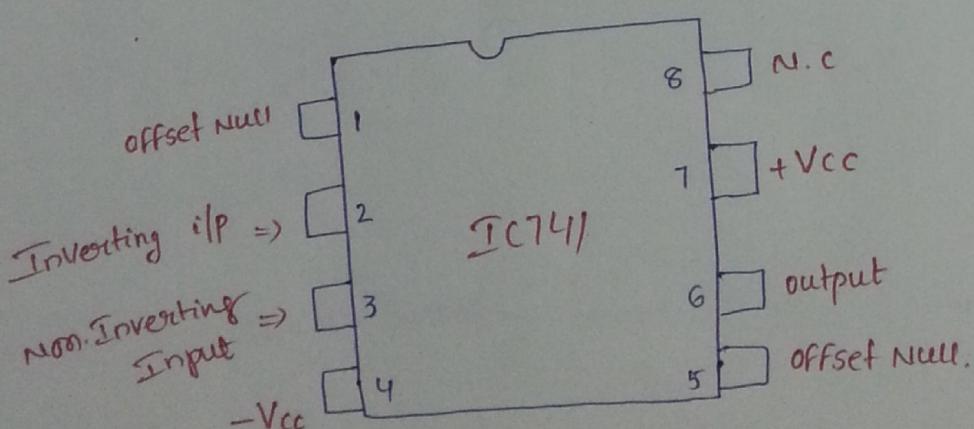
→ In practical op-Amp, $R_i = \text{high}$, $R_o = \text{low}$, Bandwidth = high, Voltage = high.

Block diagram Representation of an Op-Amp :-



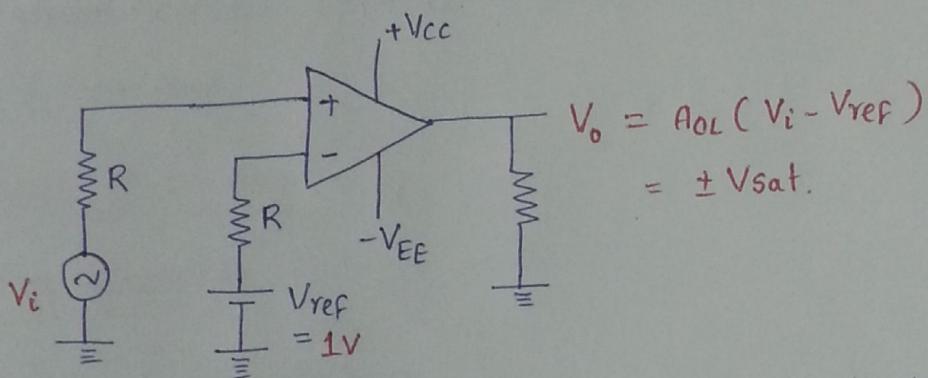
- The input stage is dual-input balanced output differential Amplifier. This stage provides most of voltage gain of Amplifier and also establishes input Resistance of op-Amp.
- The Intermediate stage is dual input, unbalanced output. Because Direct coupling is used, dc voltage at the output of intermediate stage is well above ground potential.
- Level translator circuit is used to shift the dc level at o/p intermediate stage to zero volt w.r.t. ground.
- Final stage is usually a push-pull complementary amplifier. The output stage increase the output voltage swing and raises the current supplying capability of op-Amp and also provides low output Resistance.

PIN Diagram of Op-Amp :-



COMPARATOR:-

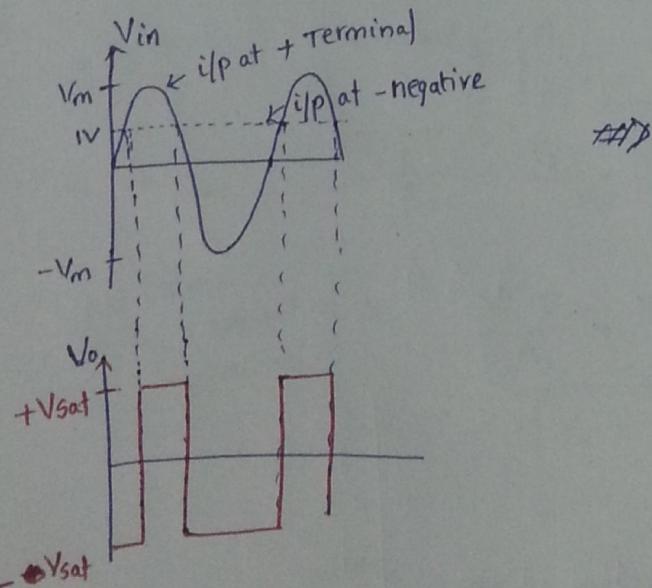
- A comparator is a circuit which compares a signal voltage applied at one input of an op-amp with a known reference voltage at the other input.
- It is basically an open-loop op-amp with output $\pm V_{sat}$ ($= V_{cc}$).
- The following circuit is called a non-inverting comparator.



- The output of above circuit will be based on the logic between the two voltages at the input terminals. i.e

$$V_o = +V_{sat} \text{ for } V_i > V_{ref}$$

$$V_o = -V_{sat} \text{ for } V_i < V_{ref}.$$



Explain the above input and output waveforms in exam.

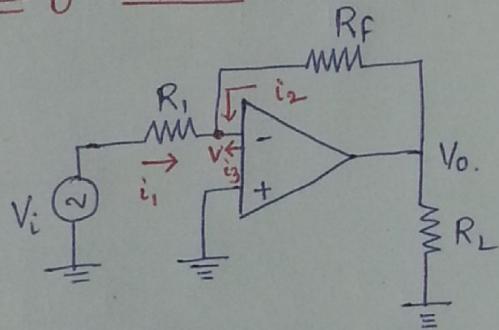
- we can design Inverting Comparator also (Schmitt trigger).

VIRTUAL GROUND CONCEPT :-

- we will assume that voltage at non inverting terminal of op-Amp will be treated as Input Voltage at the inverting terminal of Op-Amp.
- i.e. voltage at non inverting terminal = ^{virtual} voltage at Inverting terminal.
- The above concept will be valid only for negative feedback only and the concept is known as Virtual ground.
- Virtual ground concept can't be applied to open loop and positive feedback Circuits of op-Amp.

APPLICATIONS OF OP-AMP :-

(i) Inverting Amplifier.



→ By Virtual ground concept $V=0$.

→ By KCL, $i_1 + i_2 + i_3 = 0$. op-Amp can't draw any current. So $i_3 = 0$.

$$\Rightarrow \frac{Vi - V}{R_1} + \frac{V_o - V}{R_f} + 0 = 0.$$

put $V=0$
By V.ground
concept

$$\Rightarrow \frac{Vi - 0}{R_1} + \frac{V_o - 0}{R_f} = 0.$$

$$\Rightarrow \boxed{V_o = -\frac{R_f}{R_1} V_i}$$

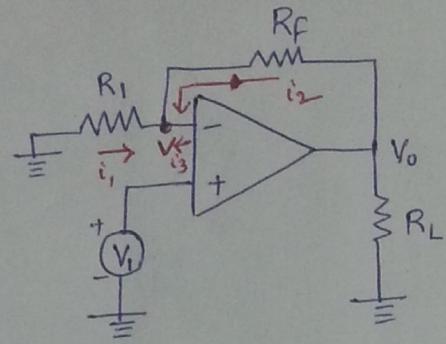
where

V_o = output Voltage

V_i = Input Voltage

$-R_f/R_1$ = Closed loop voltage gain = A_{CL} .

(ii) Non Inverting Amplifier :-



→ By Virtual ground concept $V = V_1$.

→ By KCL, $i_1 + i_2 + i_3 = 0$.

$$\Rightarrow \frac{0 - V}{R_1} + \frac{V_0 - V}{R_F} = 0.$$

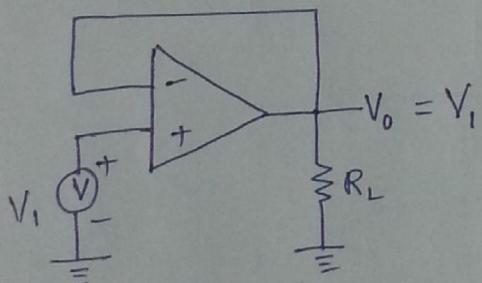
$$\text{Put } V = V_1 \Rightarrow -\frac{V_1}{R_1} + \frac{V_0 - V_1}{R_F} = 0.$$

$$\Rightarrow fV_1 \left(\frac{1}{R_1} + \frac{1}{R_F} \right) = f \frac{V_0}{R_F}.$$

$$\Rightarrow V_0 = \left(1 + \frac{R_F}{R_1} \right) V_1$$

$\therefore \boxed{V_0 = \left(1 + \frac{R_F}{R_1} \right) V_1}$ OP Voltage IP Voltage

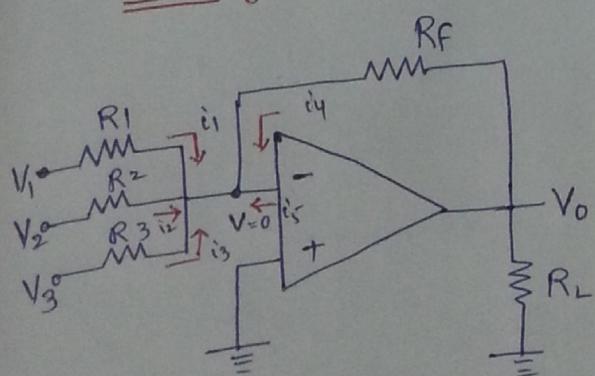
(iii) Voltage Follower :-



$$\text{i.e. } \boxed{V_0 = V_1}$$

choose $R_F = 0$ and
 $R_1 = \infty$ in
Non Inverting Amp

(iv) Summing Amplifier :-



→ By Virtual ground concept, $V = 0$.

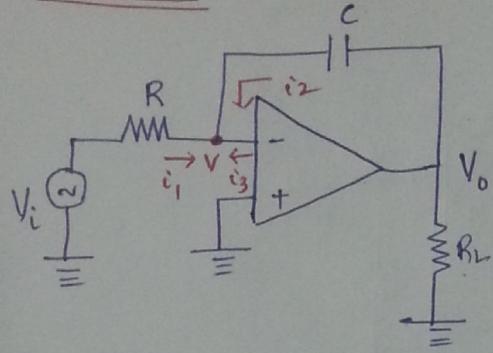
→ By KCL, $i_1 + i_2 + i_3 + i_4 + i_5 = 0$.

$$\Rightarrow \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} + \frac{V_0}{R_F} + 0 = 0.$$

$$\Rightarrow V_0 = - \left(\frac{R_F}{R_1} V_1 + \frac{R_F}{R_2} V_2 + \frac{R_F}{R_3} V_3 \right).$$

If $R_F = R_1 = R_2 = R_3 = R$ $\Rightarrow \boxed{V_0 = - (V_1 + V_2 + V_3)}$

v) Integrator



→ By virtual ground concept, $V=0$.

$$\text{By KCL, } i_1 + i_2 + i_3 = 0.$$

$$\Rightarrow \frac{V_i}{R} + i_2 + 0 = 0. \quad \text{---(1)}$$

$$i_2 = C \cdot \frac{dV_o}{dt} \quad (\text{put in (1)}).$$

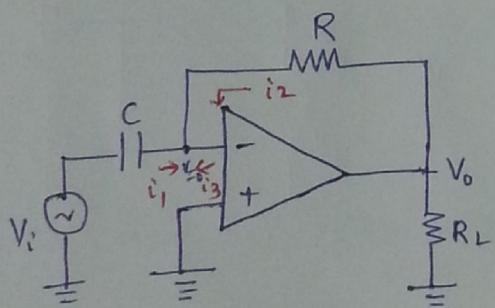
$$\therefore \frac{V_i}{R} + C \cdot \frac{dV_o}{dt} = 0.$$

$$\Rightarrow \frac{dV_o}{dt} = - \frac{V_i}{RC} \quad (\text{Apply integration on both sides})$$

$$\Rightarrow \int \frac{dV_o}{dt} dt = - \frac{1}{RC} \int V_i dt.$$

$$\Rightarrow \boxed{V_o = -\frac{1}{RC} \int V_i dt}$$

(vi) Differentiator :-



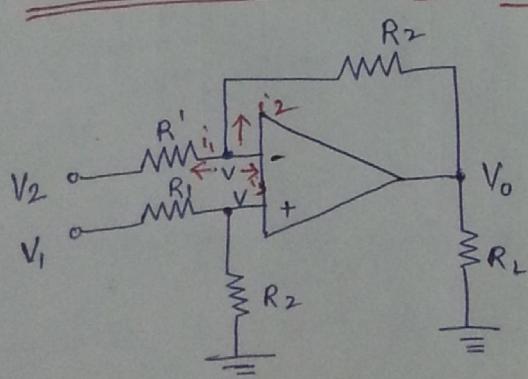
$$\text{By KCL, } i_1 + i_2 + i_3 = 0.$$

$$\Rightarrow C \cdot \frac{dV_i}{dt} + \frac{V_o}{R} + 0 = 0.$$

$$\Rightarrow \frac{V_o}{R} = -C \cdot \frac{dV_i}{dt}$$

$$\Rightarrow \boxed{V_o = -RC \cdot \frac{dV_i}{dt}}$$

(vii) Difference Amplifier (δ) Voltage Subtractor



→ Calculate voltage across R_2 at non-inverting terminal.

$$\text{i.e. } V = \frac{R_2 \cdot V_1}{R_1 + R_2} \quad \text{---(1)}$$

→ By KCL, $i_1 + i_2 + i_3 = 0$.

$$\Rightarrow \frac{V - V_2}{R_1} + \frac{V - V_o}{R_2} + 0 = 0. \quad \text{---(2)}$$

After substituting ① in ②

$$\Rightarrow \frac{V_0}{R_2} = V \left(\frac{1}{R_1} + \frac{1}{R_2} \right) - \frac{V_2}{R_1}$$

NOW substitute $V = \frac{R_2 V_1}{R_1 + R_2}$ in above.

$$\therefore \frac{V_0}{R_2} = \left(\frac{R_2 V_1}{R_1 + R_2} \right) \left(\frac{1}{R_1} + \frac{1}{R_2} \right) - \frac{V_2}{R_1}.$$

$$\Rightarrow \frac{V_0}{R_2} = \frac{R_2 V_1}{R_1 R_2} - \frac{V_2}{R_1}$$

$$\Rightarrow V_0 = \frac{R_2}{R_1} (V_1 - V_2)$$

If $R_1 = R_2 = R$ $\Rightarrow \boxed{V_0 = \underline{\underline{V_1 - V_2}}}$

open loop op-Amp

$$V_o = A_{OL}(V_1 - V_2) = A_{OP} V_{DM} \quad \text{where } V_{DM} = \text{Difference mode voltage} = V_1 - V_2.$$

and A_{DM} is Difference mode gain when $V_1 \neq V_2$

$$V_{o2} = A_2 V_2 \quad (\text{Assume})$$

$$V_{o1} = A_1 V_1 \quad (\text{Assume}).$$

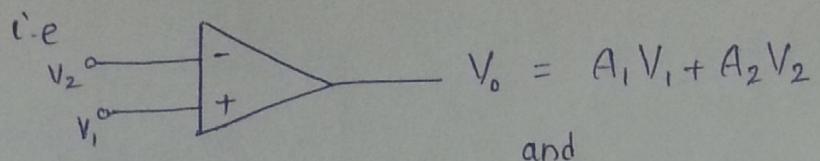
where A_2 is the open loop gain when $V_1=0, V_2=V_2$

and A_1 is the open loop gain when $V_1=V_1$ and $V_2=0$.

$$\therefore V_o = V_{o1} + V_{o2} \\ = A_1 V_1 + A_2 V_2 \quad \stackrel{\text{VIMP.}}{\circ}$$

In Ideal op-Amp, when $V_1=V_2=V$ o/p voltage is zero. But in practical op-Amp. we will get the o/p voltage as $V_o = A_{CM} V_{CM}$

where $V_{CM} = \frac{V_1 + V_2}{2}$ and A_{CM} = Common mode voltage gain.



and

$$V_0 = A_{DM} V_{DM} + A_{CM} V_{CM}$$

$$= A_{DM} (V_1 - V_2) + A_{CM} \left(\frac{V_1 + V_2}{2} \right).$$

$$= V_1 \left(\frac{A_{CM}}{2} + A_{DM} \right) + V_2 \left(\frac{A_{CM}}{2} - \frac{A_{DM}}{2} \right)$$

By comparing, $A_1 = \frac{A_{CM}}{2} + A_{DM}$ and

$$A_2 = \frac{A_{CM}}{2} - A_{DM}.$$

$$\therefore A_{CM} = A_1 + A_2$$

$$A_{DM} = \frac{A_1 - A_2}{2}$$

→ COMMON MODE REJECTION RATIO :- (CMRR)

CMRR is given by the ratio of Differential Voltage gain to Difference Signal with the Voltage gain of Common mode Signal.

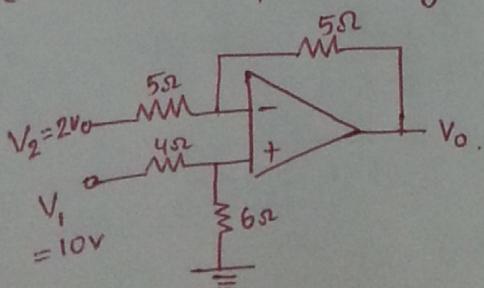
(d)

→ The relative Sensitivity of an Op-Amp to a difference signal as compared to a common mode signal is called common mode Rejection Ratio.

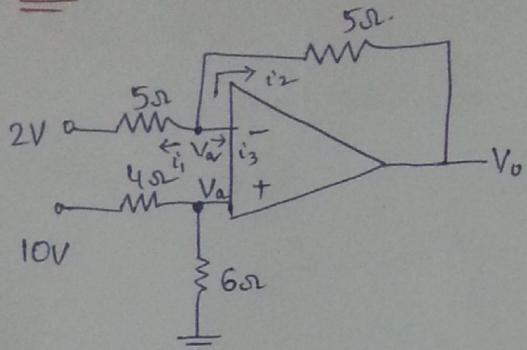
$$\rightarrow \text{CMRR is given by } f = \left| \frac{A_{DM}}{A_{CM}} \right|$$

$$\rightarrow \text{CMRR is usually expressed in dB. } \text{CMRR} = 20 \log_{10} \left| \frac{A_{DM}}{A_{CM}} \right| \text{ db.}$$

⑥ Calculate output voltage and CMRR for the following Circuit.



Sol:-



$$V_a = \frac{10(6)}{10} = \frac{10(6)}{6+4} = 6V.$$

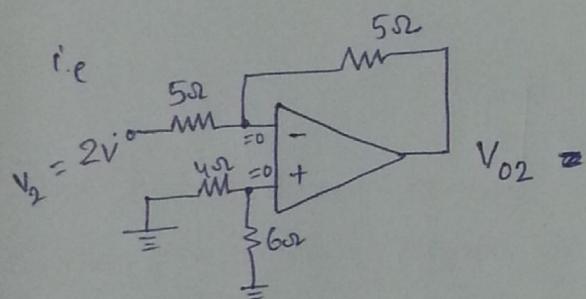
∴ By KCL, $i_1 + i_2 + i_3 = 0$.

$$\Rightarrow \frac{V_a - 2}{5} + \frac{V_a - V_0}{5} = 0.$$

$$\Rightarrow 6 - 2 + 6 - V_0 = 0$$

$$\Rightarrow \boxed{V_0 = 10V}$$

→ Convert Above Circuit into two parts,
so that $V_0 = V_{01} + V_{02}$



By KCL,

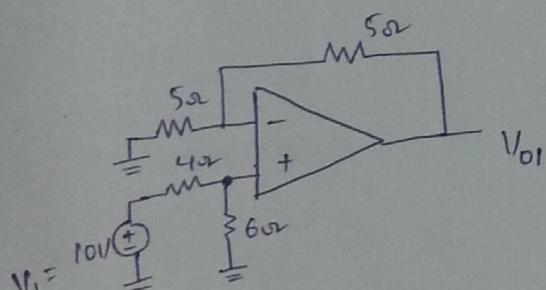
$$\frac{0-2}{5} + \frac{0-V_{02}}{5} = 0.$$

$$\Rightarrow \boxed{V_{02} = -2V}$$

$$V_2 = 2V, V_{02} = -2V.$$

$$\therefore A_2 = \frac{V_{02}}{V_2} = \frac{-2}{2} = -1.$$

$$\boxed{A_2 = -1}$$



Voltage across 6Ω $\Rightarrow 6V$.

$$\therefore \frac{6-0}{5} + \frac{6-V_{01}}{5} = 0.$$

$$\Rightarrow \boxed{V_{01} = 12V.}$$

$$V_1 = 10V, V_{01} = 12V. \quad \Rightarrow A_1 = \frac{V_{01}}{V_1} = \frac{12}{10} = 1.2$$

$$\boxed{A_1 = 1.2}$$

$$\therefore CMRR = \left| \frac{A_{DM}}{A_{CM}} \right| = \left| \frac{A_1 - A_2}{2(A_1 + A_2)} \right| = \frac{1.2 - 1}{2(1.2 + 1)} = \frac{2 \cdot 2}{2(0.2)}$$

$$\boxed{CMRR = 5.5}$$

$$CMRR = \underline{\underline{20 \log |5.5| \text{ dB}}}$$

Slew rate :-

It is the maximum rate of change of output voltage for all possible input signals.

$$\text{Slew rate} = \left| \frac{dV_o}{dt} \right|_{\text{max.}}$$

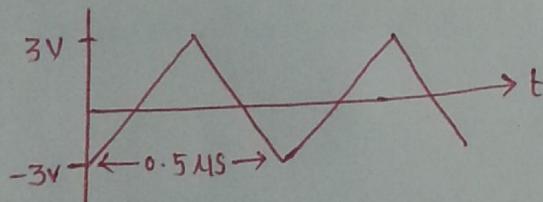
Slew rate for Sinusoidal Signals :-

If $V_o = V_{\text{max}} \sin \omega t$,

$$\begin{aligned}\text{Slew rate} &= \left| \frac{dV_o}{dt} \right| = \left| \omega V_{\text{max}} \cos \omega t \right| \\ &= 2\pi f_{\text{max}} V_{\text{max}}.\end{aligned}$$

- Q. The output of an op-amp voltage follower is a triangular wave as shown in following figure for a square wave input frequency 2 MHz and 8V pp amplitude. What is the slew rate.

Sol:-



$$\text{Sol:- Slew Rate} = \frac{dV_o}{dt} = \frac{3 - (-3)}{(0.5 \mu s)/2} = \frac{12}{0.5} = \underline{\underline{24 \text{ V}/\mu \text{sec}}}$$

- Q. An op-amp has slew rate of $1 \text{ V}/\mu \text{sec}$ with a gain of 40dB, if this amplifier has to faithfully amplify sinusoidal signal from 0 to 20KHz without introducing any distortion. What must be the maximum input signal.

Sol:-

$$\text{Slew rate} = 2\pi f_{\text{max}} V_{\text{max}}.$$

$$\Rightarrow \frac{1 \text{ V}}{14} = 2\pi (20 \text{ K}) V_{\text{max.}}$$

$$\Rightarrow V_{\text{max}} = 7.95 \text{ V.}$$

X40000

$$\text{Voltage gain} = 20 \log_{10} \left| \frac{V_{o\max}}{V_{in\max}} \right| = 40.$$

$$\Rightarrow \log_{10} \left| \frac{7.95}{V_{in\max}} \right| = 2.$$

$$\Rightarrow V_{in\max} = 79.5 \text{ mV}$$

→ Power Supply Rejection Ratio (PSRR) :-

PSRR is defined as the Ratio of the change in Supply Voltage to the equivalent (differential) output voltage it produces in op-Amp and is expressed in decibels.

$$\text{PSRR (dB)} = 20 \log_{10} \left(\frac{\Delta V_{\text{supply}}}{\Delta V_{\text{out}}} \right) \text{ dB.}$$

- Practice problems on PSRR. (Choose any Electronics op-Amp Text book).
- AS per IP, This is the Complete op-Amp Chapter.

— K. Gurugouind.

UID : 17891

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— THE END —