Sample questions paper

1. The Stack follows the sequence

a) first-in-first-out

b) first-in-last-out

c) last-in-first-out

d) last-in-last-out

2. If the processor is executing the main program that calls a subroutine, then after executing the main program up to the CALL instruction, the control will be transferred to

a) address of main program

..b) subroutine address

c) address of CALL instruction

d) none of the mentioned

3. The stack is useful for

a) storing the register status of the processor

b) temporary storage of data

c) storing contents of registers temporarily inside the CPU

..d) all of the mentioned

4. The process of storing the data in the stack is called …… the stack.

a) pulling into

b) pulling out

c) pushing into

d) popping into

5. The reverse process of transferring the data back from the stack to the CPU register is known as

a) pulling out the stack

b) pushing out the stack

c) popping out the stack

d) popping off the stack

6. The books arranged one on the other on a table is an example of

a) queue

b) queue and first-in-first out

c) stack

..d) stack and last-in-first-out

7. . In a J-K Flip Flop the function K=J' is used to realize

.. A T-Flip-Flop

B S-R Flip-Flop

C D-Flip-Flop

D M/S J-K Flip-Flop

8. A Toggle Flip-Flop can be constructed using a J-K Flip-Flop by connecting the

..A Toggle input to J and inverted form of toggle input to K

B The toggle input to J

C Inverted form of toggle input to K

D None of the above

9. Which Logic circuit would you use for addressing memory ?

A Full adder

B Multiplexer

..C Decoder

D Direct memory access circuit

10. _____ are arithmetic gates

NOT

NAND & NOR

..X-OR & X-NOR

NOT, AND, & OR

11. Combinational logic is used to _____

Compute outputs

..Compute new states

Both a and b

None of the above

12. _____ are the methods used to represent negative integer numbers

1’s compliment

Sign magnitude

2’s compliment

.. All of the above

Which of the following combinational circuit selects binary information from one of many input lines and directs it to a single output line?

A. Encoder.

B. Decoder.

C. Demultiplexer.

D. Multiplexer.

ANSWER: D

The addition and subtraction operations can be combined into one common circuit by including a _____ gate with each full adder.

A. exclusive-OR.

B. AND.

C. OR.

D. NAND.

ANSWER: A

The storage devices that stores information in a manner that the item stored last in first item retrieved

is_____.

A. queue.

B. stack.

C. CPU.

D. register.

ANSWER: B

SP stands for _____.

A. Storage Pointer.

B. Seek Pointer.

C. Stack Pointer.

D. Synchronous Pointer.

ANSWER: C

The expansion of RPN is _____.

A. Reverse Polish Notation.

B. Review Polish Notation.

C. Reverse Pointer Notation.

D. Review Pointer Notation.

ANSWER: A

. The notation A+B is _____.

A. prefix notation.

B. postfix notation.

C. infix notation.

D. none of these.

ANSWER: C

ADD R1, A, B is_____.

A. zero address instruction format.

B. one address instruction format.

C. two address instruction format.

D. three address instruction format.

ANSWER: D

. RISC stands for_____.A. Reduced Instruction Set Computer.

B. Reverse Instruction Set Computer.

C. Reduced Implied Set Computer.

D. Reverse Implied Set Computer.

ANSWER: A

. The mode in which the effective address is equal to the address part of instruction is _____.

A. indirect addressing mode.

B. direct addressing mode.

C. register addressing mode.

D. relative addressing mode.

ANSWER: B

The instruction that performs arithmetic, logic and shift operations are_____.

A. data transfer instruction.

B. data manipulation instruction.

C. register transfer instruction.

D. program control instruction.

ANSWER: B

The instruction provides decision making capabilities are_____.

A. data transfer instruction.

B. data manipulation instruction.

C. register transfer instruction.

D. program control instruction.

ANSWER: D

The _____ contains an address to specify the desired location in the memory.

A. word count register.

B. address register.

C. control register.

D. none of the above.

ANSWER: B

The notation AB+ is_____.

A. prefix notation.

B. postfix notation.

C. arithmetic notation.

D. infix notation.

ANSWER: B

The field that specifies the way the operand or the effective address is determined is _____.

A. processor field.

B. mode field.

C. operation code field.

D. address field.

ANSWER: C

The NOT gate is also called _____.

A. AND gate.

B. NAND gate.

C. XOR gate.

D. Inverter.

ANSWER: D

TOS represents_____.

A. Top Of Simulator.

B. Top Of Stack.

C. Top Of Storage.

D. Top Of System.

ANSWER: B

The 10’s complement of a decimal number is equal to its _____.

A. 9’s complement + 1.

B. 9’s complement – 1.

C. 8’s complement + 2.

D. 8’s complement – 2.

ANSWER: A

AR represents_____.

A. Auto Register.

B. Address Register.

C. Auxiliary Register.

D. Associate Register.ANSWER: B

. The addressing mode where the controls of an index register is added to the address part of the instruction_____.

A. relative addressing mode.

B. direct addressing mode.

C. indexed addressing mode.

D. immediate addressing mode.

ANSWER: B

The instructions that perform binary operations on strings of bits stored in registers_____.

A. logical instructions.

B. shift instructions.

C. arithmetic instructions.

D. complement instructions.

ANSWER: A

The _____ holds the number of words to be transferred to the memory.

A. word count register.

B. address register.

C. control register.

D. program register.

ANSWER: A

The NOR gate produce the output 1, if _____.

A. X = Y = 0.

B. X=1, Y=0.

C. X=0, Y=1.

D. X = Y = 1.

ANSWER: A

In half adder, carry will be 1, when _____.

A. X = Y = 0.

B. X=0, Y=1.

C. X=1, Y=0.

D. X = Y = 1.

ANSWER: D

The flip flop used to synchronize the state change during a clock pulse transition is _____

A. JK flip flop.

B. T flip flop.

C. edge triggered flip flop.

D. RS flip flop.

ANSWER: C