09/09/2014

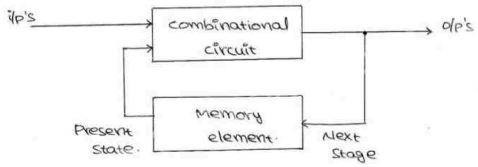
UNIT-III

SEQUENTIAL LOGIC

Differences b/w combinational circuit and sequential circuit:

combinational circuit	sequential circuit
(i) Output depends on only present inputs.	(i) Output depends on present i/p's and past outputs.
(ii) Memory unit is not required.	(ii) Memory unit is required to store the past history of o/p's.
(iii) Faster in speed.	(iii) slower than combinational circuits
(iv) Easy to design.	(iv) compared to combinational circuits harder to design.
(v) Ex:- Encoders, Decoders, MUX, DEMUX.	(v) Ex:- flip-flops, Registers, counters.

Block diagram of sequential circuit :-



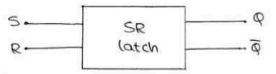
* One of the most foundamental sequential circuit is latch / flip-flop.
* A latch / flip-flop is a bistable multivibrator, that can store 1 bit of binary information (either 0 or 1).
* Because of their ability to retain a given state, these elements are useful as storage elements.

* LATCHES :-

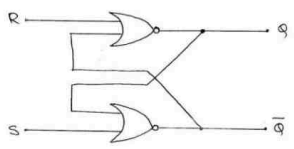
1. RS latch / SR latch / set-Reset latch / Reset-Set latch :-

* The most fundamental type of storage element is an SR latch.
* SR latch as two i/p's (S and R), two o/p's (Q & $\bar{Q}$) which are complemented to each other.
* the SR latch can be constructed from either NAND (or) NOR gates.

Logic Symbol of SR latch :-



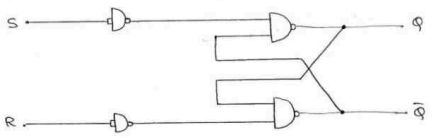
Logic circuit of RS latch using NOR gates :-



Truth table / Function table :-

i/p's R	S	Q_n	o/p Q_{n+1}	State
0	0	0	0	No change
0	0	1	1	
0	1	0	1	Set
0	1	1	1	
1	0	0	0	Reset
1	0	1	0	
1	1	0	X	Indeter-minate.
1	1	1	X	

Logic circuit of RS latch using NAND Gate :- ③

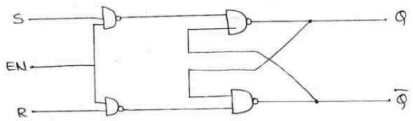


2. Gated SR latch :-

SR latch with enable i/p is known as "Gated SR latch."

Block diagram / Logic symbol :-

Logic circuit :-



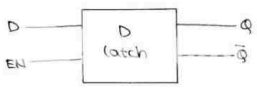
Truth table / Function table :-

i/p's			o/p	State
EN	R	S	Q_n	Q_{n+1}	
1	0	0	0	0	No change
1	0	0	1	1	
1	0	1	0	1	Set
1	0	1	1	1	
1	1	0	0	0	Reset
1	1	0	1	0	
1	1	1	0	X	Indeter-minate
1	1	1	1	X	
0	X	X	0	0	No change.
0	X	X	1	1	

3. D latch / Data latch :- ④

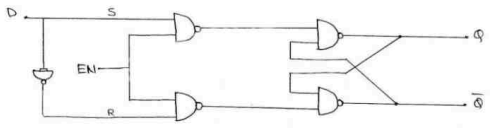
* From the truth table of SR latch it is clear that when both i/p's are same, the o/p either doesn't change or it is invalid.
* In many practical applications these i/p conditions are not required.
* These i/p conditions can be avoided by making i/p's complement to each other.
* This modified SR latch is known as "D latch".

Block diagram / Logic Symbol :-



EN → Enable i/p.

Logic circuit :-

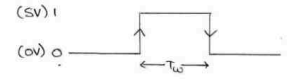


Truth table / Function table :-

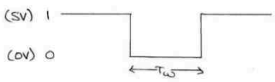
i/p's			o/p	State
EN	D	Q_n	Q_{n+1}	
0	X	0	0	No change
0	X	1	1	
1	0	0	0	Reset
1	0	1	0	
1	1	0	1	Set.
1	1	1	1	

10/09/2014

Positive pulse (0 to 1)

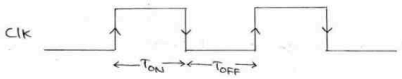


Negative pulse (1 to 0).



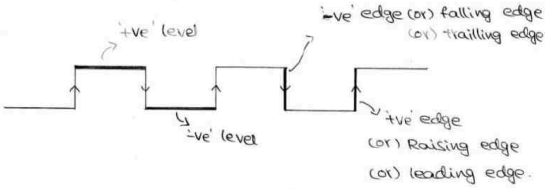
T_w → pulse width

clk → clock is a periodic pulse train



Time period of clk signal $T = T_{ON} + T_{OFF}$

frequency of clk $(f) = \frac{1}{T}$.



* Types of Triggerings :-

1. Level Triggering.
   (a) '+ve' level triggering
   (b) '-ve' level triggering
2. Edge Triggering
   (a) '+ve' edge Triggering
   (b) '-ve' edge Triggering → '-ve' edge triggered circuit responds to i/ps only at '-ve' edges of clk signal.

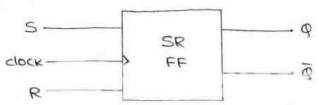
* Latches uses level triggering.
* Flip-flops uses edge triggering.

* Flip-flop :-

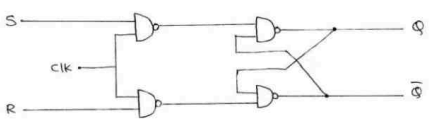
* Flip-flop is a memory element stores 1 bit of binary information.
* Flip-flop has two stable states (1 or 0).
* State of flip-flop ie bit stored is indicated by Q output.
* Other names of flip-flop are 1 bit memory cell, Bistable circuit, Bistable Multivibrator.
* on power, FF can be at 0 or 1 state

1. clocked SR flip-flop :-

(i) logic symbol of '+ve' edge Triggered SR flip-flop :



logic circuit :-



Truth table :-

i/p's			o/p	State
clk	S	R	Q_n	Q_{n+1}	
↓ (or) ↑	0	0	0	0	No change
↓ (or) ↑	0	0	1	1	
↑	0	1	0	0	Reset
↑	0	1	1	0	
↑	1	0	0	1	Set
↑	1	0	1	1	
↑	1	1	0	x	Indeter-minate
↑	1	1	1	x	
↑	x	x	0	0	No change
↑	x	x	1	1	

Q_n → state of FF before applying clk pulse

Q_{n+1} → state of FF after applying clk

characteristic table

S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	x

characteristic equation of SR flip-flop :-

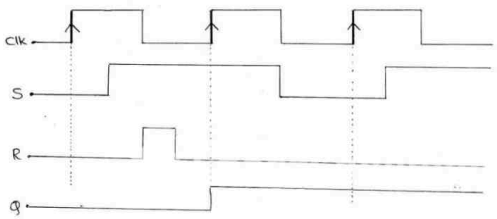
k-map for Q_{n+1}

S \ RQn	00	01	11	10
0		1		
1	1	1	X	X

$\therefore Q_{n+1} = S + \bar{R}Q_n$

$\therefore$ characteristic equation of SR flip-flop is $Q_{n+1} = S + \bar{R}Q_n$

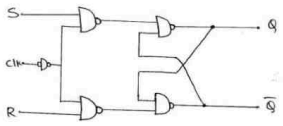
i/p & o/p waveforms of 'tve' edge triggered SR flip-flop:-



(ii) logic symbol of '-ve' edge triggered SR flip-flop :-

clock signal symbol ↓ (or) ↓

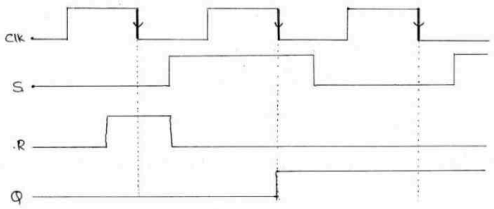
logic circuit :-



Truth table :-

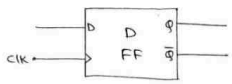
i/p's				o/p	
clk	S	R	Q_n	Q_{n+1}	State
↓ (or) ↓	0	0	0	0	No change
↓ (or) ↓	0	0	1	1	
↓ (or) ↓	0	1	0	0	Reset
↓ (or) ↓	0	1	1	0	
↓	1	0	0	1	Set
↓	1	0	1	1	
↓	1	1	0	X	Indeter-minate
↓	1	1	1	X	
↓	X	X	0	0	No change
↓	X	X	1	1	

i/p & o/p waveforms of '-ve' edge triggered SR flip-flop :-

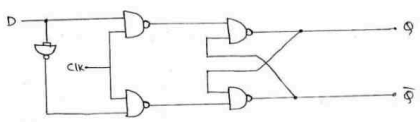


2. clocked D flip-flop :- / data flip-flop / Delay flip-flop :-

(i) logic symbol of 'tve' edge triggered D flip-flop :-



logic circuit :-



Truth table :-

i/p's			o/p	
clk	D	Q_n	Q_{n+1}	State
↑	0	0	0	Reset
↑	0	1	0	
↑	1	0	1	Set
↑	1	1	1	
0	X	0	0	No change
0	X	1	1	

≡

characteristic table :-

D	Q_{n+1}
0	0
1	1

characteristic equation of D flip-flop :-

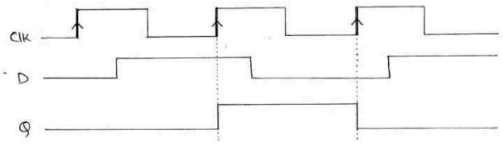
K-map for Q_{n+1}

D \ Qn	0	1
0		
1	1	1

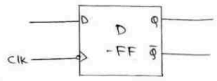
$\therefore Q_{n+1} = D$

$\therefore$ characteristic equation of D flip-flop is $Q_{n+1} = D$

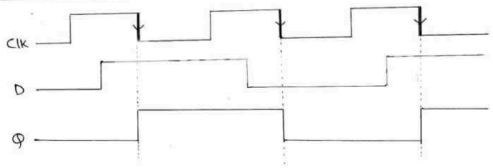
i/p & o/p waveforms of '+ve' edge triggered D flip-flop:-



(ii) logic symbol of '-ve' edge triggered D flip-flop :-



i/p & o/p waveforms of '-ve' edge triggered D flip-flop :-

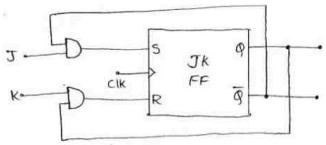


11/09/2014

3. clocked Jk flip-flop :-

the uncertinity in the state of an SR FF when S = R = 1 can be elimated by converting it into a Jk flip-flop

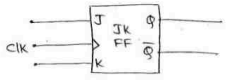
Jk flip flop using SR flip-flop :-



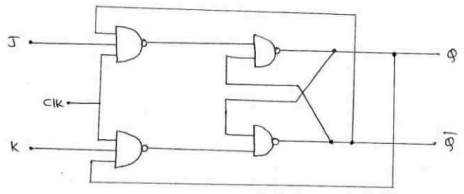
$S = J\bar{Q}$

$R = KQ$

logic Symbol of Jk Flip-flop :-



logic circuit of Jk flip-flop using NAND gates :-



Truth table :-

i/p's				o/p
Clk	J	K	Q_n	Q_{n+1}
0	x	x	0	0
0	x	x	1	1
↑	0	0	0	0
↑	0	0	1	1
↑	0	1	0	0
↑	0	1	1	0
↑	1	0	0	1
↑	1	0	1	1
↑	1	1	0	1
↑	1	1	1	0

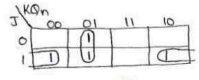
≡

characteristic table :-

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

characteristic equation of Jk flip-flop :-

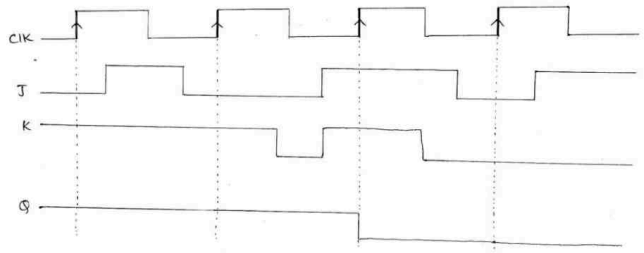
K-map for Q_{n+1}



$\therefore Q_{n+1} = \bar{K}Q_n + J\bar{Q}_n$

characteristic equation of Jk flip-flop is $Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$

i/p & o/p waveforms of +ve edge triggered JK flip-flop :-



16/09/2014

* Race around condition :-

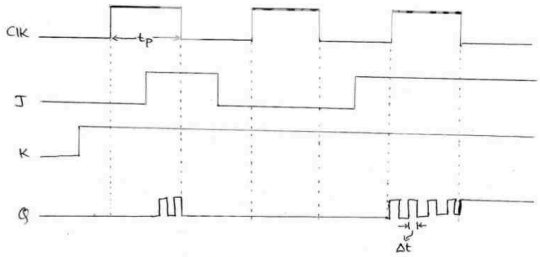


Fig:- +ve level triggered JK FF i/p & o/p waveforms

t_p → Pulse width

Δt → Propagation delay of 2 level NAND gates (considering JK FF using NAND gates circuit)

* In JK flip-flop, when J = K = 1, the o/p continously toggles in that region (o/p changes either from 0 to 1 (or) from 1 to 0). Which creates distribence in o/p this situation is referred to as the

Race around condition.

* There are 3 solutions for reducing race around condition.

(i) Use of edge triggering.

(ii) RAC exists when $t_p \geq \Delta t$. thus By keeping $t_p < \Delta t$, we can avoid RAC.

(iii) Use of Master slave flip-flop configuration.

* Master - slave JK flip-flop :-

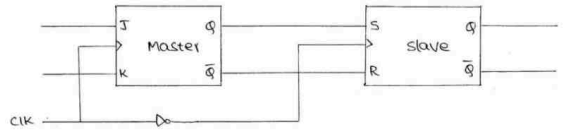


Fig:- logic diagram of Master - slave JK flipflop

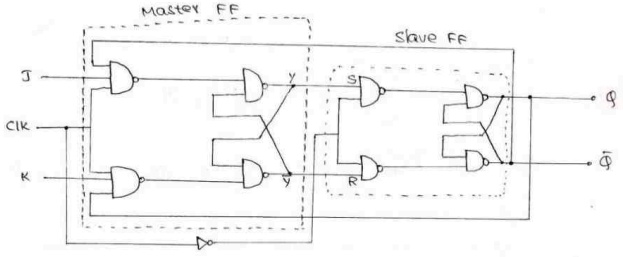


Fig:- Logic circuit of Master slave JK FF.

* Master slave JK flip-flop consists of clocked JK flip-flop as the Master and clocked SR as a slave.

* the o/p of the Master flip-flop is fed as an i/p to the slave FF.
* clock signal is connected directly to the ~~Math~~ Master flip-flop But it is connected through inverter to the slave flip-flop.

∴ the information present at the J & K i/p's is transmitted to the o/p of Master flip flop on the 'tve' clock pulse & it is held their until the '-ve' clock pulse occurs; After which it is allowed to pass through to the o/p of slave FF. The o/p of the slave FF is connected to the third i/p of the JK Master JK FF.

Truth table:-

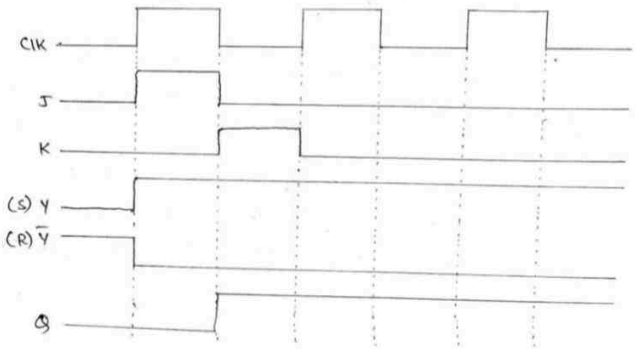
Clk	J	K	Q_n	Master FF o/p Y	Slave FF o/p Q_{n+1}
↑	0	0	0	0	No change
↓	0	0	0	NC	0
↑	0	0	1	1	NC
↓	0	0	1	No change	1
↑	0	1	0	0	NC
↓	0	1	0	NC	0
↑	0	1	1	0	NC
↓	0	1	1	NC	0
↑	1	0	0	1	NC
↓	1	0	0	NC	1
↑	1	0	1	1	NC
↓	1	0	1	NC	1
↑	1	1	0	1	NC
↓	1	1	0	NC	1
↑	1	1	1	0	NC
↓	1	1	1	NC	0

* When J=1 & K=1 Master flip-flop toggles on 'tve' clock and slave then copies the o/p of master on the -ve' clock. at this instant, feedback i/p's to the Master flip-flip are complemented but as it is -ve' half of the clock pulse Master FF is inactive.

13

This prevents Race around condition.

i/p & o/p waveforms of Master-slave JK FF:-



* JK FF Responds to 'tve' clk Pulses

* R

14

sr flip flop respond to -ve clock pulse

Differences b/w Latch & Flip-flop :-

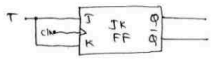
Latch	flip-flop
* A latch checks all its i/p's continuously & changes its o/p's accordingly at any time.	* flip-flop samples its i/p's & changes there its o/p's only at a time as determine by a clock signal.
* No clock is used.	* A clock is used.

12/09/2014

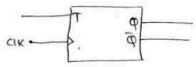
Clocked T Flip-flop / Toggle FF :-

* The T flip-flop is a modification of the JK flip-flop.
* T flip-flop is obtained from a JK flip-flop by connecting J & K i/p's together.

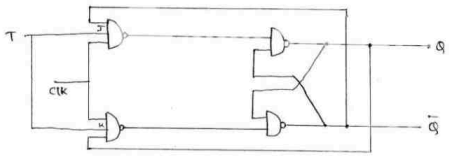
Logic diagram of T FF using JKFF :-



Logic diagram of T FF :-



Logic circuit :-



Truth table :-

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

≡

Characteristic table :-

T	Q_{n+1}
0	Q_n
1	$\bar{Q}_n$

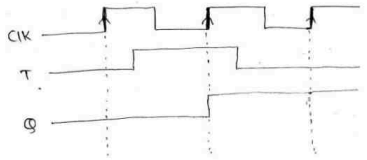
Characteristic equation of T flip flop :-

K map for Q_{n+1}

T \ Q_n	0	1
0		1
1	1	

$\therefore Q_{n+1} = \bar{T}Q_n + T\bar{Q}_n$

I/p and o/p waveforms of +ve edge triggered T-FF :-



16

* Flip-flop excitation tables :-

1. SR flip-flop :-

Characteristic table :-

S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	* → indeterminate

Excitation table :-

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

2. D flip-flop :-

Characteristic table :-

D	Q_{n+1}
0	0
1	1

Excitation table :-

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

3. JK flip-flop :-

Characteristic table :-

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

Excitation table :-

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

4. T - flip - flop :-

Characteristic table :-

T	Q_{n+1}
0	Q_n
1	$\bar{Q}_n$

Excitation table :-

Q	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Realisation of one flip-flop using other flip-flop :-

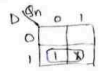
Ex: convert SR FF to D FF.

Sol: Excitation table for SR to D FF conversion :-

i/p	Present State	Next State	FF i/p's	
D	Q_n	Q_{n+1}	S	R
0	0	0	0	X
0	1	0	0	1
1	0	1	1	0
1	1	1	X	0

K-Map simplification :-

for S

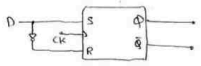


$\therefore S = D$

for R

$\therefore R = \bar{D}$

Logic diagram of DFF using SR FF :-



2. Convert D FF to TFF :-

Excitation table for D to T FF conversion :-

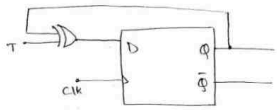
i/p	Present State	Next State	FF i/p
T	Q_n	Q_{n+1}	D
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

K-Map simplification :-

for D :-

$\therefore D = \bar{T}Q_n + T\bar{Q}_n = T \oplus Q_n$

Logic diagram of T FF using D FF :-



3. Convert SR FF to JK FF.

Excitation table for SR FF to JK FF conversion :-

i/p		Present State	Next State	FF i/p	
J	K	Q_n	Q_{n+1}	S	R
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	X	0
1	1	0	1	1	0
1	1	1	0	0	1

K-map simplification :-

for S

J \ $K\bar{Q}_n$	00	01	11	10
0		X		
1	D	X		C

$\therefore S = J\bar{Q}_n$

for R

J \ KQ_n	00	01	11	10
0	X			X
0		1	1	

$\therefore R = KQ_n$

Logic diagram of JK flip-flop using SR FF :-

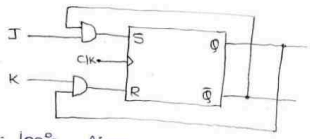


Fig:- logic diagram of JK FF using SR FF.

21/10/2014

Analysis and Design of Synchronous (or) clocked Sequential circuits

The synchronous or clocked sequential circuits are represented by two models.

(i) Moore circuit (or) Moore model (or) Moore Mechine
(ii) Mealy circuit.

1. Moore circuit :-

(i) Moore circuit o/p depends only on the present state of FF's.
(ii) I/p changes doesn't effect the o/p.
(iii) It requires more no. of states for impleme-nting function which is implemented using Mealy circuit.

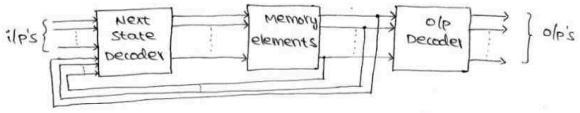


Fig:- B.D. of Moore circuit

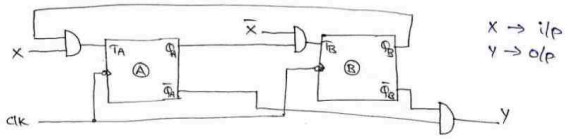


Fig:- Example of moore circuit.

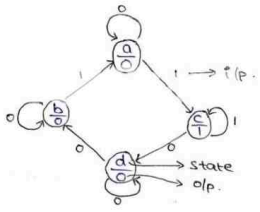


Fig:- Example State diag. for moore circuit.

2. Mealy circuit :-

(i) The o/p depends on both the present state of the FF's and on the i/p's.
(ii) I/p changes may effect the o/p of the ckt.
(iii) It requires less no. of states for implementing the function which is implemented using Moore circuit.

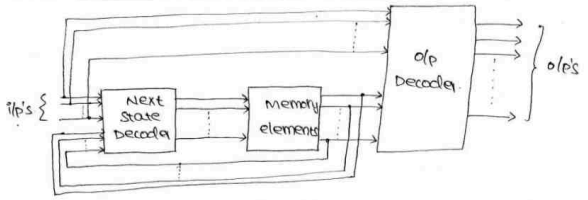


Fig:- B.D. of Melay circuit.

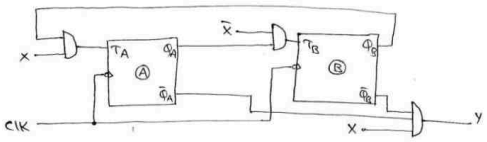


Fig:- Example of mealy circuit

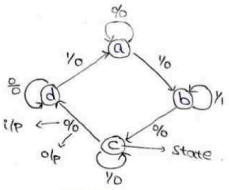


Fig:- example State diag. for mealy circuit.

Steps for the Design of a Synchronous (or) clocked Sequential circuits:-

Step 1: Obtain the state table from the given circuit information such as state diagram.

Step 2: Reduce no. of states if possible by state reduction technique.

Step 3: Assign binary values to each state in the state table

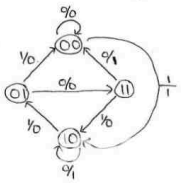
Step 4: Determine the no. of FF's needed and choose the type of FF to be used.

Step 5: From the state table derive the circuit exitation & o/p tables.

Step 6: Using K-Map, derive the circuit o/p functions and the FF i/p functions.

Step 7: Draw the logic diagram.

Q:- A sequential circuit has 1 i/p & 1 o/p. That ckt State diagram is shown below. Design the Sequential circuit with D-FF.



Sol:- Step 1: state diagram

The given state diagram has 4 states with one i/p and one o/p. considering x → i/p, y → o/p.

Present state		Next state				o/p (y)	
		x=0		x=1		x=0	x=1
Q_A	Q_B	Q_{A+1}	Q_{B+1}	Q_{A+1}	Q_{B+1}	y	y
0	0	0	0	1	0	0	1
0	1	1	1	0	0	0	0
1	0	1	0	0	1	1	0
1	1	0	0	1	0	1	0

Step 2: State Reduction and State Assignment

Here binary values are already assigned to states and it is not possible to reduce no. of states because no two present states, Next states and o/p's are same.

Step3: Determine no. of FF's required.

Determine no. of FF's required using eq.,

$2^n \geq N$ $\quad n \rightarrow$ no. of FF's. $\quad N \rightarrow$ no. of states.

$2^n \geq 4$

$\therefore n = 2$

FF's required $\longrightarrow$ 2
FF's using $\rightarrow$ D F.F's

Step4: Exitation table

Present state		i/p	Next state		FF i/p's		o/p
Q_A	Q_B	x	Q_{A+1}	Q_{B+1}	D_A	D_B	y
0	0	0	0	0	0	0	0
0	0	1	1	0	1	0	1
0	1	0	1	1	1	1	0
0	1	1	0	0	0	0	0
1	0	0	1	0	1	0	1
1	0	1	0	1	0	1	0
1	1	0	0	0	0	0	1
1	1	1	1	0	1	0	0

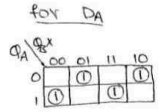
(∵ D-FF exitation table

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Step5: K-Map simplification.

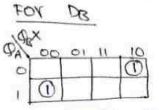
K-map simplification for FF i/p functions & sequential circuit o/p function.

for D_A



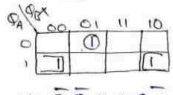
$\therefore D_A = Q_A \oplus Q_B \oplus x$

For D_B



$\therefore D_B = \bar{Q}_A Q_B \bar{x} + Q_A \bar{Q}_B \bar{x}$

For Y



$\therefore Y = \bar{Q}_A \bar{Q}_B x + Q_A \bar{x}$

23

Step6: logic diagram

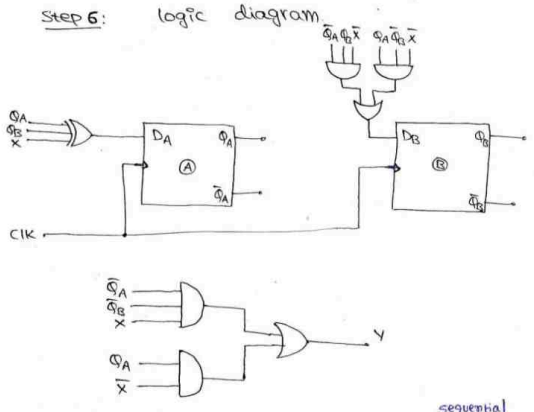
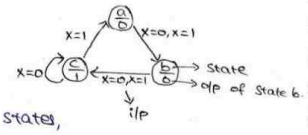


Fig: Logic diagram of mealy sequential circuit for given state diagram.

22/10/2014

Q: Realize the sequential circuit for the state diagram shown Below.



Sol: Given state diag. has 3 states, one i/p, one o/p.

considering $\quad X \longrightarrow$ i/p
$\quad Y \rightarrow$ o/p

24

Step1: State table

Present State	Next State		Output
	x=0	x=1	y
a	b	b	0
b	c	c	0
c	c	a	1

Step 2: State Reduction

There is no possibility of State Reduction since no two States, Next States & O/P's are same.

Step 3: No. of FF's Required

Determine no. of FF's required using eq.

$2^n \geq N$ $\quad n \rightarrow$ no. of FF's, $N \rightarrow$ no. of States.

$2^n \geq 3$

$\therefore n = 2$

$\therefore$ FF's required = 2
FF's using → T FF's

Step 4: State Assignment

Assign Binary values to States.

$a = 00$, $b = 01$, $c = 10$

Step 5: Exitation table

Present State Q_A	Present State Q_B	i/p X	Next State Q_{A+1}	Next State Q_{B+1}	FF i/p's T_A	FF i/p's T_B	o/p Y
0	0	0	0	1	0	1	0
0	0	1	0	1	0	1	0
0	1	0	1	0	1	1	0
0	1	1	1	0	1	1	0
1	0	0	1	0	0	0	1
1	0	1	0	0	1	0	1

∵ T-FF exitation table

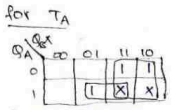
Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

State 11 is unused state. ∴ Treat that state as dont care.

Step 6: K-Map simplification

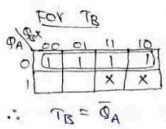
K-Map simplification for FF's i/p functions and sequential circuit o/p function.

for T_A



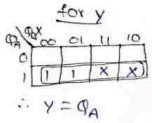
$\therefore T_A = Q_A X + Q_B$

For T_B



$\therefore T_B = \bar{Q}_A$

for Y



$\therefore Y = Q_A$

Step 6: LOGIC DIAGRAM

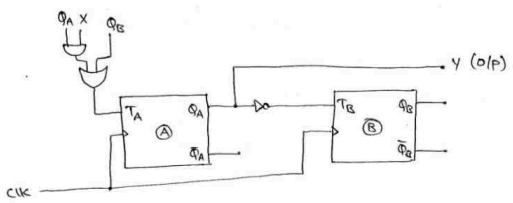
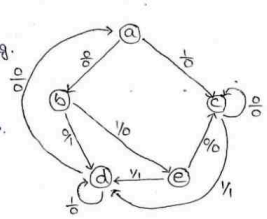


Fig:- logic diagram of Moore Sequential ckt for given State diagram.

Q:- Design a clocked sequential circuit for State diagram shown below.

Sol:- Given State diag. has 5 States with one i/p and one o/p.



considering,

$X \rightarrow$ i/p
$Y \rightarrow$ o/p.

Step 1: State table

Present State	Next State X=0	Next State X=1	o/p (Y) X=0	o/p (Y) X=1
a	b	c	0	0
b	d	e	1	0
✓ c	c	d	0	1
d	a	d	0	0
x e	c	d	0	1

c & e states Next states and o/p's are same.
∴ we can cancel either c (or) e state. if e is cancelled then replace e with c.

Reduced state table

present state	Next State x=0	Next State x=1	o/p(y) x=0	o/p(y) x=1
a	b	c	0	0
b	d	c	1	0
c	c	d	0	1
d	a	d	0	0

Step 2: Determine no. of FF's required.

no. of FF's required to design seq. ckt can be determined by the eq.,

$2^n \geq N$ n → no. of FF's, N → no. of states.

$2^n \geq 4$ (∵ After state reduction N=4)

∴ n=2

∴ no. of FF's required = 2

FF's using → D-FF's.

Step 3: State Assignment

Assign Binary values to states

a=00 , b=01 , c=10 , d=11

Step 4: Exitation table

(for procedure refer previous problem)

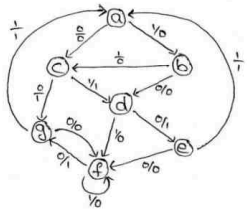
Step 5: K-map simplification

Step 6: Logic diagram

Q:- Design a clocked seq. circuit for state diagram shown below.

Sol:- The given state diag. has 7 states with one i/p & one o/p.

considering X → i/p
Y → o/p.



Step1: State table

Present state	Next State x=0	Next State x=1	o/p(y) x=0	o/p(y) x=1
a	c	b	0	0
b	d	c	0	0
c	~~g~~ e	d	1	1
d	e	f	1	0
✓ e	f	a	0	1
f	~~g~~ e	f	1	0
x ~~g~~	f	a	0	1

e & g states Next states and o/p's are same.
∴ we can cancel either e (or) g state. If 'g' is cancelled then replace g with e.

reduced state table

Present state	Next State x=0	Next State x=1	o/p(y) x=0	o/p(y) x=1
a	c	b	0	0
b	d	c	0	0
c	e	d	1	1
✓ d	e	~~f~~ d	1	0
e	~~f~~ d	a	0	1
x ~~f~~	e	f	1	0

d and f states Next states and o/p's are same.
∴ we can cancel either d (or) f state. If 'f' is cancelled then replace 'f' with 'd'

final reduced state table

present state	Next state x=0	Next state x=1	o/p (y) x=0	o/p (y) x=1
a	c	b	0	0
b	d	c	0	0
c	e	d	1	1
d	e	d	1	0
e	d	a	0	1

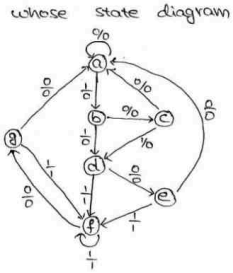
Step 2:
no. of FF's required = 3 ($\because 2^n \geq 5$, $n=3$)
FF's using → D FF's.

Step 3: state Assignment
Assign binary values to states
a = 000, b = 001, c = 010, d = 011, e = 100
101, 110, 111 are unused states.
∴ treat them as don't cares.
(i.e) for 101, 110, 111 states, Next states and i/p and o/p's are don't cares.

Step 4: Excitation table
Step 5: K-map simplification
Step 6: Logic diagram

25/10/2014

Q:- Obtain the reduced state table and reduced state diagram for a sequential ckt whose state diagram shown below.



Sol:- The give state diagram has 7 states, one i/p & 1 o/p.
considering, x → i/p

Step 1: state table

present state	Next state x=0	Next state x=1	o/p x=0	o/p x=1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
✓ e	a	f	0	1
f	~~g~~ e	f	0	1
x ~~g~~	a	f	0	1

∴ e & g states Next states and o/p's are same.
∴ we can cancel either e (or) g state. If 'g' is cancelled then replace g with e.

reduced state table

present state	Next state x=0	Next state x=1	o/p x=0	o/p x=1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
✓ d	e	~~f~~ d	0	1
e	a	~~f~~ d	0	1
x f	e	f	0	1

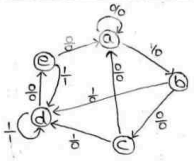
∴ d & f states next states and o/p's are same.

∴ we can cancel either d (or) f state. If 'f' is cancelled then replace 'f' with 'd'.

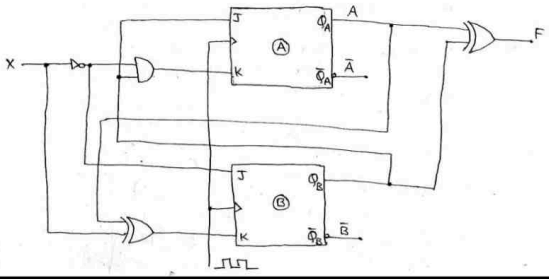
Final reduced state table

Present State	Next State X=0	Next State X=1	o/p X=0	o/p X=1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	d	0	1
e	a	d	0	1

Reduced state diagram:



Q.:- Derive the transition table, state table & state diagram for the Moore sequential circuit given below.



Sol:- Step 1: Determine the FF i/p eq.'s & the o/p eq.'s of sequential circuit from the above seq. ckt.

FF i/p eq.'s

$J_A = Q_B$

$K_A = \bar{X}Q_B$

$J_B = \bar{X}$

$K_B = Q_A \oplus X$

Seq. circuit o/p

$F = Q_A \oplus Q_B$

Step 2: Derive the transition eq.'s.

The transition eq.'s for JK FF's can be derived from the characterstic eq. of JK FF.

Char. eq. of JK FF is $Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$

$Q_{A+1} = J_A\bar{Q}_A + \bar{K}_A Q_A$

After substituting J_A & K_A eqn's,

Above eqn. becomes,

$\therefore \boxed{Q_{A+1} = Q_B\bar{Q}_A + (\bar{X}Q_B)Q_A}$

$Q_{B+1} = J_B\bar{Q}_B + \bar{K}_B Q_B$

After substituting J_B & K_B eqn's,

Above eqn. becomes,

$\therefore \boxed{Q_{B+1} = \bar{X}\bar{Q}_B + (Q_A \oplus X)Q_B}$

Step 3: Transition table

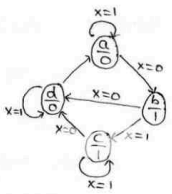
Present State Q_A	Present State Q_B	Next State X=0 Q_{A+1}	Next State X=0 Q_{B+1}	Next State X=1 Q_{A+1}	Next State X=1 Q_{B+1}	Output F
0	0	0	1	0	0	0
0	1	1	1	1	0	1
1	0	1	1	1	0	1
1	1	0	0	1	1	0

Step 4: State table

considering a=00, b=01, c=10, d=11.

Present State	Next State x=0	Next State x=1	o/p (F)
a	b	a	0
b	d	c	1
c	d	c	1
d	a	d	0

Step 5: State diagram



A	(or)	Q_A			Different representations
A^+	(or)	Q_{A+1}	(or)	A(t+1) (or)	Q_A^+

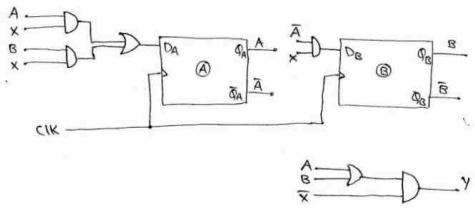
Q.: A sequential circuit with two D-FF's A & B and i/p x & o/p y. is specified by the following Next state and o/p equations.

$A(t+1) = Ax + Bx$

$B(t+1) = A'x$; $y = (A+B)x'$

(i) Draw the logic diagram of the ckt.
(ii) Derive the State table
(iii) Derive the State diagram.

Sol: (i) logic diagram



for D-FF, o/p = i/p.

$\therefore D_A = A(t+1)$

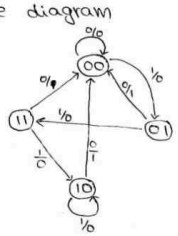
$D_B = B(t+1)$.

(ii) State table

Present State A	Present State B	Next State x=0 A(t+1)	Next State x=0 B(t+1)	Next State x=1 A(t+1)	Next State x=1 B(t+1)	o/p (y) x=0	o/p (y) x=1
0	0	0	0	0	1	0	0
0	1	0	0	1	1	1	0
1	0	0	0	1	0	1	0
1	1	0	0	1	0	1	0

(iii) State diagram

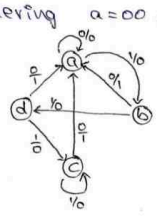
considering a=00, b=01 c=10, d=11.



present state	Next state x=0	Next state x=1	o/p(y) x=0	o/p(y) x=1
a	a	b	0	0
b	a	d	1	0
c	a	c	1	0
d	a	c	1	0

(or)

considering a=00, b=01, c=10, d=11



28/10/2014

* Hazards :-

→ Hazards are unwanted switching transients that may appear at the o/p of a circuit because different paths exibit different propagation delays.

→ Hazards occur in combinational circuits, where they may cause a temparary false o/p value. When this condition occurs in sequential circuits, it may result in a transition to a wrong stable state.

Classification of Hazards :-

There are 3 different types of Hazards.

(i) Static Hazard
- Static-0 Hazard
- Static-1 Hazard

(ii) Dynamic Hazard

(iii) Essential Hazard

1. (i) Static-1 Hazard :-

When a circuit output goes to momentarily '0', where it has to remain at constant '1', then we say that circuit has "Static-1 Hazard".

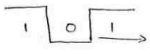


Fig:- Static-1 Hazard.

(ii) Static-0 Hazard :-

When a circuit output goes to momentarily '1'. where it has to remain at constant '0', then we say that circuit has "Static-0 Hazard".

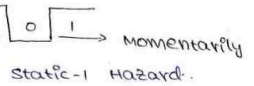


Fig:- Static-0 Hazard.

2. Dynamic Hazard :-

When the o/p is supposed to change from '0' to '1' (or) '1' to '0', if o/p changes more no. of times then this transient is called "Dynamic Hazard."

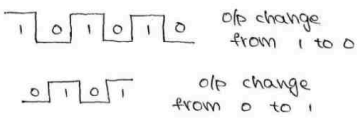
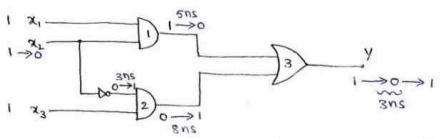


Fig:- Dynamic Hazard.

combinational circuit with static-1 Hazard



Propagation delay of AND gate = 5 ns

NOT gate = 3 ns

∴ propagation delay of 1st path is 5ns

2nd path is 8ns.

This ckt displays wrong o/p '0' for 3ns when i/p changes from $1_{x_1}\,1_{x_2}\,1_{x_3}$ to $1_{x_1}\,0_{x_2}\,1_{x_3}$

3. Essential Hazards:-

→ The static and dynamic Hazards can occur in combinational as well as sequential logic circuits.

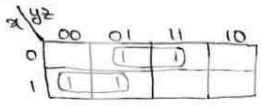
→ Essential Hazards occur in sequential circuits only.

→ An Essential Hazard is caused by unequal delays along two or more paths that originate from the same input.

Q. :- Realize the boolean function $T(x,y,z) = \Sigma(1,3,4,5)$ using logic gates for Hazard free.

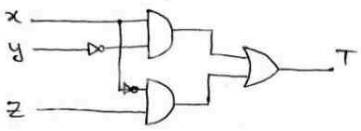
Sol:- K-map simplification & logic circuit of above function T with Hazard are :-

K-map



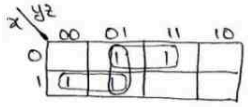
$\therefore T = x\bar{y} + \bar{x}z$

logic circuit



For designing Hazard free circuit :-

K-map



(∵ combined all the possible groups)

$\therefore T = x\bar{y} + \bar{x}z + \bar{y}z$

Hazard free logic circuit :-