Unit 3 & Unit 4

Objective type question & answer

1. Which of the following is not only an input peripheral device: -
   a. Keyboard
   b. Scanner
   c. Digitizer
   d. Magnetic tape

   Ans: d

2. Which of the following is not an input peripheral device: -
   a. Keyboard
   b. Light Pen
   c. Printer
   d. Bar code reader

   Ans: c

3. The CISC stands for _____
   a. Computer Instruction Set Compliment
   b. Complete Instruction Set Compliment
   c. Computer Indexed Set Components
   d. Complex Instruction set computer
      Ans-d
   e. Which of the architecture is power efficient?
      a) CISC
      b) RISC
      c) ISA
      d) IANA

   Ans:-b
4. The computer architecture aimed at reducing the time of execution of instructions is _____
   a) CISC
   b) RISC
   c) ISA
   d) ANNA
   Ans:-b

5. As the storing of data words onto the stack is increased, the stack pointer is: -

   a) incremented by 1
   b) decremented by 1
   c) incremented by 2
   d) decremented by 2
   Ans:- a

6. Which of the following is a data transfer instruction?

a) STA 16-bit address
b) ADD A, B
c) MUL C, D
d) RET
ans: -a

7. What kind of a flag is the sign flag?

a) General Purpose
b) Status
c) Address
d) Instruction
ans:-b

8. The instruction, Add #45,R1 does _____

a) Adds the value of 45 to the address of R1 and stores 45 in that address
b) Adds 45 to the value of R1 and stores it in R1
c) Finds the memory location 45 and adds that content to that of R1
d) None of the mentioned
ans:-b

9. The addressing mode/s, which uses the PC instead of a general-purpose register is _____

a) Indexed with offset
b) Relative
c) Direct
d) Both Indexed with offset and direct
Ans:-b

10. When we use auto increment or auto decrements, which of the following is/are true?

1) In both, the address is used to retrieve the operand and then the address gets altered
2) In auto increment, the operand is retrieved first and then the address altered
3) Both of them can be used on general purpose registers as well as memory locations
a) 1, 2, 3
b) 2
c) 1, 3
d) 2, 3
Ans:- d

11. The addressing mode, where you directly specify the operand value is _____

a) Immediate
b) Direct
c) Definite
d) Relative
Ans:- a

12. Which of the following is a group of bits that instruct the computer to perform a specific operation: -

a. Address

b. Memory
c. Program counter
d. Instruction code
Ans:- d

13. In a stack, if a user tries to remove an element from an empty stack it is called _____

a) Underflow
b) Empty collection
c) Overflow
d) Garbage Collection
Ans:-a

14. Pushing an element into stack already having five elements and stack size of 5, then stack becomes _____

a) Overflow
b) Crash
c) Underflow
d) User flow
Ans:-a

16. What is the value of the postfix expression 6 3 2 6 + – *?

a) -30
b) 40
c) 74
d) -18
Ans:-a

How to solve it, Example: - Postfix Expression is (6*(3-(2+6))) = -30.

17. What is the value of the postfix expression 6 9 2 4 + – *?

a) 28
b) 18
c) 74
d) -18
Ans:- b

18. What is the value of the postfix expression 10 3 2 4 + – *?

a) 1
b) -30
c) 74
d) 3
Ans:- b

19. What is the value of the postfix expression 6 3 2 4 + – *?

a) 1
b) 40
c) 74

d) -18
Ans: -d

20. Which one of the following control words is true for the given microoperation **R6<-- R5+1**

a. 10100001000000
b. 10100011000001
c. 10100100000001
d. 10100010000001

Ans:- b

21. Which one of the following control words is true for the given microoperation R6<-- R5-R2

a. 10101011001101
b. 10101011000101
c. 11010100100001
d. 11010100101010
Ans: b

22. Which one of the following control words is true for the given microoperation R6<-- R5+R2

a. 10101011001101
b. 10101011000010
c. 11010100100001
d. 11010100101010
Ans:- b

24. Which one of the following control words is true for the given microoperation R6<-- R5 v R2

e. 10101011001010
f. 10101011001001
g. 11010100100001
h. 11010100101010
Ans:-a

25. The postfix form of the expression (A+ B)*(C*D- E)*F / G is?

a. AB+ CD*E - FG /**
b. AB + CD* E - F **G /
c. AB + CD* E - *F *G /
d. AB + CDE * - * F *G /
Ans:- a

26. The postfix form of the expression (A- B)*(C*D- E)*F / G is?

a. AB - CD* E - F **G /
b. AB- CD*E - FG /**
c. AB -CD* E - *F *G /
d. AB - CDE * - * F *G /
Ans:- b

27. The postfix form of the expression (2+ B)*(C*D- E)*F / G is?

a. 2B + CD* E - F **G /
b. 2B + CD* E - *F *G /
c. 2B + CDE * - * F *G /
d. 2B+ CD*E - FG /**

Ans:- d

28. The postfix form of the expression (A+ B)*(C*D + E)*F / G is?

a. AB + CD* E + F **G /
b. AB + CD* E +*F *G /
c. AB+ CD*E +FG /**
d. AB + CDE * - * F *G /

Ans:- c

29. ASCII code of ND when represented using 8 binary bit is:

a. 1001110010001010
b. 0100111001000110
c. 1001110010001010
d. 0100111001000100

Ans:- d

30. ASCII code of BS when represented using 8 binary bit is:

a. 0100001001010011
b. 0100001001010111
c. 0100101001010111
d. 1000010010100011

Ans:- a

31. ASCII code of CS when represented using 8 binary bit is:

a. 0100010101110011
b. 0100001101010011
c. 0100001101010111
d. 0110001101010111

Ans:- b

32. ASCII code of EU when represented using 8 binary bit is:

a. 010001110 1010101
b. 010001010 1011101
c. 010001110 1010101
d. 010001010 1010101

Ans:-d

34. How many types of modes of I/O Data Transfer?

A. 2

B. 3

C. 4

D. 5

Answer:- b

35. Keyboard, scanner and Mouse Comes under?

A. Input peripherals

B. Output peripherals

C. Input-Output peripherals

D. None of the above

Answer:-a

36. The method which offers higher speeds of I/O transfers is _____

A. Interrupts

B. Memory mapping

C. Program-controlled I/O

D. DMA

Answer:-d

37. In memory-mapped I/O _____

A. The I/O devices have a separate address space

B. The I/O devices and the memory share the same address space

C. A part of the memory is specifically set aside for the I/O operation

D. The memory and I/O devices have an associated address space

Ans : B

38. The address of a terminal connected to a data communication processor consists of two letters of the alphabet or a letter and one of the 10 numerals. How many different addresses can be formulated.

a. 676
b. 260
c. 936
d. 1196

Ans : d

How to solve: -

Solution: - total outcomes = 26X26 + 26X10 + 10X26 = 936

39. The address of a terminal connected to a data communication processor consists of three digits of the 10 numerals. How many different addresses can be formulated.

a. 676
b. 1000
c. 936
d. 1196

Ans : B

How to solve: -
Solution: - total outcomes = 10X10X10 = 1000

40. The address of a terminal connected to a data communication processor consists of two letters. One of the alphabets and a letter of one of the 10 numerals. How many different addresses can be formulated.

a. 676
b. 260
c. 936
d. 520

Ans : d

How to solve: -
Solution: - total outcomes = 26X10 + 10X26 = 520

41. Indicate which one of the following constitute a control: -

a. Skip next instruction if flag is set.
b. Seek a given record on a magnetic disk.
c. Check if I/O device is ready.
d. Read interface status register

Ans: b

42. Indicate which one of the following constitute a status commands: -

a. Seek a given record on a magnetic disk.
b. Move printer paper to beginning of next page.
c. Check if I/O device is ready.
d. Read interface status register

Ans: c

45. Indicate which one of the following constitute a data transfer commands.

a. Skip next instruction if flag is set.
b. Check if I/O device is ready.
c. Move printer paper to beginning of next page.
d. Read interface status register

Ans: d

46. A computer uses a memory unit with 128K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part. How many bits are there in the operation code?

a. 6
b. 7
c. 8
d. 9

Ans: c

47. A computer uses a memory unit with 512K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part. How many bits are there in the operation code?

a. 6
b. 7
c. 8
d. 9

Ans: a

48. A computer uses a memory unit with 64K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part. How many bits are there in the operation code?

a. 6
b. 7
c. 8
d. 9

Ans: d

49. Which of the following is not an One-Address Instructions:-

LOAD A
ADD B
STORE T
PUSH A

50. What is the content of stack pointer (SP)?

a. Address of the top element in the stack
b. Address of current instruction
c. Address of next instruction
d. None of the above
Ans:-a

3. Which of the architecture is power efficient?

a) RISC
b) ISA
c) IANA
d) CISC

Ans:-a

51. Which of the followings is not a data transfer instruction: -
    a. Exchange
    b. Push
    c. Pop
    d. Add

    Ans:- d

52. The signal sent to the device from the processor to the device after receiving an interrupt is _____

a) Interrupt-acknowledge
b) Return signal
c) Service signal
d) Permission signal

Ans:- a

53. The return address from the interrupt-service routine is stored on the _____
    a. System heap
    b. Processor register
    c. Processor stack
    d. Memory

    Ans:- c

54. Consider the following statements.
    I. Daisy chaining is used to assign priorities in attending interrupts.
    II. When a device raises a vectored interrupt, the CPU does polling to identify the source of interrupt.
    III. In polling,the CPU periodically checks the status bits to know if any device needs its attention.
    IV. During DMA, both the CPU and DMA controller can be bus masters at the same time.

    Which of the above statements is/are TRUE?

    (A) Ⅰ and Ⅱ only

    (B) Ⅰ and Ⅳ only

    (C) Ⅰ and Ⅲ only

    (D) Ⅲ only

    Ans:-c

55. Match the following I/O concepts to their respective descriptions:

    1. Asynchronous Data Transfer

    2. Programmed I/O

    3. Interrupt I/O

4. I/O Processor

Descriptions:

A. This method allows devices to transfer data without being synchronized with the CPU clock.

B. In this approach, the CPU directly controls data transfer to and from devices.

C. It involves CPU-initiated polling for I/O device status.

D. A specialized unit assists the CPU in handling I/O operations, offloading some of the work.

Match each concept (1, 2, 3, 4) to the correct description (A, B, C, D).

a. 1-B, 2-A, 3-C, 4-D
b. 1-A, 2-B, 3-D, 4-C
c. 1-B, 2-C, 3-D, 4-A
d. 1-A, 2-B, 3-C, 4-D

Ans: - a

56. Which of the following is NOT a type of interrupt commonly used in computer systems?

a. Maskable Interrupt
b. Non-Maskable Interrupt
c. Parallel Interrupt
d. Software Interrupt

Ans:- c

57. In indexed addressing mode, what is added to the base address to calculate the effective address?
    a. The contents of the program counter
    b. The immediate value
    c. The contents of a memory location
    d. The contents of an index register

    Ans:- b

58. In computer architecture, what is the primary purpose of addressing modes?
    a. To control the clock speed of the CPU.
    b. To specify the size of the memory address bus.
    c. To define how the CPU accesses operands in memory.
    d. To determine the number of CPU registers.

    Ans:- c

59. Match the interrupt type with its description:
    A) Maskable Interrupt B) Non-Maskable Interrupt C) Priority Interrupt D) Software Interrupt
    1. Cannot be disabled or masked by the CPU.
    2. Can be disabled or enabled by the CPU as needed.
    3. Assigned priority levels to determine which interrupt to service first.

4. Generated by software instructions during program execution.
    a. A-1, B-2, C-4, D-3
    b. A-1, B-2, C-3, D-4
    c. A-2, B-1, C-4, D-3
    d. A-2, B-1, C-3, D-4
    Ans:- a