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# 文档2.2 ARMv8-A指令手册梳理报告

# ARMv8-A指令概述

ARMv8-A指令集是与ARMv8-A架构相配套的指令集，ARMv8-A架构包括两种运行环境：AArch64和AArch32。AArch64运行环境下，使用ARMv8-A64指令集，它与旧的32位指令集不同，它可以访问64位大小的内存指针，访问64位宽的寄存器并进行数据操作。AArch32运行环境下，使用A32或T32指令集，它们由原有的ARM指令集和Thumb指令集发展而来，与ARMv7架构兼容。

# 敏感指令定义

本项目根据指令的执行条件、执行语义、执行结果等信息将 A64 指令集划分为敏感指令和非敏感指令。本项目定义非敏感指令为用户态下和内核态下行为一致的指令，敏感指令为用户态下和内核态下行为可能不一致的指令。指令行为即指令对机器状态的修改，它取决于当前机器的系统配置和执行时上下文。

ARMv8-A64 指令集中，当处理器的系统配置变化时，指令的行为也会产生变化。因此，本项目根据指令依赖的系统配置情况对敏感指令进行了划分，分为无条件（Unconditional）敏感指令和有条件（Conditional）敏感指令两大类。无条件敏感指令为任意系统配置下行为均不一致的指令，在 ARMv8-A64 指令集中该类指令全部为用户态下不可执行的特权指令，它们在用户态下行为无定义（UNDEFINED），在内核态下有行为。有条件敏感指令为只有在部分系统配置下，用户态和内核态行为才不一致的指令。

综上所述，本项目将Armv8-A64指令集分为了非敏感指令、无条件敏感指令和有条件敏感指令三类，它们的形式化定义如表1所示，其中，S为所有可能的系统配置集合， 为指令在用户态下的行为， 为指令在内核态下的行为。

|  |  |  |  |
| --- | --- | --- | --- |
|  | **非敏感指令** | **无条件敏感指令** | **有条件敏感指令** |
| **用户态下行为** | -- |  |  |
| **内核态下行为** | -- |  |  |
| **行为一致性** |  |  |  |
| **解释** | 在任何配置下，行为均一致 | 存在配置使得指令行为不一致，且用户上下文中指令行为一定是UNDEFINED | 存在配置使得指令行为不一致，但用户上下文中指令行为不一定为UNDEFINED |

表格 1指令分类定义

# 敏感指令分类和处理方法

对于不同敏感指令，本项目的指令截获模块将采取不同的处理方法，本节给出所有敏感指令的分类和对应的处理方法。

对于无条件敏感指令，本模块将直接阻止该类指令的执行，一旦指令扫描时发现程序中出现了该指令就报错。

对于有条件敏感指令，本项目直接将系统配置确定为M1(TODO)机器默认的系统配置，此时，内核运行在EL2权级下，用户程序运行在EL0权级下。确定了系统配置后，有条件敏感指令将进一步被分为以下三种情况：

1. 若根据当前系统配置，该指令成为非敏感指令，则内核态应用可

以直接执行，无需处理（配置）；

1. 若根据当前系统配置，该指令成为用户态下不可执行、内核态下

可执行的敏感指令，则扫描模块将阻止该指令的执行（配置&过滤）；

1. 若根据当前系统配置，该指令成为用户态和内核态均可执行，但

行为不一致的敏感指令，则扫描模块将把该指令替换为brk指令，执行时，由模拟模块截获brk异常并模拟该指令的用户态行为后返回（配置&下陷）。

部分敏感指令的分类、配置及处理方法如表2所示。其中条件栏省略了配置条件：EL2Enable() && !HaveEL(EL3) && HCR\_EL2.<E2H,TGE>=11，这些配置表示当前系统使用EL0 和两个权级，EL2充当 host，EL0 充当 guest，EL0 下的异常由 EL2 处理。

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **序号** | **类型** | **指令** | **条件** | **阻止方法** |
| 1 | 无条件敏感指令 | DC CGDSW, DC CSW, IC IALLU... | -- | ①过滤 |
| 2 | AT S12E0R, AT S1E2R... |
| 3 | TLBI ALLE1, TLBI ASIDE1, TLBI RVAALE1... |
| 4 | MRS <Xt>,[CurrentEL/ELR\_EL1…], MSR [ELR\_EL1/PAN...],<Xt> |
| 5 | ERET, HVC… |
| 6 | 有条件敏感指令 | DC CIVAC, DC CVAC, DC CVAU, IC IVAU… | SCTLR\_EL2.<UCI,DZE> = 11 | ②配置 |
| 7 | MRS <Xt>,[FPCR/ID\_AA64AFR0\_EL1…], MSR [FPCR…],<Xt> | IDST supported && CPTR\_EL2.FPEN = 11&& CNTHCTL\_EL2.<EL0PCTEN,EL0VCTEN> = 01 |
| 8 | CASB, LDADDB, WFE, LD1 (multiple structures) … | SCTLR.EL2.<SAO,SA,E0E,EE,nTWE> = 11001 |
| 9 | ADDG, LDG, MRS <Xt> TCO, MSR TCO, <Xt>… | Unsupported Hardware Features |
| 10 | DGH |
| 11 | LD64B, ST64B, ST64BV, ST64BV0 |
| 12 | PSB CSYNC |
| 13 | TSB CSYNC |
| 14 | WFET, WFIT |
| 15 | MRS <Xt>, [RNDR/RNDRRS] |
| 16 | MRS <Xt>, [PMCCFILTR\_EL0…], MSR [PMCCFILTR\_EL0...], <Xt> |
| 17 | MRS <Xt>, [AMCFGR\_EL0…], MSR [AMCNTENCLR0\_EL0...], <Xt> |
| 18 | CFP RCTX, CPP RCTX, DVP RCTX | SCTLR\_EL2.EnRTCTX = 0 | ③配置&过滤 |
| 19 | MRS <Xt>, [CNTP\_CTL\_EL0…], MSR [CNTP\_CTL\_EL0…], <Xt> | SCTLR\_EL2.TSCXT = 1 && CNTHCTL\_EL2.<EL0PTEN,EL0VTEN,EL0PCTEN> = 000, |
| 20 | MRS <Xt>, [CTR\_EL0/MPIDR\_EL1…], WFI | IDST supported && SCTLR\_EL2.UCT = 0 && SCTLR\_EL2.nTWI = 0 | ④配置&下陷 |

表格2敏感指令分类表

# 附录：敏感指令列表

|  |
| --- |
| 无条件敏感指令-过滤 |
| C5.2.1 MRS <Xt>, CurrentEL Current Exception Level |
| C5.2.4 MRS <Xt>, ELR\_EL1 Exception Link Register (EL1) |
| C5.2.4 MSR ELR\_EL1, <Xt> Exception Link Register (EL1) |
| C5.2.4 MRS <Xt>, ELR\_EL12 Exception Link Register (EL1) |
| C5.2.4 MSR ELR\_EL12, <Xt> Exception Link Register (EL1) |
| C5.2.5 MRS <Xt>, ELR\_EL2 Exception Link Register (EL2) |
| C5.2.5 MSR ELR\_EL2, <Xt> Exception Link Register (EL2) |
| C5.2.10 MRS <Xt>, PAN Privileged Access Never |
| C5.2.10 MSR PAN, <Xt> Privileged Access Never |
| C5.2.11 MRS <Xt>, SP\_EL0 Stack Pointer (EL0) |
| C5.2.11 MSR SP\_EL0, <Xt> Stack Pointer (EL0) |
| C5.2.12 MRS <Xt>, SP\_EL1 Stack Pointer (EL1) |
| C5.2.12 MSR SP\_EL1, <Xt> Stack Pointer (EL1) |
| C5.2.15 MRS <Xt>, SPSel Stack Pointer Select |
| C5.2.15 MSR SPSel, <Xt> Stack Pointer Select |
| C5.2.16 MRS <Xt>, SPSR\_abt Saved Program Status Register (Abort mode) |
| C5.2.16 MSR SPSR\_abt, <Xt> Saved Program Status Register (Abort mode) |
| C5.2.17 MRS <Xt>, SPSR\_EL1 Saved Program Status Register (EL1) |
| C5.2.17 MSR SPSR\_EL1, <Xt> Saved Program Status Register (EL1) |
| C5.2.17 MRS <Xt>, SPSR\_EL12 Saved Program Status Register (EL1) |
| C5.2.17 MSR SPSR\_EL12, <Xt> Saved Program Status Register (EL1) |
| C5.2.18 MRS <Xt>, SPSR\_EL2 Saved Program Status Register (EL2) |
| C5.2.18 MSR SPSR\_EL2, <Xt> Saved Program Status Register (EL2) |
| C5.2.20 MRS <Xt>, SPSR\_fiq Saved Program Status Register (FIQ mode) |
| C5.2.20 MSR SPSR\_fiq, <Xt> Saved Program Status Register (FIQ mode) |
| C5.2.21 MRS <Xt>, SPSR\_irq Saved Program Status Register (IRQ mode) |
| C5.2.21 MSR SPSR\_irq, <Xt> Saved Program Status Register (IRQ mode) |
| C5.2.22 MRS <Xt>, SPSR\_und Saved Program Status Register (Undefined mode) |
| C5.2.22 MSR SPSR\_und, <Xt> Saved Program Status Register (Undefined mode) |
| C5.2.25 MRS <Xt>, UAO User Access Override |
| C5.2.25 MSR UAO, <Xt> User Access Override |
| C5.3.1 DC CGDSW Clean of Data and Allocation Tags by Set/Way |
| C5.3.5 DC CGSW Clean of Allocation Tags by Set/Way |
| C5.3.9 DC CIGDSW Clean and Invalidate of Data and Allocation Tags by Set/Way |
| C5.3.11 DC CIGSW Clean and Invalidate of Allocation Tags by Set/Way |
| C5.3.13 DC CISW Data or unified Cache line Clean and Invalidate by Set/Way |
| C5.3.15 DC CSW Data or unified Cache line Clean by Set/Way |
| C5.3.22 DC IGDSW Invalidate of Data and Allocation Tags by Set/Way |
| C5.3.23 DC IGDVAC Invalidate of Data and Allocation Tags by VA to PoC |
| C5.3.24 DC IGSW Invalidate of Allocation Tags by Set/Way |
| C5.3.25 DC IGVAC Invalidate of Allocation Tags by VA to PoC |
| C5.3.26 DC ISW Data or unified Cache line Invalidate by Set/Way |
| C5.3.27 DC IVAC Data or unified Cache line Invalidate by VA to PoC |
| C5.3.29 IC IALLU Instruction Cache Invalidate All to PoU |
| C5.3.30 IC IALLUIS Instruction Cache Invalidate All to PoU, Inner Shareable |
| C5.4.1 AT S12E0R Address Translate Stages 1 and 2 EL0 Read |
| C5.4.2 AT S12E0W Address Translate Stages 1 and 2 EL0 Write |
| C5.4.3 AT S12E1R Address Translate Stages 1 and 2 EL1 Read |
| C5.4.4 AT S12E1W Address Translate Stages 1 and 2 EL1 Write |
| C5.4.5 AT S1E0R Address Translate Stage 1 EL0 Read |
| C5.4.6 AT S1E0W Address Translate Stage 1 EL0 Write |
| C5.4.7 AT S1E1R Address Translate Stage 1 EL1 Read |
| C5.4.8 AT S1E1RP Address Translate Stage 1 EL1 Read PAN |
| C5.4.9 AT S1E1W Address Translate Stage 1 EL1 Write |
| C5.4.10 AT S1E1WP Address Translate Stage 1 EL1 Write PAN |
| C5.4.11 AT S1E2R Address Translate Stage 1 EL2 Read |
| C5.4.12 AT S1E2W Address Translate Stage 1 EL2 Write |
| C5.5.1 TLBI ALLE1 TLB Invalidate All, EL1 |
| C5.5.1 TLBI ALLE1NXS TLB Invalidate All, EL1 |
| C5.5.2 TLBI ALLE1IS TLB Invalidate All, EL1, Inner Shareable |
| C5.5.2 TLBI ALLE1ISNXS TLB Invalidate All, EL1, Inner Shareable |
| C5.5.3 TLBI ALLE1OS TL B Invalidate All, EL1, Outer Shareable |
| C5.5.3 TLBI ALLE1OSNXS TL B Invalidate All, EL1, Outer Shareable |
| C5.5.4 TLBI ALLE2 TLB Invalidate All, EL2 |
| C5.5.4 TLBI ALLE2NXS TLB Invalidate All, EL2 |
| C5.5.5 TLBI ALLE2IS TLB Invalidate All, EL2, Inner Shareable |
| C5.5.5 TLBI ALLE2ISNXS TLB Invalidate All, EL2, Inner Shareable |
| C5.5.6 TLBI ALLE2OS TL B Invalidate All, EL2, Outer Shareable |
| C5.5.6 TLBI ALLE2OSNXS TL B Invalidate All, EL2, Outer Shareable |
| C5.5.10 TLBI ASIDE1 TLB Invalidate by ASID, EL1 |
| C5.5.10 TLBI ASIDE1NXS TLB Invalidate by ASID, EL1 |
| C5.5.11 TLBI ASIDE1IS TLB Invalidate by ASID, EL1, Inner Shareable |
| C5.5.11 TLBI ASIDE1ISNXS TLB Invalidate by ASID, EL1, Inner Shareable |
| C5.5.12 TLBI ASIDE1OS TLB Invalidate by ASID, EL1, Outer Shareable |
| C5.5.12 TLBI ASIDE1OSNXS TLB Invalidate by ASID, EL1, Outer Shareable |
| C5.5.13 TLBI IPAS2E1 TLB Invalida te by Intermediate Physical Address, Stage 2, EL1 |
| C5.5.13 TLBI IPAS2E1NXS TLB Invalida te by Intermediate Physical Address, Stage 2, EL1 |
| C5.5.14 TLBI IPAS2E1IS TLB Invalidate by Intermediate Physical Address, Stage 2, EL1, Inner Shareable |
| C5.5.14 TLBI IPAS2E1ISNXS TLB Invalidate by Intermediate Physical Address, Stage 2, EL1, Inner Shareable |
| C5.5.15 TLBI IPAS2E1OS TLB Invalidate by Intermediate Physical Address, Stage 2, EL1, Outer Shareable |
| C5.5.15 TLBI IPAS2E1OSNXS TLB Invalidate by Intermediate Physical Address, Stage 2, EL1, Outer Shareable |
| C5.5.16 TLBI IPAS2LE1 TLB Invalidate by Intermediate Physical Address, Stage 2, Last level, EL1 |
| C5.5.16 TLBI IPAS2LE1NXS TLB Invalidate by Intermediate Physical Address, Stage 2, Last level, EL1 |
| C5.5.17 TLBI IPAS2LE1IS TLB Invalidate by Intermediate Physical Address, Stage 2, Last level, EL1, Inner Shareable |
| C5.5.17 TLBI IPAS2LE1ISNXS TLB Invalidate by Intermediate Physical Address, Stage 2, Last level, EL1, Inner Shareable |
| C5.5.18 TLBI IPAS2LE1OS TLB Invalidate by Intermediate Physical Address, Stage 2, Last level, EL1, Outer Shareable |
| C5.5.18 TLBI IPAS2LE1OSNXS TLB Invalidate by Intermediate Physical Address, Stage 2, Last level, EL1, Outer Shareable |
| C5.5.19 TLBI RIPAS2E1 TL B Range Invalidate by Intermediate Physical Address, Stage 2, EL1 |
| C5.5.19 TLBI RIPAS2E1NXS TL B Range Invalidate by Intermediate Physical Address, Stage 2, EL1 |
| C5.5.20 TLBI RIPAS2E1IS TLB Range Invalidate by Intermediate Physical Address, Stage 2, EL1, Inner Shareable |
| C5.5.20 TLBI RIPAS2E1ISNXS TLB Range Invalidate by Intermediate Physical Address, Stage 2, EL1, Inner Shareable |
| C5.5.21 TLBI RIPAS2E1OS TLB Range Invalidate by Intermediate Physical Address, Stage 2, EL1, Outer Shareable |
| C5.5.21 TLBI RIPAS2E1OSNXS TLB Range Invalidate by Intermediate Physical Address, Stage 2, EL1, Outer Shareable |
| C5.5.22 TLBI RIPAS2LE1 TLB Range Invalidate by Intermediate Physical Address, Stage 2, Last level, EL1 |
| C5.5.22 TLBI RIPAS2LE1NXS TLB Range Invalidate by Intermediate Physical Address, Stage 2, Last level, EL1 |
| C5.5.23 TLBI RIPAS2LE1IS TLB Range Invalidate by Intermediate Physical Address, Stage 2, Last level, EL1, Inner Shareable |
| C5.5.23 TLBI RIPAS2LE1ISNXS TLB Range Invalidate by Intermediate Physical Address, Stage 2, Last level, EL1, Inner Shareable |
| C5.5.24 TLBI RIPAS2LE1OS TLB Range Invalidate by Intermediate Physical Address, Stage 2, Last level, EL1, Outer Shareable |
| C5.5.24 TLBI RIPAS2LE1OSNXS TLB Range Invalidate by Intermediate Physical Address, Stage 2, Last level, EL1, Outer Shareable |
| C5.5.25 TLBI RVAAE1 TLB Range Invalidate by VA, All ASID, EL1 |
| C5.5.25 TLBI RVAAE1NXS TLB Range Invalidate by VA, All ASID, EL1 |
| C5.5.26 TLBI RVAAE1IS TLB Range Invalidate by VA, All ASID, EL1, Inner Shareable |
| C5.5.26 TLBI RVAAE1ISNXS TLB Range Invalidate by VA, All ASID, EL1, Inner Shareable |
| C5.5.27 TLBI RVAAE1OS TLB Ra nge Invalidate by VA, All ASID, EL1, Outer Shareable |
| C5.5.27 TLBI RVAAE1OSNXS TLB Ra nge Invalidate by VA, All ASID, EL1, Outer Shareable |
| C5.5.28 TLBI RVAALE1 TLB Range Invalidate by VA, All ASID, Last level, EL1 |
| C5.5.28 TLBI RVAALE1NXS TLB Range Invalidate by VA, All ASID, Last level, EL1 |
| C5.5.29 TLBI RVAALE1IS TLB Range Invalidate by VA, All ASID, Last Level, EL1, Inner Shareable |
| C5.5.29 TLBI RVAALE1ISNXS TLB Range Invalidate by VA, All ASID, Last Level, EL1, Inner Shareable |
| C5.5.30 TLBI RVAALE1OS TLB Range Invalidate by VA, All ASID, Last Level, EL1, Outer Shareable |
| C5.5.30 TLBI RVAALE1OSNXS TLB Range Invalidate by VA, All ASID, Last Level, EL1, Outer Shareable |
| C5.5.31 TLBI RVAE1 TLB Range Invalidate by VA, EL1 |
| C5.5.31 TLBI RVAE1NXS TLB Range Invalidate by VA, EL1 |
| C5.5.32 TLBI RVAE1IS TLB Range Invalidate by VA, EL1, Inner Shareable |
| C5.5.32 TLBI RVAE1ISNXS TLB Range Invalidate by VA, EL1, Inner Shareable |
| C5.5.33 TLBI RVAE1OS TLB Ra nge Invalidate by VA, EL1, Outer Shareable |
| C5.5.33 TLBI RVAE1OSNXS TLB Ra nge Invalidate by VA, EL1, Outer Shareable |
| C5.5.34 TLBI RVAE2 TLB Range Invalidate by VA, EL2 |
| C5.5.34 TLBI RVAE2NXS TLB Range Invalidate by VA, EL2 |
| C5.5.35 TLBI RVAE2IS TLB Range Invalidate by VA, EL2, Inner Shareable |
| C5.5.35 TLBI RVAE2ISNXS TLB Range Invalidate by VA, EL2, Inner Shareable |
| C5.5.36 TLBI RVAE2OS TLB Ra nge Invalidate by VA, EL2, Outer Shareable |
| C5.5.36 TLBI RVAE2OSNXS TLB Ra nge Invalidate by VA, EL2, Outer Shareable |
| C5.5.40 TLBI RVALE1 TLB Ra nge Invalidate by VA, Last level, EL1 |
| C5.5.40 TLBI RVALE1NXS TLB Ra nge Invalidate by VA, Last level, EL1 |
| C5.5.41 TLBI RVALE1IS TLB Ra nge Invalidate by VA, Last level, EL1, Inner Shareable |
| C5.5.41 TLBI RVALE1ISNXS TLB Ra nge Invalidate by VA, Last level, EL1, Inner Shareable |
| C5.5.42 TLBI RVALE1OS TLB Ra nge Invalidate by VA, Last level, EL1, Outer Shareable |
| C5.5.42 TLBI RVALE1OSNXS TLB Ra nge Invalidate by VA, Last level, EL1, Outer Shareable |
| C5.5.43 TLBI RVALE2 TLB Ra nge Invalidate by VA, Last level, EL2 |
| C5.5.43 TLBI RVALE2NXS TLB Ra nge Invalidate by VA, Last level, EL2 |
| C5.5.44 TLBI RVALE2IS TLB Ra nge Invalidate by VA, Last level, EL2, Inner Shareable |
| C5.5.44 TLBI RVALE2ISNXS TLB Ra nge Invalidate by VA, Last level, EL2, Inner Shareable |
| C5.5.45 TLBI RVALE2OS TLB Ra nge Invalidate by VA, Last level, EL2, Outer Shareable |
| C5.5.45 TLBI RVALE2OSNXS TLB Ra nge Invalidate by VA, Last level, EL2, Outer Shareable |
| C5.5.49 TLBI VAAE1 TL B Invalidate by VA, All ASID, EL1 |
| C5.5.49 TLBI VAAE1NXS TL B Invalidate by VA, All ASID, EL1 |
| C5.5.50 TLBI VAAE1IS TLB In validate by VA, All ASID, EL1, Inner Shareable |
| C5.5.50 TLBI VAAE1ISNXS TLB In validate by VA, All ASID, EL1, Inner Shareable |
| C5.5.51 TLBI VAAE1OS TLB In validate by VA, All ASID, EL1, Outer Shareable |
| C5.5.51 TLBI VAAE1OSNXS TLB In validate by VA, All ASID, EL1, Outer Shareable |
| C5.5.52 TLBI VAALE1 TLB In validate by VA, All ASID, Last level, EL1 |
| C5.5.52 TLBI VAALE1NXS TLB In validate by VA, All ASID, Last level, EL1 |
| C5.5.53 TLBI VAALE1IS TLB Inva lidate by VA, All ASID, Last Level, EL1, Inner Shareable |
| C5.5.53 TLBI VAALE1ISNXS TLB Inva lidate by VA, All ASID, Last Level, EL1, Inner Shareable |
| C5.5.54 TLBI VAALE1OS TLB Inva lidate by VA, All ASID, Last Level, EL1, Outer Shareable |
| C5.5.54 TLBI VAALE1OSNXS TLB Inva lidate by VA, All ASID, Last Level, EL1, Outer Shareable |
| C5.5.55 TLBI VAE1 TLB Invalidate by VA, EL1 |
| C5.5.55 TLBI VAE1NXS TLB Invalidate by VA, EL1 |
| C5.5.56 TLBI VAE1IS TLB Invalidate by VA, EL1, Inner Shareable |
| C5.5.56 TLBI VAE1ISNXS TLB Invalidate by VA, EL1, Inner Shareable |
| C5.5.57 TLBI VAE1OS TLB Invalidate by VA, EL1, Outer Shareable |
| C5.5.57 TLBI VAE1OSNXS TLB Invalidate by VA, EL1, Outer Shareable |
| C5.5.58 TLBI VAE2 TLB Invalidate by VA, EL2 |
| C5.5.58 TLBI VAE2NXS TLB Invalidate by VA, EL2 |
| C5.5.59 TLBI VAE2IS TLB Invalidate by VA, EL2, Inner Shareable |
| C5.5.59 TLBI VAE2ISNXS TLB Invalidate by VA, EL2, Inner Shareable |
| C5.5.60 TLBI VAE2OS TLB Invalidate by VA, EL2, Outer Shareable |
| C5.5.60 TLBI VAE2OSNXS TLB Invalidate by VA, EL2, Outer Shareable |
| C5.5.64 TLBI VALE1 TL B Invalidate by VA, Last level, EL1 |
| C5.5.64 TLBI VALE1NXS TL B Invalidate by VA, Last level, EL1 |
| C5.5.65 TLBI VALE1IS TLB Invali date by VA, Last level, EL1, Inner Shareable |
| C5.5.65 TLBI VALE1ISNXS TLB Invali date by VA, Last level, EL1, Inner Shareable |
| C5.5.66 TLBI VALE1OS TLB Inva lidate by VA, Last level, EL1, Outer Shareable |
| C5.5.66 TLBI VALE1OSNXS TLB Inva lidate by VA, Last level, EL1, Outer Shareable |
| C5.5.67 TLBI VALE2 TL B Invalidate by VA, Last level, EL2 |
| C5.5.67 TLBI VALE2NXS TL B Invalidate by VA, Last level, EL2 |
| C5.5.68 TLBI VALE2IS TLB Invali date by VA, Last level, EL2, Inner Shareable |
| C5.5.68 TLBI VALE2ISNXS TLB Invali date by VA, Last level, EL2, Inner Shareable |
| C5.5.69 TLBI VALE2OS TLB Inva lidate by VA, Last level, EL2, Outer Shareable |
| C5.5.69 TLBI VALE2OSNXS TLB Inva lidate by VA, Last level, EL2, Outer Shareable |
| C5.5.73 TLBI VMALLE1 TLB Invalidate by VMID, All at stage 1, EL1 |
| C5.5.73 TLBI VMALLE1NXS TLB Invalidate by VMID, All at stage 1, EL1 |
| C5.5.74 TLBI VMALLE1IS TLB In validate by VMID, All at stage 1, EL1, Inner Shareable |
| C5.5.74 TLBI VMALLE1ISNXS TLB In validate by VMID, All at stage 1, EL1, Inner Shareable |
| C5.5.75 TLBI VMALLE1OS TLB In validate by VMID, All at stage 1, EL1, Outer Shareable |
| C5.5.75 TLBI VMALLE1OSNXS TLB In validate by VMID, All at stage 1, EL1, Outer Shareable |
| C5.5.76 TLBI VMALLS12E1 TLB Invalidate by VMID, All at Stage 1 and 2, EL1 |
| C5.5.76 TLBI VMALLS12E1NXS TLB Invalidate by VMID, All at Stage 1 and 2, EL1 |
| C5.5.77 TLBI VMALLS12E1IS TLB Invalidate by VMID, All at Stage 1 and 2, EL1, Inner Shareable |
| C5.5.77 TLBI VMALLS12E1ISNXS TLB Invalidate by VMID, All at Stage 1 and 2, EL1, Inner Shareable |
| C5.5.78 TLBI VMALLS12E1OS TLB Invalidate by VMID, All at Stage 1 and 2, EL1, Outer Shareable |
| C5.5.78 TLBI VMALLS12E1OSNXS TLB Invalidate by VMID, All at Stage 1 and 2, EL1, Outer Shareable |
| C6.2.87 ERET |
| C6.2.88 ERETAA, ERETA |
| C6.2.93 HLT |
| C6.2.94 HVC |
| C6.2.195 MSR (immediate)\* |
| C6.2.241   SMC |
| D13.2.1 MRS <Xt>, ACCDATA\_EL1 Accelerator Data |
| D13.2.1 MSR ACCDATA\_EL1, <Xt> Accelerator Data |
| D13.2.2 MRS <Xt>, ACTLR\_EL1 Auxiliary Control Register (EL1) |
| D13.2.2 MSR ACTLR\_EL1, <Xt> Auxiliary Control Register (EL1) |
| D13.2.3 MRS <Xt>, ACTLR\_EL2 Auxiliary Control Register (EL2) |
| D13.2.3 MSR ACTLR\_EL2, <Xt> Auxiliary Control Register (EL2) |
| D13.2.5 MRS <Xt>, AFSR0\_EL1 Auxiliary Fault Status Register 0 (EL1) |
| D13.2.5 MSR AFSR0\_EL1, <Xt> Auxiliary Fault Status Register 0 (EL1) |
| D13.2.5 MRS <Xt>, AFSR0\_EL12 Auxiliary Fault Status Register 0 (EL1) |
| D13.2.5 MSR AFSR0\_EL12, <Xt> Auxiliary Fault Status Register 0 (EL1) |
| D13.2.6 MRS <Xt>, AFSR0\_EL2 Auxiliary Fault Status Register 0 (EL2) |
| D13.2.6 MSR AFSR0\_EL2, <Xt> Auxiliary Fault Status Register 0 (EL2) |
| D13.2.8 MRS <Xt>, AFSR1\_EL1 Auxiliary Fault Status Register 1 (EL1) |
| D13.2.8 MSR AFSR1\_EL1, <Xt> Auxiliary Fault Status Register 1 (EL1) |
| D13.2.8 MRS <Xt>, AFSR1\_EL12 Auxiliary Fault Status Register 1 (EL1) |
| D13.2.8 MSR AFSR1\_EL12, <Xt> Auxiliary Fault Status Register 1 (EL1) |
| D13.2.9 MRS <Xt>, AFSR1\_EL2 Auxiliary Fault Status Register 1 (EL2) |
| D13.2.9 MSR AFSR1\_EL2, <Xt> Auxiliary Fault Status Register 1 (EL2) |
| D13.2.12 MRS <Xt>, AMAIR\_EL1 Auxiliary Memory Attribute Indirection Register (EL1) |
| D13.2.12 MSR AMAIR\_EL1, <Xt> Auxiliary Memory Attribute Indirection Register (EL1) |
| D13.2.12 MRS <Xt>, AMAIR\_EL12 Auxiliary Memory Attribute Indirection Register (EL1) |
| D13.2.12 MSR AMAIR\_EL12, <Xt> Auxiliary Memory Attribute Indirection Register (EL1) |
| D13.2.13 MRS <Xt>, AMAIR\_EL2 Auxiliary Memory Attribute Indirection Register (EL2) |
| D13.2.13 MSR AMAIR\_EL2, <Xt> Auxiliary Memory Attribute Indirection Register (EL2) |
| D13.2.15 MRS <Xt>, APDAKeyHi\_EL1 Pointer Authentication Key A for Data (bits[127:64]) |
| D13.2.15 MSR APDAKeyHi\_EL1, <Xt> Pointer Authentication Key A for Data (bits[127:64]) |
| D13.2.16 MRS <Xt>, APDAKeyLo\_EL1 Pointer Authentication Key A for Data (bits[63:0]) |
| D13.2.16 MSR APDAKeyLo\_EL1, <Xt> Pointer Authentication Key A for Data (bits[63:0]) |
| D13.2.17 MRS <Xt>, APDBKeyHi\_EL1 Pointer Authentication Key B for Data (bits[127:64]) |
| D13.2.17 MSR APDBKeyHi\_EL1, <Xt> Pointer Authentication Key B for Data (bits[127:64]) |
| D13.2.18 MRS <Xt>, APDBKeyLo\_EL1 Pointer Authentication Key B for Data (bits[63:0]) |
| D13.2.18 MSR APDBKeyLo\_EL1, <Xt> Pointer Authentication Key B for Data (bits[63:0]) |
| D13.2.19 MRS <Xt>, APGAKeyHi\_EL1 Pointer Authentication Key A for Code (bits[127:64]) |
| D13.2.19 MSR APGAKeyHi\_EL1, <Xt> Pointer Authentication Key A for Code (bits[127:64]) |
| D13.2.20 MRS <Xt>, APGAKeyLo\_EL1 Pointer Authentication Key A for Code (bits[63:0]) |
| D13.2.20 MSR APGAKeyLo\_EL1, <Xt> Pointer Authentication Key A for Code (bits[63:0]) |
| D13.2.21 MRS <Xt>, APIAKeyHi\_EL1 Pointer Authentication Key A for Instruction (bits[127:64]) |
| D13.2.21 MSR APIAKeyHi\_EL1, <Xt> Pointer Authentication Key A for Instruction (bits[127:64]) |
| D13.2.22 MRS <Xt>, APIAKeyLo\_EL1 Pointer Authentication Key A for Instruction (bits[63:0]) |
| D13.2.22 MSR APIAKeyLo\_EL1, <Xt> Pointer Authentication Key A for Instruction (bits[63:0]) |
| D13.2.23 MRS <Xt>, APIBKeyHi\_EL1 Pointer Authentication Key B for Instruction (bits[127:64]) |
| D13.2.23 MSR APIBKeyHi\_EL1, <Xt> Pointer Authentication Key B for Instruction (bits[127:64]) |
| D13.2.24 MRS <Xt>, APIBKeyLo\_EL1 Pointer Authentication Key B for Instruction (bits[63:0]) |
| D13.2.24 MSR APIBKeyLo\_EL1, <Xt> Pointer Authentication Key B for Instruction (bits[63:0]) |
| D13.2.28 MRS <Xt>, CONTEXTIDR\_EL1 Context ID Register (EL1) |
| D13.2.28 MSR CONTEXTIDR\_EL1, <Xt> Context ID Register (EL1) |
| D13.2.28 MRS <Xt>, CONTEXTIDR\_EL12 Context ID Register (EL1) |
| D13.2.28 MSR CONTEXTIDR\_EL12, <Xt> Context ID Register (EL1) |
| D13.2.29 MRS <Xt>, CONTEXTIDR\_EL2 Context ID Register (EL2) |
| D13.2.29 MSR CONTEXTIDR\_EL2, <Xt> Context ID Register (EL2) |
| D13.2.30 MRS <Xt>, CPACR\_EL1 Architectural Feature Access Control Register |
| D13.2.30 MSR CPACR\_EL1, <Xt> Architectural Feature Access Control Register |
| D13.2.30 MRS <Xt>, CPACR\_EL12 Architectural Feature Access Control Register |
| D13.2.30 MSR CPACR\_EL12, <Xt> Architectural Feature Access Control Register |
| D13.2.31 MRS <Xt>, CPTR\_EL2 Architectural Feature Trap Register (EL2) |
| D13.2.31 MSR CPTR\_EL2, <Xt> Architectural Feature Trap Register (EL2) |
| D13.2.33 MRS <Xt>, CSSELR\_EL1 Cache Size Selection Register |
| D13.2.33 MSR CSSELR\_EL1, <Xt> Cache Size Selection Register |
| D13.2.35 MRS <Xt>, DACR32\_EL2 Domain Access Control Register |
| D13.2.35 MSR DACR32\_EL2, <Xt> Domain Access Control Register |
| D13.2.37 MRS <Xt>, ESR\_EL1 Exception Syndrome Register (EL1) |
| D13.2.37 MSR ESR\_EL1, <Xt> Exception Syndrome Register (EL1) |
| D13.2.37 MRS <Xt>, ESR\_EL12 Exception Syndrome Register (EL1) |
| D13.2.37 MSR ESR\_EL12, <Xt> Exception Syndrome Register (EL1) |
| D13.2.38 MRS <Xt>, ESR\_EL2 Exception Syndrome Register (EL2) |
| D13.2.38 MSR ESR\_EL2, <Xt> Exception Syndrome Register (EL2) |
| D13.2.40 MRS <Xt>, FAR\_EL1 Fault Address Register (EL1) |
| D13.2.40 MSR FAR\_EL1, <Xt> Fault Address Register (EL1) |
| D13.2.40 MRS <Xt>, FAR\_EL12 Fault Address Register (EL1) |
| D13.2.40 MSR FAR\_EL12, <Xt> Fault Address Register (EL1) |
| D13.2.41 MRS <Xt>, FAR\_EL2 Fault Address Register (EL2) |
| D13.2.41 MSR FAR\_EL2, <Xt> Fault Address Register (EL2) |
| D13.2.43 MRS <Xt>, FPEXC32\_EL2 Floating-Point Exception Control register |
| D13.2.43 MSR FPEXC32\_EL2, <Xt> Floating-Point Exception Control register |
| D13.2.44 MRS <Xt>, GCR\_EL1 Tag Control Register. |
| D13.2.44 MSR GCR\_EL1, <Xt> Tag Control Register. |
| D13.2.46 MRS <Xt>, HACR\_EL2 Hypervisor Auxiliary Control Register |
| D13.2.46 MSR HACR\_EL2, <Xt> Hypervisor Auxiliary Control Register |
| D13.2.47 MRS <Xt>, HAFGRTR\_EL2 Hypervisor Activity Monitors Fine-Grained Read Trap Register |
| D13.2.47 MSR HAFGRTR\_EL2, <Xt> Hypervisor Activity Monitors Fine-Grained Read Trap Register |
| D13.2.48 MRS <Xt>, HCR\_EL2 Hypervisor Configuration Register |
| D13.2.48 MSR HCR\_EL2, <Xt> Hypervisor Configuration Register |
| D13.2.49 MRS <Xt>, HCRX\_EL2 Extended Hypervisor Configuration Register |
| D13.2.49 MSR HCRX\_EL2, <Xt> Extended Hypervisor Configuration Register |
| D13.2.50 MRS <Xt>, HDFGRTR\_EL2 Hypervisor Debug Fine-Grained Read Trap Register |
| D13.2.50 MSR HDFGRTR\_EL2, <Xt> Hypervisor Debug Fine-Grained Read Trap Register |
| D13.2.51 MRS <Xt>, HDFGWTR\_EL2 Hypervisor Debug Fine-Grained Write Trap Register |
| D13.2.51 MSR HDFGWTR\_EL2, <Xt> Hypervisor Debug Fine-Grained Write Trap Register |
| D13.2.52 MRS <Xt>, HFGITR\_EL2 Hypervisor Fine-Grained Instruction Trap Register |
| D13.2.52 MSR HFGITR\_EL2, <Xt> Hypervisor Fine-Grained Instruction Trap Register |
| D13.2.53 MRS <Xt>, HFGRTR\_EL2 Hypervisor Fine-Grained Read Trap Register |
| D13.2.53 MSR HFGRTR\_EL2, <Xt> Hypervisor Fine-Grained Read Trap Register |
| D13.2.54 MRS <Xt>, HFGWTR\_EL2 Hypervisor Fine-Grained Write Trap Register |
| D13.2.54 MSR HFGWTR\_EL2, <Xt> Hypervisor Fine-Grained Write Trap Register |
| D13.2.55 MRS <Xt>, HPFAR\_EL2 Hypervisor IPA Fault Address Register |
| D13.2.55 MSR HPFAR\_EL2, <Xt> Hypervisor IPA Fault Address Register |
| D13.2.56 MRS <Xt>, HSTR\_EL2 Hypervisor System Trap Register |
| D13.2.56 MSR HSTR\_EL2, <Xt> Hypervisor System Trap Register |
| D13.2.88 MRS <Xt>, IFSR32\_EL2 Instruction Fault Status Register (EL2) |
| D13.2.88 MSR IFSR32\_EL2, <Xt> Instruction Fault Status Register (EL2) |
| D13.2.89 MRS <Xt>, ISR\_EL1 Interrupt Status Register |
| D13.2.90 MRS <Xt>, LORC\_EL1 LORegion Control (EL1) |
| D13.2.90 MSR LORC\_EL1, <Xt> LORegion Control (EL1) |
| D13.2.91 MRS <Xt>, LOREA\_EL1 LORegion End Address (EL1) |
| D13.2.91 MSR LOREA\_EL1, <Xt> LORegion End Address (EL1) |
| D13.2.92 MRS <Xt>, LORID\_EL1 LORegionID (EL1) |
| D13.2.93 MRS <Xt>, LORN\_EL1 LORegion Number (EL1) |
| D13.2.93 MSR LORN\_EL1, <Xt> LORegion Number (EL1) |
| D13.2.94 MRS <Xt>, LORSA\_EL1 LORegion Start Address (EL1) |
| D13.2.94 MSR LORSA\_EL1, <Xt> LORegion Start Address (EL1) |
| D13.2.95 MRS <Xt>, MAIR\_EL1 Memory Attribute Indirection Register (EL1) |
| D13.2.95 MSR MAIR\_EL1, <Xt> Memory Attribute Indirection Register (EL1) |
| D13.2.95 MRS <Xt>, MAIR\_EL12 Memory Attribute Indirection Register (EL1) |
| D13.2.95 MSR MAIR\_EL12, <Xt> Memory Attribute Indirection Register (EL1) |
| D13.2.96 MRS <Xt>, MAIR\_EL2 Memory Attribute Indirection Register (EL2) |
| D13.2.96 MSR MAIR\_EL2, <Xt> Memory Attribute Indirection Register (EL2) |
| D13.2.103 MRS <Xt>, PAR\_EL1 Physical Address Register |
| D13.2.103 MSR PAR\_EL1, <Xt> Physical Address Register |
| D13.2.105 MRS <Xt>, RGSR\_EL1 Random Allocation Tag Seed Register. |
| D13.2.105 MSR RGSR\_EL1, <Xt> Random Allocation Tag Seed Register. |
| D13.2.107 MRS <Xt>,RMR\_EL2, Reset Management Register (EL2) |
| D13.2.107 MSR RMR\_EL2,<Xt> Reset Management Register (EL2) |
| D13.2.112 MRS <Xt>,RVBAR\_EL2, Reset Vector Base Address Register (if EL3 not implemented) |
| D13.2.116 MRS <Xt>, SCTLR\_EL1 System Control Register (EL1) |
| D13.2.116 MSR SCTLR\_EL1, <Xt> System Control Register (EL1) |
| D13.2.116 MRS <Xt>, SCTLR\_EL12 System Control Register (EL1) |
| D13.2.116 MSR SCTLR\_EL12, <Xt> System Control Register (EL1) |
| D13.2.117 MRS <Xt>, SCTLR\_EL2 System Control Register (EL2) |
| D13.2.117 MSR SCTLR\_EL2, <Xt> System Control Register (EL2) |
| D13.2.120 MRS <Xt>, SCXTNUM\_EL1 EL1 Read/Write Software Context Number |
| D13.2.120 MSR SCXTNUM\_EL1, <Xt> EL1 Read/Write Software Context Number |
| D13.2.120 MRS <Xt>, SCXTNUM\_EL12 EL1 Read/Write Software Context Number |
| D13.2.120 MSR SCXTNUM\_EL12, <Xt> EL1 Read/Write Software Context Number |
| D13.2.121 MRS <Xt>, SCXTNUM\_EL2 EL2 Read/Write Software Context Number |
| D13.2.121 MSR SCXTNUM\_EL2, <Xt> EL2 Read/Write Software Context Number |
| D13.2.123 MRS <Xt>, TCR\_EL1 Translation Control Register (EL1) |
| D13.2.123 MSR TCR\_EL1, <Xt> Translation Control Register (EL1) |
| D13.2.123 MRS <Xt>, TCR\_EL12 Translation Control Register (EL1) |
| D13.2.123 MSR TCR\_EL12, <Xt> Translation Control Register (EL1) |
| D13.2.124 MRS <Xt>, TCR\_EL2 Translation Control Register (EL2) |
| D13.2.124 MSR TCR\_EL2, <Xt> Translation Control Register (EL2) |
| D13.2.126 MRS <Xt>, TFSRE0\_EL1 Tag Fault Status Register (EL0). |
| D13.2.126 MSR TFSRE0\_EL1, <Xt> Tag Fault Status Register (EL0). |
| D13.2.127 MRS <Xt>, TFSR\_EL1 Tag Fault Status Register (EL1) |
| D13.2.127 MSR TFSR\_EL1, <Xt> Tag Fault Status Register (EL1) |
| D13.2.127 MRS <Xt>, TFSR\_EL12 Tag Fault Status Register (EL1) |
| D13.2.127 MSR TFSR\_EL12, <Xt> Tag Fault Status Register (EL1) |
| D13.2.128 MRS <Xt>, TFSR\_EL2 Tag Fault Status Register (EL2) |
| D13.2.128 MSR TFSR\_EL2, <Xt> Tag Fault Status Register (EL2) |
| D13.2.131 MRS <Xt>, TPIDR\_EL1 EL1 Software Thread ID Register |
| D13.2.131 MSR TPIDR\_EL1, <Xt> EL1 Software Thread ID Register |
| D13.2.132 MRS <Xt>, TPIDR\_EL2 EL2 Software Thread ID Register |
| D13.2.132 MSR TPIDR\_EL2, <Xt> EL2 Software Thread ID Register |
| D13.2.134 MSR TPIDRRO\_EL0, <Xt> EL0 Read-Only Software Thread ID Register |
| D13.2.135 MRS <Xt>, TTBR0\_EL1 Translation Table Base Register 0 (EL1) |
| D13.2.135 MSR TTBR0\_EL1, <Xt> Translation Table Base Register 0 (EL1) |
| D13.2.135 MRS <Xt>, TTBR0\_EL12 Translation Table Base Register 0 (EL1) |
| D13.2.135 MSR TTBR0\_EL12, <Xt> Translation Table Base Register 0 (EL1) |
| D13.2.136 MRS <Xt>, TTBR0\_EL2 Translation Table Base Register 0 (EL2) |
| D13.2.136 MSR TTBR0\_EL2, <Xt> Translation Table Base Register 0 (EL2) |
| D13.2.138 MRS <Xt>, TTBR1\_EL1 Translation Table Base Register 1 (EL1) |
| D13.2.138 MSR TTBR1\_EL1, <Xt> Translation Table Base Register 1 (EL1) |
| D13.2.138 MRS <Xt>, TTBR1\_EL12 Translation Table Base Register 1 (EL1) |
| D13.2.138 MSR TTBR1\_EL12, <Xt> Translation Table Base Register 1 (EL1) |
| D13.2.139 MRS <Xt>, TTBR1\_EL2 Translation Table Base Register 1 (EL2) |
| D13.2.139 MSR TTBR1\_EL2, <Xt> Translation Table Base Register 1 (EL2) |
| D13.2.140 MRS <Xt>, VBAR\_EL1 Vector Base Address Register (EL1) |
| D13.2.140 MSR VBAR\_EL1, <Xt> Vector Base Address Register (EL1) |
| D13.2.140 MRS <Xt>, VBAR\_EL12 Vector Base Address Register (EL1) |
| D13.2.140 MSR VBAR\_EL12, <Xt> Vector Base Address Register (EL1) |
| D13.2.141 MRS <Xt>, VBAR\_EL2 Vector Base Address Register (EL2) |
| D13.2.141 MSR VBAR\_EL2, <Xt> Vector Base Address Register (EL2) |
| D13.2.143 MRS <Xt>, VMPIDR\_EL2 Virtualization Multiprocessor ID Register |
| D13.2.143 MSR VMPIDR\_EL2, <Xt> Virtualization Multiprocessor ID Register |
| D13.2.144 MRS <Xt>, VNCR\_EL2 Virtual Nested Control Register |
| D13.2.144 MSR VNCR\_EL2, <Xt> Virtual Nested Control Register |
| D13.2.145 MRS <Xt>, VPIDR\_EL2 Virtualization Processor ID Register |
| D13.2.145 MSR VPIDR\_EL2, <Xt> Virtualization Processor ID Register |
| D13.2.146 MRS <Xt>, VSTCR\_EL2 Virtualization Secure Translation Control Register |
| D13.2.146 MSR VSTCR\_EL2, <Xt> Virtualization Secure Translation Control Register |
| D13.2.147 MRS <Xt>, VSTTBR\_EL2 Virtualization Secure Translation Table Base Register |
| D13.2.147 MSR VSTTBR\_EL2, <Xt> Virtualization Secure Translation Table Base Register |
| D13.2.148 MRS <Xt>, VTCR\_EL2 Virtualization Translation Control Register |
| D13.2.148 MSR VTCR\_EL2, <Xt> Virtualization Translation Control Register |
| D13.2.149 MRS <Xt>, VTTBR\_EL2 Virtualization Translation Table Base Register |
| D13.2.149 MSR VTTBR\_EL2, <Xt> Virtualization Translation Table Base Register |
| D13.3.1 MRS <Xt>, DBGAUTHSTATUS\_EL1 Debug Authentication Status register |
| D13.3.2 MRS <Xt>, DBGBCR<n>\_EL1 Debug Breakpoint Control Registers, n = 0 - 15 |
| D13.3.2 MSR DBGBCR<n>\_EL1, <Xt> Debug Breakpoint Control Registers, n = 0 - 15 |
| D13.3.3 MRS <Xt>, DBGBVR<n>\_EL1 Debug Breakpoint Value Registers, n = 0 - 15 |
| D13.3.3 MSR DBGBVR<n>\_EL1, <Xt> Debug Breakpoint Value Registers, n = 0 - 15 |
| D13.3.4 MRS <Xt>, DBGCLAIMCLR\_EL1 Debug CLAIM Tag Clear register |
| D13.3.4 MSR DBGCLAIMCLR\_EL1, <Xt> Debug CLAIM Tag Clear register |
| D13.3.5 MRS <Xt>, DBGCLAIMSET\_EL1 Debug CLAIM Tag Set register |
| D13.3.5 MSR DBGCLAIMSET\_EL1, <Xt> Debug CLAIM Tag Set register |
| D13.3.9 MRS <Xt>, DBGPRCR\_EL1 Debug Power Control Register |
| D13.3.9 MSR DBGPRCR\_EL1, <Xt> Debug Power Control Register |
| D13.3.10 MRS <Xt>, DBGVCR32\_EL2 Debug Vector Catch Register |
| D13.3.10 MSR DBGVCR32\_EL2, <Xt> Debug Vector Catch Register |
| D13.3.11 MRS <Xt>, DBGWCR<n>\_EL1 Debug Watchpoint Control Registers, n = 0 - 15 |
| D13.3.11 MSR DBGWCR<n>\_EL1, <Xt> Debug Watchpoint Control Registers, n = 0 - 15 |
| D13.3.12 MRS <Xt>, DBGWVR<n>\_EL1 Debug Watchpoint Value Registers, n = 0 - 15 |
| D13.3.12 MSR DBGWVR<n>\_EL1, <Xt> Debug Watchpoint Value Registers, n = 0 - 15 |
| D13.3.15 MRS <Xt>, MDCCINT\_EL1 Monitor DCC Interrupt Enable Register |
| D13.3.15 MSR MDCCINT\_EL1, <Xt> Monitor DCC Interrupt Enable Register |
| D13.3.17 MRS <Xt>, MDCR\_EL2 Monitor Debug Configuration Register (EL2) |
| D13.3.17 MSR MDCR\_EL2, <Xt> Monitor Debug Configuration Register (EL2) |
| D13.3.19 MRS <Xt>, MDRAR\_EL1 Monitor Debug ROM Address Register |
| D13.3.20 MRS <Xt>, MDSCR\_EL1 Monitor Debug System Control Register |
| D13.3.20 MSR MDSCR\_EL1, <Xt> Monitor Debug System Control Register |
| D13.3.21 MRS <Xt>, OSDLR\_EL1 OS Double Lock Register |
| D13.3.21 MSR OSDLR\_EL1, <Xt> OS Double Lock Register |
| D13.3.22 MRS <Xt>, OSDTRRX\_EL1 OS Lock Data Transfer Register, Receive |
| D13.3.22 MSR OSDTRRX\_EL1, <Xt> OS Lock Data Transfer Register, Receive |
| D13.3.23 MRS <Xt>, OSDTRTX\_EL1 OS Lock Data Transfer Register, Transmit |
| D13.3.23 MSR OSDTRTX\_EL1, <Xt> OS Lock Data Transfer Register, Transmit |
| D13.3.24 MRS <Xt>, OSECCR\_EL1 OS Lock Exception Catch Control Register |
| D13.3.24 MSR OSECCR\_EL1, <Xt> OS Lock Exception Catch Control Register |
| D13.3.25 MSR OSLAR\_EL1, <Xt> OS Lock Access Register |
| D13.3.26 MRS <Xt>, OSLSR\_EL1 OS Lock Status Register |
| D13.3.27 MRS <Xt>, SDER32\_EL2 AArch32 Secure Debug Enable Register |
| D13.3.27 MSR SDER32\_EL2, <Xt> AArch32 Secure Debug Enable Register |
| D13.3.29 MRS <Xt>, TRFCR\_EL1 Trace Filter Control Register (EL1) |
| D13.3.29 MSR TRFCR\_EL1, <Xt> Trace Filter Control Register (EL1) |
| D13.3.29 MRS <Xt>, TRFCR\_EL12 Trace Filter Control Register (EL1) |
| D13.3.29 MSR TRFCR\_EL12, <Xt> Trace Filter Control Register (EL1) |
| D13.3.30 MRS <Xt>, TRFCR\_EL2 Trace Filter Control Register (EL2) |
| D13.3.30 MSR TRFCR\_EL2, <Xt> Trace Filter Control Register (EL2) |
| D13.4.10 MRS <Xt>, PMINTENCLR\_EL1 Performance M onitors Interrupt Enable Clear register |
| D13.4.10 MSR PMINTENCLR\_EL1, <Xt> Performance M onitors Interrupt Enable Clear register |
| D13.4.11 MRS <Xt>, PMINTENSET\_EL1 Performance Monitors Interrupt Enable Set register |
| D13.4.11 MSR PMINTENSET\_EL1, <Xt> Performance Monitors Interrupt Enable Set register |
| D13.4.12 MRS <Xt>, PMMIR\_EL1 Performance Monitors Machine Identification Register |
| D13.4.17 MSR PMUSERENR\_EL0, <Xt> Performance Monitors User Enable Register |
| D13.5.11 MRS <Xt>, AMEVCNTVOFF0<n>\_EL2 Activity Monitors Event Counter Virtual Offset Registers 0, n = 0 - 15 |
| D13.5.11 MSR AMEVCNTVOFF0<n>\_EL2, <Xt> Activity Monitors Event Counter Virtual Offset Registers 0, n = 0 - 15 |
| D13.5.12 MRS <Xt>, AMEVCNTVOFF1<n>\_EL2 Activity Monitors Event Counter Virtual Offset Registers 1, n = 0 - 15 |
| D13.5.12 MSR AMEVCNTVOFF1<n>\_EL2, <Xt> Activity Monitors Event Counter Virtual Offset Registers 1, n = 0 - 15 |
| D13.5.15 MSR AMUSERENR\_EL0, <Xt> Activity Monitors User Enable Register |
| D13.6.1 MRS <Xt>, PMBIDR\_EL1 Profiling Buffer ID Register |
| D13.6.2 MRS <Xt>, PMBLIMITR\_EL1 Profiling Buffer Limit Address Register |
| D13.6.2 MSR PMBLIMITR\_EL1, <Xt> Profiling Buffer Limit Address Register |
| D13.6.3 MRS <Xt>, PMBPTR\_EL1 Profiling Buffer Write Pointer Register |
| D13.6.3 MSR PMBPTR\_EL1, <Xt> Profiling Buffer Write Pointer Register |
| D13.6.4 MRS <Xt>, PMBSR\_EL1 Profiling Buffer Status/syndrome Register |
| D13.6.4 MSR PMBSR\_EL1, <Xt> Profiling Buffer Status/syndrome Register |
| D13.6.5 MRS <Xt>, PMSCR\_EL1 Statistical Profiling Control Register (EL1) |
| D13.6.5 MSR PMSCR\_EL1, <Xt> Statistical Profiling Control Register (EL1) |
| D13.6.5 MRS <Xt>, PMSCR\_EL12 Statistical Profiling Control Register (EL1) |
| D13.6.5 MSR PMSCR\_EL12, <Xt> Statistical Profiling Control Register (EL1) |
| D13.6.6 MRS <Xt>, PMSCR\_EL2 Statistical Profiling Control Register (EL2) |
| D13.6.6 MSR PMSCR\_EL2, <Xt> Statistical Profiling Control Register (EL2) |
| D13.6.7 MRS <Xt>, PMSEVFR\_EL1 Sampling Event Filter Register |
| D13.6.7 MSR PMSEVFR\_EL1, <Xt> Sampling Event Filter Register |
| D13.6.8 MRS <Xt>, PMSFCR\_EL1 Sampling Filter Control Register |
| D13.6.8 MSR PMSFCR\_EL1, <Xt> Sampling Filter Control Register |
| D13.6.9 MRS <Xt>, PMSICR\_EL1 Sampling Interval Counter Register |
| D13.6.9 MSR PMSICR\_EL1, <Xt> Sampling Interval Counter Register |
| D13.6.10 MRS <Xt>, PMSIDR\_EL1 Sampling Profiling ID Register |
| D13.6.11 MRS <Xt>, PMSIRR\_EL1 Sampling Interval Reload Register |
| D13.6.11 MSR PMSIRR\_EL1, <Xt> Sampling Interval Reload Register |
| D13.6.12 MRS <Xt>, PMSLATFR\_EL1 Sampling Latency Filter Register |
| D13.6.12 MSR PMSLATFR\_EL1, <Xt> Sampling Latency Filter Register |
| D13.6.13 MRS <Xt>, PMSNEVFR\_EL1 Sampling Inverted Event Filter Register |
| D13.6.13 MSR PMSNEVFR\_EL1, <Xt> Sampling Inverted Event Filter Register |
| D13.7.1 MRS <Xt>, DISR\_EL1 Deferred Interrupt Status Register |
| D13.7.1 MSR DISR\_EL1, <Xt> Deferred Interrupt Status Register |
| D13.7.2 MRS <Xt>, ERRIDR\_EL1 Error Record ID Register |
| D13.7.3 MRS <Xt>, ERRSELR\_EL1 Error Record Select Register |
| D13.7.3 MSR ERRSELR\_EL1, <Xt> Error Record Select Register |
| D13.7.4 MRS <Xt>, ERXADDR\_EL1 Selected Error Record Address Register |
| D13.7.4 MSR ERXADDR\_EL1, <Xt> Selected Error Record Address Register |
| D13.7.5 MRS <Xt>, ERXCTLR\_EL1 Selected Error Record Control Register |
| D13.7.5 MSR ERXCTLR\_EL1, <Xt> Selected Error Record Control Register |
| D13.7.6 MRS <Xt>, ERXFR\_EL1 Selected Error Record Feature Register |
| D13.7.7 MRS <Xt>, ERXMISC0\_EL1 Selected Error Record Miscellaneous Register 0 |
| D13.7.7 MSR ERXMISC0\_EL1, <Xt> Selected Error Record Miscellaneous Register 0 |
| D13.7.8 MRS <Xt>, ERXMISC1\_EL1 Selected Error Record Miscellaneous Register 1 |
| D13.7.8 MSR ERXMISC1\_EL1, <Xt> Selected Error Record Miscellaneous Register 1 |
| D13.7.9 MRS <Xt>, ERXMISC2\_EL1 Selected Error Record Miscellaneous Register 2 |
| D13.7.9 MSR ERXMISC2\_EL1, <Xt> Selected Error Record Miscellaneous Register 2 |
| D13.7.10 MRS <Xt>, ERXMISC3\_EL1 Selected Error Record Miscellaneous Register 3 |
| D13.7.10 MSR ERXMISC3\_EL1, <Xt> Selected Error Record Miscellaneous Register 3 |
| D13.7.11 MRS <Xt>, ERXPFGCDN\_EL1 Selected Pseudo-fault Generation Countdown register |
| D13.7.11 MSR ERXPFGCDN\_EL1, <Xt> Selected Pseudo-fault Generation Countdown register |
| D13.7.12 MRS <Xt>, ERXPFGCTL\_EL1 Selected Pseudo-fault Generation Control register |
| D13.7.12 MSR ERXPFGCTL\_EL1, <Xt> Selected Pseudo-fault Generation Control register |
| D13.7.13 MRS <Xt>, ERXPFGF\_EL1 Selected Pseudo-fault Generation Feature register |
| D13.7.14 MRS <Xt>, ERXSTATUS\_EL1 Selected Error Record Primary Status Register |
| D13.7.14 MSR ERXSTATUS\_EL1, <Xt> Selected Error Record Primary Status Register |
| D13.7.15 MRS <Xt>, VDISR\_EL2 Virtual Deferred Interrupt Status Register |
| D13.7.15 MSR VDISR\_EL2, <Xt> Virtual Deferred Interrupt Status Register |
| D13.7.16 MRS <Xt>, VSESR\_EL2 Virtual SError Exception Syndrome Register |
| D13.7.16 MSR VSESR\_EL2, <Xt> Virtual SError Exception Syndrome Register |
| D13.8.1 MSR CNTFRQ\_EL0,,<Xt> Counter-timer Frequency register |
| D13.8.2 MRS <Xt>, CNTHCTL\_EL2 Counter-timer Hypervisor Control register |
| D13.8.2 MSR CNTHCTL\_EL2, <Xt> Counter-timer Hypervisor Control register |
| D13.8.3 MRS <Xt>, CNTHP\_CTL\_EL2 Counter-timer Hypervisor Physical Timer Control register |
| D13.8.3 MSR CNTHP\_CTL\_EL2, <Xt> Counter-timer Hypervisor Physical Timer Control register |
| D13.8.4 MRS <Xt>, CNTHP\_CVAL\_EL2 Counter-timer Physical Timer CompareValue register (EL2) |
| D13.8.4 MSR CNTHP\_CVAL\_EL2, <Xt> Counter-timer Physical Timer CompareValue register (EL2) |
| D13.8.5 MRS <Xt>, CNTHP\_TVAL\_EL2 Counter-timer Ph ysical Timer TimerValue register (EL2) |
| D13.8.5 MSR CNTHP\_TVAL\_EL2, <Xt> Counter-timer Ph ysical Timer TimerValue register (EL2) |
| D13.8.6 MRS <Xt>, CNTHPS\_CTL\_EL2 Counter-timer Secure Physical Timer Control register (EL2) |
| D13.8.6 MSR CNTHPS\_CTL\_EL2, <Xt> Counter-timer Secure Physical Timer Control register (EL2) |
| D13.8.7 MRS <Xt>, CNTHPS\_CVAL\_EL2 Counter-timer Secure Physical Timer CompareValue register (EL2) |
| D13.8.7 MSR CNTHPS\_CVAL\_EL2, <Xt> Counter-timer Secure Physical Timer CompareValue register (EL2) |
| D13.8.8 MRS <Xt>, CNTHPS\_TVAL\_EL2 Counter-timer Secure Physical Timer TimerValue register (EL2) |
| D13.8.8 MSR CNTHPS\_TVAL\_EL2, <Xt> Counter-timer Secure Physical Timer TimerValue register (EL2) |
| D13.8.9 MRS <Xt>, CNTHV\_CTL\_EL2 Counter-timer Virtual Timer Control register (EL2) |
| D13.8.9 MSR CNTHV\_CTL\_EL2, <Xt> Counter-timer Virtual Timer Control register (EL2) |
| D13.8.10 MRS <Xt>, CNTHV\_CVAL\_EL2 Counter-timer Vi rtual Timer CompareValue register (EL2) |
| D13.8.10 MSR CNTHV\_CVAL\_EL2, <Xt> Counter-timer Vi rtual Timer CompareValue register (EL2) |
| D13.8.11 MRS <Xt>, CNTHV\_TVAL\_EL2 Counter-timer Virtual Timer TimerValue Register (EL2) |
| D13.8.11 MSR CNTHV\_TVAL\_EL2, <Xt> Counter-timer Virtual Timer TimerValue Register (EL2) |
| D13.8.12 MRS <Xt>, CNTHVS\_CTL\_EL2 Counter-timer Secure Virtual Timer Control register (EL2) |
| D13.8.12 MSR CNTHVS\_CTL\_EL2, <Xt> Counter-timer Secure Virtual Timer Control register (EL2) |
| D13.8.13 MRS <Xt>, CNTHVS\_CVAL\_EL2 Counter-timer Secure Virtual Timer CompareValue register (EL2) |
| D13.8.13 MSR CNTHVS\_CVAL\_EL2, <Xt> Counter-timer Secure Virtual Timer CompareValue register (EL2) |
| D13.8.14 MRS <Xt>, CNTHVS\_TVAL\_EL2 Counter-timer Secu re Virtual Timer TimerValue register (EL2) |
| D13.8.14 MSR CNTHVS\_TVAL\_EL2, <Xt> Counter-timer Secu re Virtual Timer TimerValue register (EL2) |
| D13.8.15 MRS <Xt>, CNTKCTL\_EL1 Counter-timer Kernel Control register |
| D13.8.15 MSR CNTKCTL\_EL1, <Xt> Counter-timer Kernel Control register |
| D13.8.15 MRS <Xt>, CNTKCTL\_EL12 Counter-timer Kernel Control register |
| D13.8.15 MSR CNTKCTL\_EL12, <Xt> Counter-timer Kernel Control register |
| D13.8.16 MRS <Xt>, CNTP\_CTL\_EL02 Counter-timer Physical Timer Control register |
| D13.8.16 MSR CNTP\_CTL\_EL02, <Xt> Counter-timer Physical Timer Control register |
| D13.8.17 MRS <Xt>, CNTP\_CVAL\_EL02 Counter-timer Physical Timer CompareValue register |
| D13.8.17 MSR CNTP\_CVAL\_EL02, <Xt> Counter-timer Physical Timer CompareValue register |
| D13.8.18 MRS <Xt>, CNTP\_TVAL\_EL02 Counter-timer Physical Timer TimerValue register |
| D13.8.18 MSR CNTP\_TVAL\_EL02, <Xt> Counter-timer Physical Timer TimerValue register |
| D13.8.22 MRS <Xt>, CNTPOFF\_EL2 Counter-timer Physical Offset register |
| D13.8.22 MSR CNTPOFF\_EL2, <Xt> Counter-timer Physical Offset register |
| D13.8.25 MRS <Xt>, CNTV\_CTL\_EL02 Counter-timer Virtual Timer Control register |
| D13.8.25 MSR CNTV\_CTL\_EL02, <Xt> Counter-timer Virtual Timer Control register |
| D13.8.26 MRS <Xt>, CNTV\_CVAL\_EL02 Counter-timer Virtual Timer CompareValue register |
| D13.8.26 MSR CNTV\_CVAL\_EL02, <Xt> Counter-timer Virtual Timer CompareValue register |
| D13.8.27 MRS <Xt>, CNTV\_TVAL\_EL02 Counter-timer Virtual Timer TimerValue register |
| D13.8.27 MSR CNTV\_TVAL\_EL02, <Xt> Counter-timer Virtual Timer TimerValue register |
| D13.8.30 MRS <Xt>, CNTVOFF\_EL2 Counter-timer Virtual Offset register |
| D13.8.30 MSR CNTVOFF\_EL2, <Xt> Counter-timer Virtual Offset register |

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| 有条件敏感指令-配置 |
| C5.2.7 MRS <Xt>,FPCR, Floating-point Control Register |
| C5.2.7 MSR FPCR,<Xt> Floating-point Control Register |
| C5.2.8 MRS <Xt>,FPSR, Floating-point Status Register |
| C5.2.8 MSR FPSR,<Xt> Floating-point Status Register |
| C5.3.2 DC CGDVAC, Clean of Data and Allocation Tags by VA to PoC |
| C5.3.3 DC CGDVADP, Clean of Data and Allocation Tags by VA to PoDP |
| C5.3.4 DC CGDVAP, Clean of Data and Allocation Tags by VA to PoP |
| C5.3.6 DC CGVAC, Clean of Allocation Tags by VA to PoC |
| C5.3.7 DC CGVADP, Clean of Allocation Tags by VA to PoDP |
| C5.3.8 DC CGVAP, Clean of Allocation Tags by VA to PoP |
| C5.3.10 DC CIGDVAC, Clean and Invalidate of Data and Allocation Tags by VA to PoC |
| C5.3.12 DC CIGVAC, Clean and Invalidate of Allocation Tags by VA to PoC |
| C5.3.14 DC CIVAC, Data or unified Cache line Clean and Invalidate by VA to PoC |
| C5.3.16 DC CVAC, Data or unified Cache line Clean by VA to PoC |
| C5.3.17 DC CVADP, Data or unified Cache line Clean by VA to PoDP |
| C5.3.18 DC CVAP, Data or unified Cache line Clean by VA to PoP |
| C5.3.19 DC CVAU, Data or unified Cache line Clean by VA to PoU |
| C5.3.20 DC GVA, Data Cache set Allocation Tag by VA |
| C5.3.21 DC GZVA, Data Cache set Allocation Tags and Zero by VA |
| C5.3.28 DC ZVA, Data Cache Zero by VA |
| C5.3.31 IC IVAU, Instruction Cache line Invalidate by VA to PoU |
| D13.2.36 MRS <Xt>,DCZID\_EL0, Data Cache Zero ID register |
| D13.2.109 MRS <Xt>, RNDR, Random Number |
| D13.2.110 MRS <Xt>, RNDRRS, Reseeded Random Number |
| D13.2.130 MRS <Xt>,TPIDR\_EL0, EL0 Read/Write Software Thread ID Register |
| D13.2.130 MSR TPIDR\_EL0,<Xt> EL0 Read/Write Software Thread ID Register |
| D13.2.134 MRS <Xt>,TPIDRRO\_EL0, EL0 Read-Only Software Thread ID Register |
| D13.4.1 MRS <Xt>,PMCCFILTR\_EL0, Performance Monitors Cycle Count Filter Register |
| D13.4.1 MSR PMCCFILTR\_EL0,<Xt> Performance M onitors Cycle Count Filter Register |
| D13.4.2 MRS <Xt>,PMCCNTR\_EL0, Performance Monitors Cycle Count Register |
| D13.4.2 MSR PMCCNTR\_EL0,<Xt> Performance Monitors Cycle Count Register |
| D13.4.3 MRS <Xt>,PMCEID0\_EL0, Performance Monitors Common Event Identification register 0 |
| D13.4.4 MRS <Xt>,PMCEID1\_EL0, Performance Monitors Common Event Identification register 1 |
| D13.4.5 MRS <Xt>,PMCNTENCLR\_EL0, Performance Monitors Count Enable Clear register |
| D13.4.5 MSR PMCNTENCLR\_EL0,<Xt> Performance Monitors Count Enable Clear register |
| D13.4.6 MRS <Xt>,PMCNTENSET\_EL0, Performance Monitors Count Enable Set register |
| D13.4.6 MSR PMCNTENSET\_EL0,<Xt> Performance Monitors Count Enable Set register |
| D13.4.7 MRS <Xt>,PMCR\_EL0, Performance Monitors Control Register |
| D13.4.7 MSR PMCR\_EL0,<Xt> Performance Monitors Control Register |
| D13.4.8 MRS <Xt>,PMEVCNTR<n>\_EL0, n = 0 - 30 |
| D13.4.8 MSR PMEVCNTR<n>\_EL0,<Xt> n = 0 - 30 |
| D13.4.9 MRS <Xt>,PMEVTYPER<n>\_EL0, n = 0 - 30 |
| D13.4.9 MSR PMEVTYPER<n>\_EL0,<Xt> n = 0 - 30 |
| D13.4.13 MRS <Xt>,PMOVSCLR\_EL0, Performance Monito rs Overflow Flag Status Clear Register |
| D13.4.13 MSR PMOVSCLR\_EL0,<Xt> Performance Monito rs Overflow Flag Status Clear Register |
| D13.4.14 MRS <Xt>,PMOVSSET\_EL0, Performance Monitors Overflow Flag Status Set register |
| D13.4.14 MSR PMOVSSET\_EL0,<Xt> Performance Monitors Overflow Flag Status Set register |
| D13.4.15 MRS <Xt>,PMSELR\_EL0, Performance Monitors Event Counter Selection Register |
| D13.4.15 MSR PMSELR\_EL0,<Xt> Performance Monitors Event Counter Selection Register |
| D13.4.16 MSR PMSWINC\_EL0,<Xt> Performance Monitors Software Increment register |
| D13.4.17 MRS <Xt>,PMUSERENR\_EL0, Performance Monitors User Enable Register |
| D13.4.18 MRS <Xt>,PMXEVCNTR\_EL0, Performance M onitors Selected Event Count Register |
| D13.4.18 MSR PMXEVCNTR\_EL0,<Xt> Performance M onitors Selected Event Count Register |
| D13.4.19 MRS <Xt>,PMXEVTYPER\_EL0, Performance Mo nitors Selected Event Type Register |
| D13.4.19 MSR PMXEVTYPER\_EL0,<Xt> Performance Mo nitors Selected Event Type Register |
| D13.5.1 MRS <Xt>,AMCFGR\_EL0, Activity Monitors Configuration Register |
| D13.5.2 MRS <Xt>,AMCG1IDR\_EL0, Activity Monitors Counter Group 1 Identification Register |
| D13.5.3 MRS <Xt>,AMCGCR\_EL0, Activity Monitors Counter Group Configuration Register |
| D13.5.4 MRS <Xt>,AMCNTENCLR0\_EL0, Activity Moni tors Count Enable Clear Register 0 |
| D13.5.4 MSR AMCNTENCLR0\_EL0,<Xt> Activity Monitors Count Enable Clear Register 0 |
| D13.5.5 MRS <Xt>,AMCNTENCLR1\_EL0, Activity Moni tors Count Enable Clear Register 1 |
| D13.5.5 MSR AMCNTENCLR1\_EL0,<Xt> Activity Moni tors Count Enable Clear Register 1 |
| D13.5.6 MRS <Xt>,AMCNTENSET0\_EL0, Activity Monitors Count Enable Set Register 0 |
| D13.5.6 MSR AMCNTENSET0\_EL0,<Xt> Activity Monitors Count Enable Set Register 0 |
| D13.5.7 MRS <Xt>,AMCNTENSET1\_EL0, Activity Monitors Count Enable Set Register 1 |
| D13.5.7 MSR AMCNTENSET1\_EL0,<Xt> Activity Monitors Count Enable Set Register 1 |
| D13.5.8 MRS <Xt>,AMCR\_EL0, Activity Monitors Control Register |
| D13.5.8 MSR AMCR\_EL0,<Xt> Activity Monitors Control Register |
| D13.5.9 MRS <Xt>,AMEVCNTR0<n>\_EL0, n = 0 - 3 |
| D13.5.9 MSR AMEVCNTR0<n>\_EL0,<Xt> n = 0 - 3 |
| D13.5.10 MRS <Xt>,AMEVCNTR1<n>\_EL0, n = 0 - 15 |
| D13.5.10 MSR AMEVCNTR1<n>\_EL0,<Xt> n = 0 - 15 |
| D13.5.13 MRS <Xt>,AMEVTYPER0<n>\_EL0, n = 0 - 3 |
| D13.5.14 MRS <Xt>,AMEVTYPER1<n>\_EL0, n = 0 - 15 |
| D13.5.14 MSR AMEVTYPER1<n>\_EL0,<Xt> n = 0 - 15 |
| D13.5.15 MRS <Xt>,AMUSERENR\_EL0, Activity Monitors User Enable Register |
| D13.8.1 MRS <Xt>,CNTFRQ\_EL0, Counter-timer Frequency register |
| D13.8.28 MRS <Xt>,CNTVCTSS\_EL0, Counter-timer Self-Synchronized Virtual Count register |
| D13.8.29 MRS <Xt>,CNTVCT\_EL0, Counter-timer Virtual Count register |
| C6.2.6 ADDG |
| C6.2.40 CASB, CASAB, CASALB, CASLB |
| C6.2.41 CASH, CASAH, CASALH, CASLH |
| C6.2.42 CASP, CASPA, CASPAL, CASPL |
| C6.2.43 CAS, CASA, CASAL, CASL |
| C6.2.76 DCPS1 |
| C6.2.77 DCPS2 |
| C6.2.78 DCPS3 |
| C6.2.79 DGH |
| C6.2.81 DRPS |
| C6.2.96   IRG |
| C6.2.98   LD64B |
| C6.2.99 LDADDB, LDADDAB, LDADDALB, LDADDLB |
| C6.2.100 LDADDH, LDADDAH, LDADDALH, LDADDLH |
| C6.2.101 LDADD, LDADDA, LDADDAL, LDADDL |
| C6.2.102 LDAPR |
| C6.2.103 LDAPRB |
| C6.2.104 LDAPRH |
| C6.2.105 LDAPUR |
| C6.2.106 LDAPURB |
| C6.2.107 LDAPURH |
| C6.2.108 LDAPURSB |
| C6.2.109 LDAPURSH |
| C6.2.110 LDAPURSW |
| C6.2.111 LDAR |
| C6.2.112 LDARB |
| C6.2.113 LDARH |
| C6.2.114 LDAXP |
| C6.2.115 LDAXR |
| C6.2.116 LDAXRB |
| C6.2.117 LDAXRH |
| C6.2.118 LDCLRB, LDCLRAB, LDCLRALB, LDCLRLB |
| C6.2.119 LDCLRH, LDCLRAH, LDCLRALH, LDCLRLH |
| C6.2.120 LDCLR, LDCLRA, LDCLRAL, LDCLRL |
| C6.2.121 LDEORB, LDEORAB, LDEORALB, LDEORLB |
| C6.2.122 LDEORH, LDEORAH, LDEORALH, LDEORLH |
| C6.2.123 LDEOR, LDEORA, LDEORAL, LDEORL |
| C6.2.124 LDG |
| C6.2.125 LDGM |
| C6.2.126 LDLARB |
| C6.2.127 LDLARH |
| C6.2.128 LDLAR |
| C6.2.129 LDNP |
| C6.2.130 LDP |
| C6.2.131 LDPSW |
| C6.2.132 LDR (immediate) |
| C6.2.134 LDR (register) |
| C6.2.135 LDRAA, LDRAB |
| C6.2.136 LDRB (immediate) |
| C6.2.137 LDRB (register) |
| C6.2.138 LDRH (immediate) |
| C6.2.139 LDRH (register) |
| C6.2.140 LDRSB (immediate) |
| C6.2.141 LDRSB (register) |
| C6.2.142 LDRSH (immediate) |
| C6.2.143 LDRSH (register) |
| C6.2.144 LDRSW (immediate) |
| C6.2.145 LDRSW (literal) |
| C6.2.146 LDRSW (register) |
| C6.2.147 LDSETB, LDSETAB, LDSETALB, LDSETLB |
| C6.2.148 LDSETH, LDSETAH, LDSETALH, LDSETLH |
| C6.2.149 LDSET, LDSETA, LDSETAL, LDSETL |
| C6.2.150 LDSMAXB, LDSMAXAB, LDSMAXALB, LDSMAXLB |
| C6.2.151 LDSMAXH, LDSMAXAH, LDSMAXALH, LDSMAXLH |
| C6.2.152 LDSMAX, LDSMAXA, LDSMAXAL, LDSMAXL |
| C6.2.153 LDSMINB, LDSMINAB, LDSMINALB, LDSMINLB |
| C6.2.154 LDSMINH, LDSMINAH, LDSMINALH, LDSMINLH |
| C6.2.155 LDSMIN, LDSMINA, LDSMINAL, LDSMINL |
| C6.2.156 LDTR |
| C6.2.157 LDTRB |
| C6.2.158 LDTRH |
| C6.2.159 LDTRSB |
| C6.2.160 LDTRSH |
| C6.2.161 LDTRSW |
| C6.2.162 LDUMAXB, LDUMAXAB, LDUMAXALB, LDUMAXLB |
| C6.2.163 LDUMAXH, LDUMAXAH, LDUMAXALH, LDUMAXLH |
| C6.2.164 LDUMAX, LDUMAXA, LDUMAXAL, LDUMAXL |
| C6.2.165 LDUMINB, LDUMINAB, LDUMINALB, LDUMINLB |
| C6.2.166 LDUMINH, LDUMINAH, LDUMINALH, LDUMINLH |
| C6.2.167 LDUMIN, LDUMINA, LDUMINAL, LDUMINL |
| C6.2.168 LDUR |
| C6.2.169 LDURB |
| C6.2.170 LDURH |
| C6.2.171 LDURSB |
| C6.2.172 LDURSH |
| C6.2.173 LDURSW |
| C6.2.174 LDXP |
| C6.2.175 LDXR |
| C6.2.176 LDXRB |
| C6.2.177 LDXRH |
| C6.2.217 PSB CSYNC |
| C6.2.247 ST2G |
| C6.2.248 ST64B |
| C6.2.249 ST64BV |
| C6.2.250 ST64BV0 |
| C6.2.251 STADDB, STADDLB |
| C6.2.252 STADDH, STADDLH |
| C6.2.253 STADD, STADDL |
| C6.2.254 STCLRB, STCLRLB |
| C6.2.255 STCLRH, STCLRLH |
| C6.2.256 STCLR, STCLRL |
| C6.2.257 STEORB, STEORLB |
| C6.2.258 STEORH, STEORLH |
| C6.2.259 STEOR, STEORL |
| C6.2.260 STG |
| C6.2.261 STGM |
| C6.2.262 STGP |
| C6.2.263 STLLRB |
| C6.2.264 STLLRH |
| C6.2.265 STLLR |
| C6.2.266 STLR |
| C6.2.267 STLRB |
| C6.2.268 STLRH |
| C6.2.269 STLUR |
| C6.2.270 STLURB |
| C6.2.271 STLURH |
| C6.2.272 STLXP |
| C6.2.273 STLXR |
| C6.2.274 STLXRB |
| C6.2.275 STLXRH |
| C6.2.276 STNP |
| C6.2.277 STP |
| C6.2.278 STR (immediate) |
| C6.2.279 STR (register) |
| C6.2.280 STRB (immediate) |
| C6.2.281 STRB (register) |
| C6.2.282 STRH (immediate) |
| C6.2.283 STRH (register) |
| C6.2.284 STSETB, STSETLB |
| C6.2.285 STSETH, STSETLH |
| C6.2.286 STSET, STSETL |
| C6.2.287 STSMAXB, STSMAXLB |
| C6.2.288 STSMAXH, STSMAXLH |
| C6.2.289 STSMAX, STSMAXL |
| C6.2.290 STSMINB, STSMINLB |
| C6.2.291 STSMINH, STSMINLH |
| C6.2.292 STSMIN, STSMINL |
| C6.2.293 STTR |
| C6.2.294 STTRB |
| C6.2.295 STTRH |
| C6.2.296 STUMAXB, STUMAXLB |
| C6.2.297 STUMAXH, STUMAXLH |
| C6.2.298 STUMAX, STUMAXL |
| C6.2.299 STUMINB, STUMINLB |
| C6.2.300 STUMINH, STUMINLH |
| C6.2.301 STUMIN, STUMINL |
| C6.2.302 STUR |
| C6.2.303 STURB |
| C6.2.304 STURH |
| C6.2.305 STXP |
| C6.2.306 STXR |
| C6.2.307 STXRB |
| C6.2.308 STXRH |
| C6.2.309 STZ2G |
| C6.2.310 STZG |
| C6.2.311 STZGM |
| C6.2.315 SUBG |
| C6.2.322 SWPB, SWPAB, SWPALB, SWPLB |
| C6.2.323 SWPH, SWPAH, SWPALH, SWPLH |
| C6.2.324 SWP, SWPA, SWPAL, SWPL |
| C6.2.333 TSB CSYNC |
| C6.2.348 WFE |
| C6.2.349 WFET |
| C6.2.350 WFIT |
| C7.2.177 LD1 (multiple structures) |
| C7.2.178 LD1 (single structure) |
| C7.2.179 LD1R |
| C7.2.180 LD2 (multiple structures) |
| C7.2.181 LD2 (single structure) |
| C7.2.182 LD2R |
| C7.2.183 LD3 (multiple structures) |
| C7.2.184 LD3 (single structure) |
| C7.2.185 LD3R |
| C7.2.186 LD4 (multiple structures) |
| C7.2.187 LD4 (single structure) |
| C7.2.188 LD4R |
| C7.2.189 LDNP (SIMD&FP) |
| C7.2.190 LDP (SIMD&FP) |
| C7.2.191 LDR (immediate, SIMD&FP) |
| C7.2.192 LDR (literal, SIMD&FP) |
| C7.2.193 LDR (register, SIMD&FP) |
| C7.2.194 LDUR (SIMD&FP) |
| C7.2.321 ST1 (multiple structures) |
| C7.2.322 ST1 (single structure) |
| C7.2.323 ST2 (multiple structures) |
| C7.2.324 ST2 (single structure) |
| C7.2.325 ST3 (multiple structures) |
| C7.2.326 ST3 (single structure) |
| C7.2.327 ST4 (multiple structures) |
| C7.2.328 ST4 (single structure) |
| C7.2.329 STNP (SIMD&FP) |
| C7.2.330 STP (SIMD&FP) |
| C7.2.331 STR (immediate, SIMD&FP) |
| C7.2.332 STR (register, SIMD&FP) |
| C7.2.333 STUR (SIMD&FP) |

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| 有条件敏感指令-配置&过滤 |
| C5.2.2 MRS <Xt>,DAIF, Interrupt Mask Bits |
| C5.2.2 MSR DAIF,<Xt> Interrupt Mask Bits |
| C5.6.1 CFP RCTX, Control Flow Prediction Restriction by Context |
| C5.6.2 CPP RCTX, Cache Prefetch Prediction Restriction by Context |
| C5.6.3 DVP RCTX, Data Value Prediction Restriction by Context |
| D13.2.11 MRS <Xt>,AIDR\_EL1, Auxiliary ID Register |
| D13.2.25 MRS <Xt>,CCSIDR2\_EL1, Current Cache Size ID Register 2 |
| D13.2.26 MRS <Xt>,CCSIDR\_EL1, Current Cache Size ID Register |
| D13.2.27 MRS <Xt>,CLIDR\_EL1, Cache Level ID Register |
| D13.2.45 MRS <Xt>,GMID\_EL1, Multiple tag transfer ID register |
| D13.2.69 MRS <Xt>,ID\_AFR0\_EL1, AArch32 Auxiliary Feature Register 0 |
| D13.2.70 MRS <Xt>,ID\_DFR0\_EL1, AArch32 Debug Feature Register 0 |
| D13.2.71 MRS <Xt>,ID\_DFR1\_EL1, Debug Feature Register 1 |
| D13.2.72 MRS <Xt>,ID\_ISAR0\_EL1, AArch32 Instruction Set Attribute Register 0 |
| D13.2.73 MRS <Xt>,ID\_ISAR1\_EL1, AArch32 Instruction Set Attribute Register 1 |
| D13.2.74 MRS <Xt>,ID\_ISAR2\_EL1, AArch32 Instruction Set Attribute Register 2 |
| D13.2.75 MRS <Xt>,ID\_ISAR3\_EL1, AArch32 Instruction Set Attribute Register 3 |
| D13.2.76 MRS <Xt>,ID\_ISAR4\_EL1, AArch32 Instruction Set Attribute Register 4 |
| D13.2.77 MRS <Xt>,ID\_ISAR5\_EL1, AArch32 Instruction Set Attribute Register 5 |
| D13.2.78 MRS <Xt>,ID\_ISAR6\_EL1, AArch32 Instruction Set Attribute Register 6 |
| D13.2.79 MRS <Xt>,ID\_MMFR0\_EL1, AArch32 Memory Model Feature Register 0 |
| D13.2.80 MRS <Xt>,ID\_MMFR1\_EL1, AArch32 Memory Model Feature Register 1 |
| D13.2.81 MRS <Xt>,ID\_MMFR2\_EL1, AArch32 Memory Model Feature Register 2 |
| D13.2.82 MRS <Xt>,ID\_MMFR3\_EL1, AArch32 Memory Model Feature Register 3 |
| D13.2.83 MRS <Xt>,ID\_MMFR4\_EL1, AArch32 Memory Model Feature Register 4 |
| D13.2.84 MRS <Xt>,ID\_MMFR5\_EL1, AArch32 Memory Model Feature Register 5 |
| D13.2.85 MRS <Xt>,ID\_PFR0\_EL1, AArch32 Processor Feature Register 0 |
| D13.2.86 MRS <Xt>,ID\_PFR1\_EL1, AArch32 Processor Feature Register 1 |
| D13.2.87 MRS <Xt>,ID\_PFR2\_EL1, AArch32 Processor Feature Register 2 |
| D13.2.100 MRS <Xt>,MVFR0\_EL1, AArch32 Media and VFP Feature Register 0 |
| D13.2.101 MRS <Xt>,MVFR1\_EL1, AArch32 Media and VFP Feature Register 1 |
| D13.2.102 MRS <Xt>,MVFR2\_EL1, AArch32 Media and VFP Feature Register 2 |
| D13.2.119 MRS <Xt>,SCXTNUM\_EL0, EL0 Read/Write Software Context Number |
| D13.2.119 MSR SCXTNUM\_EL0,<Xt> EL0 Read/Write Software Context Number |
| D13.3.6 MSR DBGDTR\_EL0,<Xt> half-duplex |
| D13.3.6 MRS <Xt>,DBGDTR\_EL0, half-duplex |
| D13.3.7 MRS <Xt>,DBGDTRRX\_EL0, Debug Data Transfer Register, Receive |
| D13.3.8 MSR DBGDTRTX\_EL0,<Xt> Debug Data Transfer Register, Transmit |
| D13.3.16 MRS <Xt>,MDCCSR\_EL0, Monitor DCC Status Register |
| D13.8.16 MRS <Xt>,CNTP\_CTL\_EL0, Counter-timer Physical Timer Control register |
| D13.8.16 MSR CNTP\_CTL\_EL0,<Xt> Counter-timer Physical Timer Control register |
| D13.8.17 MRS <Xt>,CNTP\_CVAL\_EL0, Counter-timer Physical Timer CompareValue register |
| D13.8.17 MSR CNTP\_CVAL\_EL0,<Xt> Counter-timer Physical Timer CompareValue register |
| D13.8.18 MRS <Xt>,CNTP\_TVAL\_EL0, Counter-timer Physical Timer TimerValue register |
| D13.8.18 MSR CNTP\_TVAL\_EL0,<Xt> Counter-timer Physical Timer TimerValue register |
| D13.8.19 MRS <Xt>,CNTPCTSS\_EL0, Counter-timer Self-Synchronized Physical Count register |
| D13.8.20 MRS <Xt>,CNTPCT\_EL0, Counter-timer Physical Count register |
| D13.8.25 MRS <Xt>,CNTV\_CTL\_EL0, Counter-timer Virtual Timer Control register |
| D13.8.25 MSR CNTV\_CTL\_EL0,<Xt> Counter-timer Virtual Timer Control register |
| D13.8.26 MRS <Xt>,CNTV\_CVAL\_EL0, Counter-timer Virtual Timer CompareValue register |
| D13.8.26 MSR CNTV\_CVAL\_EL0,<Xt> Counter-timer Virtual Timer CompareValue register |
| D13.8.27 MRS <Xt>,CNTV\_TVAL\_EL0, Counter-timer Virtual Timer TimerValue register |
| D13.8.27 MSR CNTV\_TVAL\_EL0,<Xt> Counter-timer Virtual Timer TimerValue register |

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| 有条件敏感指令-配置&下陷 |
| D13.2.34 MRS <Xt>,CTR\_EL0, Cache Type Register |
| D13.2.59 MRS <Xt>,ID\_AA64DFR0\_EL1, AArch64 Debug Feature Register 0 |
| D13.2.61 MRS <Xt>,ID\_AA64ISAR0\_EL1, AArch64 Instruction Set Attribute Register |
| D13.2.62 MRS <Xt>,ID\_AA64ISAR1\_EL1, AArch64 Instruction Set Attribute Register 1 |
| D13.2.64 MRS <Xt>,ID\_AA64MMFR0\_EL1, AArch64 Memory Model Feature Register 0 |
| D13.2.65 MRS <Xt>,ID\_AA64MMFR1\_EL1, AArch64 Memory Model Feature Register 1 |
| D13.2.66 MRS <Xt>,ID\_AA64MMFR2\_EL1, AArch64 Memory Model Feature Register 2 |
| D13.2.67 MRS <Xt>,ID\_AA64PFR0\_EL1, AArch64 Processor Feature Register 0 |
| D13.2.99 MRS <Xt>,MPIDR\_EL1, Multiprocessor Affinity Register |
| C6.2.350 WFI |
| D13.2.57 MRS <Xt>,ID\_AA64AFR0\_EL1, AArch64 Auxiliary Feature Register 0 |
| D13.2.58 MRS <Xt>,ID\_AA64AFR1\_EL1, AArch64 Auxiliary Feature Register 1 |
| D13.2.60 MRS <Xt>,ID\_AA64DFR1\_EL1, AArch64 Debug Feature Register 1 |
| D13.2.63 MRS <Xt>,ID\_AA64ISAR2\_EL1, AArch64 Instruction Set Attribute Register 2 |
| D13.2.68 MRS <Xt>,ID\_AA64PFR1\_EL1, AArch64 Processor Feature Register 1 |
| D13.2.98 MRS <Xt>,MIDR\_EL1, Main ID Register |
| D13.2.104 MRS <Xt>,REVIDR\_EL1, Revision ID Register |