**文档交付**

2.1 性能摸底报告：进行终端设备典型应用、典型使用场景运行时系统性能摸底（如抖音上下滑动、小视频播放，淘宝应用冷启动，首页滑动等系统调用开销、占比）

2.2 ARMv8-A指令手册梳理报告（lqj）

# ARMv8-A指令概述

ARMv8-A指令集是与ARMv8-A架构相配套的指令集，ARMv8-A架构包括两种运行环境：AArch64和AArch32。AArch64运行环境下，使用ARMv8-A64指令集，它与旧的32位指令集不同，它可以访问64位大小的内存指针，访问64位宽的寄存器并进行数据操作。AArch32运行环境下，使用A32或T32指令集，它们由原有的ARM指令集和Thumb指令集发展而来，与ARMv7架构兼容。

# 敏感指令定义

本项目根据指令的执行条件、执行语义、执行结果等信息将 A64 指令集划分为敏感指令和非敏感指令。本项目定义非敏感指令为用户态下和内核态下行为一致的指令，敏感指令为用户态下和内核态下行为可能不一致的指令。指令行为即指令对机器状态的修改，它取决于当前机器的系统配置和执行时上下文。

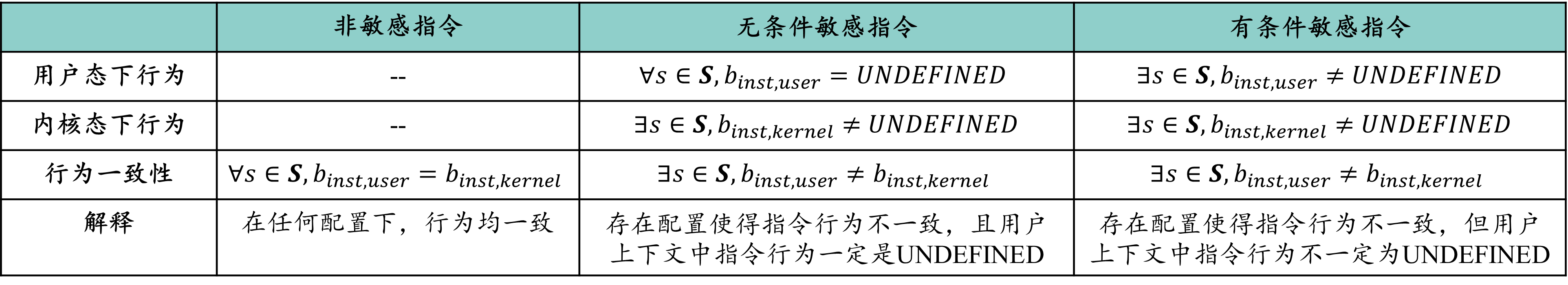
ARMv8-A64 指令集中，当处理器的系统配置变化时，指令的行为也会产生变化。

因此，本项目根据指令依赖的系统配置情况对敏感指令进行了划分，分为无条件（Unconditional）敏感指令和有条件（Conditional）敏感指令两大类。无条件敏感指令为任意系统配置下行为均不一致的指令，在 ARMv8-A64 指令集中该类指令全部为用户态下不可执行的特权指令，

它们在用户态下行为无定义（UNDEFINED），在内核态下有行为。有条件敏感指令为只有在部分系统配置下，用户态和内核态行为才不一致的指令。

综上所述，本项目将Armv8-A64指令集分为了非敏感指令、无条件敏感指令和有条件敏感指令三类，它们的形式化定义如下表所示，其中，S为所有可能的系统配置集合，

binst,user为指令在用户态下的行为，binst,kernel 为指令在内核态下的行为。



# 敏感指令分类和处理方法

对于不同敏感指令，本项目的指令截获模块将采取不同的处理方法，本节给出所有敏感指令的分类和对应的处理方法。

对于无条件敏感指令，本模块将直接阻止该类指令的执行，一旦指令扫描时发现程序中出现了该指令就报错。

对于有条件敏感指令，本项目直接将系统配置确定为M1(TODO)机器默认的系统配置，

此时，内核运行在EL2权级下，用户程序运行在EL0权级下。确定了系统配置后，有条件敏感指令将进一步被分为以下三种情况：

1. 若根据当前系统配置，该指令成为非敏感指令，则内核态应用可以直接执行，无需处理

（配置）；

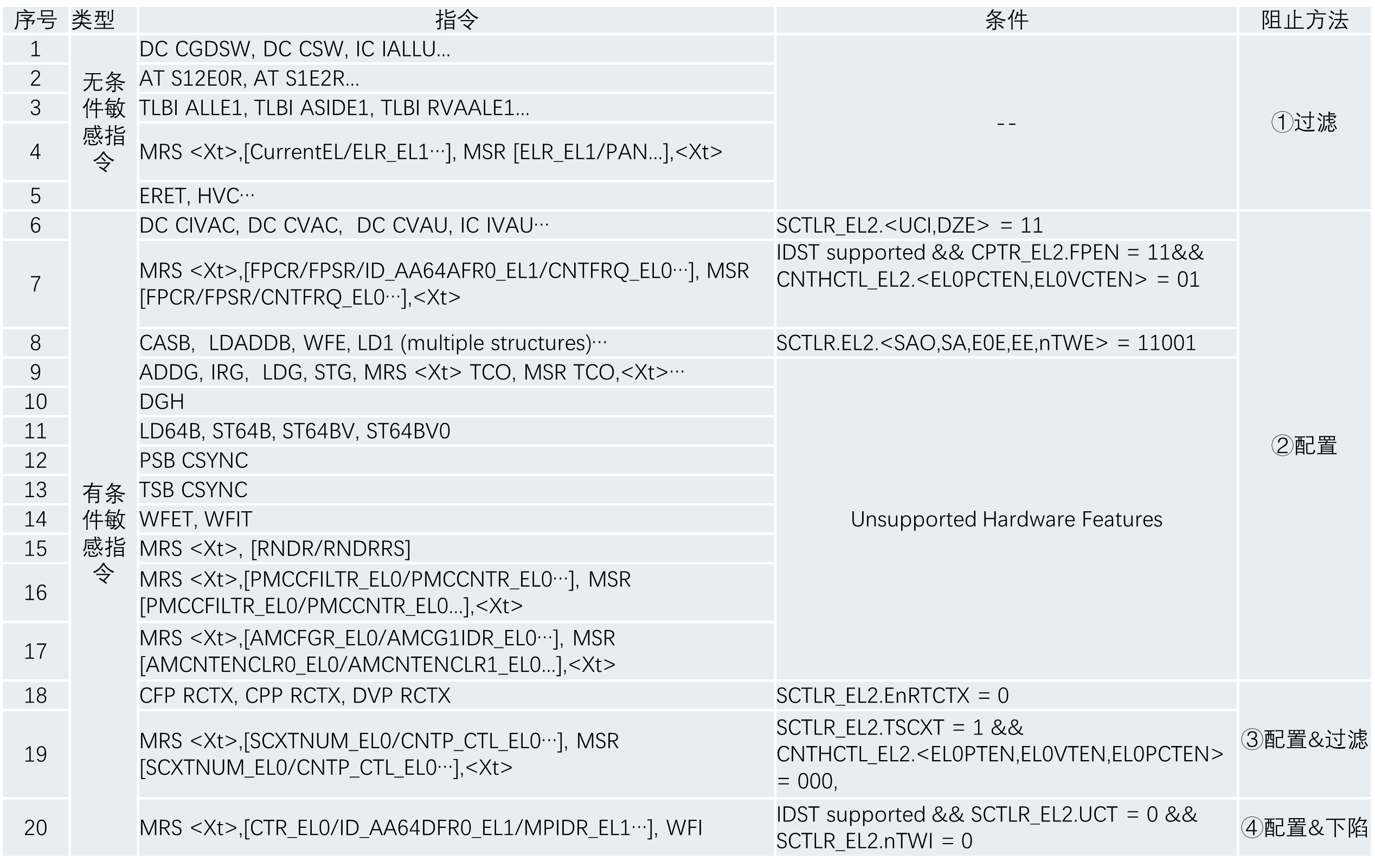
1. 若根据当前系统配置，该指令成为用户态下不可执行、内核态下可执行的敏感指令，

则扫描模块将阻止该指令的执行（配置&过滤）；

1. 若根据当前系统配置，该指令成为用户态和内核态均可执行，但行为不一致的敏感指令

，则扫描模块将把该指令替换为brk指令，执行时，由模拟模块截获brk异常并模拟该指令的用户态行为后返回（配置&下陷）。

部分敏感指令的分类、配置及处理方法如下表所示。其中条件栏省略了配置条件：EL2Enable() && !HaveEL(EL3) && HCR\_EL2.<E2H,TGE>=11，这些配置表示当前系统使用EL0 和两个权级，EL2充当 host，EL0 充当 guest，EL0 下的异常由 EL2 处理。



# 附录：敏感指令列表

2.3 框架设计方案：包括用户进程运行在内核态的方案，多进程、多线程等场景支持方案，典型应用和场景支持、性能优化方案

2.4 阶段1 报告和代码文档（xmy）

2.5 安全设计方案：包括二进制代码扫描技术方案、敏感指令安全使用方案、进程页表安全使用技术方案、页表页面安全使用置换技术方案、安全接口设计方案等

# 二进制代码扫描技术方案

## 运行时敏感指令编码扫描（lqj）

运行时的敏感指令扫描包括三个模块：扫描模块，监控模块和模拟模块。扫描模块对指定地址的代码进行扫描，并根据扫描结果决定是否报错，对于需要进行模拟的指令，扫描模块会将其替换为brk指令，并将信息包含在brk指令的立即数域中。监控模块在程序执行时对内存中的可执行页进行监控，并调用扫描模块对指令进行扫描，若发现敏感指令，则同样报错或对指令进行替换。模拟模块在程序执行时截获 brk 导致的异常，并对敏感指令在用户态下的行为进行模拟。

**1.1扫描模块的指令扫描算法。**

本项目设计的扫描算法将扫描从指定地址开始，指定大小内存的所有指令。扫描到每条指令时，算法可能执行以下三种行为：

* 1. 通过（Pass）：指令分类结果显示应允许该指令正常执行，因此算法在扫描到该指令时不做任何操作。这类指令都是非敏感指令。
  2. 阻止（Ban）：指令分类结果显示应阻止该指令执行，因此算法在扫描到该指令时将直接报错并终止扫描。这类指令都是敏感指令。
  3. 替换（Replace）：指令分类结果显示应模拟该指令的执行，因此算法在扫描到该指令时将会把它替换成一条brk指令，并将指令信息附加在brk指令的立即数域中。这类指令都是敏感指令。

如果扫描的内存中不包含需要阻止的指令，扫描算法将允许该内存的代码执行。

ARMv8-A64 指令集为定长指令集，一条指令的长度为 32 位。本项目根据指令所在的章节将指令集中的所有指令分为了系统指令与基础指令两大类，这两类指令可以根据指令码的前 13 位进行区分。同时，基于指令分类结果，系统指令中只有少部分（117 条）为非敏感指令，而基础指令中只有少部分（7 条）为敏感指令。因此，对于一条系统指令，只需将其与所有系统指令中的非敏感指令进行比较即可得知它是否是敏感指令。同理，对于一条基础指令，只需将其与所有基础指令中的敏感指令进行比较即可。另外，系统指令中需要进行模拟的指令数量为 9 条，而基础指令中需要进行模拟的指令数量为 1 条。

根据上述特征，本项目设计的扫描算法将对系统指令和敏感指令执行不同的判断逻辑，以提升算法性能。

本项目实现了基于双哈希表的扫描算法。本算法使用哈希来完成指令的匹配功能，算法将首先根据指令编码前缀确定它是系统指令还是基础指令，然后执行不同的判断逻辑。以系统指令为例，所有系统指令将通过哈希函数来转换成一个 10 位的二进制数。同时，其中的非敏感指令和需要模拟的指令将依据哈希函数结果建立哈希表，哈希表中的每一项包含一个键值对，表示一个从哈希值到对应指令及操作的映射。

在进行指令匹配时，算法首先获得待匹配指令对应的哈希值，然后利用该值来查询哈希表，以确定待匹配指令是否是非敏感指令（对应操作为“通过”）或需要模拟（对应操作为“替换”）的指令。若该指令不在哈希表中，则对应的操作为“阻止”。

同理，对于基础指令来说，哈希表中将存储所有敏感指令（包括需要“阻止”或“模拟”的指令）。在进行指令匹配时，算法将查询哈希表来确定待匹配指令是否是敏感指令（对应操作为“阻止”或“模拟”）。若该指令不在哈希表中，则该指令为非敏感指令，对应的操作为“允许”。

**1.2监控模块**

监控模块需要监控程序执行过程中新增可执行页的时刻，并在此时调用扫描模块。本项目将新增可执行页时机分为以下三种：

* 1. 系统为某个虚拟页创建虚实映射，并设置为可执行页；
  2. 系统将某个已建立虚实映射的虚拟页设置为可执行页；
  3. 可执行页内容被修改。

下面依次介绍三种情况的发生场景和处理方案。

（1）系统为某个虚拟页创建虚实映射，并设置为可执行页；

Linux系统在为进程分配虚拟页时并不会为其分配物理页，进程之后首次访问该页时将触发缺页异常，此时操作系统才会真正为其分配物理页并建立虚实映射。此时，若该出错页为文件页（磁盘上有文件与之对应，比如代码页），则操作系统将从磁盘将对应的文件内容填充到物理页中；若该页为匿名页（磁盘上没有文件与之对应，比如堆栈页面），则操作系统将直接分配一个全零的物理页。另外，针对读文件页导致的缺页异常，操作系统还会进行预读，为出错地址的邻近若干页都分配物理页。

该类情况广泛出现在程序的代码页中，例如，操作系统将可执行文件加载到内存时同样仅分配虚拟页，并不建立虚实地址映射。因此，在程序的某一页首次被执行时，系统将分配一个新的物理页，从磁盘读取代码并填充，然后将对应的虚拟页设置为可执行页。

处理方案：

在建立虚实映射时扫描。

  访问未建立虚实映射的虚拟页导致将触发异常，内核调用缺页异常处理函数处理该异常。针对匿名页异常，内核在异常处理函数中为其分配的是清零页，无需扫描。针对文件页异常，本监控模块将监控内核对其出错地址页和预读页的页表项填充函数，在其执行之前，判断将要设置的页表项是否有执行权限，若有，则扫描页表项中指定物理地址的内容。

（2）系统将某个已建立虚实映射的虚拟页设置为可执行页；

用户可以通过 mprotect 系统调用修改指定区间虚存的访问权限，在系统调用返回前，内核将直接修改区间内各页面页表项的权限。

处理方案：

在 mprotect 系统调用处进行扫描。

监控 mprotect 系统调用函数，在设置权限之前，判断新权限是否有执行权限。若有，对区间内的页面内容进行扫描。

（3）可执行页内容被修改

用户可以通过mmap、mprotect等系统调用设置虚拟页权限为可写可执行，由此，某个可执行页可能需要多次扫描：页面在某次执行前若发生了内容修改，则需要重新扫描页面内容。而根据 Linux 内核的内存管理逻辑，页面除了在没有建立虚实映射和权限不符等情况下会触发异常之外，大部分读写执行操作都将直接执行，不下陷到内核，监控模块无法感知页面修改。

处理方案：

只允许页面同时拥有写和执行权限之一，在权限异常处理函数中翻转权限，并扫描。

在内核为页面置上页表的写权限时，监控模块将其执行权限删去；后续页面若需要执行，则会触发执行异常，此时监控模块为其置上执行权限，删去写权限并扫描页面内容。同理，之后页面写时将触发写异常，监控模块为其置上写权限，删去执行权限。

另外，多进程可能通过共享内存方式同时拥有页面的可写可执行权限，此时监控模块对页面的权限设置需要查找反向映射表（reverse map），以修改所有共享虚拟页的权限。

**1.3模拟模块**

模拟模块监控内核对于brk指令的异常处理函数，依据 brk 指令的立即数域判断需要模拟的是哪条指令，并对原指令的用户态行为进行模拟，然后返回用户态并执行下条指令。

考虑需要模拟的指令 MRS <Xt>,CTR\_EL0，该指令读取系统寄存器 CTR\_EL0 的值到某个通用寄存器中，在特权态和用户态下该寄存器的读取值不一致。截获模块在扫描到该指令时会将该指令替换为brk指令，在立即数域中指明该指令为MRS CTR\_EL0 指令，且指令目标寄存器号。模拟模块截获 brk 异常后，将会把用户态下CTR\_EL0 寄存器的读取值放在指定的寄存器中，然后跳转到下条指令执行。

## 通过二进制重写消除可执行数据中的敏感指令编码（hxa）

**软件交付**

* 1. 阶段1框架代码：内核态APP 技术基础框架
  2. 阶段1安全代码：二进制代码扫描模块代码

敏感指令列表

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 无条件敏感指令-过滤 |  |  |  |  |  |
| C5.2.1 MRS <Xt>,CurrentEL, Current Exception Level |  |  |  |  |  |
| C5.2.4 MRS <Xt>,ELR\_EL1, Exception Link Register (EL1) |  |  |  |  |  |
| C5.2.4 MRS <Xt>,ELR\_EL12, Exception Link Register (EL1) |  |  |  |  |  |
| C5.2.4 MSR ELR\_EL1,<Xt> Exception Link Register (EL1) |  |  |  |  |  |
| C5.2.4 MSR ELR\_EL12,<Xt> Exception Link Register (EL1) |  |  |  |  |  |
| C5.2.5 MRS <Xt>,ELR\_EL2, Exception Link Register (EL2) |  |  |  |  |  |
| C5.2.5 MSR ELR\_EL2,<Xt> Exception Link Register (EL2) |  |  |  |  |  |
| C5.2.6 MRS <Xt>,ELR\_EL3, Exception Link Register (EL3) |  |  |  |  |  |
| C5.2.10 MRS <Xt>,PAN, Privileged Access Never |  |  |  |  |  |
| C5.2.10 MSR PAN,<Xt> Privileged Access Never |  |  |  |  |  |
| C5.2.11 MRS <Xt>,SP\_EL0, Stack Pointer (EL0) |  |  |  |  |  |
| C5.2.11 MSR SP\_EL0,<Xt> Stack Pointer (EL0) |  |  |  |  |  |
| C5.2.12 MRS <Xt>,SP\_EL1, Stack Pointer (EL1) |  |  |  |  |  |
| C5.2.12 MSR SP\_EL1,<Xt> Stack Pointer (EL1) |  |  |  |  |  |
| C5.2.13 MRS <Xt>,SP\_EL2, Stack Pointer (EL2) |  |  |  |  |  |
| C5.2.15 MRS <Xt>,SPSel, Stack Pointer Select |  |  |  |  |  |
| C5.2.15 MSR SPSel,<Xt> Stack Pointer Select |  |  |  |  |  |
| C5.2.16 MRS <Xt>,SPSR\_abt, Saved Program Status Register (Abort mode) |  |  |  |  |  |
| C5.2.16 MSR SPSR\_abt,<Xt> Saved Program Status Register (Abort mode) |  |  |  |  |  |
| C5.2.17 MRS <Xt>,SPSR\_EL1, Saved Program Status Register (EL1) |  |  |  |  |  |
| C5.2.17 MRS <Xt>,SPSR\_EL12, Saved Program Status Register (EL1) |  |  |  |  |  |
| C5.2.17 MSR SPSR\_EL1,<Xt> Saved Program Status Register (EL1) |  |  |  |  |  |
| C5.2.17 MSR SPSR\_EL12,<Xt> Saved Program Status Register (EL1) |  |  |  |  |  |
| C5.2.18 MRS <Xt>,SPSR\_EL2, Saved Program Status Register (EL2) |  |  |  |  |  |
| C5.2.18 MSR SPSR\_EL2,<Xt> Saved Program Status Register (EL2) |  |  |  |  |  |
| C5.2.19 MRS <Xt>,SPSR\_EL3, Saved Program Status Register (EL3) |  |  |  |  |  |
| C5.2.20 MRS <Xt>,SPSR\_fiq, Saved Program Status Register (FIQ mode) |  |  |  |  |  |
| C5.2.20 MSR SPSR\_fiq,<Xt> Saved Program Status Register (FIQ mode) |  |  |  |  |  |
| C5.2.21 MRS <Xt>,SPSR\_irq, Saved Program Status Register (IRQ mode) |  |  |  |  |  |
| C5.2.21 MSR SPSR\_irq,<Xt> Saved Program Status Register (IRQ mode) |  |  |  |  |  |
| C5.2.22 MRS <Xt>,SPSR\_und, Saved Program Status Register (Undefined mode) |  |  |  |  |  |
| C5.2.22 MSR SPSR\_und,<Xt> Saved Program Status Register (Undefined mode) |  |  |  |  |  |
| C5.2.25 MRS <Xt>,UAO, User Access Override |  |  |  |  |  |
| C5.2.25 MSR UAO,<Xt> User Access Override |  |  |  |  |  |
| C5.3.1 DC CGDSW, Clean of Data and Allocation Tags by Set/Way |  |  |  |  |  |
| C5.3.5 DC CGSW, Clean of Allocation Tags by Set/Way |  |  |  |  |  |
| C5.3.9 DC CIGDSW, Clean and Invalidate of Data and Allocation Tags by Set/W |  |  |  |  |  |
| C5.3.11 DC CIGSW, Clean and Invalidate of Allocation Tags by Set/Way |  |  |  |  |  |
| C5.3.13 DC CISW, Data or unified Cache line Clean and Invalidate by Set/Way |  |  |  |  |  |
| C5.3.15 DC CSW, Data or unified Cache line Clean by Set/Way |  |  |  |  |  |
| C5.3.22 DC IGDSW, Invalidate of Data and Allocation Tags by Set/Way |  |  |  |  |  |
| C5.3.23 DC IGDVAC, Invalidate of Data and Allocation Tags by VA to PoC |  |  |  |  |  |
| C5.3.24 DC IGSW, Invalidate of Allocation Tags by Set/Way |  |  |  |  |  |
| C5.3.25 DC IGVAC, Invalidate of Allocation Tags by VA to PoC |  |  |  |  |  |
| C5.3.26 DC ISW, Data or unified Cache line Invalidate by Set/Way |  |  |  |  |  |
| C5.3.27 DC IVAC, Data or unified Cache line Invalidate by VA to PoC |  |  |  |  |  |
| C5.3.29 IC IALLU, Instruction Cache Invalidate All to PoU |  |  |  |  |  |
| C5.3.30 IC IALLUIS, Instruction Cache Invalidate All to PoU, Inner Shareable |  |  |  |  |  |
| C5.4.1 AT S12E0R, Address Translate Stages 1 and 2 EL0 Read |  |  |  |  |  |
| C5.4.2 AT S12E0W, Address Translate Stages 1 and 2 EL0 Write |  |  |  |  |  |
| C5.4.3 AT S12E1R, Address Translate Stages 1 and 2 EL1 Read |  |  |  |  |  |
| C5.4.4 AT S12E1W, Address Translate Stages 1 and 2 EL1 Write |  |  |  |  |  |
| C5.4.5 AT S1E0R, Address Translate Stage 1 EL0 Read |  |  |  |  |  |
| C5.4.6 AT S1E0W, Address Translate Stage 1 EL0 Write |  |  |  |  |  |
| C5.4.7 AT S1E1R, Address Translate Stage 1 EL1 Read |  |  |  |  |  |
| C5.4.8 AT S1E1RP, Address Translate Stage 1 EL1 Read PAN |  |  |  |  |  |
| C5.4.9 AT S1E1W, Address Translate Stage 1 EL1 Write |  |  |  |  |  |
| C5.4.10 AT S1E1WP, Address Translate Stage 1 EL1 Write PAN |  |  |  |  |  |
| C5.4.11 AT S1E2R, Address Translate Stage 1 EL2 Read |  |  |  |  |  |
| C5.4.12 AT S1E2W, Address Translate Stage 1 EL2 Write |  |  |  |  |  |
| C5.4.13 AT S1E3R, Address Translate Stage 1 EL3 Read |  |  |  |  |  |
| C5.4.14 AT S1E3W, Address Translate Stage 1 EL3 Write |  |  |  |  |  |
| C5.5.1 TLBI ALLE1, TLBI ALLE1NXS, TLB Invalidate All, EL1 |  |  |  |  |  |
| C5.5.2 TLBI ALLE1IS, TLBI ALLE1ISNXS, TLB Invalidate All, EL1, Inner Shareable |  |  |  |  |  |
| C5.5.3 TLBI ALLE1OS, TLBI ALLE1OSNXS, TL B Invalidate All, EL1, Outer Shareable |  |  |  |  |  |
| C5.5.4 TLBI ALLE2, TLBI ALLE2NXS, TLB Invalidate All, EL2 |  |  |  |  |  |
| C5.5.5 TLBI ALLE2IS, TLBI ALLE2ISNXS, TLB Invalidate All, EL2, Inner Shareable |  |  |  |  |  |
| C5.5.6 TLBI ALLE2OS, TLBI ALLE2OSNXS, TL B Invalidate All, EL2, Outer Shareable |  |  |  |  |  |
| C5.5.7 TLBI ALLE3, TLBI ALLE3NXS, TLB Invalidate All, EL3 |  |  |  |  |  |
| C5.5.8 TLBI ALLE3IS, TLBI ALLE3ISNXS, TLB Invalidate All, EL3, Inner Shareable |  |  |  |  |  |
| C5.5.9 TLBI ALLE3OS, TLBI ALLE3OSNXS, TL B Invalidate All, EL3, Outer Shareable |  |  |  |  |  |
| C5.5.10 TLBI ASIDE1, TLBI ASIDE1NXS, TLB Invalidate by ASID, EL1 |  |  |  |  |  |
| C5.5.11 TLBI ASIDE1IS, TLBI ASIDE1ISNXS, TLB Invalidate by ASID, EL1, Inner Shareable |  |  |  |  |  |
| C5.5.12 TLBI ASIDE1OS, TLBI ASIDE1OSNXS, TLB Invalidate by ASID, EL1, Outer Shareable |  |  |  |  |  |
| C5.5.13 TLBI IPAS2E1, TLBI IPAS2E1NXS, TLB Invalida te by Intermediate Physical Address, Stage 2, EL1 |  |  |  |  |  |
| C5.5.14 TLBI IPAS2E1IS, TLBI IPAS2E1ISNXS, TLB Invalidate by Intermediate Physical Address, Stage 2, EL1, Inner Shareable | | |  |  |  |
| C5.5.15 TLBI IPAS2E1OS, TLBI IPAS2E1OSNXS, TLB Invalidate by Intermediate Physical Address, Stage 2, EL1, Outer Shareable | | | |  |  |
| C5.5.16 TLBI IPAS2LE1, TLBI IPAS2LE1NXS, TLB Invalidate by Intermediate Physical Address, Stage 2, Last level, EL1 | |  |  |  |  |
| C5.5.17 TLBI IPAS2LE1IS, TLBI IPAS2LE1ISNXS, TLB Invalidate by Intermediate Physical Address, Stage 2, Last level, EL1, Inner Shareable | | | |  |  |
| C5.5.18 TLBI IPAS2LE1OS, TLBI IPAS2LE1OSNXS, TLB Invalidate by Intermediate Physical Address, Stage 2, Last level, EL1, Outer Shareable | | | | |  |
| C5.5.19 TLBI RIPAS2E1, TLBI RIPAS2E1NXS, TL B Range Invalidate by Intermediate Physical Address, Stage 2, EL1 | |  |  |  |  |
| C5.5.20 TLBI RIPAS2E1IS, TLBI RIPAS2E1ISNXS, TLB Range Invalidate by Intermediate Physical Address, Stage 2, EL1, Inner Shareable | | | |  |  |
| C5.5.21 TLBI RIPAS2E1OS, TLBI RIPAS2E1OSNXS, TLB Range Invalidate by Intermediate Physical Address, Stage 2, EL1, Outer Shareable | | | |  |  |
| C5.5.22 TLBI RIPAS2LE1, TLBI RIPAS2LE1NXS, TLB Range Invalidate by Intermediate Physical Address, Stage 2, Last level, EL1 | | |  |  |  |
| C5.5.23 TLBI RIPAS2LE1IS, TLBI RIPAS2LE1ISNXS, TLB Range Invalidate by Intermediate Physical Address, Stage 2, Last level, EL1, Inner Shareable | | | | |  |
| C5.5.24 TLBI RIPAS2LE1OS, TLBI RIPAS2LE1OSNXS, TLB Range Invalidate by Intermediate Physical Address, Stage 2, Last level, EL1, Outer Shareable | | | | | |
| C5.5.25 TLBI RVAAE1, TLBI RVAAE1NXS, TLB Range Invalidate by VA, All ASID, EL1 |  |  |  |  |  |
| C5.5.26 TLBI RVAAE1IS, TLBI RVAAE1ISNXS, TLB Range Invalidate by VA, All ASID, EL1, Inner Shareable |  |  |  |  |  |
| C5.5.27 TLBI RVAAE1OS, TLBI RVAAE1OSNXS, TLB Ra nge Invalidate by VA, All ASID, EL1, Outer Shareable | |  |  |  |  |
| C5.5.28 TLBI RVAALE1, TLBI RVAALE1NXS, TLB Range Invalidate by VA, All ASID, Last level, EL1 |  |  |  |  |  |
| C5.5.29 TLBI RVAALE1IS, TLBI RVAALE1ISNXS, TLB Range Invalidate by VA, All ASID, Last Level, EL1, Inner Shareable | | |  |  |  |
| C5.5.30 TLBI RVAALE1OS, TLBI RVAALE1OSNXS, TLB Range Invalidate by VA, All ASID, Last Level, EL1, Outer Shareable | | |  |  |  |
| C5.5.31 TLBI RVAE1, TLBI RVAE1NXS, TLB Range Invalidate by VA, EL1 |  |  |  |  |  |
| C5.5.32 TLBI RVAE1IS, TLBI RVAE1ISNXS, TLB Range Invalidate by VA, EL1, Inner Shareable |  |  |  |  |  |
| C5.5.33 TLBI RVAE1OS, TLBI RVAE1OSNXS, TLB Ra nge Invalidate by VA, EL1, Outer Shareable |  |  |  |  |  |
| C5.5.34 TLBI RVAE2, TLBI RVAE2NXS, TLB Range Invalidate by VA, EL2 |  |  |  |  |  |
| C5.5.35 TLBI RVAE2IS, TLBI RVAE2ISNXS, TLB Range Invalidate by VA, EL2, Inner Shareable |  |  |  |  |  |
| C5.5.36 TLBI RVAE2OS, TLBI RVAE2OSNXS, TLB Ra nge Invalidate by VA, EL2, Outer Shareable |  |  |  |  |  |
| C5.5.37 TLBI RVAE3, TLBI RVAE3NXS, TLB Range Invalidate by VA, EL3 |  |  |  |  |  |
| C5.5.38TLBI RVAE3IS, TLBI RVAE3ISNXS, TLB Range Invalidate by VA, EL3, Inner Shareable |  |  |  |  |  |
| C5.5.39 TLBI RVAE3OS, TLBI RVAE3OSNXS, TLB Ra nge Invalidate by VA, EL3, Outer Shareable |  |  |  |  |  |
| C5.5.40 TLBI RVALE1, TLBI RVALE1NXS, TLB Ra nge Invalidate by VA, Last level, EL1 |  |  |  |  |  |
| C5.5.41 TLBI RVALE1IS, TLBI RVALE1ISNXS, TLB Ra nge Invalidate by VA, Last level, EL1, Inner Shareable |  |  |  |  |  |
| C5.5.42 TLBI RVALE1OS, TLBI RVALE1OSNXS, TLB Ra nge Invalidate by VA, Last level, EL1, Outer Shareable | |  |  |  |  |
| C5.5.43 TLBI RVALE2, TLBI RVALE2NXS, TLB Ra nge Invalidate by VA, Last level, EL2 |  |  |  |  |  |
| C5.5.44 TLBI RVALE2IS, TLBI RVALE2ISNXS, TLB Ra nge Invalidate by VA, Last level, EL2, Inner Shareable |  |  |  |  |  |
| C5.5.45 TLBI RVALE2OS, TLBI RVALE2OSNXS, TLB Ra nge Invalidate by VA, Last level, EL2, Outer Shareable | |  |  |  |  |
| C5.5.46 TLBI RVALE3, TLBI RVALE3NXS, TLB Ra nge Invalidate by VA, Last level, EL3 |  |  |  |  |  |
| C5.5.47 TLBI RVALE3IS, TLBI RVALE3ISNXS, TLB Ra nge Invalidate by VA, Last level, EL3, Inner Shareable |  |  |  |  |  |
| C5.5.48 TLBI RVALE3OS, TLBI RVALE3OSNXS, TLB Ra nge Invalidate by VA, Last level, EL3, Outer Shareable | |  |  |  |  |
| C5.5.49 TLBI VAAE1, TLBI VAAE1NXS, TL B Invalidate by VA, All ASID, EL1 |  |  |  |  |  |
| C5.5.50 TLBI VAAE1IS, TLBI VAAE1ISNXS, TLB In validate by VA, All ASID, EL1, Inner Shareable |  |  |  |  |  |
| C5.5.51 TLBI VAAE1OS, TLBI VAAE1OSNXS, TLB In validate by VA, All ASID, EL1, Outer Shareable |  |  |  |  |  |
| C5.5.52 TLBI VAALE1, TLBI VAALE1NXS, TLB In validate by VA, All ASID, Last level, EL1 |  |  |  |  |  |
| C5.5.53 TLBI VAALE1IS, TLBI VAALE1ISNXS, TLB Inva lidate by VA, All ASID, Last Level, EL1, Inner Shareable | |  |  |  |  |
| C5.5.54 TLBI VAALE1OS, TLBI VAALE1OSNXS, TLB Inva lidate by VA, All ASID, Last Level, EL1, Outer Shareable | |  |  |  |  |
| C5.5.55 TLBI VAE1, TLBI VAE1NXS, TLB Invalidate by VA, EL1 |  |  |  |  |  |
| C5.5.56 TLBI VAE1IS, TLBI VAE1ISNXS, TLB Invalidate by VA, EL1, Inner Shareable |  |  |  |  |  |
| C5.5.57 TLBI VAE1OS, TLBI VAE1OSNXS, TLB Invalidate by VA, EL1, Outer Shareable |  |  |  |  |  |
| C5.5.58 TLBI VAE2, TLBI VAE2NXS, TLB Invalidate by VA, EL2 |  |  |  |  |  |
| C5.5.59 TLBI VAE2IS, TLBI VAE2ISNXS, TLB Invalidate by VA, EL2, Inner Shareable |  |  |  |  |  |
| C5.5.60 TLBI VAE2OS, TLBI VAE2OSNXS, TLB Invalidate by VA, EL2, Outer Shareable |  |  |  |  |  |
| C5.5.61 TLBI VAE3, TLBI VAE3NXS, TLB Invalidate by VA, EL3 |  |  |  |  |  |
| C5.5.62 TLBI VAE3IS, TLBI VAE3ISNXS, TLB Invalidate by VA, EL3, Inner Shareable |  |  |  |  |  |
| C5.5.63 TLBI VAE3OS, TLBI VAE3OSNXS, TLB Invalidate by VA, EL3, Outer Shareable |  |  |  |  |  |
| C5.5.64 TLBI VALE1, TLBI VALE1NXS, TL B Invalidate by VA, Last level, EL1 |  |  |  |  |  |
| C5.5.65 TLBI VALE1IS, TLBI VALE1ISNXS, TLB Invali date by VA, Last level, EL1, Inner Shareable |  |  |  |  |  |
| C5.5.66 TLBI VALE1OS, TLBI VALE1OSNXS, TLB Inva lidate by VA, Last level, EL1, Outer Shareable |  |  |  |  |  |
| C5.5.67 TLBI VALE2, TLBI VALE2NXS, TL B Invalidate by VA, Last level, EL2 |  |  |  |  |  |
| C5.5.68 TLBI VALE2IS, TLBI VALE2ISNXS, TLB Invali date by VA, Last level, EL2, Inner Shareable |  |  |  |  |  |
| C5.5.69 TLBI VALE2OS, TLBI VALE2OSNXS, TLB Inva lidate by VA, Last level, EL2, Outer Shareable |  |  |  |  |  |
| C5.5.70 TLBI VALE3, TLBI VALE3NXS, TL B Invalidate by VA, Last level, EL3 |  |  |  |  |  |
| C5.5.71 TLBI VALE3IS, TLBI VALE3ISNXS, TLB Invali date by VA, Last level, EL3, Inner Shareable |  |  |  |  |  |
| C5.5.72 TLBI VALE3OS, TLBI VALE3OSNXS, TLB Inva lidate by VA, Last level, EL3, Outer Shareable |  |  |  |  |  |
| C5.5.73 TLBI VMALLE1, TLBI VMALLE1NXS, TLB Invalidate by VMID, All at stage 1, EL1 |  |  |  |  |  |
| C5.5.74 TLBI VMALLE1IS, TLBI VMALLE1ISNXS, TLB In validate by VMID, All at stage 1, EL1, Inner Shareable | |  |  |  |  |
| C5.5.75 TLBI VMALLE1OS, TLBI VMALLE1OSNXS, TLB In validate by VMID, All at stage 1, EL1, Outer Shareable | |  |  |  |  |
| C5.5.76 TLBI VMALLS12E1, TLBI VMALLS12E1NXS, TLB Invalidate by VMID, All at Stage 1 and 2, EL1 |  |  |  |  |  |
| C5.5.77 TLBI VMALLS12E1IS, TLBI VMALLS12E1ISNXS, TLB Invalidate by VMID, All at Stage 1 and 2, EL1, Inner Shareable | | |  |  |  |
| C5.5.78 TLBI VMALLS12E1OS, TLBI VMALLS12E1OSNXS, TLB Invalidate by VMID, All at Stage 1 and 2, EL1, Outer Shareable | | |  |  |  |
| C6.2.87 ERET |  |  |  |  |  |
| C6.2.88 ERETAA, ERETA |  |  |  |  |  |
| C6.2.93 HLT |  |  |  |  |  |
| C6.2.94 HVC |  |  |  |  |  |
| C6.2.195 MSR (immediate)仅部分编码属于该类 |  |  |  |  |  |
| C6.2.241   SMC |  |  |  |  |  |
| D13.2.1 MRS <Xt>,ACCDATA\_EL1, Accelerator Data |  |  |  |  |  |
| D13.2.1 MSR ACCDATA\_EL1,<Xt> Accelerator Data |  |  |  |  |  |
| D13.2.2 MRS <Xt>,ACTLR\_EL1, Auxiliary Control Register (EL1) |  |  |  |  |  |
| D13.2.2 MSR ACTLR\_EL1,<Xt> Auxiliary Control Register (EL1) |  |  |  |  |  |
| D13.2.3 MRS <Xt>,ACTLR\_EL2, Auxiliary Control Register (EL2) |  |  |  |  |  |
| D13.2.3 MSR ACTLR\_EL2,<Xt> Auxiliary Control Register (EL2) |  |  |  |  |  |
| D13.2.4 MRS <Xt>,ACTLR\_EL3, Auxiliary Control Register (EL3) |  |  |  |  |  |
| D13.2.5 MRS <Xt>,AFSR0\_EL1, Auxiliary Fault Status Register 0 (EL1) |  |  |  |  |  |
| D13.2.5 MRS <Xt>,AFSR0\_EL12, Auxiliary Fault Status Register 0 (EL1) |  |  |  |  |  |
| D13.2.5 MSR AFSR0\_EL1,<Xt> Auxiliary Fault Status Register 0 (EL1) |  |  |  |  |  |
| D13.2.5 MSR AFSR0\_EL12,<Xt> Auxiliary Fault Status Register 0 (EL1) |  |  |  |  |  |
| D13.2.6 MRS <Xt>,AFSR0\_EL2, Auxiliary Fault Status Register 0 (EL2) |  |  |  |  |  |
| D13.2.6 MSR AFSR0\_EL2,<Xt> Auxiliary Fault Status Register 0 (EL2) |  |  |  |  |  |
| D13.2.7 MRS <Xt>,AFSR0\_EL3, Auxiliary Fault Status Register 0 (EL3) |  |  |  |  |  |
| D13.2.8 MRS <Xt>,AFSR1\_EL1, Auxiliary Fault Status Register 1 (EL1) |  |  |  |  |  |
| D13.2.8 MRS <Xt>,AFSR1\_EL12, Auxiliary Fault Status Register 1 (EL1) |  |  |  |  |  |
| D13.2.8 MSR AFSR1\_EL1,<Xt> Auxiliary Fault Status Register 1 (EL1) |  |  |  |  |  |
| D13.2.8 MSR AFSR1\_EL12,<Xt> Auxiliary Fault Status Register 1 (EL1) |  |  |  |  |  |
| D13.2.9 MRS <Xt>,AFSR1\_EL2, Auxiliary Fault Status Register 1 (EL2) |  |  |  |  |  |
| D13.2.9 MSR AFSR1\_EL2,<Xt> Auxiliary Fault Status Register 1 (EL2) |  |  |  |  |  |
| D13.2.10 MRS <Xt>,AFSR1\_EL3, Auxiliary Fault Status Register 1 (EL3) |  |  |  |  |  |
| D13.2.11 MRS <Xt>,AIDR\_EL1, Auxiliary ID Register |  |  |  |  |  |
| D13.2.12 MRS <Xt>,AMAIR\_EL1, Auxiliary Memory Attribute Indirection Register (EL1) |  |  |  |  |  |
| D13.2.12 MRS <Xt>,AMAIR\_EL12, Auxiliary Memory Attribute Indirection Register (EL1) |  |  |  |  |  |
| D13.2.12 MSR AMAIR\_EL1,<Xt> Auxiliary Memory Attribute Indirection Register (EL1) |  |  |  |  |  |
| D13.2.12 MSR AMAIR\_EL12,<Xt> Auxiliary Memory Attribute Indirection Register (EL1) |  |  |  |  |  |
| D13.2.13 MRS <Xt>,AMAIR\_EL2, Auxiliary Memory Attribute Indirection Register (EL2) |  |  |  |  |  |
| D13.2.13 MSR AMAIR\_EL2,<Xt> Auxiliary Memory Attribute Indirection Register (EL2) |  |  |  |  |  |
| D13.2.14 MRS <Xt>,AMAIR\_EL3, Auxiliary Memory Attribute Indirection Register (EL3) |  |  |  |  |  |
| D13.2.15 MRS <Xt>,APDAKeyHi\_EL1, Pointer Authentication Key A for Data (bits[127:64]) |  |  |  |  |  |
| D13.2.15 MSR APDAKeyHi\_EL1,<Xt> Pointer Authentication Key A for Data (bits[127:64]) |  |  |  |  |  |
| D13.2.16 MRS <Xt>,APDAKeyLo\_EL1, Pointer Authentication Key A for Data (bits[63:0]) |  |  |  |  |  |
| D13.2.16 MSR APDAKeyLo\_EL1,<Xt> Pointer Authentication Key A for Data (bits[63:0]) |  |  |  |  |  |
| D13.2.17 MRS <Xt>,APDBKeyHi\_EL1, Pointer Authentication Key B for Data (bits[127:64]) |  |  |  |  |  |
| D13.2.17 MSR APDBKeyHi\_EL1,<Xt> Pointer Authentication Key B for Data (bits[127:64]) |  |  |  |  |  |
| D13.2.18 MRS <Xt>,APDBKeyLo\_EL1, Pointer Authentication Key B for Data (bits[63:0]) |  |  |  |  |  |
| D13.2.18 MSR APDBKeyLo\_EL1,<Xt> Pointer Authentication Key B for Data (bits[63:0]) |  |  |  |  |  |
| D13.2.19 MRS <Xt>,APGAKeyHi\_EL1, Pointer Authentication Key A for Code (bits[127:64]) |  |  |  |  |  |
| D13.2.19 MSR APGAKeyHi\_EL1,<Xt> Pointer Authentication Key A for Code (bits[127:64]) |  |  |  |  |  |
| D13.2.20 MRS <Xt>,APGAKeyLo\_EL1, Pointer Authentication Key A for Code (bits[63:0]) |  |  |  |  |  |
| D13.2.20 MSR APGAKeyLo\_EL1,<Xt> Pointer Authentication Key A for Code (bits[63:0]) |  |  |  |  |  |
| D13.2.21 MRS <Xt>,APIAKeyHi\_EL1, Pointer Authentication Key A for Instruction (bits[127:64]) |  |  |  |  |  |
| D13.2.21 MSR APIAKeyHi\_EL1,<Xt> Pointer Authentication Key A for Instruction (bits[127:64]) |  |  |  |  |  |
| D13.2.22 MRS <Xt>,APIAKeyLo\_EL1, Pointer Authentication Key A for Instruction (bits[63:0]) |  |  |  |  |  |
| D13.2.22 MSR APIAKeyLo\_EL1,<Xt> Pointer Authentication Key A for Instruction (bits[63:0]) |  |  |  |  |  |
| D13.2.23 MRS <Xt>,APIBKeyHi\_EL1, Pointer Authentication Key B for Instruction (bits[127:64]) |  |  |  |  |  |
| D13.2.23 MSR APIBKeyHi\_EL1,<Xt> Pointer Authentication Key B for Instruction (bits[127:64]) |  |  |  |  |  |
| D13.2.24 MRS <Xt>,APIBKeyLo\_EL1, Pointer Authentication Key B for Instruction (bits[63:0]) |  |  |  |  |  |
| D13.2.24 MSR APIBKeyLo\_EL1,<Xt> Pointer Authentication Key B for Instruction (bits[63:0]) |  |  |  |  |  |
| D13.2.25 MRS <Xt>,CCSIDR2\_EL1, Current Cache Size ID Register 2 |  |  |  |  |  |
| D13.2.26 MRS <Xt>,CCSIDR\_EL1, Current Cache Size ID Register |  |  |  |  |  |
| D13.2.27 MRS <Xt>,CLIDR\_EL1, Cache Level ID Register |  |  |  |  |  |
| D13.2.28 MRS <Xt>,CONTEXTIDR\_EL1, Context ID Register (EL1) |  |  |  |  |  |
| D13.2.28 MRS <Xt>,CONTEXTIDR\_EL12, Context ID Register (EL1) |  |  |  |  |  |
| D13.2.28 MSR CONTEXTIDR\_EL1,<Xt> Context ID Register (EL1) |  |  |  |  |  |
| D13.2.28 MSR CONTEXTIDR\_EL12,<Xt> Context ID Register (EL1) |  |  |  |  |  |
| D13.2.29 MRS <Xt>,CONTEXTIDR\_EL2, Context ID Register (EL2) |  |  |  |  |  |
| D13.2.29 MSR CONTEXTIDR\_EL2,<Xt> Context ID Register (EL2) |  |  |  |  |  |
| D13.2.30 MRS <Xt>,CPACR\_EL1, Architectural Feature Access Control Register |  |  |  |  |  |
| D13.2.30 MRS <Xt>,CPACR\_EL12, Architectural Feature Access Control Register |  |  |  |  |  |
| D13.2.30 MSR CPACR\_EL1,<Xt> Architectural Feature Access Control Register |  |  |  |  |  |
| D13.2.30 MSR CPACR\_EL12,<Xt> Architectural Feature Access Control Register |  |  |  |  |  |
| D13.2.31 MRS <Xt>,CPTR\_EL2, Architectural Feature Trap Register (EL2) |  |  |  |  |  |
| D13.2.31 MSR CPTR\_EL2,<Xt> Architectural Feature Trap Register (EL2) |  |  |  |  |  |
| D13.2.32 MRS <Xt>,CPTR\_EL3, Architectural Feature Trap Register (EL3) |  |  |  |  |  |
| D13.2.33 MRS <Xt>,CSSELR\_EL1, Cache Size Selection Register |  |  |  |  |  |
| D13.2.33 MSR CSSELR\_EL1,<Xt> Cache Size Selection Register |  |  |  |  |  |
| D13.2.35 MRS <Xt>,DACR32\_EL2, Domain Access Control Register |  |  |  |  |  |
| D13.2.35 MSR DACR32\_EL2,<Xt> Domain Access Control Register |  |  |  |  |  |
| D13.2.37 MRS <Xt>,ESR\_EL1, Exception Syndrome Register (EL1) |  |  |  |  |  |
| D13.2.37 MRS <Xt>,ESR\_EL12, Exception Syndrome Register (EL1) |  |  |  |  |  |
| D13.2.37 MSR ESR\_EL1,<Xt> Exception Syndrome Register (EL1) |  |  |  |  |  |
| D13.2.37 MSR ESR\_EL12,<Xt> Exception Syndrome Register (EL1) |  |  |  |  |  |
| D13.2.38 MRS <Xt>,ESR\_EL2, Exception Syndrome Register (EL2) |  |  |  |  |  |
| D13.2.38 MSR ESR\_EL2,<Xt> Exception Syndrome Register (EL2) |  |  |  |  |  |
| D13.2.39 MRS <Xt>,ESR\_EL3, Exception Syndrome Register (EL3) |  |  |  |  |  |
| D13.2.40 MRS <Xt>,FAR\_EL1, Fault Address Register (EL1) |  |  |  |  |  |
| D13.2.40 MRS <Xt>,FAR\_EL12, Fault Address Register (EL1) |  |  |  |  |  |
| D13.2.40 MSR FAR\_EL1,<Xt> Fault Address Register (EL1) |  |  |  |  |  |
| D13.2.40 MSR FAR\_EL12,<Xt> Fault Address Register (EL1) |  |  |  |  |  |
| D13.2.41 MRS <Xt>,FAR\_EL2, Fault Address Register (EL2) |  |  |  |  |  |
| D13.2.41 MSR FAR\_EL2,<Xt> Fault Address Register (EL2) |  |  |  |  |  |
| D13.2.42 MRS <Xt>,FAR\_EL3, Fault Address Register (EL3) |  |  |  |  |  |
| D13.2.43 MRS <Xt>,FPEXC32\_EL2, Floating-Point Exception Control register |  |  |  |  |  |
| D13.2.43 MSR FPEXC32\_EL2,<Xt> Floating-Point Exception Control register |  |  |  |  |  |
| D13.2.44 MRS <Xt>,GCR\_EL1, Tag Control Register. |  |  |  |  |  |
| D13.2.44 MSR GCR\_EL1,<Xt> Tag Control Register. |  |  |  |  |  |
| D13.2.45 MRS <Xt>,GMID\_EL1, Multiple tag transfer ID register |  |  |  |  |  |
| D13.2.46 MRS <Xt>,HACR\_EL2, Hypervisor Auxiliary Control Register |  |  |  |  |  |
| D13.2.46 MSR HACR\_EL2,<Xt> Hypervisor Auxiliary Control Register |  |  |  |  |  |
| D13.2.47 MRS <Xt>,HAFGRTR\_EL2, Hypervisor Activity Monitors Fine-Grained Read Trap Register |  |  |  |  |  |
| D13.2.47 MSR HAFGRTR\_EL2,<Xt> Hypervisor Activity Monitors Fine-Grained Read Trap Register |  |  |  |  |  |
| D13.2.48 MRS <Xt>,HCR\_EL2, Hypervisor Configuration Register |  |  |  |  |  |
| D13.2.48 MSR HCR\_EL2,<Xt> Hypervisor Configuration Register |  |  |  |  |  |
| D13.2.49 MRS <Xt>,HCRX\_EL2, Extended Hypervisor Configuration Register |  |  |  |  |  |
| D13.2.49 MSR HCRX\_EL2,<Xt> Extended Hypervisor Configuration Register |  |  |  |  |  |
| D13.2.50 MRS <Xt>,HDFGRTR\_EL2, Hypervisor Debug Fine-Grained Read Trap Register |  |  |  |  |  |
| D13.2.50 MSR HDFGRTR\_EL2,<Xt> Hypervisor Debug Fine-Grained Read Trap Register |  |  |  |  |  |
| D13.2.51 MRS <Xt>,HDFGWTR\_EL2, Hypervisor Debug Fine-Grained Write Trap Register |  |  |  |  |  |
| D13.2.51 MSR HDFGWTR\_EL2,<Xt> Hypervisor Debug Fine-Grained Write Trap Register |  |  |  |  |  |
| D13.2.52 MRS <Xt>,HFGITR\_EL2, Hypervisor Fine-Grained Instruction Trap Register |  |  |  |  |  |
| D13.2.52 MSR HFGITR\_EL2,<Xt> Hypervisor Fine-Grained Instruction Trap Register |  |  |  |  |  |
| D13.2.53 MRS <Xt>,HFGRTR\_EL2, Hypervisor Fine-Grained Read Trap Register |  |  |  |  |  |
| D13.2.53 MSR HFGRTR\_EL2,<Xt> Hypervisor Fine-Grained Read Trap Register |  |  |  |  |  |
| D13.2.54 MRS <Xt>,HFGWTR\_EL2, Hypervisor Fine-Grained Write Trap Register |  |  |  |  |  |
| D13.2.54 MSR HFGWTR\_EL2,<Xt> Hypervisor Fine-Grained Write Trap Register |  |  |  |  |  |
| D13.2.55 MRS <Xt>,HPFAR\_EL2, Hypervisor IPA Fault Address Register |  |  |  |  |  |
| D13.2.55 MSR HPFAR\_EL2,<Xt> Hypervisor IPA Fault Address Register |  |  |  |  |  |
| D13.2.56 MRS <Xt>,HSTR\_EL2, Hypervisor System Trap Register |  |  |  |  |  |
| D13.2.56 MSR HSTR\_EL2,<Xt> Hypervisor System Trap Register |  |  |  |  |  |
| D13.2.69 MRS <Xt>,ID\_AFR0\_EL1, AArch32 Auxiliary Feature Register 0 |  |  |  |  |  |
| D13.2.70 MRS <Xt>,ID\_DFR0\_EL1, AArch32 Debug Feature Register 0 |  |  |  |  |  |
| D13.2.71 MRS <Xt>,ID\_DFR1\_EL1, Debug Feature Register 1 |  |  |  |  |  |
| D13.2.72 MRS <Xt>,ID\_ISAR0\_EL1, AArch32 Instruction Set Attribute Register 0 |  |  |  |  |  |
| D13.2.73 MRS <Xt>,ID\_ISAR1\_EL1, AArch32 Instruction Set Attribute Register 1 |  |  |  |  |  |
| D13.2.74 MRS <Xt>,ID\_ISAR2\_EL1, AArch32 Instruction Set Attribute Register 2 |  |  |  |  |  |
| D13.2.75 MRS <Xt>,ID\_ISAR3\_EL1, AArch32 Instruction Set Attribute Register 3 |  |  |  |  |  |
| D13.2.76 MRS <Xt>,ID\_ISAR4\_EL1, AArch32 Instruction Set Attribute Register 4 |  |  |  |  |  |
| D13.2.77 MRS <Xt>,ID\_ISAR5\_EL1, AArch32 Instruction Set Attribute Register 5 |  |  |  |  |  |
| D13.2.78 MRS <Xt>,ID\_ISAR6\_EL1, AArch32 Instruction Set Attribute Register 6 |  |  |  |  |  |
| D13.2.79 MRS <Xt>,ID\_MMFR0\_EL1, AArch32 Memory Model Feature Register 0 |  |  |  |  |  |
| D13.2.80 MRS <Xt>,ID\_MMFR1\_EL1, AArch32 Memory Model Feature Register 1 |  |  |  |  |  |
| D13.2.81 MRS <Xt>,ID\_MMFR2\_EL1, AArch32 Memory Model Feature Register 2 |  |  |  |  |  |
| D13.2.82 MRS <Xt>,ID\_MMFR3\_EL1, AArch32 Memory Model Feature Register 3 |  |  |  |  |  |
| D13.2.83 MRS <Xt>,ID\_MMFR4\_EL1, AArch32 Memory Model Feature Register 4 |  |  |  |  |  |
| D13.2.84 MRS <Xt>,ID\_MMFR5\_EL1, AArch32 Memory Model Feature Register 5 |  |  |  |  |  |
| D13.2.85 MRS <Xt>,ID\_PFR0\_EL1, AArch32 Processor Feature Register 0 |  |  |  |  |  |
| D13.2.86 MRS <Xt>,ID\_PFR1\_EL1, AArch32 Processor Feature Register 1 |  |  |  |  |  |
| D13.2.87 MRS <Xt>,ID\_PFR2\_EL1, AArch32 Processor Feature Register 2 |  |  |  |  |  |
| D13.2.88 MRS <Xt>,IFSR32\_EL2, Instruction Fault Status Register (EL2) |  |  |  |  |  |
| D13.2.88 MSR IFSR32\_EL2,<Xt> Instruction Fault Status Register (EL2) |  |  |  |  |  |
| D13.2.89 MRS <Xt>,ISR\_EL1, Interrupt Status Register |  |  |  |  |  |
| D13.2.90 MRS <Xt>,LORC\_EL1, LORegion Control (EL1) |  |  |  |  |  |
| D13.2.90 MSR LORC\_EL1,<Xt> LORegion Control (EL1) |  |  |  |  |  |
| D13.2.91 MRS <Xt>,LOREA\_EL1, LORegion End Address (EL1) |  |  |  |  |  |
| D13.2.91 MSR LOREA\_EL1,<Xt> LORegion End Address (EL1) |  |  |  |  |  |
| D13.2.92 MRS <Xt>,LORID\_EL1, LORegionID (EL1) |  |  |  |  |  |
| D13.2.93 MRS <Xt>,LORN\_EL1, LORegion Number (EL1) |  |  |  |  |  |
| D13.2.93 MSR LORN\_EL1,<Xt> LORegion Number (EL1) |  |  |  |  |  |
| D13.2.94 MRS <Xt>,LORSA\_EL1, LORegion Start Address (EL1) |  |  |  |  |  |
| D13.2.94 MSR LORSA\_EL1,<Xt> LORegion Start Address (EL1) |  |  |  |  |  |
| D13.2.95 MRS <Xt>,MAIR\_EL1, Memory Attribute Indirection Register (EL1) |  |  |  |  |  |
| D13.2.95 MRS <Xt>,MAIR\_EL12, Memory Attribute Indirection Register (EL1) |  |  |  |  |  |
| D13.2.95 MSR MAIR\_EL1,<Xt> Memory Attribute Indirection Register (EL1) |  |  |  |  |  |
| D13.2.95 MSR MAIR\_EL12,<Xt> Memory Attribute Indirection Register (EL1) |  |  |  |  |  |
| D13.2.96 MRS <Xt>,MAIR\_EL2, Memory Attribute Indirection Register (EL2) |  |  |  |  |  |
| D13.2.96 MSR MAIR\_EL2,<Xt> Memory Attribute Indirection Register (EL2) |  |  |  |  |  |
| D13.2.97 MRS <Xt>,MAIR\_EL3, Memory Attribute Indirection Register (EL3) |  |  |  |  |  |
| D13.2.100 MRS <Xt>,MVFR0\_EL1, AArch32 Media and VFP Feature Register 0 |  |  |  |  |  |
| D13.2.101 MRS <Xt>,MVFR1\_EL1, AArch32 Media and VFP Feature Register 1 |  |  |  |  |  |
| D13.2.102 MRS <Xt>,MVFR2\_EL1, AArch32 Media and VFP Feature Register 2 |  |  |  |  |  |
| D13.2.103 MRS <Xt>,PAR\_EL1, Physical Address Register |  |  |  |  |  |
| D13.2.103 MSR PAR\_EL1,<Xt> Physical Address Register |  |  |  |  |  |
| D13.2.105 MRS <Xt>,RGSR\_EL1, Random Allocation Tag Seed Register. |  |  |  |  |  |
| D13.2.105 MSR RGSR\_EL1,<Xt> Random Allocation Tag Seed Register. |  |  |  |  |  |
| D13.2.106 MRS <Xt>,RMR\_EL1, Reset Management Register (EL1) |  |  |  |  |  |
| D13.2.106 MSR RMR\_EL1,<Xt> Reset Management Register (EL1) |  |  |  |  |  |
| D13.2.107 MRS <Xt>,RMR\_EL2, Reset Management Register (EL2) |  |  |  |  |  |
| D13.2.107 MSR RMR\_EL2,<Xt> Reset Management Register (EL2) |  |  |  |  |  |
| D13.2.108 MRS <Xt>,RMR\_EL3, Reset Management Register (EL3) |  |  |  |  |  |
| D13.2.111 MRS <Xt>,RVBAR\_EL1, Reset Vector Base Address Register (if EL2 and EL3 not implemented) |  |  |  |  |  |
| D13.2.112 MRS <Xt>,RVBAR\_EL2, Reset Vector Base Address Register (if EL3 not implemented) |  |  |  |  |  |
| D13.2.113 MRS <Xt>,RVBAR\_EL3, Reset Vector Base Address Register (if EL3 implemented) |  |  |  |  |  |
| D13.2.115 MRS <Xt>,SCR\_EL3, Secure Configuration Register |  |  |  |  |  |
| D13.2.116 MRS <Xt>,SCTLR\_EL1, System Control Register (EL1) |  |  |  |  |  |
| D13.2.116 MRS <Xt>,SCTLR\_EL12, System Control Register (EL1) |  |  |  |  |  |
| D13.2.116 MSR SCTLR\_EL1,<Xt> System Control Register (EL1) |  |  |  |  |  |
| D13.2.116 MSR SCTLR\_EL12,<Xt> System Control Register (EL1) |  |  |  |  |  |
| D13.2.117 MRS <Xt>,SCTLR\_EL2, System Control Register (EL2) |  |  |  |  |  |
| D13.2.117 MSR SCTLR\_EL2,<Xt> System Control Register (EL2) |  |  |  |  |  |
| D13.2.118 MRS <Xt>,SCTLR\_EL3, System Control Register (EL3) |  |  |  |  |  |
| D13.2.120 MRS <Xt>,SCXTNUM\_EL1, EL1 Read/Write Software Context Number |  |  |  |  |  |
| D13.2.120 MRS <Xt>,SCXTNUM\_EL12, EL1 Read/Write Software Context Number |  |  |  |  |  |
| D13.2.120 MSR SCXTNUM\_EL1,<Xt> EL1 Read/Write Software Context Number |  |  |  |  |  |
| D13.2.120 MSR SCXTNUM\_EL12,<Xt> EL1 Read/Write Software Context Number |  |  |  |  |  |
| D13.2.121 MRS <Xt>,SCXTNUM\_EL2, EL2 Read/Write Software Context Number |  |  |  |  |  |
| D13.2.121 MSR SCXTNUM\_EL2,<Xt> EL2 Read/Write Software Context Number |  |  |  |  |  |
| D13.2.122 MRS <Xt>,SCXTNUM\_EL3, EL3 Read/Write Software Context Number |  |  |  |  |  |
| D13.2.122 MRS <Xt>,SCXTNUM\_EL3, EL3 Read/Write Software Context Number |  |  |  |  |  |
| D13.2.123 MRS <Xt>,TCR\_EL1, Translation Control Register (EL1) |  |  |  |  |  |
| D13.2.123 MRS <Xt>,TCR\_EL12, Translation Control Register (EL1) |  |  |  |  |  |
| D13.2.123 MSR TCR\_EL1,<Xt> Translation Control Register (EL1) |  |  |  |  |  |
| D13.2.123 MSR TCR\_EL12,<Xt> Translation Control Register (EL1) |  |  |  |  |  |
| D13.2.124 MRS <Xt>,TCR\_EL2, Translation Control Register (EL2) |  |  |  |  |  |
| D13.2.124 MSR TCR\_EL2,<Xt> Translation Control Register (EL2) |  |  |  |  |  |
| D13.2.125 MRS <Xt>,TCR\_EL3, Translation Control Register (EL3) |  |  |  |  |  |
| D13.2.126 MRS <Xt>,TFSRE0\_EL1, Tag Fault Status Register (EL0). |  |  |  |  |  |
| D13.2.126 MSR TFSRE0\_EL1,<Xt> Tag Fault Status Register (EL0). |  |  |  |  |  |
| D13.2.127 MRS <Xt>,TFSR\_EL1, Tag Fault Status Register (EL1) |  |  |  |  |  |
| D13.2.127 MRS <Xt>,TFSR\_EL12, Tag Fault Status Register (EL1) |  |  |  |  |  |
| D13.2.127 MSR TFSR\_EL1,<Xt> Tag Fault Status Register (EL1) |  |  |  |  |  |
| D13.2.127 MSR TFSR\_EL12,<Xt> Tag Fault Status Register (EL1) |  |  |  |  |  |
| D13.2.128 MRS <Xt>,TFSR\_EL2, Tag Fault Status Register (EL2) |  |  |  |  |  |
| D13.2.128 MSR TFSR\_EL2,<Xt> Tag Fault Status Register (EL2) |  |  |  |  |  |
| D13.2.129 MRS <Xt>,TFSR\_EL3, Tag Fault Status Register (EL3) |  |  |  |  |  |
| D13.2.131 MRS <Xt>,TPIDR\_EL1, EL1 Software Thread ID Register |  |  |  |  |  |
| D13.2.131 MSR TPIDR\_EL1,<Xt> EL1 Software Thread ID Register |  |  |  |  |  |
| D13.2.132 MRS <Xt>,TPIDR\_EL2, EL2 Software Thread ID Register |  |  |  |  |  |
| D13.2.132 MSR TPIDR\_EL2,<Xt> EL2 Software Thread ID Register |  |  |  |  |  |
| D13.2.133 MRS <Xt>,TPIDR\_EL3, EL3 Software Thread ID Register |  |  |  |  |  |
| D13.2.134 MSR TPIDRRO\_EL0,<Xt> EL0 Read-Only Software Thread ID Register |  |  |  |  |  |
| D13.2.135 MRS <Xt>,TTBR0\_EL1, Translation Table Base Register 0 (EL1) |  |  |  |  |  |
| D13.2.135 MRS <Xt>,TTBR0\_EL12, Translation Table Base Register 0 (EL1) |  |  |  |  |  |
| D13.2.135 MSR TTBR0\_EL1,<Xt> Translation Table Base Register 0 (EL1) |  |  |  |  |  |
| D13.2.135 MSR TTBR0\_EL12,<Xt> Translation Table Base Register 0 (EL1) |  |  |  |  |  |
| D13.2.136 MRS <Xt>,TTBR0\_EL2, Translation Table Base Register 0 (EL2) |  |  |  |  |  |
| D13.2.136 MSR TTBR0\_EL2,<Xt> Translation Table Base Register 0 (EL2) |  |  |  |  |  |
| D13.2.137 MRS <Xt>,TTBR0\_EL3, Translation Table Base Register 0 (EL3) |  |  |  |  |  |
| D13.2.138 MRS <Xt>,TTBR1\_EL1, Translation Table Base Register 1 (EL1) |  |  |  |  |  |
| D13.2.138 MRS <Xt>,TTBR1\_EL12, Translation Table Base Register 1 (EL1) |  |  |  |  |  |
| D13.2.138 MSR TTBR1\_EL1,<Xt> Translation Table Base Register 1 (EL1) |  |  |  |  |  |
| D13.2.138 MSR TTBR1\_EL12,<Xt> Translation Table Base Register 1 (EL1) |  |  |  |  |  |
| D13.2.139 MRS <Xt>,TTBR1\_EL2, Translation Table Base Register 1 (EL2) |  |  |  |  |  |
| D13.2.139 MSR TTBR1\_EL2,<Xt> Translation Table Base Register 1 (EL2) |  |  |  |  |  |
| D13.2.140 MRS <Xt>,VBAR\_EL1, Vector Base Address Register (EL1) |  |  |  |  |  |
| D13.2.140 MRS <Xt>,VBAR\_EL12, Vector Base Address Register (EL1) |  |  |  |  |  |
| D13.2.140 MSR VBAR\_EL1,<Xt> Vector Base Address Register (EL1) |  |  |  |  |  |
| D13.2.140 MSR VBAR\_EL12,<Xt> Vector Base Address Register (EL1) |  |  |  |  |  |
| D13.2.141 MRS <Xt>,VBAR\_EL2, Vector Base Address Register (EL2) |  |  |  |  |  |
| D13.2.141 MSR VBAR\_EL2,<Xt> Vector Base Address Register (EL2) |  |  |  |  |  |
| D13.2.142 MRS <Xt>,VBAR\_EL3, Vector Base Address Register (EL3) |  |  |  |  |  |
| D13.2.143 MSR VMPIDR\_EL2,<Xt> Virtualization Multiprocessor ID Register |  |  |  |  |  |
| D13.2.144 MRS <Xt>,VNCR\_EL2, Virtual Nested Control Register |  |  |  |  |  |
| D13.2.144 MSR VNCR\_EL2,<Xt> Virtual Nested Control Register |  |  |  |  |  |
| D13.2.145 MRS <Xt>,VPIDR\_EL2, Virtualization Processor ID Register |  |  |  |  |  |
| D13.2.145 MSR VPIDR\_EL2,<Xt> Virtualization Processor ID Register |  |  |  |  |  |
| D13.2.146 MRS <Xt>,VSTCR\_EL2, Virtualization Secure Translation Control Register |  |  |  |  |  |
| D13.2.146 MSR VSTCR\_EL2,<Xt> Virtualization Secure Translation Control Register |  |  |  |  |  |
| D13.2.147 MRS <Xt>,VSTTBR\_EL2, Virtualization Secure Translation Table Base Register |  |  |  |  |  |
| D13.2.147 MSR VSTTBR\_EL2,<Xt> Virtualization Secure Translation Table Base Register |  |  |  |  |  |
| D13.2.148 MRS <Xt>,VTCR\_EL2, Virtualization Translation Control Register |  |  |  |  |  |
| D13.2.148 MSR VTCR\_EL2,<Xt> Virtualization Translation Control Register |  |  |  |  |  |
| D13.2.149 MRS <Xt>,VTTBR\_EL2, Virtualization Translation Table Base Register |  |  |  |  |  |
| D13.2.149 MSR VTTBR\_EL2,<Xt> Virtualization Translation Table Base Register |  |  |  |  |  |
| D13.3.1 MRS <Xt>,DBGAUTHSTATUS\_EL1, Debug Authentication Status register |  |  |  |  |  |
| D13.3.2 MRS <Xt>,DBGBCR<n>\_EL1, n = 0 - 15 |  |  |  |  |  |
| D13.3.2 MSR DBGBCR<n>\_EL1,<Xt> n = 0 - 15 |  |  |  |  |  |
| D13.3.3 MSR DBGBVR<n>\_EL1,<Xt> n = 0 - 15 |  |  |  |  |  |
| D13.3.4 MRS <Xt>,DBGCLAIMCLR\_EL1, Debug CLAIM Tag Clear register |  |  |  |  |  |
| D13.3.4 MSR DBGCLAIMCLR\_EL1,<Xt> Debug CLAIM Tag Clear register |  |  |  |  |  |
| D13.3.5 MRS <Xt>,DBGCLAIMSET\_EL1, Debug CLAIM Tag Set register |  |  |  |  |  |
| D13.3.5 MSR DBGCLAIMSET\_EL1,<Xt> Debug CLAIM Tag Set register |  |  |  |  |  |
| D13.3.9 MRS <Xt>,DBGPRCR\_EL1, Debug Power Control Register |  |  |  |  |  |
| D13.3.9 MSR DBGPRCR\_EL1,<Xt> Debug Power Control Register |  |  |  |  |  |
| D13.3.10 MRS <Xt>,DBGVCR32\_EL2, Debug Vector Catch Register |  |  |  |  |  |
| D13.3.10 MSR DBGVCR32\_EL2,<Xt> Debug Vector Catch Register |  |  |  |  |  |
| D13.3.11 MRS <Xt>,DBGWCR<n>\_EL1, n = 0 - 15 |  |  |  |  |  |
| D13.3.11 MSR DBGWCR<n>\_EL1,<Xt> n = 0 - 15 |  |  |  |  |  |
| D13.3.12 MRS <Xt>,DBGWVR<n>\_EL1, n = 0 - 15 |  |  |  |  |  |
| D13.3.12 MSR DBGWVR<n>\_EL1,<Xt> n = 0 - 15 |  |  |  |  |  |
| D13.3.15 MRS <Xt>,MDCCINT\_EL1, Monitor DCC Interrupt Enable Register |  |  |  |  |  |
| D13.3.15 MSR MDCCINT\_EL1,<Xt> Monitor DCC Interrupt Enable Register |  |  |  |  |  |
| D13.3.17 MRS <Xt>,MDCR\_EL2, Monitor Debug Configuration Register (EL2) |  |  |  |  |  |
| D13.3.17 MSR MDCR\_EL2,<Xt> Monitor Debug Configuration Register (EL2) |  |  |  |  |  |
| D13.3.18 MRS <Xt>,MDCR\_EL3, Monitor Debug Configuration Register (EL3) |  |  |  |  |  |
| D13.3.18 MRS <Xt>,MDCR\_EL3, Monitor Debug Configuration Register (EL3) |  |  |  |  |  |
| D13.3.19 MRS <Xt>,MDRAR\_EL1, Monitor Debug ROM Address Register |  |  |  |  |  |
| D13.3.20 MRS <Xt>,MDSCR\_EL1, Monitor Debug System Control Register |  |  |  |  |  |
| D13.3.20 MSR MDSCR\_EL1,<Xt> Monitor Debug System Control Register |  |  |  |  |  |
| D13.3.21 MRS <Xt>,OSDLR\_EL1, OS Double Lock Register |  |  |  |  |  |
| D13.3.21 MSR OSDLR\_EL1,<Xt> OS Double Lock Register |  |  |  |  |  |
| D13.3.22 MRS <Xt>,OSDTRRX\_EL1, Receive |  |  |  |  |  |
| D13.3.22 MSR OSDTRRX\_EL1,<Xt> Receive |  |  |  |  |  |
| D13.3.23 MRS <Xt>,OSDTRTX\_EL1, Transmit |  |  |  |  |  |
| D13.3.23 MSR OSDTRTX\_EL1,<Xt> Transmit |  |  |  |  |  |
| D13.3.24 MRS <Xt>,OSECCR\_EL1, OS Lock Exception Catch Control Register |  |  |  |  |  |
| D13.3.24 MSR OSECCR\_EL1,<Xt> OS Lock Exception Catch Control Register |  |  |  |  |  |
| D13.3.25 MSR OSLAR\_EL1,<Xt> OS Lock Access Register |  |  |  |  |  |
| D13.3.26 MRS <Xt>,OSLSR\_EL1, OS Lock Status Register |  |  |  |  |  |
| D13.3.27 MRS <Xt>,SDER32\_EL2, AArch32 Secure Debug Enable Register |  |  |  |  |  |
| D13.3.27 MSR SDER32\_EL2,<Xt> AArch32 Secure Debug Enable Register |  |  |  |  |  |
| D13.3.28 MRS <Xt>,SDER32\_EL3, AArch32 Secure Debug Enable Register |  |  |  |  |  |
| D13.3.28 MRS <Xt>,SDER32\_EL3, AArch32 Secure Debug Enable Register |  |  |  |  |  |
| D13.3.29 MRS <Xt>,TRFCR\_EL1, Trace Filter Control Register (EL1) |  |  |  |  |  |
| D13.3.29 MRS <Xt>,TRFCR\_EL12, Trace Filter Control Register (EL1) |  |  |  |  |  |
| D13.3.29 MSR TRFCR\_EL1,<Xt> Trace Filter Control Register (EL1) |  |  |  |  |  |
| D13.3.29 MSR TRFCR\_EL12,<Xt> Trace Filter Control Register (EL1) |  |  |  |  |  |
| D13.3.30 MRS <Xt>,TRFCR\_EL2, Trace Filter Control Register (EL2) |  |  |  |  |  |
| D13.3.30 MSR TRFCR\_EL2,<Xt> Trace Filter Control Register (EL2) |  |  |  |  |  |
| D13.4.10 MRS <Xt>,PMINTENCLR\_EL1, Performance M onitors Interrupt Enable Clear register |  |  |  |  |  |
| D13.4.10 MSR PMINTENCLR\_EL1,<Xt> Performance M onitors Interrupt Enable Clear register |  |  |  |  |  |
| D13.4.11 MRS <Xt>,PMINTENSET\_EL1, Performance Monitors Interrupt Enable Set register |  |  |  |  |  |
| D13.4.11 MSR PMINTENSET\_EL1,<Xt> Performance Monitors Interrupt Enable Set register |  |  |  |  |  |
| D13.4.12 MRS <Xt>,PMMIR\_EL1, Performance Monitors Machine Identification Register |  |  |  |  |  |
| D13.4.17 MSR PMUSERENR\_EL0,<Xt> Performance Monitors User Enable Register |  |  |  |  |  |
| D13.5.11 MRS <Xt>,AMEVCNTVOFF0<n>\_EL2, n = 0 - 15 |  |  |  |  |  |
| D13.5.11 MSR AMEVCNTVOFF0<n>\_EL2,<Xt> n = 0 - 15 |  |  |  |  |  |
| D13.5.12 MRS <Xt>,AMEVCNTVOFF1<n>\_EL2, n = 0 - 15 |  |  |  |  |  |
| D13.5.12 MSR AMEVCNTVOFF1<n>\_EL2,<Xt> n = 0 - 15 |  |  |  |  |  |
| D13.5.15 MSR AMUSERENR\_EL0,<Xt> Activity Monitors User Enable Register |  |  |  |  |  |
| D13.6.1 MRS <Xt>,PMBIDR\_EL1, Profiling Buffer ID Register |  |  |  |  |  |
| D13.6.2 MRS <Xt>,PMBLIMITR\_EL1, Profiling Buffer Limit Address Register |  |  |  |  |  |
| D13.6.2 MSR PMBLIMITR\_EL1,<Xt> Profiling Buffer Limit Address Register |  |  |  |  |  |
| D13.6.3 MRS <Xt>,PMBPTR\_EL1, Profiling Buffer Write Pointer Register |  |  |  |  |  |
| D13.6.3 MSR PMBPTR\_EL1,<Xt> Profiling Buffer Write Pointer Register |  |  |  |  |  |
| D13.6.4 MRS <Xt>,PMBSR\_EL1, Profiling Buffer Status/syndrome Register |  |  |  |  |  |
| D13.6.4 MSR PMBSR\_EL1,<Xt> Profiling Buffer Status/syndrome Register |  |  |  |  |  |
| D13.6.5 MRS <Xt>,PMSCR\_EL1, Statistical Profiling Control Register (EL1) |  |  |  |  |  |
| D13.6.5 MRS <Xt>,PMSCR\_EL12, Statistical Profiling Control Register (EL1) |  |  |  |  |  |
| D13.6.5 MSR PMSCR\_EL1,<Xt> Statistical Profiling Control Register (EL1) |  |  |  |  |  |
| D13.6.5 MSR PMSCR\_EL12,<Xt> Statistical Profiling Control Register (EL1) |  |  |  |  |  |
| D13.6.6 MRS <Xt>,PMSCR\_EL2, Statistical Profiling Control Register (EL2) |  |  |  |  |  |
| D13.6.6 MSR PMSCR\_EL2,<Xt> Statistical Profiling Control Register (EL2) |  |  |  |  |  |
| D13.6.7 MRS <Xt>,PMSEVFR\_EL1, Sampling Event Filter Register |  |  |  |  |  |
| D13.6.7 MSR PMSEVFR\_EL1,<Xt> Sampling Event Filter Register |  |  |  |  |  |
| D13.6.8 MRS <Xt>,PMSFCR\_EL1, Sampling Filter Control Register |  |  |  |  |  |
| D13.6.8 MSR PMSFCR\_EL1,<Xt> Sampling Filter Control Register |  |  |  |  |  |
| D13.6.9 MRS <Xt>,PMSICR\_EL1, Sampling Interval Counter Register |  |  |  |  |  |
| D13.6.9 MSR PMSICR\_EL1,<Xt> Sampling Interval Counter Register |  |  |  |  |  |
| D13.6.10 MRS <Xt>,PMSIDR\_EL1, Sampling Profiling ID Register |  |  |  |  |  |
| D13.6.11 MRS <Xt>,PMSIRR\_EL1, Sampling Interval Reload Register |  |  |  |  |  |
| D13.6.11 MSR PMSIRR\_EL1,<Xt> Sampling Interval Reload Register |  |  |  |  |  |
| D13.6.12 MRS <Xt>,PMSLATFR\_EL1, Sampling Latency Filter Register |  |  |  |  |  |
| D13.6.12 MSR PMSLATFR\_EL1,<Xt> Sampling Latency Filter Register |  |  |  |  |  |
| D13.6.13 MRS <Xt>,PMSNEVFR\_EL1, Sampling Inverted Event Filter Register |  |  |  |  |  |
| D13.6.13 MSR PMSNEVFR\_EL1,<Xt> Sampling Inverted Event Filter Register |  |  |  |  |  |
| D13.7.1 MRS <Xt>,DISR\_EL1, Deferred Interrupt Status Register |  |  |  |  |  |
| D13.7.1 MSR DISR\_EL1,<Xt> Deferred Interrupt Status Register |  |  |  |  |  |
| D13.7.2 MRS <Xt>,ERRIDR\_EL1, Error Record ID Register |  |  |  |  |  |
| D13.7.3 MRS <Xt>,ERRSELR\_EL1, Error Record Select Register |  |  |  |  |  |
| D13.7.3 MSR ERRSELR\_EL1,<Xt> Error Record Select Register |  |  |  |  |  |
| D13.7.4 MRS <Xt>,ERXADDR\_EL1, Selected Error Record Address Register |  |  |  |  |  |
| D13.7.4 MSR ERXADDR\_EL1,<Xt> Selected Error Record Address Register |  |  |  |  |  |
| D13.7.5 MRS <Xt>,ERXCTLR\_EL1, Selected Error Record Control Register |  |  |  |  |  |
| D13.7.5 MSR ERXCTLR\_EL1,<Xt> Selected Error Record Control Register |  |  |  |  |  |
| D13.7.6 MRS <Xt>,ERXFR\_EL1, Selected Error Record Feature Register |  |  |  |  |  |
| D13.7.7 MRS <Xt>,ERXMISC0\_EL1, Selected Error Record Miscellaneous Register 0 |  |  |  |  |  |
| D13.7.7 MSR ERXMISC0\_EL1,<Xt> Selected Error Record Miscellaneous Register 0 |  |  |  |  |  |
| D13.7.8 MRS <Xt>,ERXMISC1\_EL1, Selected Error Record Miscellaneous Register 1 |  |  |  |  |  |
| D13.7.8 MSR ERXMISC1\_EL1,<Xt> Selected Error Record Miscellaneous Register 1 |  |  |  |  |  |
| D13.7.9 MRS <Xt>,ERXMISC2\_EL1, Selected Error Record Miscellaneous Register 2 |  |  |  |  |  |
| D13.7.9 MSR ERXMISC2\_EL1,<Xt> Selected Error Record Miscellaneous Register 2 |  |  |  |  |  |
| D13.7.10 MRS <Xt>,ERXMISC3\_EL1, Selected Error Record Miscellaneous Register 3 |  |  |  |  |  |
| D13.7.10 MSR ERXMISC3\_EL1,<Xt> Selected Error Record Miscellaneous Register 3 |  |  |  |  |  |
| D13.7.11 MRS <Xt>,ERXPFGCDN\_EL1, Selected Pseudo-fault Generation Countdown register |  |  |  |  |  |
| D13.7.11 MSR ERXPFGCDN\_EL1,<Xt> Selected Pseudo-fault Generation Countdown register |  |  |  |  |  |
| D13.7.12 MRS <Xt>,ERXPFGCTL\_EL1, Selected Pseudo-fault Generation Control register |  |  |  |  |  |
| D13.7.12 MSR ERXPFGCTL\_EL1,<Xt> Selected Pseudo-fault Generation Control register |  |  |  |  |  |
| D13.7.13 MRS <Xt>,ERXPFGF\_EL1, Selected Pseudo-fault Generation Feature register |  |  |  |  |  |
| D13.7.14 MRS <Xt>,ERXSTATUS\_EL1, Selected Error Record Primary Status Register |  |  |  |  |  |
| D13.7.14 MSR ERXSTATUS\_EL1,<Xt> Selected Error Record Primary Status Register |  |  |  |  |  |
| D13.7.15 MRS <Xt>,VDISR\_EL2, Virtual Deferred Interrupt Status Register |  |  |  |  |  |
| D13.7.15 MSR VDISR\_EL2,<Xt> Virtual Deferred Interrupt Status Register |  |  |  |  |  |
| D13.7.16 MRS <Xt>,VSESR\_EL2, Virtual SError Exception Syndrome Register |  |  |  |  |  |
| D13.7.16 MSR VSESR\_EL2,<Xt> Virtual SError Exception Syndrome Register |  |  |  |  |  |
| D13.8.2 MRS <Xt>,CNTHCTL\_EL2, Counter-timer Hypervisor Control register |  |  |  |  |  |
| D13.8.2 MSR CNTHCTL\_EL2,<Xt> Counter-timer Hypervisor Control register |  |  |  |  |  |
| D13.8.3 MRS <Xt>,CNTHP\_CTL\_EL2, Counter-timer Hypervisor Physical Timer Control register |  |  |  |  |  |
| D13.8.3 MSR CNTHP\_CTL\_EL2,<Xt> Counter-timer Hypervisor Physical Timer Control register |  |  |  |  |  |
| D13.8.4 MRS <Xt>,CNTHP\_CVAL\_EL2, Counter-timer Physical Timer CompareValue register (EL2) |  |  |  |  |  |
| D13.8.4 MSR CNTHP\_CVAL\_EL2,<Xt> Counter-timer Physical Timer CompareValue register (EL2) |  |  |  |  |  |
| D13.8.5 MRS <Xt>,CNTHP\_TVAL\_EL2, Counter-timer Ph ysical Timer TimerValue register (EL2) |  |  |  |  |  |
| D13.8.5 MSR CNTHP\_TVAL\_EL2,<Xt> Counter-timer Ph ysical Timer TimerValue register (EL2) |  |  |  |  |  |
| D13.8.6 MRS <Xt>,CNTHPS\_CTL\_EL2, Counter-timer Secure Physical Timer Control register (EL2) |  |  |  |  |  |
| D13.8.6 MSR CNTHPS\_CTL\_EL2,<Xt> Counter-timer Secure Physical Timer Control register (EL2) |  |  |  |  |  |
| D13.8.7 MRS <Xt>,CNTHPS\_CVAL\_EL2, Counter-timer Secure Physical Timer CompareValue register (EL2) | |  |  |  |  |
| D13.8.7 MSR CNTHPS\_CVAL\_EL2,<Xt> Counter-timer Secure Physical Timer CompareValue register (EL2) | |  |  |  |  |
| D13.8.8 MRS <Xt>,CNTHPS\_TVAL\_EL2, Counter-timer Secure Physical Timer TimerValue register (EL2) | |  |  |  |  |
| D13.8.8 MSR CNTHPS\_TVAL\_EL2,<Xt> Counter-timer Secure Physical Timer TimerValue register (EL2) | |  |  |  |  |
| D13.8.9 MRS <Xt>,CNTHV\_CTL\_EL2, Counter-timer Virtual Timer Control register (EL2) |  |  |  |  |  |
| D13.8.9 MSR CNTHV\_CTL\_EL2,<Xt> Counter-timer Virtual Timer Control register (EL2) |  |  |  |  |  |
| D13.8.10 MRS <Xt>,CNTHV\_CVAL\_EL2, Counter-timer Vi rtual Timer CompareValue register (EL2) |  |  |  |  |  |
| D13.8.10 MSR CNTHV\_CVAL\_EL2,<Xt> Counter-timer Vi rtual Timer CompareValue register (EL2) |  |  |  |  |  |
| D13.8.11 MRS <Xt>,CNTHV\_TVAL\_EL2, Counter-timer Virtual Timer TimerValue Register (EL2) |  |  |  |  |  |
| D13.8.11 MSR CNTHV\_TVAL\_EL2,<Xt> Counter-timer Virtual Timer TimerValue Register (EL2) |  |  |  |  |  |
| D13.8.12 MRS <Xt>,CNTHVS\_CTL\_EL2, Counter-timer Secure Virtual Timer Control register (EL2) |  |  |  |  |  |
| D13.8.12 MSR CNTHVS\_CTL\_EL2,<Xt> Counter-timer Secure Virtual Timer Control register (EL2) |  |  |  |  |  |
| D13.8.13 MRS <Xt>,CNTHVS\_CVAL\_EL2, Counter-timer Secure Virtual Timer CompareValue register (EL2) | |  |  |  |  |
| D13.8.13 MSR CNTHVS\_CVAL\_EL2,<Xt> Counter-timer Secure Virtual Timer CompareValue register (EL2) | |  |  |  |  |
| D13.8.14 MRS <Xt>,CNTHVS\_TVAL\_EL2, Counter-timer Secu re Virtual Timer TimerValue register (EL2) |  |  |  |  |  |
| D13.8.14 MSR CNTHVS\_TVAL\_EL2,<Xt> Counter-timer Secu re Virtual Timer TimerValue register (EL2) |  |  |  |  |  |
| D13.8.15 MRS <Xt>,CNTKCTL\_EL1, Counter-timer Kernel Control register |  |  |  |  |  |
| D13.8.15 MRS <Xt>,CNTKCTL\_EL12, Counter-timer Kernel Control register |  |  |  |  |  |
| D13.8.15 MSR CNTKCTL\_EL1,<Xt> Counter-timer Kernel Control register |  |  |  |  |  |
| D13.8.15 MSR CNTKCTL\_EL12,<Xt> Counter-timer Kernel Control register |  |  |  |  |  |
| D13.8.16 MRS <Xt>,CNTP\_CTL\_EL02, Counter-timer Physical Timer Control register |  |  |  |  |  |
| D13.8.16 MSR CNTP\_CTL\_EL02,<Xt> Counter-timer Physical Timer Control register |  |  |  |  |  |
| D13.8.17 MRS <Xt>,CNTP\_CVAL\_EL02, Counter-timer Physical Timer CompareValue register |  |  |  |  |  |
| D13.8.17 MSR CNTP\_CVAL\_EL02,<Xt> Counter-timer Physical Timer CompareValue register |  |  |  |  |  |
| D13.8.18 MRS <Xt>,CNTP\_TVAL\_EL02, Counter-timer Physical Timer TimerValue register |  |  |  |  |  |
| D13.8.18 MSR CNTP\_TVAL\_EL02,<Xt> Counter-timer Physical Timer TimerValue register |  |  |  |  |  |
| D13.8.21 MRS <Xt>,CNTPS\_CTL\_EL1, Counter-time r Physical Secure Timer Control register |  |  |  |  |  |
| D13.8.21 MSR CNTPS\_CTL\_EL1,<Xt> Counter-time r Physical Secure Timer Control register |  |  |  |  |  |
| D13.8.22 MRS <Xt>,CNTPOFF\_EL2, Counter-timer Physical Offset register |  |  |  |  |  |
| D13.8.22 MSR CNTPOFF\_EL2,<Xt> Counter-timer Physical Offset register |  |  |  |  |  |
| D13.8.23 MRS <Xt>,CNTPS\_CVAL\_EL1, Counter-timer Physical Secure Timer CompareValue register |  |  |  |  |  |
| D13.8.23 MSR CNTPS\_CVAL\_EL1,<Xt> Counter-timer Physical Secure Timer CompareValue register |  |  |  |  |  |
| D13.8.24 MRS <Xt>,CNTPS\_TVAL\_EL1, Counter-timer Physical Secure Timer TimerValue register |  |  |  |  |  |
| D13.8.24 MSR CNTPS\_TVAL\_EL1,<Xt> Counter-timer Physical Secure Timer TimerValue register |  |  |  |  |  |
| D13.8.25 MRS <Xt>,CNTV\_CTL\_EL02, Counter-timer Virtual Timer Control register |  |  |  |  |  |
| D13.8.25 MSR CNTV\_CTL\_EL02,<Xt> Counter-timer Virtual Timer Control register |  |  |  |  |  |
| D13.8.26 MRS <Xt>,CNTV\_CVAL\_EL02, Counter-timer Virtual Timer CompareValue register |  |  |  |  |  |
| D13.8.26 MSR CNTV\_CVAL\_EL02,<Xt> Counter-timer Virtual Timer CompareValue register |  |  |  |  |  |
| D13.8.27 MRS <Xt>,CNTV\_TVAL\_EL02, Counter-timer Virtual Timer TimerValue register |  |  |  |  |  |
| D13.8.27 MSR CNTV\_TVAL\_EL02,<Xt> Counter-timer Virtual Timer TimerValue register |  |  |  |  |  |
| D13.8.30 MRS <Xt>,CNTVOFF\_EL2, Counter-timer Virtual Offset register |  |  |  |  |  |
| D13.8.30 MSR CNTVOFF\_EL2,<Xt> Counter-timer Virtual Offset register |  |  |  |  |  |

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| 有条件敏感指令-配置 | 配置 |
| C5.2.7 MRS <Xt>,FPCR, Floating-point Control Register | CPTR\_EL2.FPEN == '11' |
| C5.2.7 MSR FPCR,<Xt> Floating-point Control Register | CPTR\_EL2.FPEN == '11' |
| C5.2.8 MRS <Xt>,FPSR, Floating-point Status Register | CPTR\_EL2.FPEN == '11' |
| C5.2.8 MSR FPSR,<Xt> Floating-point Status Register | CPTR\_EL2.FPEN == '11' |
| C5.2.24 MRS <Xt>,TCO, Tag Check Override | MTE未开启，指令无定义 |
| C5.2.24 MSR TCO,<Xt> Tag Check Override | MTE未开启，指令无定义 |
| C5.3.2 DC CGDVAC, Clean of Data and Allocation Tags by VA to PoC | MTE未开启，指令无定义 |
| C5.3.3 DC CGDVADP, Clean of Data and Allocation Tags by VA to PoDP | MTE未开启，指令无定义 |
| C5.3.4 DC CGDVAP, Clean of Data and Allocation Tags by VA to PoP | MTE未开启，指令无定义 |
| C5.3.6 DC CGVAC, Clean of Allocation Tags by VA to PoC | MTE未开启，指令无定义 |
| C5.3.7 DC CGVADP, Clean of Allocation Tags by VA to PoDP | MTE未开启，指令无定义 |
| C5.3.8 DC CGVAP, Clean of Allocation Tags by VA to PoP | MTE未开启，指令无定义 |
| C5.3.10 DC CIGDVAC, Clean and Invalidate of Data and Allocation Tags by VA to PoC | MTE未开启，指令无定义 |
| C5.3.12 DC CIGVAC, Clean and Invalidate of Allocation Tags by VA to PoC | MTE未开启，指令无定义 |
| C5.3.14 DC CIVAC, Data or unified Cache line Clean and Invalidate by VA to PoC | SCTLR\_EL2.UCI == '1' |
| C5.3.16 DC CVAC, Data or unified Cache line Clean by VA to PoC | SCTLR\_EL2.UCI == '1' |
| C5.3.17 DC CVADP, Data or unified Cache line Clean by VA to PoDP | SCTLR\_EL2.UCI == '1' |
| C5.3.18 DC CVAP, Data or unified Cache line Clean by VA to PoP | SCTLR\_EL2.UCI == '1' |
| C5.3.19 DC CVAU, Data or unified Cache line Clean by VA to PoU | SCTLR\_EL2.UCI == '1' |
| C5.3.20 DC GVA, Data Cache set Allocation Tag by VA | MTE未开启，指令无定义 |
| C5.3.21 DC GZVA, Data Cache set Allocation Tags and Zero by VA | MTE未开启，指令无定义 |
| C5.3.28 DC ZVA, Data Cache Zero by VA | SCTLR\_EL2.DZE == '1' |
| C5.3.31 IC IVAU, Instruction Cache line Invalidate by VA to PoU | SCTLR\_EL2.DZE == '1' |
| C6.2.6 ADDG | MTE未开启，指令无定义 |
| C6.2.40 CASB, CASAB, CASALB, CASLB | SCTLR\_EL2.SA0 =1, SCTLR\_EL2.SA = 1,SCTLR\_EL2.E0E = 0,SCTLR\_EL2.EE = 0 |
| C6.2.41 CASH, CASAH, CASALH, CASLH | SCTLR\_EL2.SA0 =1, SCTLR\_EL2.SA = 1,SCTLR\_EL2.E0E = 0,SCTLR\_EL2.EE = 0 |
| C6.2.42 CASP, CASPA, CASPAL, CASPL | SCTLR\_EL2.SA0 =1, SCTLR\_EL2.SA = 1,SCTLR\_EL2.E0E = 0,SCTLR\_EL2.EE = 0 |
| C6.2.43 CAS, CASA, CASAL, CASL | SCTLR\_EL2.SA0 =1, SCTLR\_EL2.SA = 1,SCTLR\_EL2.E0E = 0,SCTLR\_EL2.EE = 0 |
| C6.2.76 DCPS1 | !halted, 指令无定义 |
| C6.2.77 DCPS2 | !halted, 指令无定义 |
| C6.2.78 DCPS3 | !halted, 指令无定义 |
| C6.2.79 DGH | DGH未开启 |
| C6.2.81 DRPS | !halted, 指令无定义 |

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| 有条件敏感指令-配置&过滤 | 配置 |
| C5.2.2 MRS <Xt>,DAIF, Interrupt Mask Bits | EL2Enabled(), HCR\_EL2.<E2H,TGE> == '11' |
| C5.2.2 MSR DAIF,<Xt> Interrupt Mask Bits | EL2Enabled(), HCR\_EL2.<E2H,TGE> == '11' |
| C5.6.1 CFP RCTX, Control Flow Prediction Restriction by Context | SCTLR\_EL2.EnRTCTX == '0' |
| C5.6.2 CPP RCTX, Cache Prefetch Prediction Restriction by Context | SCTLR\_EL2.EnRTCTX == '0' |
| C5.6.3 DVP RCTX, Data Value Prediction Restriction by Context | SCTLR\_EL2.EnRTCTX == '0' |
| D13.2.114 MRS <Xt>,S3\_<op1>\_<Cn>\_<Cm>\_<op2>, IMPLEMENTATION DEFINED registers | IMPLEMENTATION DEFINED |
| D13.2.114 MSR S3\_<op1>\_<Cn>\_<Cm>\_<op2>,<Xt> IMPLEMENTATION DEFINED registers | IMPLEMENTATION DEFINED |
| D13.2.119 MRS <Xt>,SCXTNUM\_EL0, EL0 Read/Write Software Context Number | SCTLR\_EL2.TSCXT == '1' |
| D13.2.119 MSR SCXTNUM\_EL0,<Xt> EL0 Read/Write Software Context Number | SCTLR\_EL2.TSCXT == '1' |
| D13.3.6 MSR DBGDTR\_EL0,<Xt> half-duplex | EL2Enabled(), HCR\_EL2.<E2H,TGE> == '11' |
| D13.3.6 MRS <Xt>,DBGDTR\_EL0, half-duplex | EL2Enabled(), HCR\_EL2.<E2H,TGE> == '11' |
| D13.3.7 MRS <Xt>,DBGDTRRX\_EL0, Debug Data Transfer Register, Receive | EL2Enabled(), HCR\_EL2.<E2H,TGE> == '11' |
| D13.3.8 MSR DBGDTRTX\_EL0,<Xt> Debug Data Transfer Register, Transmit | EL2Enabled(), HCR\_EL2.<E2H,TGE> == '11' |
| D13.3.13 MRS <Xt>, DLR\_EL0, Debug Link Register | !halted, 指令无定义 |
| D13.3.13 MSR DLR\_EL0,<Xt> Debug Link Register | !halted, 指令无定义 |
| D13.3.14 MRS <Xt>, DSPSR\_EL0, Debug Saved Program Status Register | !halted, 指令无定义 |
| D13.3.14 MSR DSPSR\_EL0,<Xt> Debug Saved Program Status Register | !halted, 指令无定义 |
| D13.3.16 MRS <Xt>,MDCCSR\_EL0, Monitor DCC Status Register | EL2Enabled(), HCR\_EL2.<E2H,TGE> == '11' |
| D13.8.16 MRS <Xt>,CNTP\_CTL\_EL0, Counter-timer Physical Timer Control register | CNTHCTL\_EL2.EL0PTEN == '0' |
| D13.8.16 MSR CNTP\_CTL\_EL0,<Xt> Counter-timer Physical Timer Control register | CNTHCTL\_EL2.EL0PTEN == '0' |
| D13.8.17 MRS <Xt>,CNTP\_CVAL\_EL0, Counter-timer Physical Timer CompareValue register | CNTHCTL\_EL2.EL0PTEN == '0' |
| D13.8.17 MSR CNTP\_CVAL\_EL0,<Xt> Counter-timer Physical Timer CompareValue register | CNTHCTL\_EL2.EL0PTEN == '0' |
| D13.8.18 MRS <Xt>,CNTP\_TVAL\_EL0, Counter-timer Physical Timer TimerValue register | CNTHCTL\_EL2.EL0PTEN == '0' |
| D13.8.18 MSR CNTP\_TVAL\_EL0,<Xt> Counter-timer Physical Timer TimerValue register | CNTHCTL\_EL2.EL0PTEN == '0' |
| D13.8.19 MRS <Xt>,CNTPCTSS\_EL0, Counter-timer Self-Synchronized Physical Count register | CNTHCTL\_EL2.EL0PCTEN == '0' |
| D13.8.20 MRS <Xt>,CNTPCT\_EL0, Counter-timer Physical Count register | CNTHCTL\_EL2.EL0PCTEN == '0' |
| D13.8.25 MRS <Xt>,CNTV\_CTL\_EL0, Counter-timer Virtual Timer Control register | CNTHCTL\_EL2.EL0VTEN == '0' |
| D13.8.25 MSR CNTV\_CTL\_EL0,<Xt> Counter-timer Virtual Timer Control register | CNTHCTL\_EL2.EL0VTEN == '0' |
| D13.8.26 MRS <Xt>,CNTV\_CVAL\_EL0, Counter-timer Virtual Timer CompareValue register | CNTHCTL\_EL2.EL0VTEN == '0' |
| D13.8.26 MSR CNTV\_CVAL\_EL0,<Xt> Counter-timer Virtual Timer CompareValue register | CNTHCTL\_EL2.EL0VTEN == '0' |
| D13.8.27 MRS <Xt>,CNTV\_TVAL\_EL0, Counter-timer Virtual Timer TimerValue register | CNTHCTL\_EL2.EL0VTEN == '0' |
| D13.8.27 MSR CNTV\_TVAL\_EL0,<Xt> Counter-timer Virtual Timer TimerValue register | CNTHCTL\_EL2.EL0VTEN == '0' |

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| 有条件敏感指令-配置&下陷 | 配置 |
| C6.2.350 WFI | SCTLR\_EL2.nTWI == '0' |
| D13.2.34 MRS <Xt>,CTR\_EL0, Cache Type Register | SCTLR\_EL2.UCT == '0' |
| D13.2.59 MRS <Xt>,ID\_AA64DFR0\_EL1, AArch64 Debug Feature Register 0 | FEAT\_IDST开启 |
| D13.2.61 MRS <Xt>,ID\_AA64ISAR0\_EL1, AArch64 Instruction Set Attribute Register 0 | FEAT\_IDST开启 |
| D13.2.62 MRS <Xt>,ID\_AA64ISAR1\_EL1, AArch64 Instruction Set Attribute Register 1 | FEAT\_IDST开启 |
| D13.2.64 MRS <Xt>,ID\_AA64MMFR0\_EL1, AArch64 Memory Model Feature Register 0 | FEAT\_IDST开启 |
| D13.2.65 MRS <Xt>,ID\_AA64MMFR1\_EL1, AArch64 Memory Model Feature Register 1 | FEAT\_IDST开启 |
| D13.2.66 MRS <Xt>,ID\_AA64MMFR2\_EL1, AArch64 Memory Model Feature Register 2 | FEAT\_IDST开启 |
| D13.2.67 MRS <Xt>,ID\_AA64PFR0\_EL1, AArch64 Processor Feature Register 0 | FEAT\_IDST开启 |
| D13.2.99 MRS <Xt>,MPIDR\_EL1, Multiprocessor Affinity Register | FEAT\_IDST开启 |