(1) Set RB_SPI_MODE_SLAVE in R8_SPI_CTRL_MOD to 1, to configure SPI to slave mode;

(2) Set RB_SPI_SLV_CMD_MOD in R8_SPI_CTRL_MOD as needed, to select the slave first byte mode or data stream mode;

(3) Set RB_SPI_FIFO_DIR in R8_SPI_CTRL_MOD, to configure the FIFO direction. If it is 1, FIFO is used to receive; if it is 0, FIFO is used to transmit;

(4) Set RB_SPI_MOSI_OE and RB_SPI_SCK_OE in R8_SPI0_CTRL_MOD to 0, and set RB_SPI_MISO_OE to 1, and set GPIO direction configuration register (R32_PA/PB_DIR) to make MOSI pin, SCK pin and SCS pin as input, MISO pin as input (support connect multiple slaves under the bus; MISO will automatically switch to output after chip select; one master with one slave is also supported) or output (only for connection of one master with one slave). In SPI slave mode, the I/O pin direction of MISO can be set as output by GPIO direction configuration register, it can also automatically switch to output during the period of valid SPI chip select. But its output data is selected by RB_SPI_MISO_OE, it outputs SPI data when it is 1, and it outputs data of GPIO data output register when it is 0. It is recommended to set the MISO pin as input, so that MISO does not output when chip select is invalid, so that SPI bus can be shared during multiple-device operation;

(5) In 2-wire mode, SCK is unchanged, RB_SPI_MISO_OE=0, and MOSI is not needed. In 3-wire mode, input (Rb _ SPI _ MISO _ OE = 0 and pin set as input) and output (RB_SPI_MISO_OE=1 and pin set as output) are realized by miso half-duplex, and the direction is manually switched.

(6) Optional, set the preset data register (R8_SPI_SLAVE_PRE) in SPI0 slave mode, used to be automatically loaded into the buffer for the first time after chip select for external output. After 8 clocks (that is, the first data byte is exchanged between the master and the slave), the controller will obtain the first data byte (command code) sent by the external SPI host, and the external SPI host obtains the preset data (status value) in R8_SPI_SLAVE_PRE through exchange. The bit7 of R8_SPI_SLAVE_PRE will be automatically loaded into the MISO pin during SCK low level period after the SPI chip select is valid. For SPI mode 0 (CLK is at low level by default), if the bit7 of R8_SPI_SLAVE_PRE is preset, the external SPI host will obtain the preset value of bit7 of R8_SPI_SLAVE_PRE by inquiring the MISO pin when the SPI chip select is valid but has no data transmission, thereby the value of bit7 of R8_SPI_SLAVE_PRE can be obtained only by a valid SPI chip select (Usually a busy status is provided for the host, so that the host can quickly query);

(7) Optional. If DMA is enabled, it is needed to write the start address of transceiver buffer to R16_SPI_DMA_BEG and write the end address (not included) to R16_SPI_DMA_END. It is recommended to set RB_SPI_DMA_ENABLE after setting RB_SPI_FIFO_DIR.

Data transmission:

(1) Set RB_SPI_FIFO_DIR in R8_SPI_CTRL_MOD to 0, and the current FIFO direction as output;

(2) Optional step. If DMA is enabled, it is needed to set RB_SPI_DMA_ENABLE to 1 to enable DMA function;

(3) Write multiple transmission data into FIFO register R8_SPI_FIFO, and the external host determines when to take it away. If DMA is enabled, DMA will automatically load FIFO to complete this step;

(4) Query R8_SPI_FIFO_COUNT, if it is not full, continue to write data to be sent to FIFO.