Chapter 10 Serial Peripheral Interface (SPI)

10.1 Introduction to SPI

SPI is a full-duplex serial interface with a host and several slaves connected to the bus, and only a pair of host and slave is communicating at the same time. Usually, SPI interface consists of 4 pins: SPI chip selected pin SCS, SPI clock pin (SCK), SPI serial data pin MISO (master input/slave output pin) and SPI serial data pin MOSI (master output/slave input pin).

10.1.1 Main Features

The CH572 and CH570 chip provides 1 SPI interface with the following characteristics:

- Support both master mode and slave mode.
- Compatible with Serial Peripheral Interface (SPI) specification.
- Data transfer modes: mode0 and mode3.
- 8-bit data transmission mode, optional data bit sequence: low bits of a byte are in front or high bits are in front.
- Clock frequency can be up to half of the system clock frequency (Fsys).
- 8-byte FIFO.
- Slave mode supports the first byte as command mode or data stream mode.
- Support DMA, so the data transmission efficiency is higher.

10.2 Register Description

Table 10-1 SPI registers

Name	Access address	Description	Reset value
R8_SPI_CTRL_MOD	0x40004000	SPI0 mode control register	0x02
R8_SPI_CTRL_CFG	0x40004001	SPI0 configuration register	0x00
R8_SPI_INTER_EN	0x40004002	SPI0 interrupt enable register	0x00
R8_SPI_CLOCK_DIV R8_SPI_SLAVE_PRE	0x40004003	SPI0 clock divider register in master mode SPI0 preset data register in slave mode	0x10
R8_SPI_BUFFER	0x40004004	SPI0 data buffer	0xXX
R8_SPI_RUN_FLAG	0x40004005	SPI0 working status register	0x00
R8_SPI_INT_FLAG	0x40004006	SPI0 interrupt flag register	0x40
R8_SPI_FIFO_COUNT	0x40004007	SPI0 transceiver FIFO count register	0x00
R8_SPI_INT_TYPE	0x40004008	SPI interrupt trigger mode selection register	0x00
R8_SPI_INTER1_EN	0x40004009	SPI interrupt 1 enable register	0x00
R8_SPI_INT1_FLAG	0x4000400A	SPI interrupt 1 flag register	0x00
R16_SPI_TOTAL_CNT	0x4000400C	SPI0 transceiver data total length register	0x0000
R8_SPI_FIFO	0x40004010	SPI0 data FIFO register	0xXX
R8_SPI_FIFO_COUNT1	0x40004013	SPI0 transceiver FIFO count register	0x00
R16_SPI_DMA_NOW	0x40004014	SPI0 DMA buffer current address	0xXXXX
R16_SPI_DMA_BEG	0x40004018	SPI0 DMA buffer start address	0xXXXX