6	RB_SPI_MST_DLY_EN	RW	Input delay enable in master mode: 1: Enable, used for high-speed applications such as SPI clock close to half of Fsys; 0: Disable, regular applications.	0
5	RB_SPI_BIT_ORDER	RW	SPI data bit order selection: 1: LSB first, 0: MSB first.	0
4	RB_SPI_AUTO_IF	RW	Enable the function of automatically clearing flag bit RB_SPI_IF_BYTE_END when accessing BUFFER/FIFO: 1: Enable; 0: Disable.	0
3	Reserved	RO	Reserved	0
2	RB_SPI_DMA_LOOP	RW	DMA address loop enable: 1: Enable address loop; 0: Disable address loop. If the DMA address loop is enabled, when the DMA address is added to the set end address, the auto loop points to the set first address.	0
1	RB_MST_CLK_SEL	RW	RB_SPI_MODE_SLAVE = 0 for main clock polarity selection: 1: polarity reversed; 0: polarity unchanged. RB_SPI_MODE_SLAVE = 1 is the two-wire mode slave input and output direction selection: 1: Slave input; 0: slave output.	0
0	RB_SPI_DMA_ENABLE	RW	DMA enable (only supported by SPI0): 1: Enable; 0: Disable.	0

SPI Interrupt Enable Register (R8_SPI_INTER_EN)

Bit	Name	Access	Description	Reset value
7	RB_SPI_IE_FST_BYTE	RW	In the first byte command mode of slave mode, first byte interrupt receive enable: 1: Enable receiving the first byte interrupt; 0: Disable receiving the first byte interrupt.	0
[6:5]	Reserved	RO	Reserved	00b
4	RB_SPI_IE_FIFO_OV	RW	FIFO overflow (FIFO is full when receiving, or FIFO is empty when transmitting) interrupt enable: 1: Interrupt enabled; 0: Interrupt disabled.	0
3	RB_SPI_IE_DMA_END	RW	DMA end interrupt enable: 1: Interrupt enabled; 0: Interrupt disabled.	0
2	RB_SPI_IE_FIFO_HF	RW	More than half of FIFO used interrupt enable:	0