			slave mode, that is, completing the exchange of first byte data: 1: That has just been exchanged is the first byte; 0: The first byte has not been exchanged or it is not the first byte.	
[3:0]	Reserved	RO	Reserved	0000b

SPI Interrupt Flag Register (R8_SPI_INT_FLAG)

Bit	Name	Access	Description	Reset value
7	RB_SPI_IF_FST_BYTE	RW1	First byte received flag in slave mode: 1: The first byte has been received; 0: The first byte is not received.	0
6	RB_SPI_FREE	RO	Current SPI free: 1: Free; 0: Not free.	1
5	Reserved	RO	Reserved	0
4	RB_SPI_IF_FIFO_OV	RW1	FIFO overflow (FIFO is full when receiving or FIFO is empty when transmitting) flag. Write 1 to reset: 1: Overflow; 0: Not overflow.	0
3	RB_SPI_IF_DMA_END	RW1	DMA end flag. Write 1 to reset: 1: End; 0: Not end.	0
2	RB_SPI_IF_FIFO_HF	RW1	More than half of FIFO used (FIFO>=4 when receiving or FIFO<4 when transmitting) flag. Write 1 to reset: 1: More than half of FIFO has been used; 0: FIFO has been used not more than half.	0
1	RB_SPI_IF_BYTE_END	RW1	SPI single byte transfer end flag. Write 1 to reset: 1: End; 0: Not end.	0
0	RB_SPI_IF_CNT_END	RW1	SPI all byte transfer end flag. Write 1 to reset: 1: All byte transfer ends; 0: All byte transfer not end.	0

SPI Transceiver FIFO Count Register (R8_SPIx_FIFO_COUNT)

Bit	Name	Access	Description	Reset value
[7:4]	Reserved	RO	Reserved	0h
[3:0]	R8_SPI_FIFO_COUNT	RW	Current byte count in FIFO.	0h