SPI Interrupt 1 Enable Register (R8_SPI_INTER1_EN)

Bit	Name	Access	Description	Reset value
[7:2]	Reserved	RO	Reserved	0
1	RB_SPI_IE_FIFO_FULL	RW	Current FIFO data full interrupt enable: 1: Turn on enable; 0: Turn off enable.	0
0	RB_SPI_IE_FIFO_EMPTY	RW	Current FIFO data empty interrupt enable: 1: Turn on enable; 0: Turn off enable.	0

SPI Interrupt 1 Flag Register (R8_SPI_INT1_FLAG)

Bit	Name	Access	Description	Reset value
[7:2]	Reserved	RO	Reserved	0
0	RB_SPI_IF_FIFO_FULL	RW1	Current FIFO data full flag bit, write 1 to clear: 1: FIFO is full; 0: FIFO is not full.	0
0	RB_SPI_IF_FIFO_EMPTY	RW1	Current FIFO data empty flag bit, write 1 to clear: 1: FIFO is empty; 0: FIFO not empty.	0

SPI0 DMA Buffer Current Address (R16_SPI_DMA_NOW)

Bit	Name	Access	Description	Reset value
[31:17]	Reserved	RO	Reserved	0
[15:0]	R16_SPI_DMA_NOW	RW	DMA data buffer current address. It can be used to calculate the number of conversions. COUNT=SPI_DMA_NOW-SPI_DMA_BEG.	XXXXh

SPI DMA Buffer Start Address (R16_SPI_DMA_BEG)

Bit	Name	Access	Description	Reset value
[31:17]	Reserved	RO	Reserved	0
[16:0]	R16_SPI_DMA_BEG	RW	DMA data buffer start address, only the lower 14 bits are valid.	XXXXh

SPI0 DMA Buffer End Address (R16_SPI_DMA_END)

Bit	Name	Access	Description	Reset value
[31:17]	Reserved	RO	Reserved	0
[16:0]	R16_SPI_DMA_END	RW	DMA data buffer end address (not included) ,	XXXXh