R16_SPI_DMA_END	0x4000401C	SPI0 DMA buffer end address	0xXXXX

SPI Mode Control Register (R8_SPI_CTRL_MOD)

Bit	Name	Access	Description	Reset value
7	RB_SPI_MISO_OE	RW	MISO pin output enable (can be used at data line switching direction in 2-wire mode): 1: MISO output enabled; 0: MISO output disabled.	0
6	RB_SPI_MOSI_OE	RW	MOSI pin output enable: 1: MOSI output enabled; 0: MOSI output disabled.	0
5	RB_SPI_SCK_OE	RW	SCK pin output enable: 1: SCK output enabled; 0: SCK output disabled.	0
4	RB_SPI_FIFO_DIR	RW	FIFO direction: 1: Input (receive data); 0: Output (transmit data).	0
3	RB_SPI_SLV_CMD_MOD	RW	First byte mode selection in SPI slave mode: 1: First byte command mode; 0: Data stream mode. In the first byte command mode, it will be regarded as a command code when receiving the first byte of data after the SPI chip select is valid and RB_SPI_IF_FST_BYTE will be set to 1.	0
3	RB_SPI_MST_SCK_MOD	RW	Clock idle mode selection in master mode: 1: Mode3 (SCK is at high level when idle); 0: Mode0 (SCK is at low level when idle).	0
2	RB_SPI_2WIRE_MOD	RW	2-wire or 3-wire SPI mode selection: 1: 2-wire mode/halfduplex (MISO in slave mode /MOSI in master mode); 0: 3-wire mode/full duplex (SCK/MOSI/MISO).	0
1	RB_SPI_ALL_CLEAR	RW	SPI FIFO/counter/interrupt flag clear: 1: Force to empty and clear; 0: Not clear.	1
0	RB_SPI_MODE_SLAVE	RW	SPI master/slave mode selection: 1: Slave mode; 0: Master mode.	0

SPI Configuration Register (R8_SPI_CTRL_CFG)

Bit	Name	Access	Description	Reset value
7	Reserved	RO	Reserved	0