(2) Set RB_SPI_MODE_SLAVE in R8_SPI_CTRL_MOD to 0, to configure SPI to master mode;

(3) Set RB_SPI_MST_SCK_MOD in R8_SPI_CTRL_MOD, to select clock idle mode0 or mode3;

(4) Set the RB_SPI_FIFO_DIR in R8_SPI_CTRL_MOD to configure the FIFO direction. If it is 1, FIFO is used to receive. If it is 0, FIFO is used to transmit;

(5) Set RB_SPI_MOSI_OE and RB_SPI_SCK_OE in R8_SPI_CTRL_MOD to 1, and set RB_SPI_MISO_OE to 0, and set GPIO direction configuration register (R32_PA/PB_DIR), to set the MOSI pin and SCK pin as output, and MISO pin as input;

(6) In 2-wire mode, SCK is unchanged, RB_SPI_MOSI_OE = 0, and MISO is not needed. In 3-wire mode, input (Rb_SPI_MOSI_OE = 0 and pin set as input) and output (RB_SPI_MOSI_OE = 1 and pin set as output) are realized by MOSI half-duplex, and the direction is manually switched.

(7) Optional. If DMA is enabled, it is needed to write the start address of transceiver buffer to R16_SPI_DMA_BEG and write the end address (not included) to R16_SPI_DMA_END. It is recommended to set RB_SPI_DMA_ENABLE after setting RB_SPI_FIFO_DIR. If R16_SPI_TOTAL_CNT is confirmed as 0, RB_SPI_DMA_ENABLE can be first set to 1 to enable DMA function.

Data transmission:

(1) Set RB_SPI_FIFO_DIR to 0, and the current FIFO direction is output;

(2) Write to the R16_SPI_TOTAL_CNT register, and set the length of the data to be sent;

(3) Write to the R8_SPI_FIFO register and write the data to be transmitted to FIFO. If R8_SPI_FIFO_COUNT is less than FIFO capacity, continue to write FIFO. If DMA is enabled, DMA will automatically load FIFO to complete this step;

(4) As long as R16_SPI_TOTAL_CNT is not 0 and there is data in FIFO, SPI master will automatically transmit data, otherwise, it will pause;

(5) Wait until R16_SPI_TOTAL_CNT register becomes 0, indicating that the data transmission is completed. If only one byte is sent, you can also query and wait for RB_SPI_FREE to be idle or wait for R8_SPI_FIFO_COUNT to be 0.

Data reception:

(1) Set RB_SPI_FIFO_DIR to 1, to set the current FIFO direction to input;

(2) Write to the R16_SPI_TOTAL_CNT register, to set the length of the data to be received;

(3) As long as R16_SPI_TOTAL_CNT is not 0 and FIFO is not full, SPI master will automatically receive data, otherwise, it will pause;

(4) Wait until R8_SPI_FIFO_COUNT register is not 0, indicating that the return data is received, the value read in R8_SPI0_FIFO is the received data. If DMA is enabled, DMA will automatically read FIFO to complete this step.

10.4.2 Slave Mode

SPI supports the slave mode. In the slave mode, SCK pin is used to receive the serial clock of SPI master connected to the external.

Configuration procedure: