			1: Interrupt enabled; 0: Interrupt disabled.	
1	RB_SPI_IE_BYTE_END	RW	SPI single byte transmission completion interrupt enable: 1: Interrupt enabled; 0: Interrupt disabled.	0
0	RB_SPI_IE_CNT_END	RW	SPI all byte transmission completion interrupt enable: 1: Interrupt enabled; 0: Interrupt disabled.	0

SPI Clock Divider Register in Master Mode (R8_SPI_CLOCK_DIV)

Bit	Name	Access	Description	Reset value
[7:0]	R8_SPI_CLOCK_DIV	RW	Frequency division factor in master mode, the minimum value is 2, up to 254. Fsck= Fsys/frequency division factor.	10h

SPI Preset Data Register in Slave Mode (R8_SPI_SLAVE_PRE)

Bit	Name	Access	Description	Reset value
[7:0]	R8_SPI_SLAVE_PRE	RW	Preset data first returned in slave mode. Used to receive the returned data after first byte of data.	10h

SPI Data Buffer (R8_SPI_BUFFER)

Bit	Name	Access	Description	Reset value
[7:0]	R8_SPI_BUFFER	RW	SPI data transmit and receive buffer.	XXh

SPI Working Status Register (R8_SPI_RUN_FLAG)

Bit	Name	Access	Description	Reset value
7	RB_SPI_SLV_SELECT	RO	Chip select status in slave mode: 1: Being selected; 0: No chip selected.	0
6	RB_SPI_SLV_CS_LOAD	RO	First loading status after chip select in slave mode: 1: Being loading R8_SPI_SLAVE_PRE; 0: Not yet loaded or has completed.	0
5	RB_SPI_FIFO_READY	RO	FIFO ready: 1: FIFO is ready (R16_SPI_TOTAL_CNT is not 0, and the FIFO is not full when receiving or the FIFO is not empty when transmitting); 0: FIFO is not ready.	0
4	RB_SPI_SLV_CMD_ACT	RO	Command received completion status in	0