Data reception:

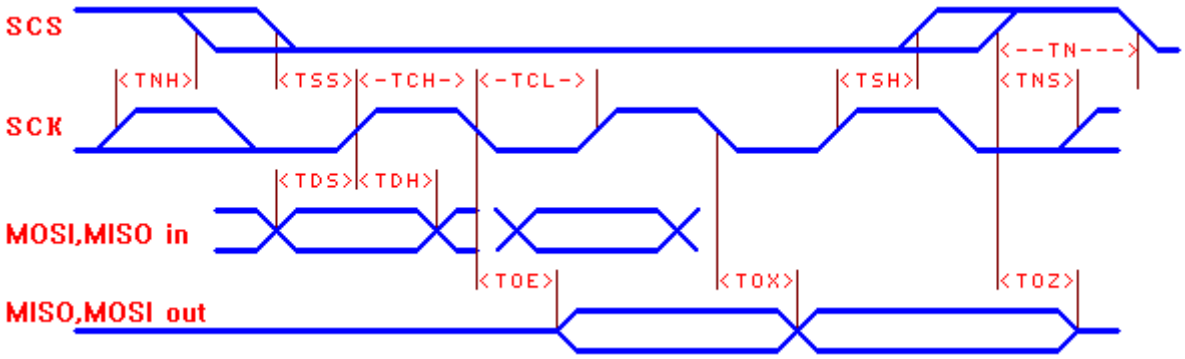
(1) Set RB_SPI_FIFO_DIR of R8_SPI_CTRL_MOD to 1, and the current FIFO direction as input;

(2) Optional step. If DMA is enabled, it is needed to set RB_SPI_DMA_ENABLE to 1 to enable DMA function;

(3) Query R8_SPI_FIFO_COUNT, if it is not empty, the data has been received and the data will be taken away by reading R8_SPI_FIFO. If DMA is enabled, DMA will automatically read FIFO to complete this step;

(4) For reception of the single byte data, R8_SPI_BUFFER can be read directly without using FIFO.

10.5 SPI Timing



Name	Parameter description (TA=25°C, VIO33=3.3V)	Min.	Typ.	Max.	Unit
TSS	Setup time of valid SCS before SCK rising edge	Tsys*1.05			nS
TSH	Hold time of valid SCS before SCK rising edge	Tsys*1.05			nS
TNS	Setup time of invalid SCS before SCK rising edge	15			nS
TNH	Hold time of invalid SCS before SCK rising edge	15			nS
TN	Time of invalid SCS (interval time of SPI operation)	Tsys*2			nS
TCH	Time of SCK clock at high level	Tsys*0.55			nS
TCL	Time of SCK clock at low level	Tsys*0.55			nS
TDS	Setup time of MOSI/MISO input before SCK rising edge	8			nS
TDH	Hold time of MOSI/MISO input before SCK rising edge	5			nS
TOE	SCK falling edge to MISO/MOSI output valid	0		18	nS
TOX	SCK falling edge to MISO/MOSI output change	0	5	16	nS
TOZ	SCS invalid to MISO/MOSI output invalid	2		24	nS

Note: Tsys is the cycle of system clock frequency (1/Fsys).