SPI Transceiver Data Total Length Register (R16_SPI_TOTAL_CNT)

Bit	Name	Access	Description	Reset value
[15:0]	R16_SPI_TOTAL_CNT	RW	Total number of bytes of SPI data transceiver in master mode, and the lower 12 bits are valid. At most 4095 bytes can be received/transmitted at a time when using DMA. It is not supported in slave mode.	0

SPI Data FIFO Register (R8_SPI_FIFO)

Bit	Name	Access	Description	Reset value
[7:0]	R8_SPI_FIFO	RO/ WO	Data FIFO register.	XXh

The registers R8_SPI_BUFFER and R8_SPI_FIFO are both SPI data related registers, and the main differences between them are:
Reading R8_SPI_BUFFER means to obtain the data from the last exchange of SPI, and it does not affect FIFO and R8_SPIx_FIFO_COUNT;

Writing to R8_SPI_BUFFER in master mode means to send the byte directly, and the write operation in slave mode is not defined;

Reading R8_SPI_FIFO means to obtain the data from the earliest exchange in FIFO, which will reduce FIFO and R8_SPI_FIFO_COUNT;

Writing to R8_SPI_FIFO means to temporarily store the data in FIFO. In slave mode, the external SPI host decides when to take it. In master mode, the transmission is automatically started when R16_SPI_TOTAL_CNT is not 0.

SPI Transceiver FIFO Count Register (R8_SPI_FIFO_COUNT1)

Bit	Name	Access	Description	Reset value
[7:4]	Reserved	RO	Reserved	0h
[3:0]	R8_SPI_FIFO_COUNT1	RW	Current byte count in FIFO. The same as R8_SPI_FIFO_COUNT.	0h

SPI Interrupt Trigger Mode Selection Register (R8_SPI_INT_TYPE)

Bit	Name	Access	Description	Reset value
[7:5]	Reserved	RO	Reserved	0
[4:0]	RB_SPI_INT_TYPE	RW	Interrupt trigger mode selection, 1= pulse trigger, 0= edge trigger. bit[4]: RB_SPI_IF_FIFO_FULL; bit[3]: RB_SPI_IF_FIFO_EMPTY; bit[2]: RB_SPI_IF_DMA_END; bit[1]: RB_SPI_IF_FIFO_HF; bit[0]: RB_SPI_IF_CNT_END.	0