

DD lab3

Digilent Nexys4 FPGA Board & Xilinx Vivado Development Suite

負責助教：郭政頡、陳冠良、方泰翔、鄭東昇、陳憲億

Outline

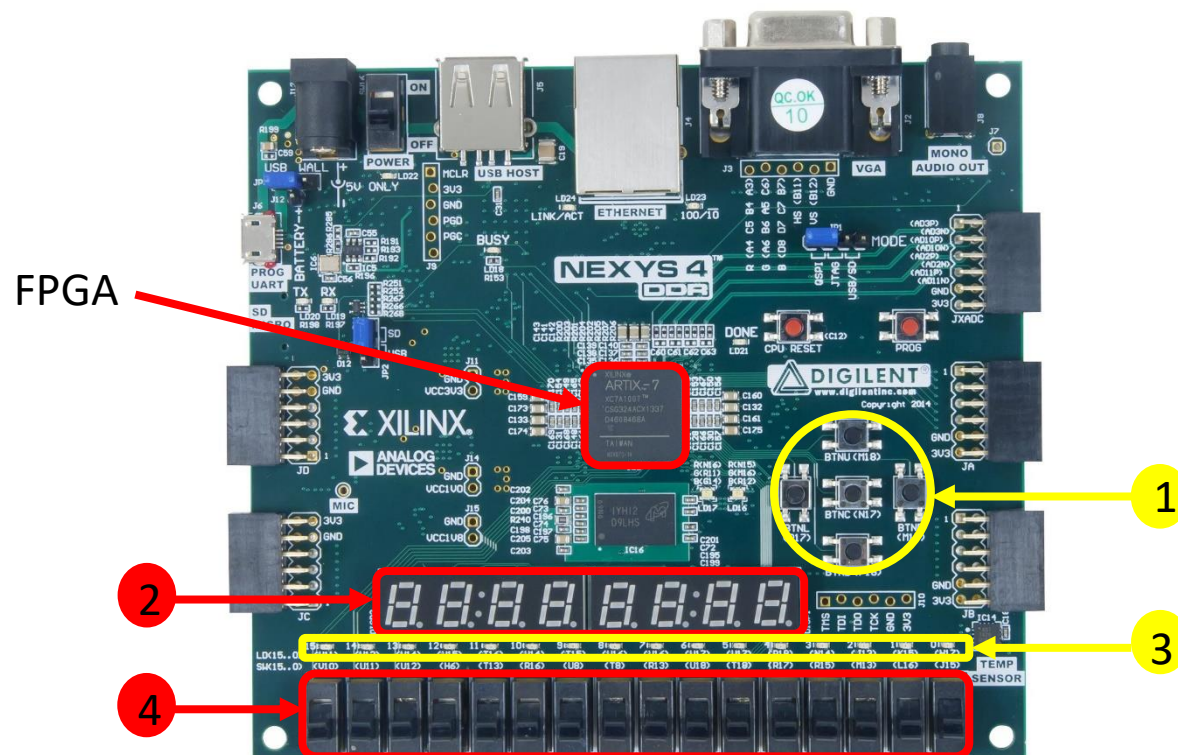
- 課程目的
- 課程工具
- 課程實驗
- Lab作業
- 課程評分方式
- 附錄

課程目的

在Lab3的課程中，同學們將學會如何利用Vivado開發工具將設計電路燒錄到Nexys4 FPGA開發板上，並透過Nexys4 FPGA開發板上的Switches及LEDs等周邊元件來驗證RTL電路設計的正确性

課程工具

- Nexys4上的FPGA可以用RTL code來描述電路行為
- Nexys4上有按鈕開關、LED、七段顯示器以及指撥開關等開發板周邊元件，可以用來作為FPGA的輸入與輸出



	周邊元件
1	Push Button
2	7 segment display
3	LED
4	Switch

課程實驗

- 使用16個Switches (SW0 – SW15)分別控制16個LEDs (LED0 – LED15)的亮滅

LED輸出結果

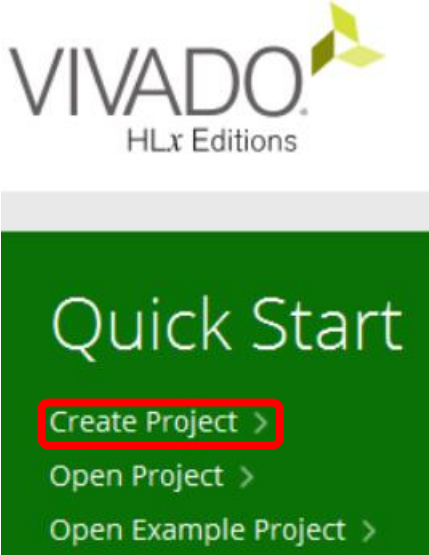



SW輸入

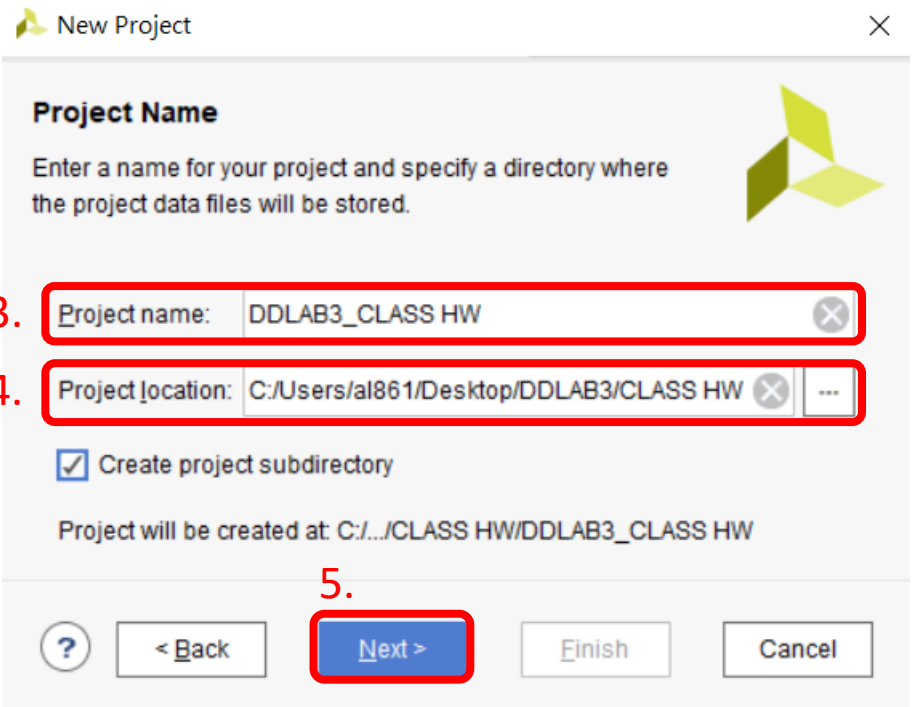
- 實驗教學內容
 - 使用Vivado建立專案
 - 使用Vivado創立專案原始檔
 - .xdc檔設定
 - 生成.bit檔並燒錄至Nexys4上

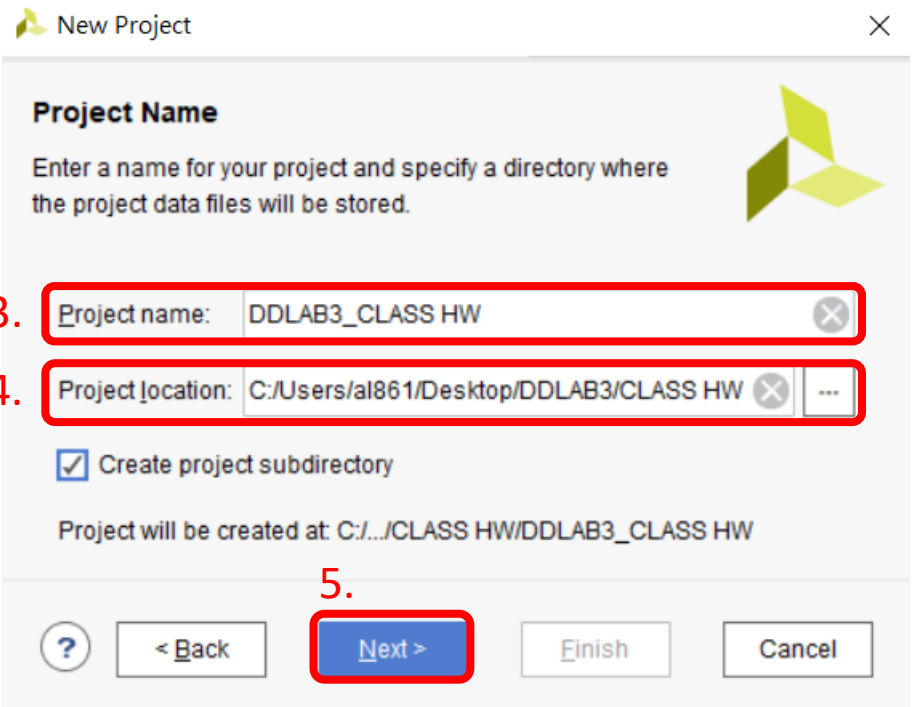
Vivado建立專案 (1/3)

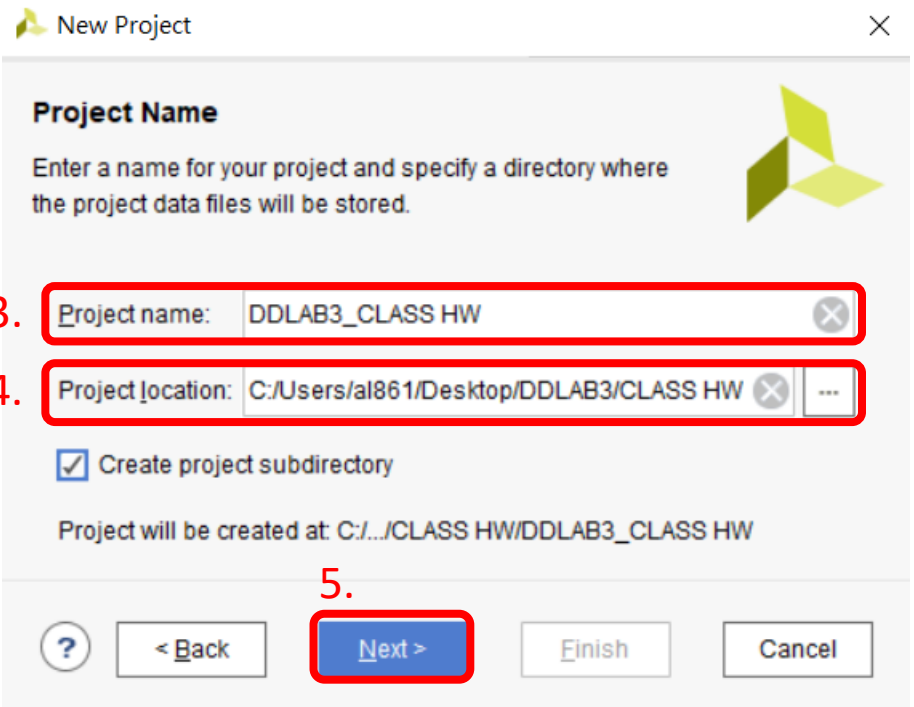
- 練習建立Vivado專案
 - 開啟Vivado軟體 -> Create Project -> Next -> 輸入專案名稱 -> 選擇專案位置 -> Next

1.  The Vivado Quick Start dialog box is shown. The 'Create Project >' button is highlighted with a red box.

2.  The 'New Project' dialog box is shown. The 'Next >' button is highlighted with a red box.

3.  The 'New Project' dialog box is shown. The 'Project name' field is highlighted with a red box and contains the text 'DDLAB3_CLASS HW'.

4.  The 'New Project' dialog box is shown. The 'Project location' field is highlighted with a red box and contains the text 'C:/Users/al861/Desktop/DDLAB3/CLASS HW'.

5.  The 'New Project' dialog box is shown. The 'Next >' button is highlighted with a red box.

Vivado建立專案 (2/3)

- 選擇RTL Project -> Next -> Next -> Next

New Project

Project Type
Specify the type of project to create.

1.

☒ **RTL Project**
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.

☐ Do not specify sources at this time

☐ **Post-synthesis Project**
You will be able to add sources, view device resources, run design analysis, planning and implementation.

☐ Do not specify sources at this time

☐ **I/O Planning Project**
Do not specify design sources. You will be able to view part/package resources.

☐ **Imported Project**
Create a Vivado project from a Synplify, XST or ISE Project File.

☐ **Example Project**
Create a new Vivado project from a predefined template.

2.

? < Back **Next >** Finish Cancel

New Project

Add Sources
Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project.

+ - ↑ ↓

Use Add Files, Add Directories or Create File buttons below

Add Files Add Directories Create File

☐ Scan and add RTL include files into project

☐ Copy sources into project

☒ Add sources from subdirectories

Target language: Verilog Simulator language: Mixed

3.

? < Back **Next >** Finish Cancel

New Project

Add Constraints (optional)
Specify or create constraint files for physical and timing constraints.

+ - ↑ ↓

Use Add Files or Create File buttons below

Add Files Create File

☐ Copy constraints files into project

4.

? < Back **Next >** Finish Cancel

Vivado建立專案 (3/3)

- Family選擇Artix-7 -> Package選擇csg324 -> Speed grade選擇-3 ->選擇xc7a100tcs324-3 -> Finish

New Project

Default Part
Choose a default Xilinx part or board for your project. This can be changed later.

Select: ☒ Parts ☐ Boards

Filter

Product category: All

1. Family: Artix-7

2. Package: csg324

3. Speed grade: -3

Temp grade: All R...

Reset All Filters

Search: Q

Part	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	Ultra RAMs	DSPs
xc7a15tcsg324-3	324	210	10400	20800	25	0	45
xc7a35tcsg324-3	324	210	20800	41600	50	0	90
xc7a50tcsg324-3	324	210	32600	65200	75	0	120
xc7a75tcsg324-3	324	210	47200	94400	105	0	180
4. xc7a100tcsg324-3	324	210	63400	126800	135	0	240

Back Next Finish Cancel

New Project

VIVADO
HLx Editions

New Project Summary

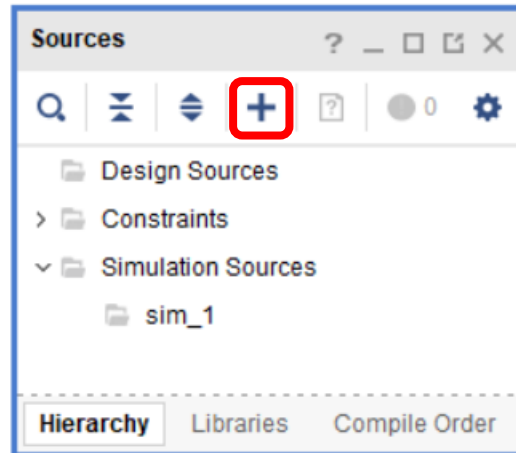
- A new RTL project named 'DDLAB3_CLASS_HW' will be created.
- No source files or directories will be added. Use Add Sources to add them later.
- No constraints files will be added. Use Add Sources to add them later.
- The default part and product family for the new project:
Default Part: xc7a100tcsg324-3
Product: Artix-7
Family: Artix-7
Package: csg324
Speed Grade: -3

To create the project, click Finish

5. Finish Back Next Cancel

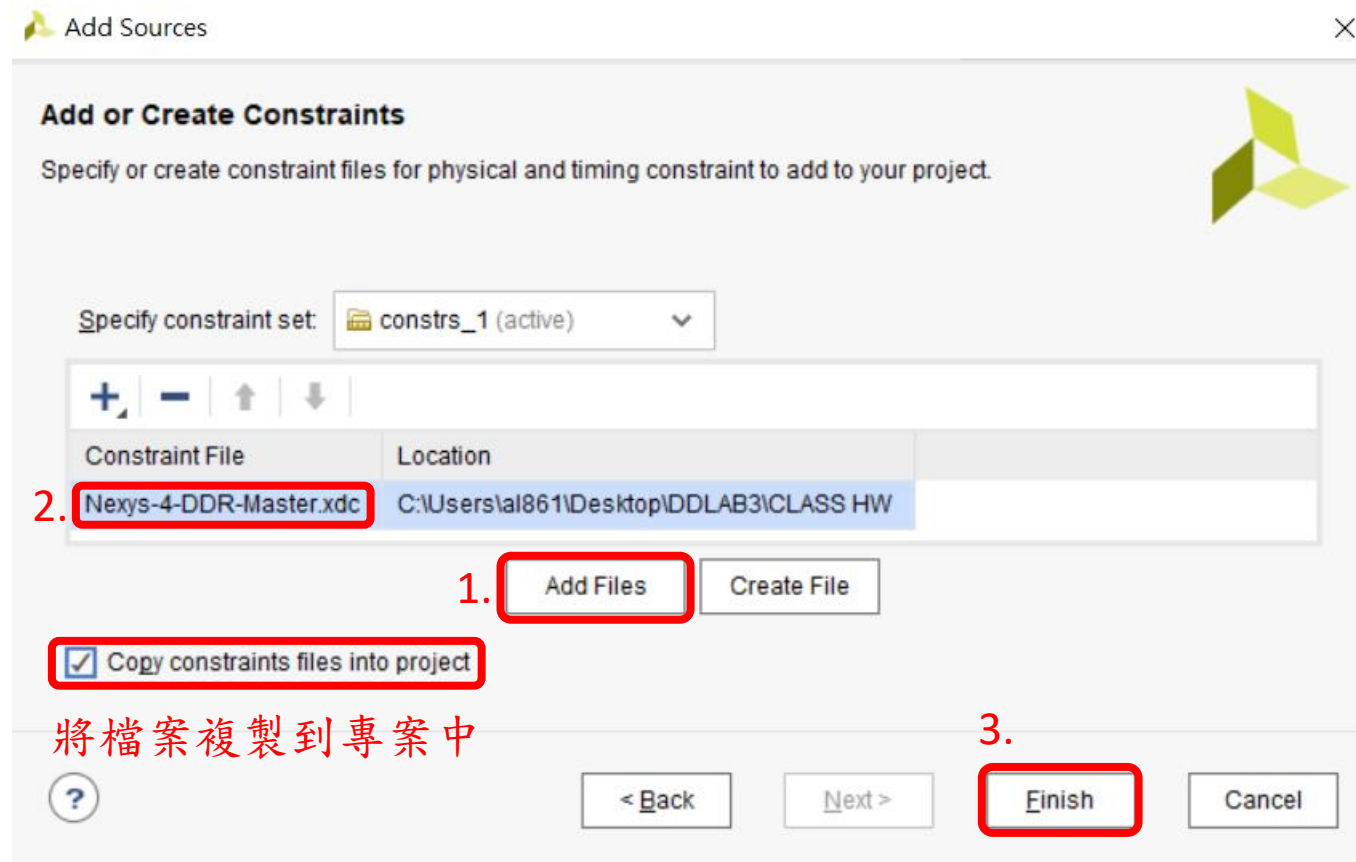
Vivado創建專案原始檔 (1/3)

- 點選+符號並選擇欲添加檔案的類型
 - a) Add or create constraints
 - Constraints (.xdc檔)：用來描述.v檔與實體線路的連接關係
 - b) Add or create design sources
 - design sources (.v檔)：用來描述電路行為



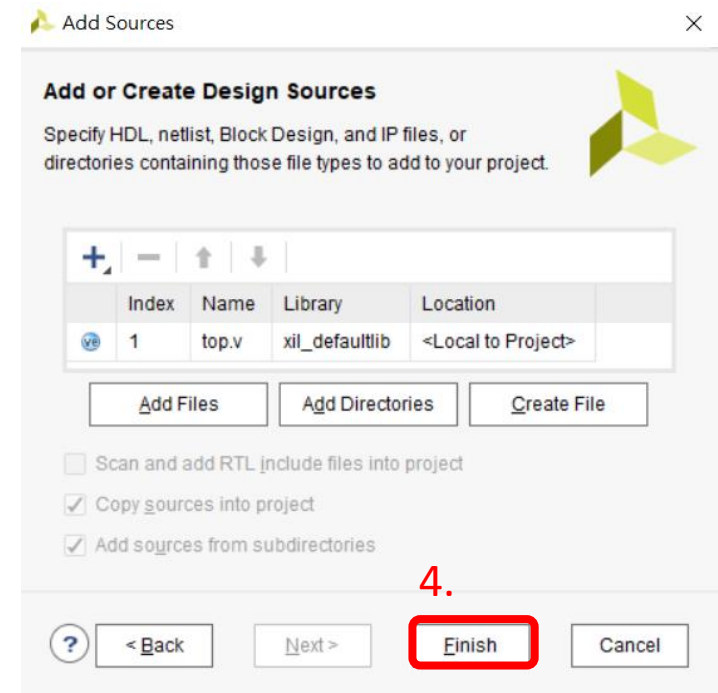
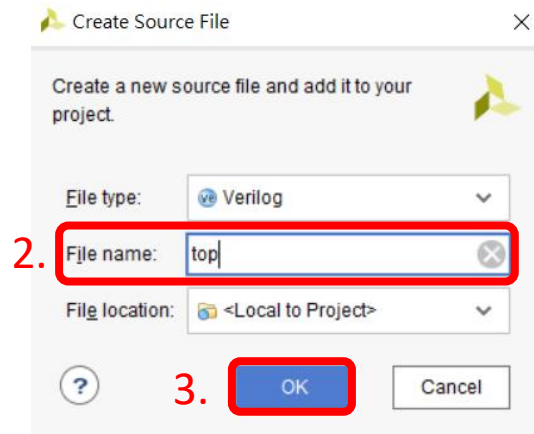
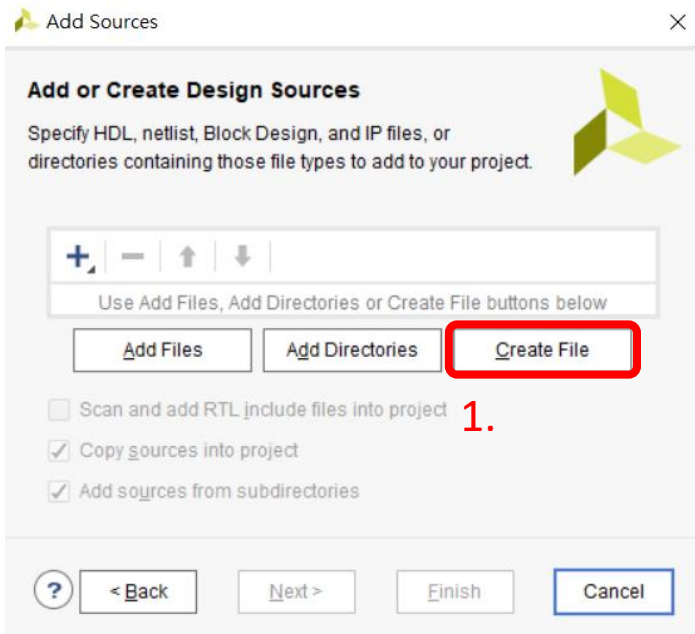
Vivado創建專案原始檔 (2/3)

- 加入.xdc檔
 - 選擇Add or create constraints -> Next -> Add Files -> 選擇Nexys-4-DDR-Master.xdc -> Finish



Vivado創建專案原始檔 (3/3)

- 建立.v檔：
 - 選擇Add or create design sources -> Next -> Create File -> 輸入檔案名稱 -> OK -> Finish



設定.xdc檔

- Xilinx Design Constraints file (簡稱為xdc file)
 - .xdc檔為開發板上的周邊元件設定檔
 - 根據開發板上的需要用的元件PIN腳的名稱做設定

對應.v檔中定義的input及output名稱

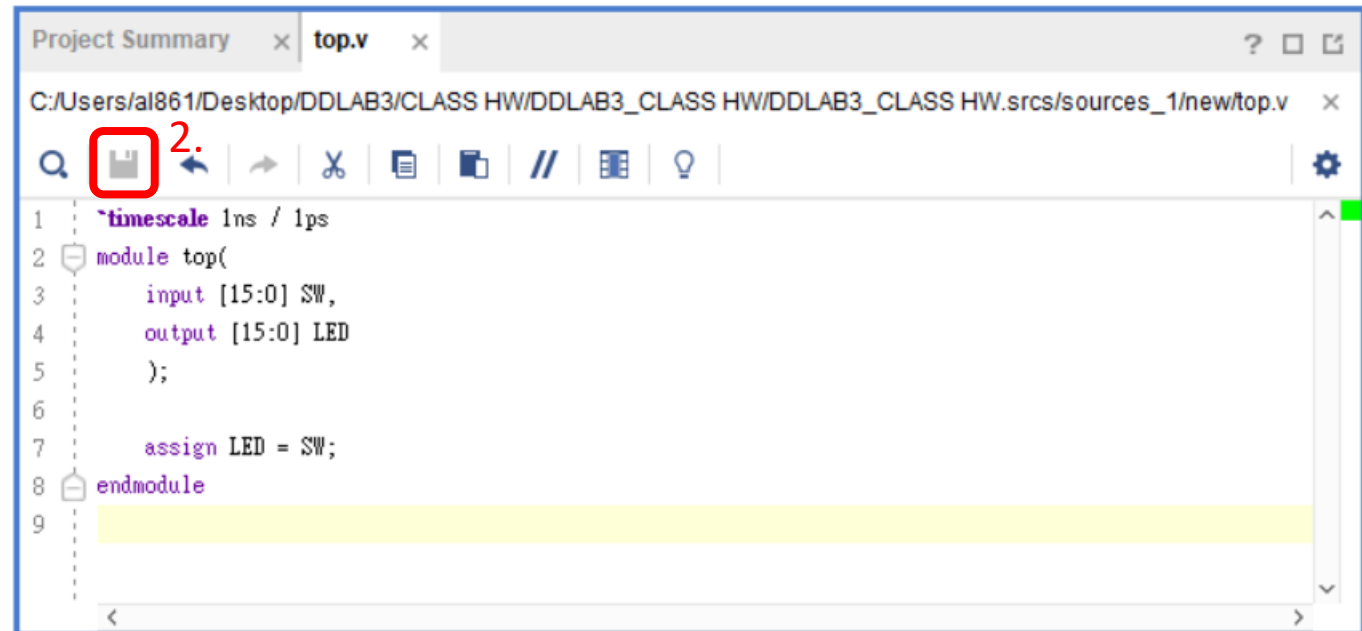
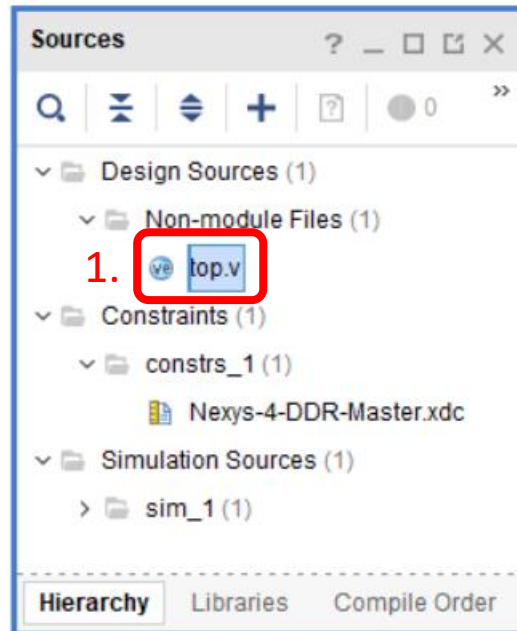
```
set_property -dict { PACKAGE_PIN J15 IOSTANDARD LVCOS33 } [get_ports { SW[0] }]; #IO_L24N_T3_RS0_15 Sch=sw[0]
set_property -dict { PACKAGE_PIN L16 IOSTANDARD LVCOS33 } [get_ports { SW[1] }]; #IO_L3N_T0_DQS_EMCCCLK_14 Sch=sw[1]
set_property -dict { PACKAGE_PIN M13 IOSTANDARD LVCOS33 } [get_ports { SW[2] }]; #IO_L6N_T0_D08_VREF_14 Sch=sw[2]
set_property -dict { PACKAGE_PIN R15 IOSTANDARD LVCOS33 } [get_ports { SW[3] }]; #IO_L13N_T2_MRCC_14 Sch=sw[3]
set_property -dict { PACKAGE_PIN R17 IOSTANDARD LVCOS33 } [get_ports { SW[4] }]; #IO_L12N_T1_MRCC_14 Sch=sw[4]
set_property -dict { PACKAGE_PIN T18 IOSTANDARD LVCOS33 } [get_ports { SW[5] }]; #IO_L7N_T1_D10_14 Sch=sw[5]
set_property -dict { PACKAGE_PIN U18 IOSTANDARD LVCOS33 } [get_ports { SW[6] }]; #IO_L17N_T2_A13_D29_14 Sch=sw[6]
set_property -dict { PACKAGE_PIN R13 IOSTANDARD LVCOS33 } [get_ports { SW[7] }]; #IO_L5N_T0_D07_14 Sch=sw[7]
```

對應開發板上的PIN腳名稱



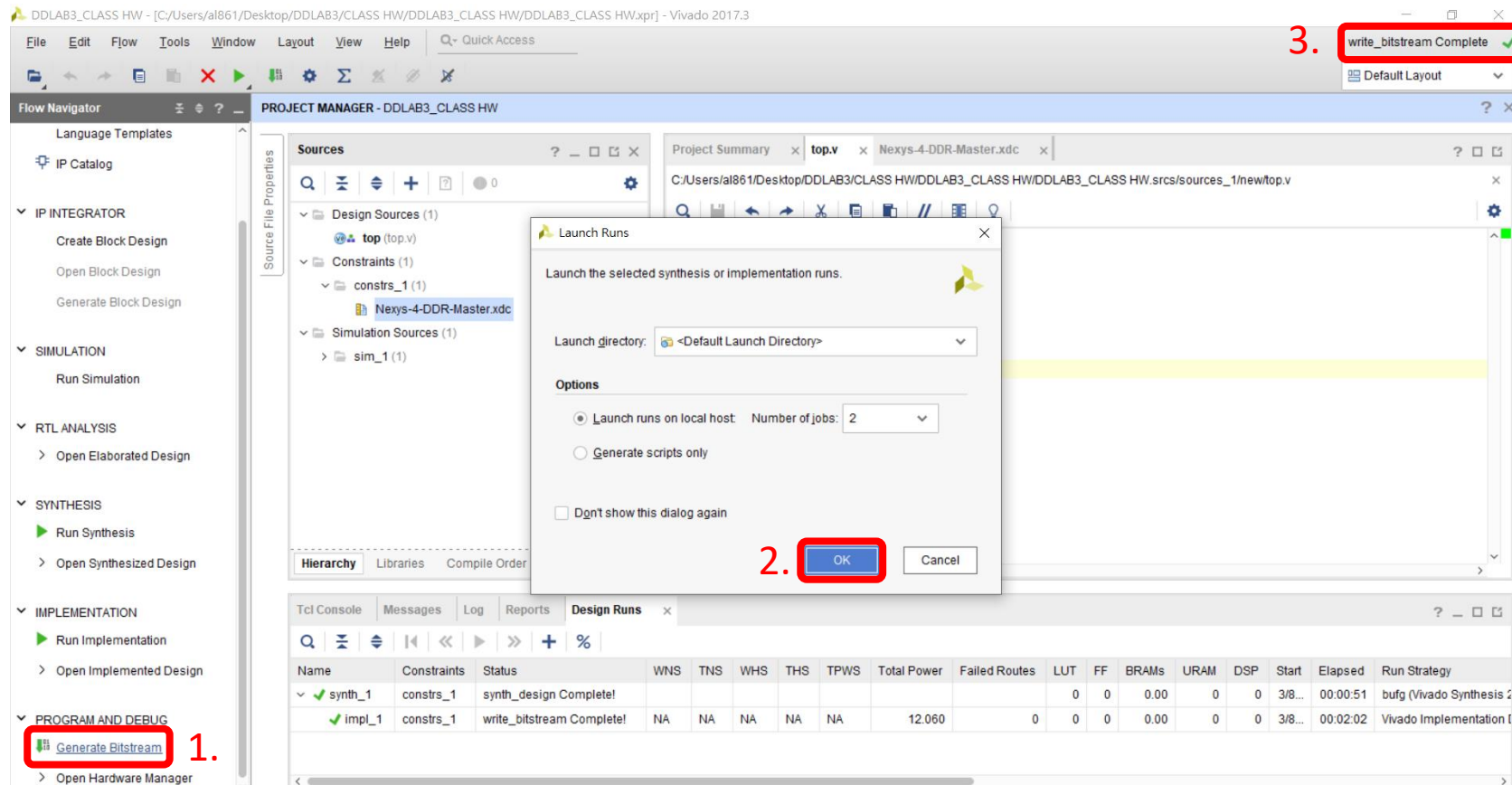
課堂練習範例程式碼

- 在左方欄位中的Design Source中找到top.v打開 -> 輸入範例程式碼後並存檔



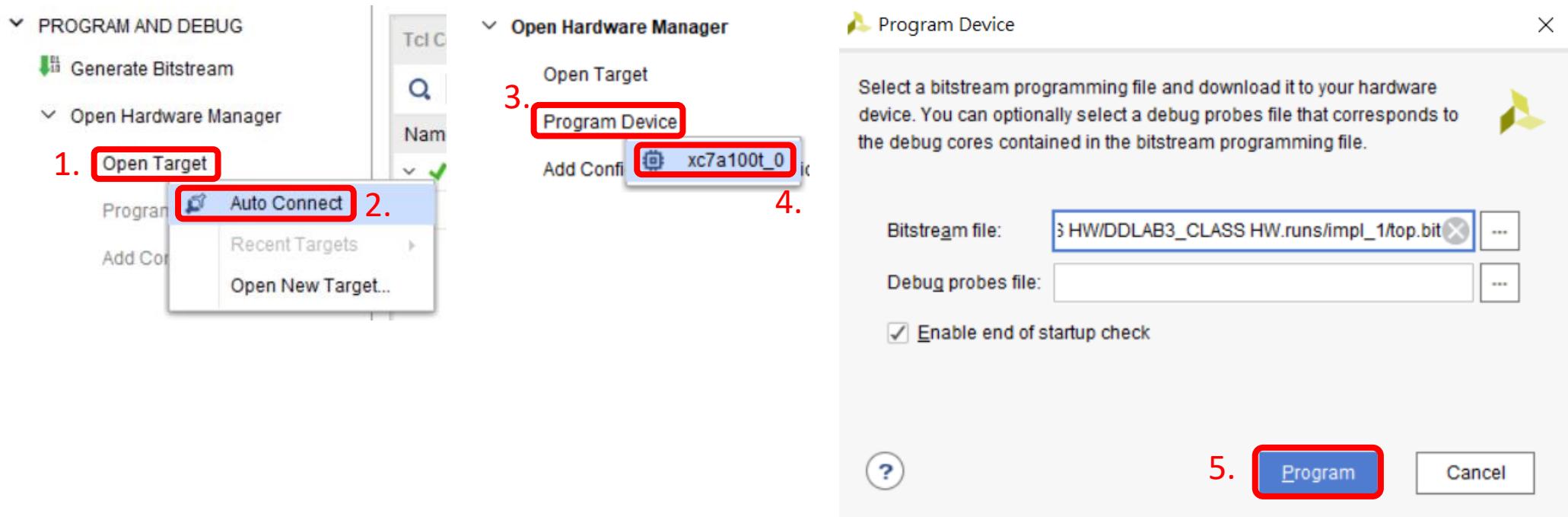
燒錄到FPGA驗證功能 (1/2)

- 完成專案後將專案的電路燒錄到FPGA上驗證功能正確與否
 - 左下角欄位中選擇Generate bitstream -> OK -> 等待完成後右上角會出現成功訊息✓



燒錄到FPGA驗證功能 (2/2)

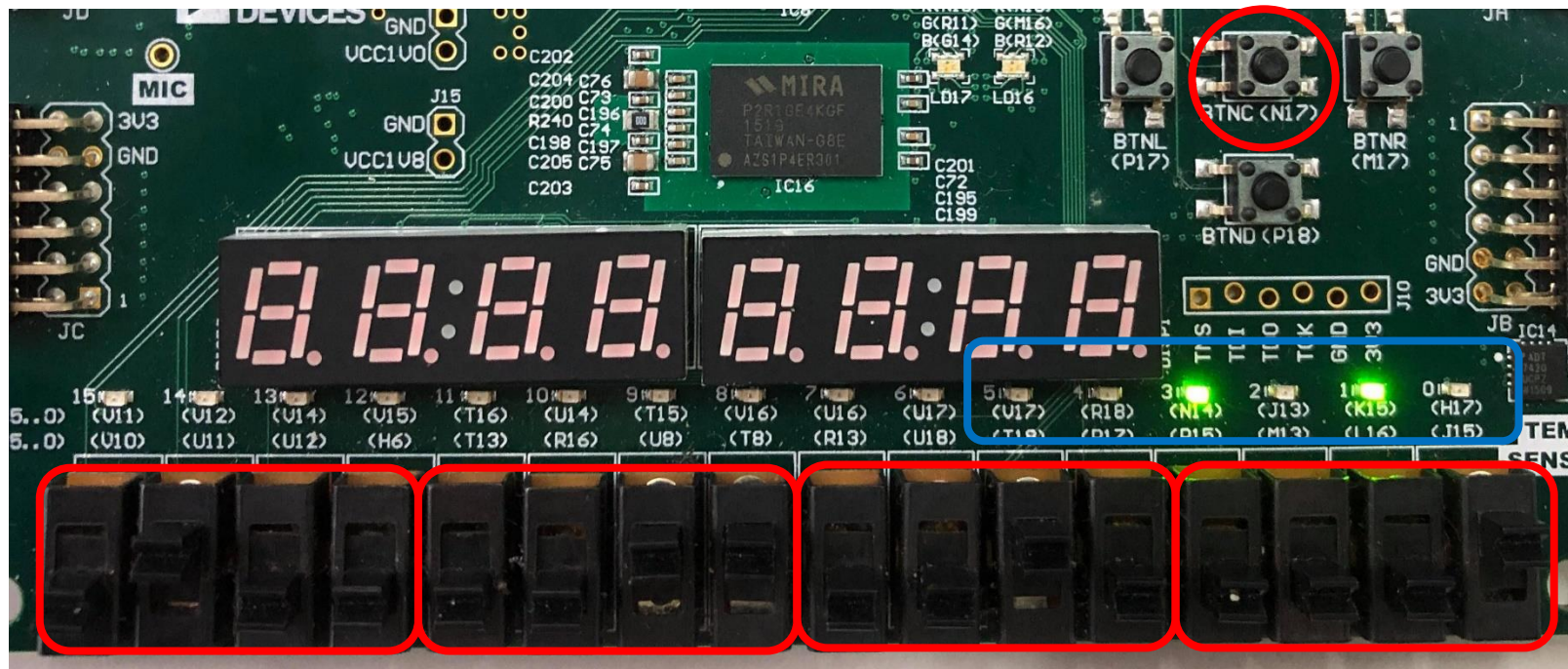
- 打開Nexys4的電源 -> Open Target -> Auto Connect -> Program Device -> xc7a100t_0 -> Program
 - 燒錄上FPGA後確認switches是否可以控制對應的LEDs的亮滅



Lab作業

- 將Lab1作業四個4-bits的加法器在FPGA上實作，使用Nexys4開發板上從右到左每四個Switches當作一個input，當按下Button(N17)，就會將加法器四個input相加結果以binary形式更新到LEDs上，相加結果以6-bits來表示

按下 Button 即將
相加結果更新



相加結果

Input d[3:0]

Input c[3:0]

Input b[3:0]

Input a[3:0]

課程評分

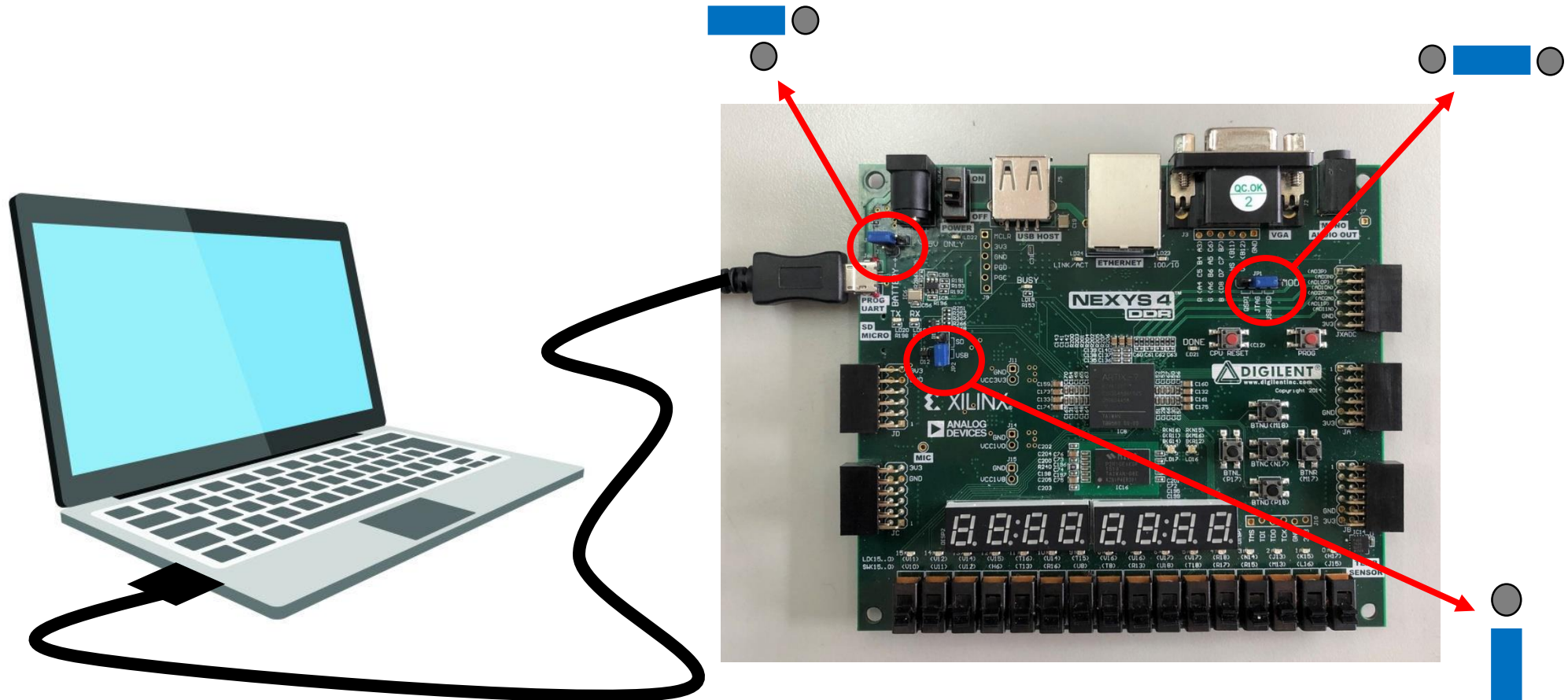
- Demo時間：2021.3.29(一)、4.7(三)，按照規定Demo時間自行前往Demo地點
- Demo地點：資工館501A
- 攜帶檔案：bitstream (.bit檔) (可以在創建專案的資料夾 -> .runs -> impl_1 中找到)
- 課程評分方式
 - 加法器四個input相加結果正確，並可以透過按下Button將相加結果更新到LED燈上(100%)

附錄

- 實驗環境架設
- Vivado軟體安裝

實驗環境架設

- 請同學們使用前請先檢查一下Nexys4 FPGA開發板上的3個Jumper是否與下圖一致，若有不同可能會造成Nexys4 FPGA開發板無法正常動作



Vivado軟體安裝 (1/9)

- 下載網址超連結 ->
<https://www.xilinx.com/support/download/index.html/content/xilinx/en/downloadNav/vivado-design-tools/archive.html>
- 選擇2017.3

The screenshot shows the Xilinx website's download page for Vivado. The navigation bar includes 'Solutions', 'Products', and 'Support'. The main heading is 'Downloads'. Below this, there are tabs for 'Licensing Help' and 'Alveo Accelerator Card'. A horizontal menu lists various categories: 'Vivado (HW Developer)', 'Vitis (SW Developer)', 'Vitis Embedded Platforms', 'Alveo Packages', 'PetaLinux', 'Device Models', and 'Documentation Navigator'. The 'Vivado (HW Developer)' tab is selected. On the left, a 'Version' sidebar lists '2020.2', '2020.1', '2019.2', 'Vivado Archive' (highlighted), 'ISE Archive', 'CAE Vendor Libraries', and 'Archive'. The main content area displays a recommendation to use the latest releases, followed by a list of years: 2019, 2018, and 2017. Under 2017, the version '2017.3' is highlighted with a red box. A 'Feedback' button is visible on the right side.

Version	Recommendation
2020.2	We strongly recommend using the latest releases available.
2020.1	
2019.2	
Vivado Archive	2019
ISE Archive	2018
CAE Vendor Libraries	2018.3
Archive	2018.2
	2018.1
	2017
	2017.4
	2017.3

Vivado軟體安裝 (2/9)

● 選擇All OS版本

[Solutions](#) [Products](#) [Support](#)

XILINX

Important

We **strongly recommend** to use the web installers as it reduces download time and saves significant disk space.

Please see [Installer Information](#) for details.

Vivado HLx 2017.3: WebPACK and Editions - Windows Self Extracting Web Installer (EXE - 51.22 MB)

MD5 SUM Value : f25ec28dab1a3711dd1346dcab2640e8

Vivado HLx 2017.3: WebPACK and Editions - Linux Self Extracting Web Installer (BIN - 100.61 MB)

MD5 SUM Value : d80a2721483fd5b1a6a77c481f98f988

Vivado HLx 2017.3: All OS installer Single-File Download (TAR/GZIP - 16.23 GB)

MD5 SUM Value : d443f58d703ff691cebc59c2173ae782

Download Includes

Vivado Design Suite HLx Editions (All Editions)

Download Type

Full Product Installation

Last Updated

Oct 9, 2017

Answers

[2017.x - Vivado Known Issues](#)

Documentation

[2017.3 - Release Notes](#)

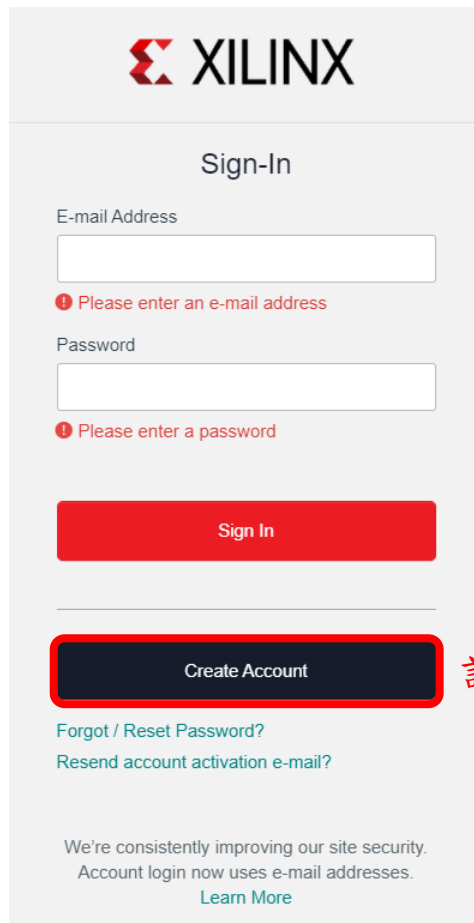
Enablement

[License Solution Center](#)

edback

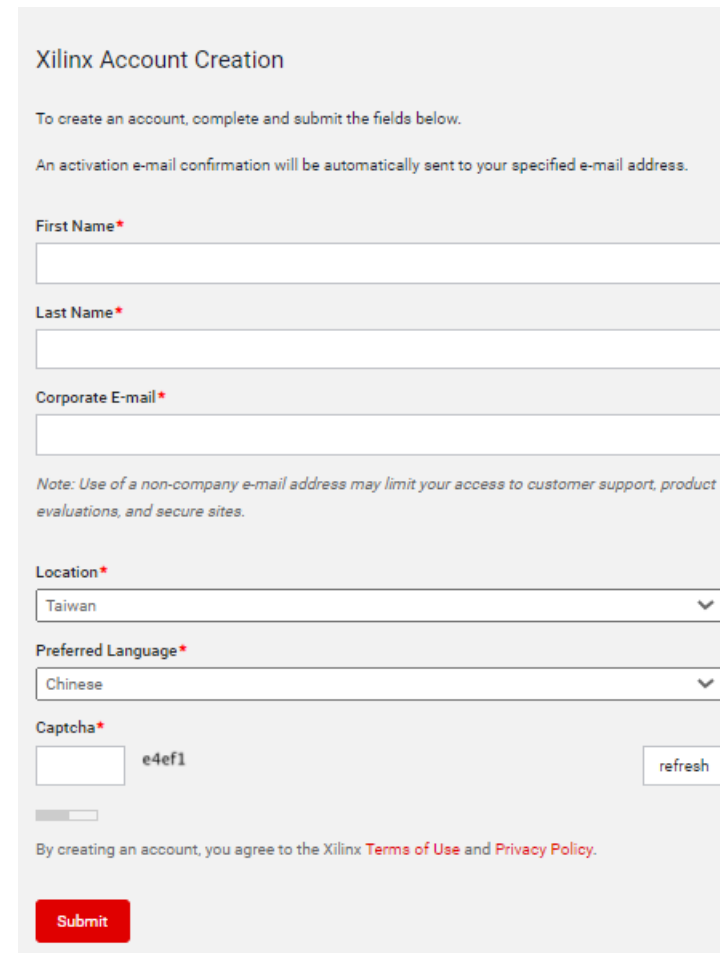
Vivado軟體安裝 (3/9)

- 註冊XILINX帳號 -> 填寫資料 -> E-mail認證



The image shows the Xilinx website's login and registration interface. At the top is the XILINX logo. Below it is a 'Sign-In' section with fields for 'E-mail Address' and 'Password'. Both fields have red error messages: 'Please enter an e-mail address' and 'Please enter a password'. A red 'Sign In' button is below these fields. Further down is a 'Create Account' button, which is highlighted with a red border. Below this button are links for 'Forgot / Reset Password?' and 'Resend account activation e-mail?'. At the bottom, there is a note about site security improvements and a 'Learn More' link.

註冊XILINX帳號



The image shows the Xilinx Account Creation page. It has a title 'Xilinx Account Creation' and instructions: 'To create an account, complete and submit the fields below.' and 'An activation e-mail confirmation will be automatically sent to your specified e-mail address.' The form includes fields for 'First Name *', 'Last Name *', and 'Corporate E-mail *'. Below these is a note: 'Note: Use of a non-company e-mail address may limit your access to customer support, product evaluations, and secure sites.' There are dropdown menus for 'Location *' (set to Taiwan) and 'Preferred Language *' (set to Chinese). A 'Captcha *' field shows the code 'e4ef1' with a 'refresh' button. At the bottom, there is a 'Submit' button and a line of text: 'By creating an account, you agree to the Xilinx Terms of Use and Privacy Policy.'

Vivado軟體安裝 (4/9)

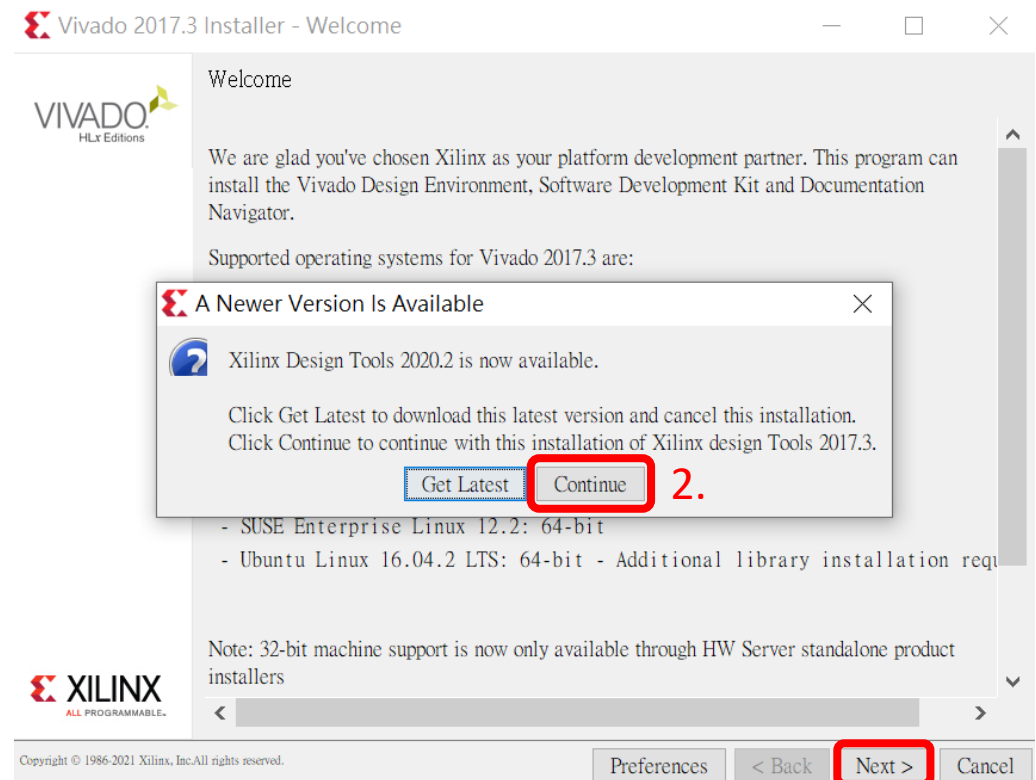
- 登入完成填寫資料後開始下載Vivado軟體

First Name*	Last Name*
<input type="text"/>	<input type="text"/>
Business E-mail*	
<input type="text"/>	
Company Name*	
<input type="text" value="CCU University"/>	
<small>Please enter the name of your business or institution.</small>	
Address 1*	
<input type="text" value="Sec 1, University Road, Minxiong Township, Chiayi Country 621, Taiwan"/>	
Address 2	
<input type="text"/>	
Location*	State/Province
<input type="text" value="Taiwan"/>	<input type="text" value="TW"/>
City*	Postal Code
<input type="text" value="Chiayi Minxiong"/>	<input type="text" value="621"/>
Phone	
<input type="text"/>	
Job Function*	
<input type="text" value="Student"/>	
<small>For more information about how we process your personal information, please see our privacy policy.</small>	
<input type="button" value="Download"/>	

Vivado軟體安裝 (5/9)

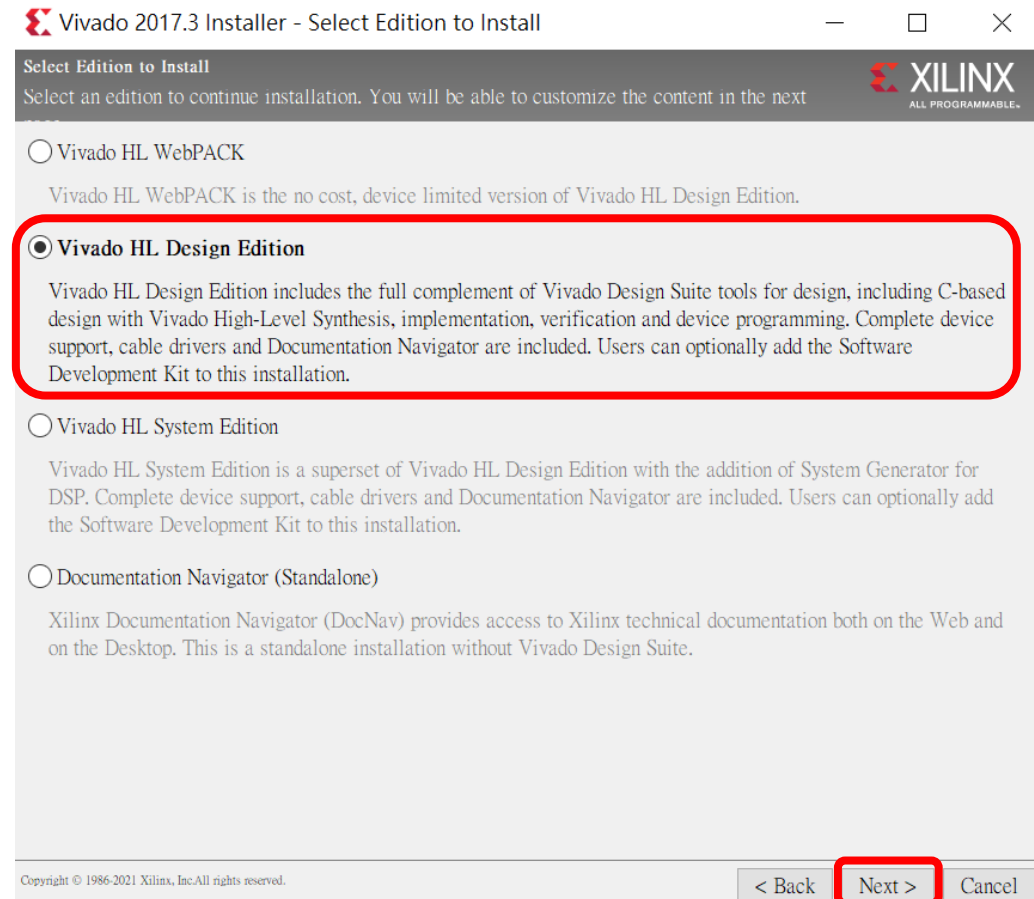
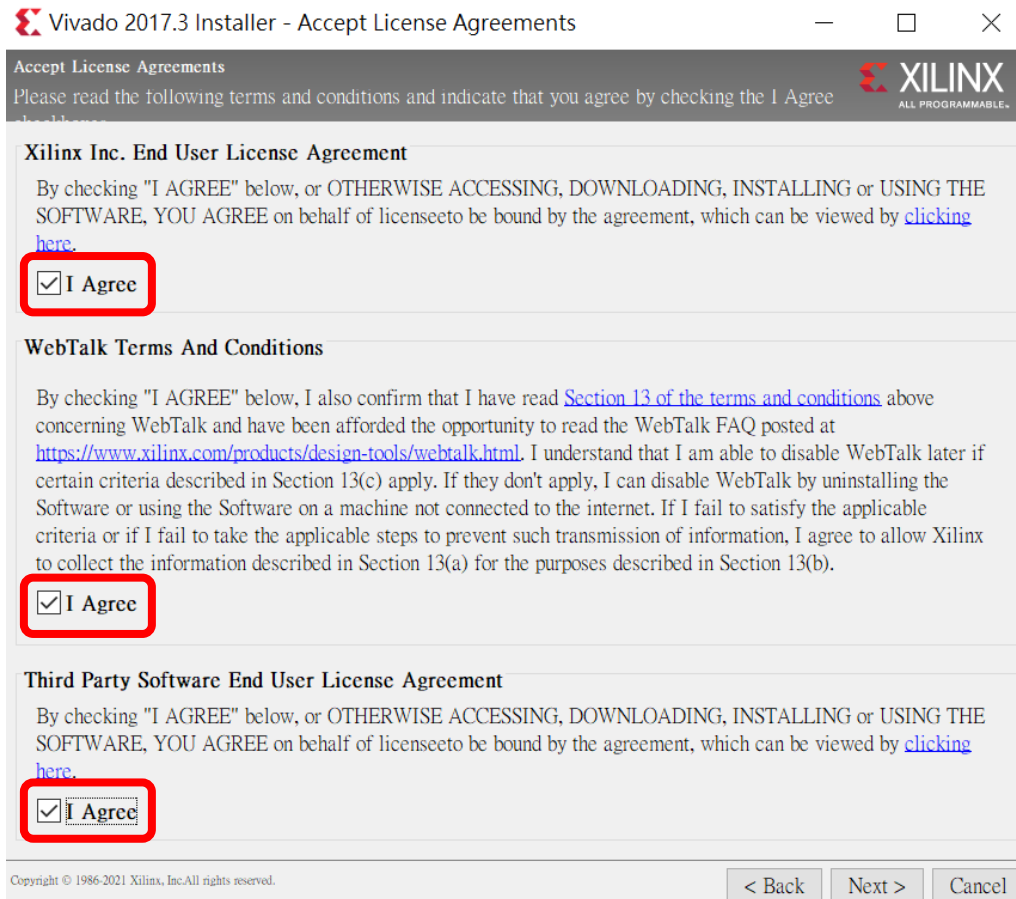
- 下載完成後解壓縮檔案 -> 點選xsetup -> Continue -> Next

名稱	修改日期	類型	大小
api-ms-win-crt-private-l1-1-0.dll	2017/10/5 上午 10:31	應用程式擴充	72 KB
api-ms-win-crt-process-l1-1-0.dll	2017/10/5 上午 10:31	應用程式擴充	20 KB
api-ms-win-crt-runtime-l1-1-0.dll	2017/10/5 上午 10:31	應用程式擴充	23 KB
api-ms-win-crt-stdio-l1-1-0.dll	2017/10/5 上午 10:31	應用程式擴充	25 KB
api-ms-win-crt-string-l1-1-0.dll	2017/10/5 上午 10:31	應用程式擴充	25 KB
api-ms-win-crt-time-l1-1-0.dll	2017/10/5 上午 10:31	應用程式擴充	21 KB
api-ms-win-crt-utility-l1-1-0.dll	2017/10/5 上午 10:31	應用程式擴充	19 KB
concr140.dll	2017/10/5 上午 10:31	應用程式擴充	240 KB
msvc140.dll	2017/10/5 上午 10:31	應用程式擴充	433 KB
ucrtbase.dll	2017/10/5 上午 10:31	應用程式擴充	880 KB
vccorlib140.dll	2017/10/5 上午 10:31	應用程式擴充	265 KB
vcruntime140.dll	2017/10/5 上午 10:31	應用程式擴充	84 KB
xsetup	2017/10/5 上午 10:31	檔案	3 KB
1. xsetup	2017/10/5 上午 10:01	應用程式	435 KB



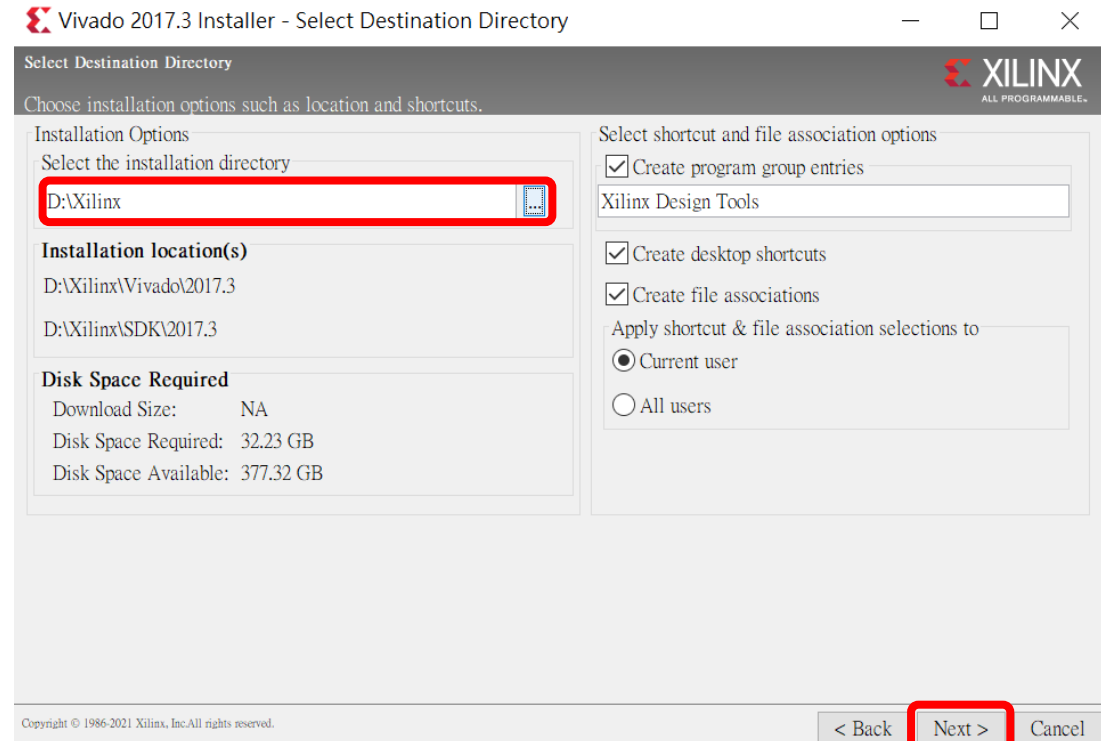
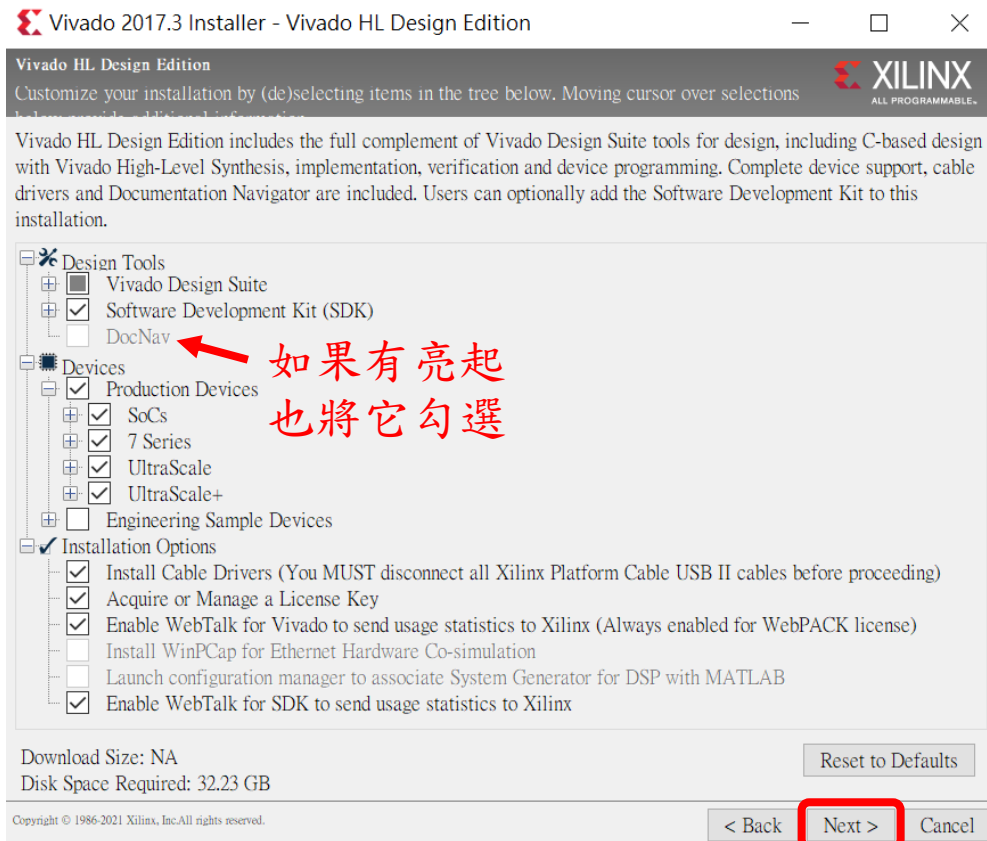
Vivado軟體安裝 (6/9)

- 依照下圖紅框勾選 -> Next



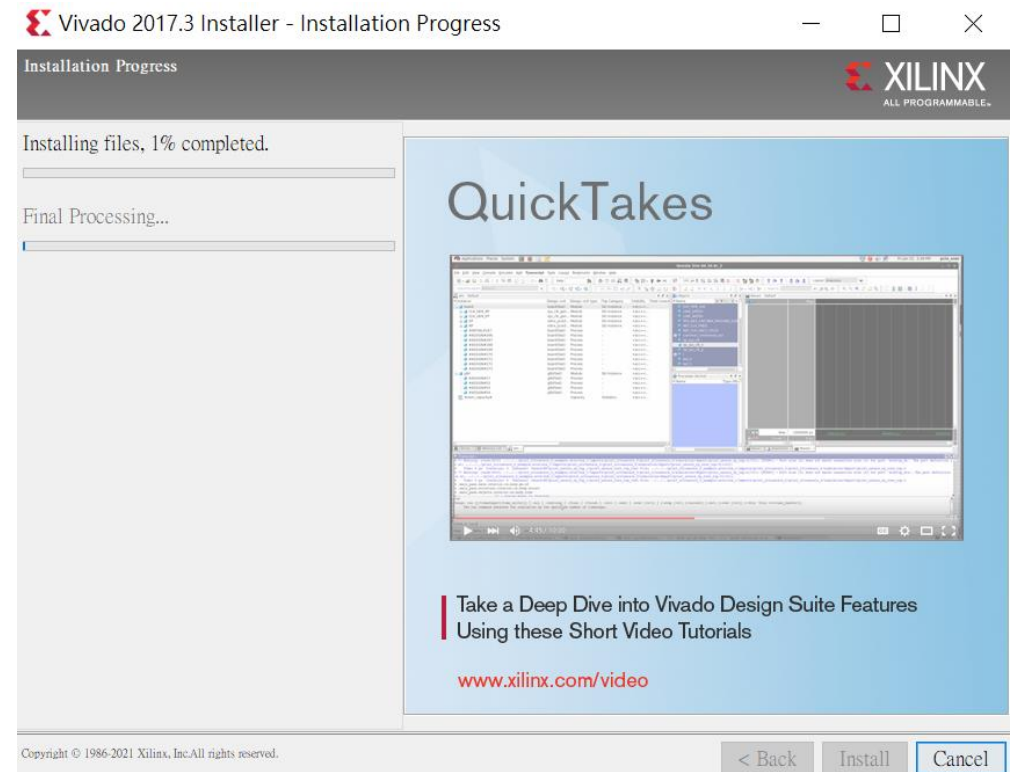
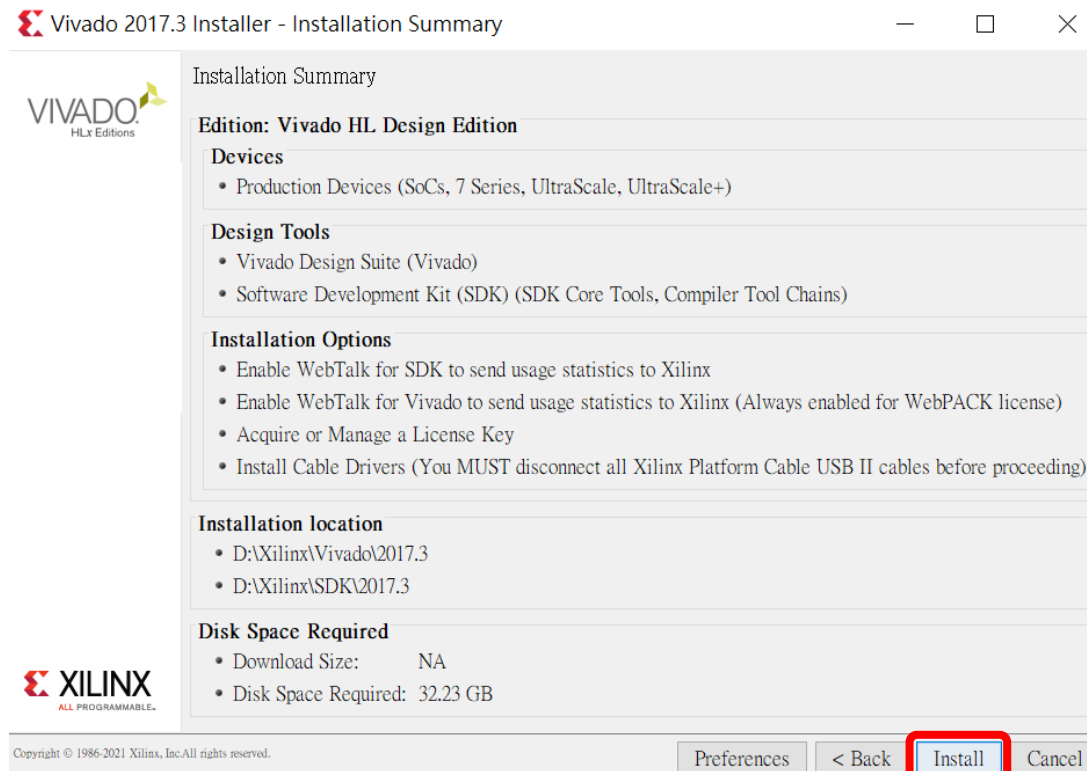
Vivado軟體安裝 (7/9)

- 依照左圖勾選 -> Next -> 選擇安裝路徑 -> Next



Vivado軟體安裝 (8/9)

- Next -> 等待安裝完成



Vivado軟體安裝 (9/9)

- 開啟Vivado軟體 -> Help -> Manage License -> Load License -> Copy License-> 選取vivado License 資料夾中的xilinx_full.lic

