DD lab3
Digilent Nexys4 FPGA Board & Xilinx Vivado Development Suite

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Outline

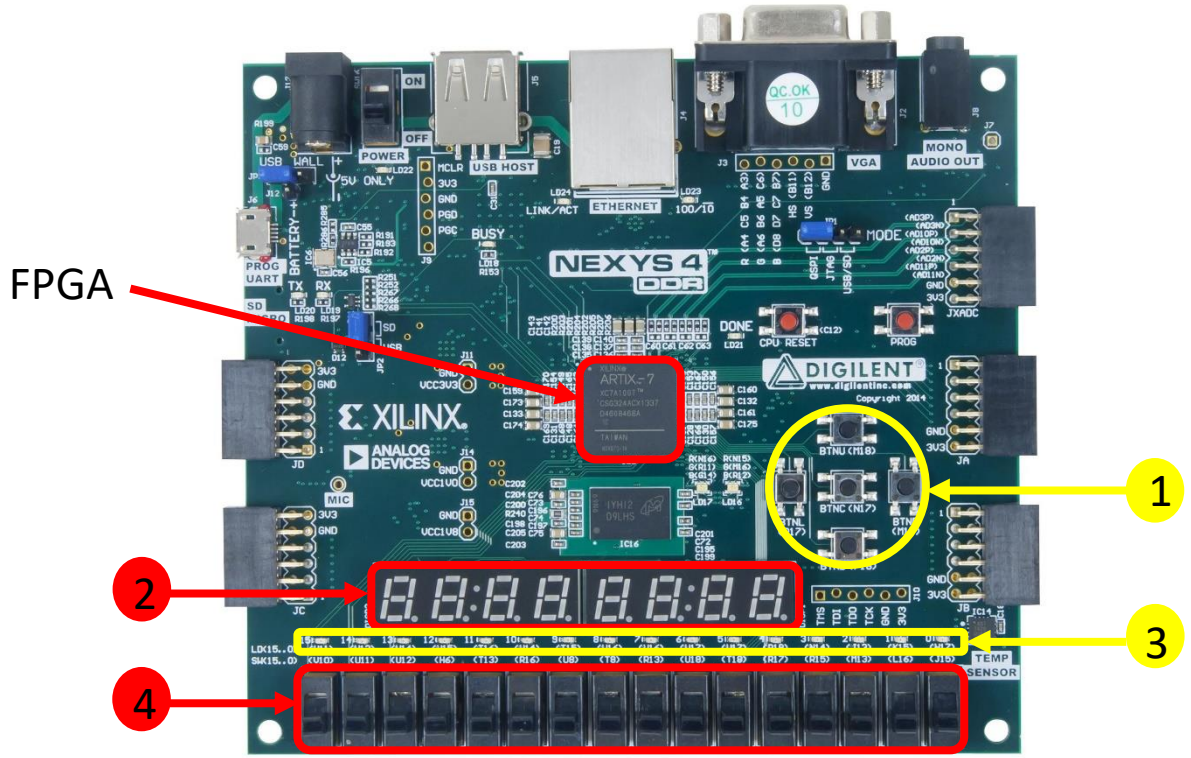
- 課程目的
- 課程工具
- 課程實驗
- Lab作業
- 課程評分方式
- 附錄

課程目的

在Lab3的課程中，同學們將學會如何利用Vivado開發工具將設計電路燒錄到Nexys4 FPGA開發板上，並透過Nexys4 FPGA開發板上的Switches及LEDs等周邊元件來驗證RTL電路設計的正確性

課程工具

- Nexys4上的FPGA可以用RTL code來描述電路行為
- Nexys4上有按鈕開關、 LED、七段顯示器以及指撥開關等開發板周邊元件，可以用來作為FPGA的輸入與輸出



	周邊元件
1	Push Button
2	7 segment display
3	LED
4	Switch

課程實驗

- 使用16個Switches (SW0 – SW15)分別控制16個LEDs (LED0 – LED15)的亮滅

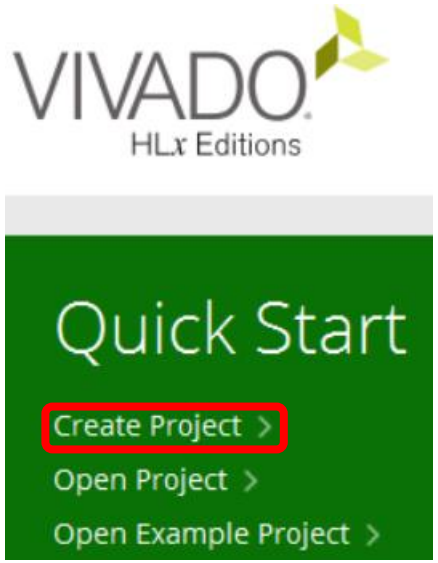
LED輸出結果

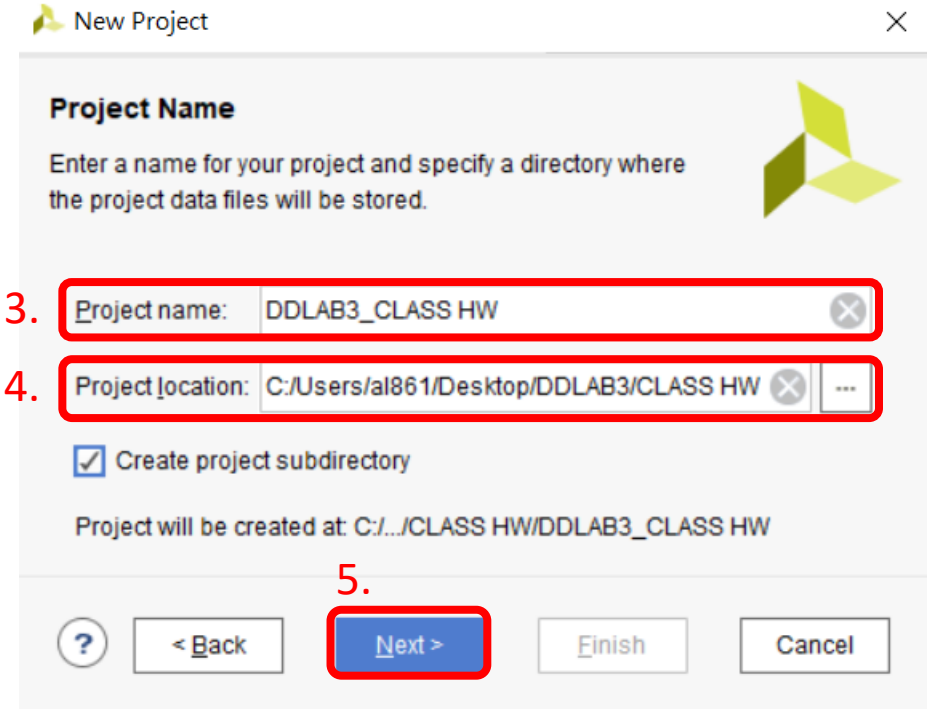
SW輸入

- 實驗教學內容
  - 使用Vivado建立專案
  - 使用Vivado創立專案原始檔
  - .xdc檔設定
  - 生成.bit檔並燒錄至Nexys4上

Vivado建立專案 (1/3)

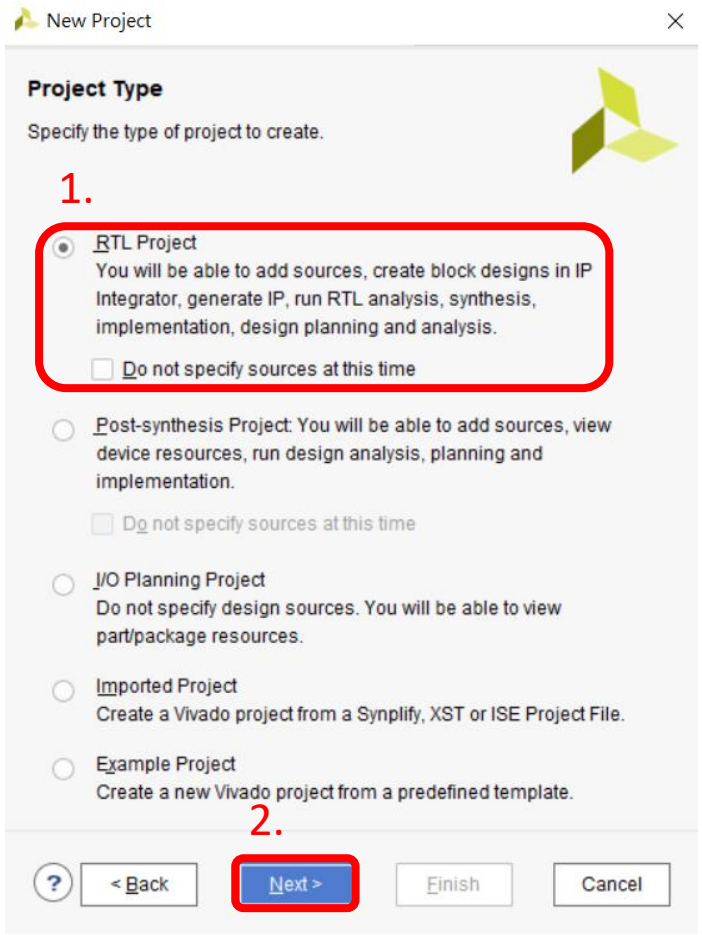
- 練習建立Vivado專案
  - 開啟Vivado軟體 -> Create Project -> Next -> 輸入專案名稱 -> 選擇專案位置 -> Next

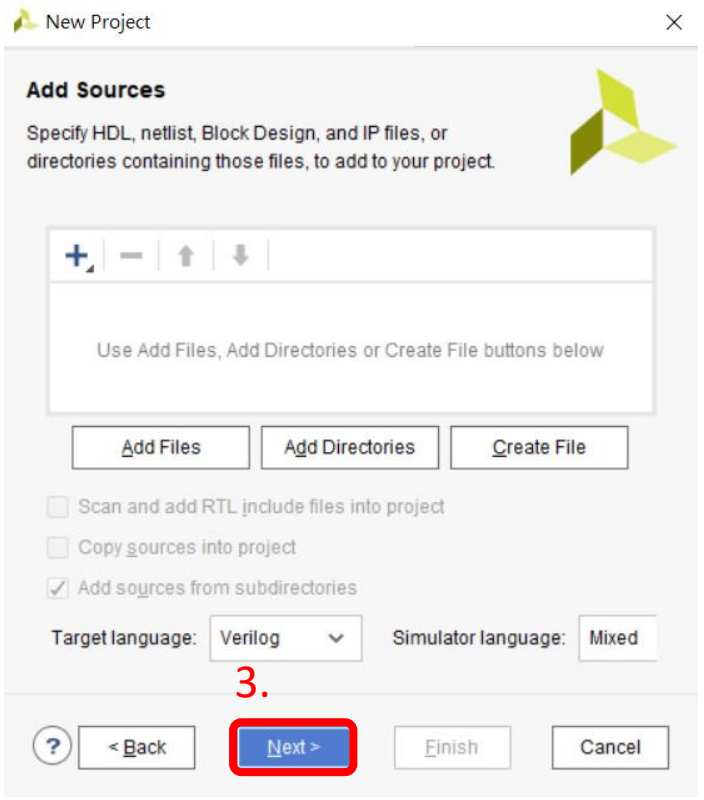


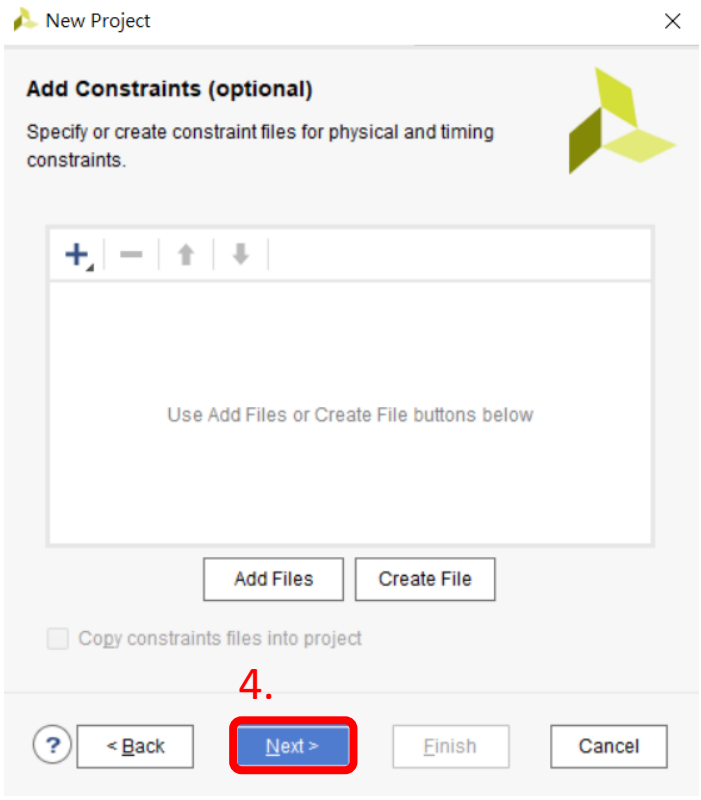


Vivado建立專案 (2/3)

- 選擇RTL Project -> Next -> Next -> Next

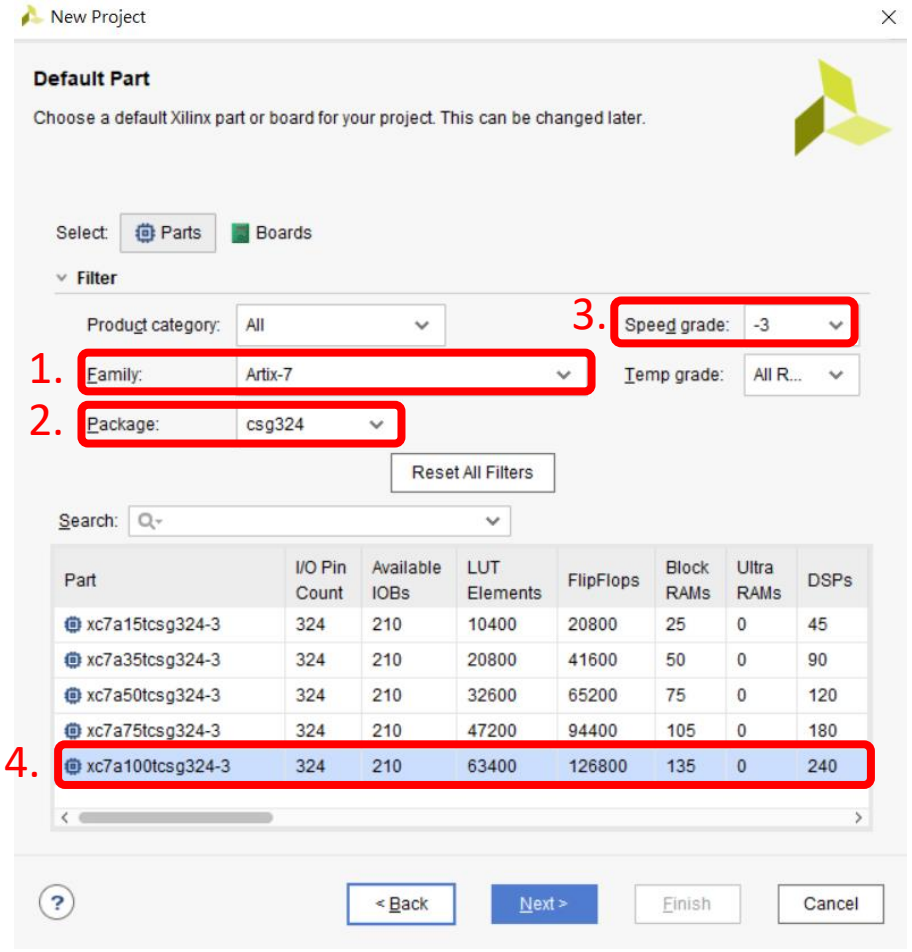


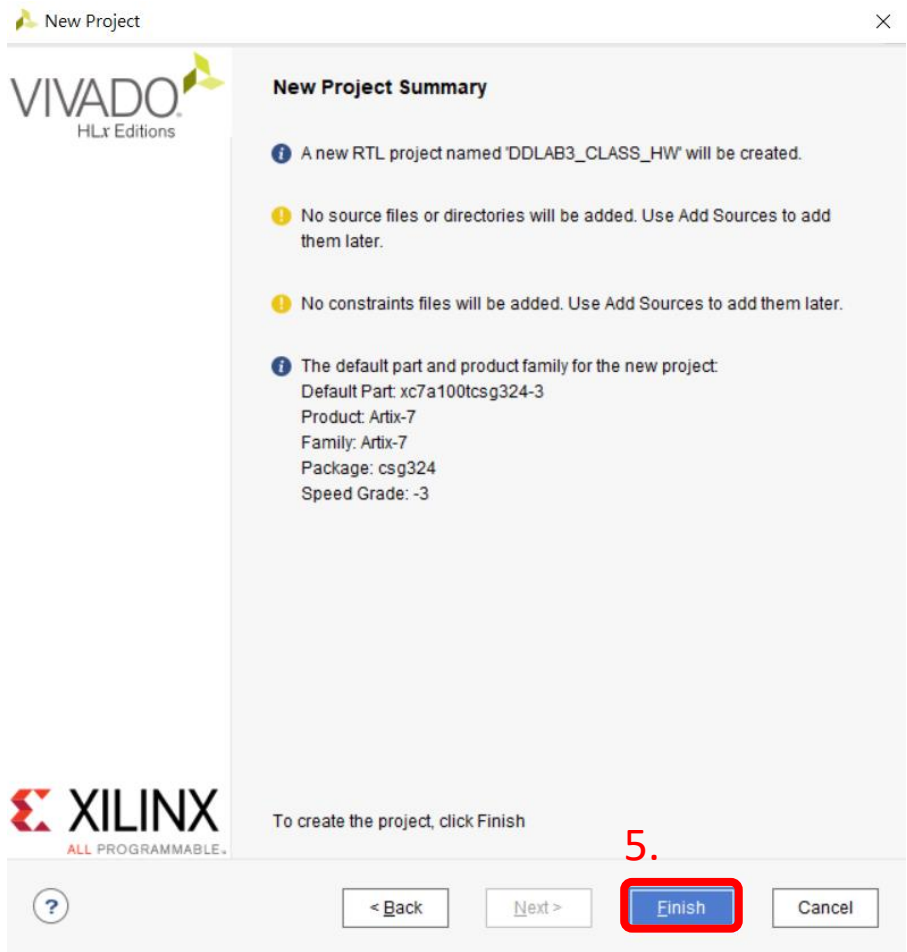




Vivado建立專案 (3/3)

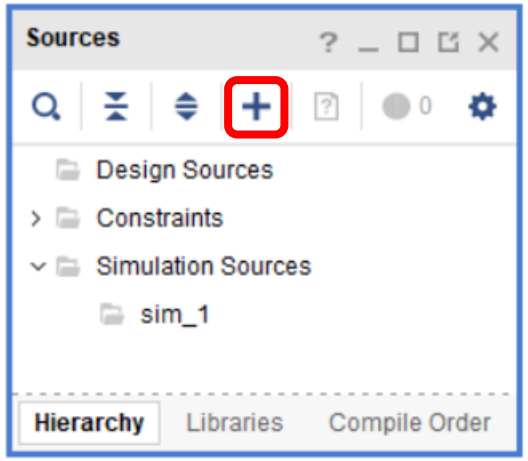
- Family選擇Artix-7 -> Package選擇csg324 -> Speed grade選擇-3 ->選擇xc7a100tcs324-3 -> Finish





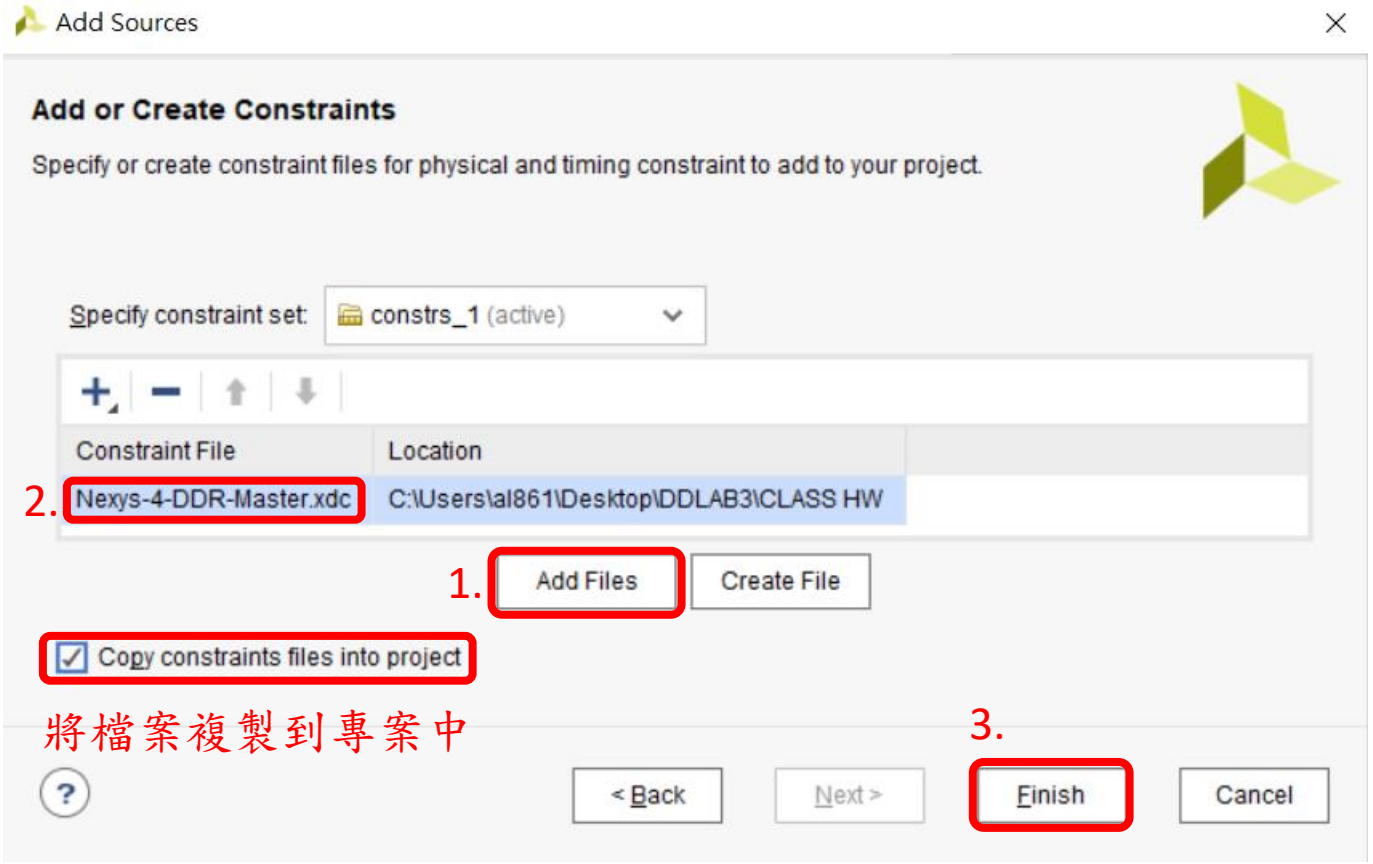
Vivado創建專案原始檔 (1/3)

- 點選+符號並選擇欲添加檔案的類型
  a) Add or create constraints
     - Constraints (.xdc檔)：用來描述.v檔與實體線路的連接關係
  b) Add or create design sources
     - design sources (.v檔)：用來描述電路行為



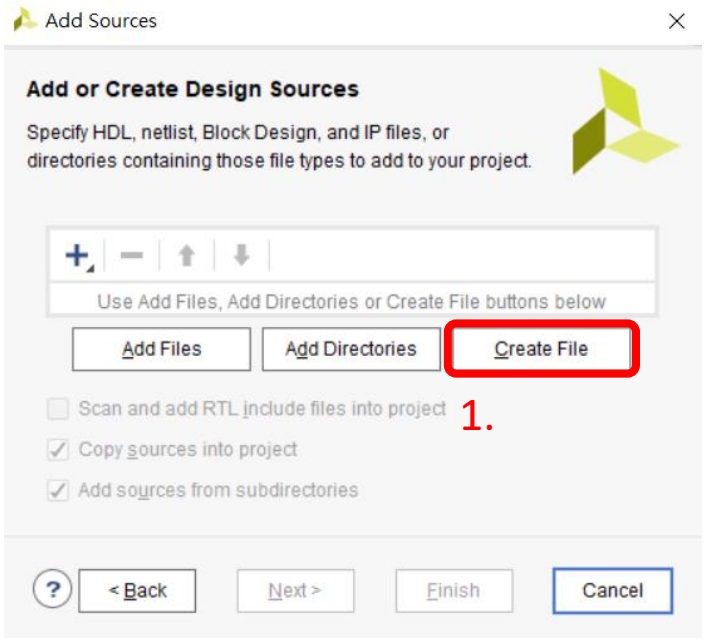
Vivado創建專案原始檔 (2/3)

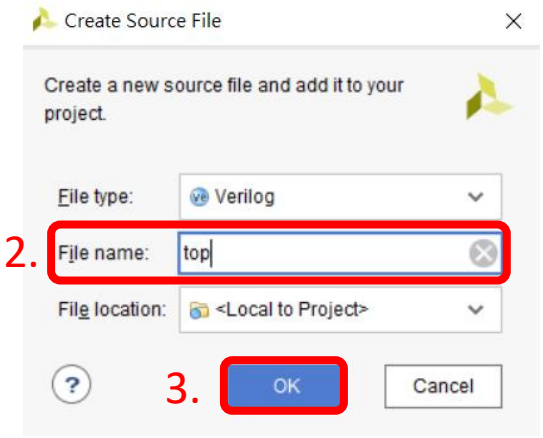
- 加入.xdc檔
  - 選擇Add or create constraints -> Next -> Add Files -> 選擇Nexys-4-DDR-Master.xdc -> Finish

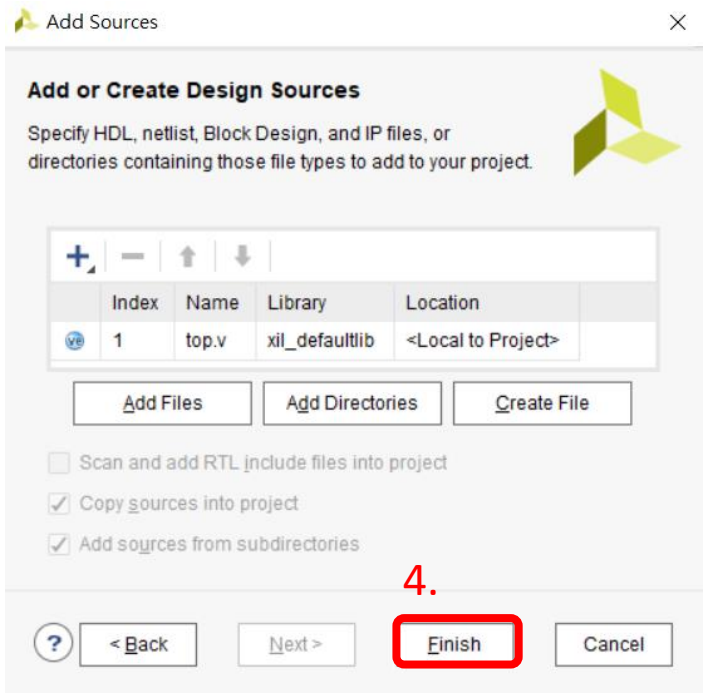


Vivado創建專案原始檔 (3/3)

- 建立.v檔：
  - 選擇Add or create design sources -> Next -> Create File -> 輸入檔案名稱 -> OK -> Finish







設定.xdc檔

- Xilinx Design Constraints file (簡稱為xdc file)
  - .xdc檔為開發板上的周邊元件設定檔
  - 根據開發板上的需要用的元件PIN腳的名稱做設定

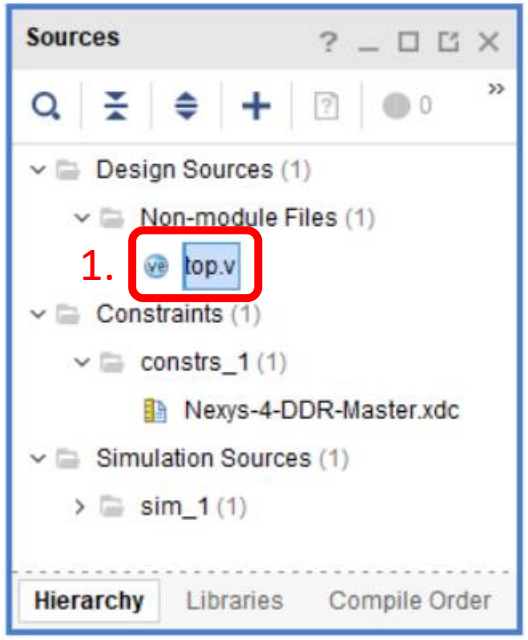
對應.v檔中定義的input及output名稱

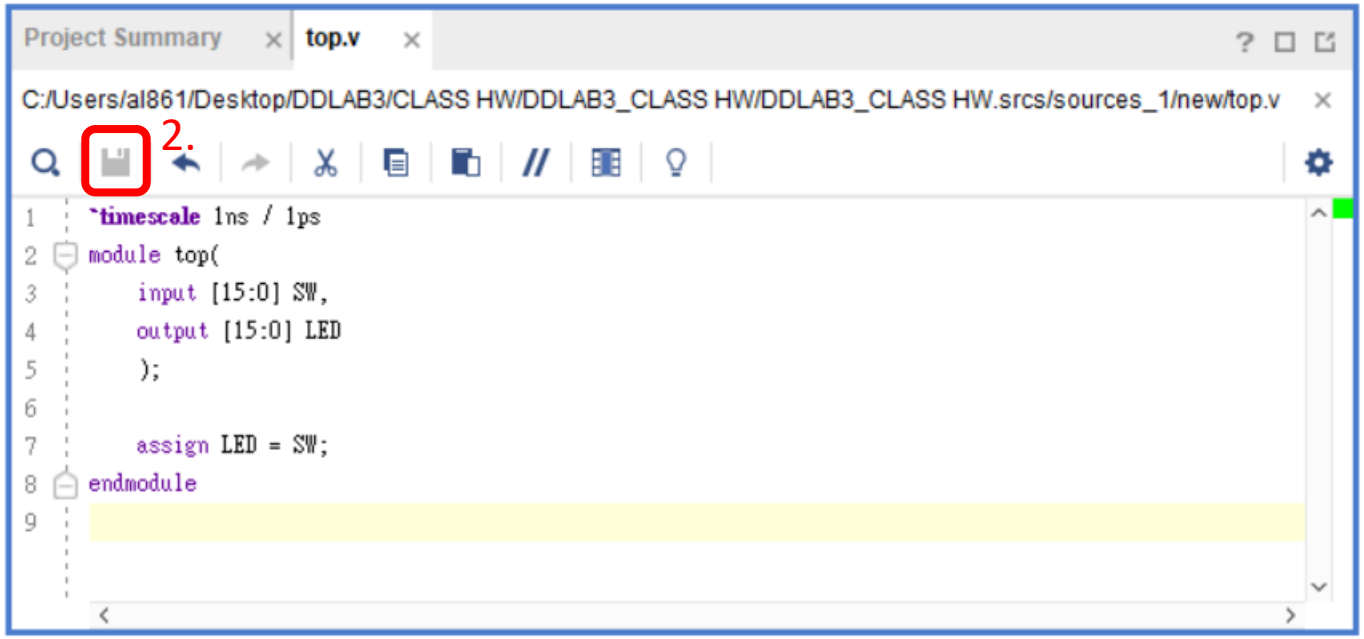
```
set_property -dict { PACKAGE_PIN J15   IOSTANDARD LVCMOS33 } [get_ports { SW[0] }]; #IO_L24N_T3_RS0_15 Sch=sw[0]
set_property -dict { PACKAGE_PIN L16   IOSTANDARD LVCMOS33 } [get_ports { SW[1] }]; #IO_L3N_T0_DQS_EMCCLK_14 Sch=sw[1]
set_property -dict { PACKAGE_PIN M13   IOSTANDARD LVCMOS33 } [get_ports { SW[2] }]; #IO_L6N_T0_D08_VREF_14 Sch=sw[2]
set_property -dict { PACKAGE_PIN R15   IOSTANDARD LVCMOS33 } [get_ports { SW[3] }]; #IO_L13N_T2_MRCC_14 Sch=sw[3]
set_property -dict { PACKAGE_PIN R17   IOSTANDARD LVCMOS33 } [get_ports { SW[4] }]; #IO_L12N_T1_MRCC_14 Sch=sw[4]
set_property -dict { PACKAGE_PIN T18   IOSTANDARD LVCMOS33 } [get_ports { SW[5] }]; #IO_L7N_T1_D10_14 Sch=sw[5]
set_property -dict { PACKAGE_PIN U18   IOSTANDARD LVCMOS33 } [get_ports { SW[6] }]; #IO_L17N_T2_A13_D29_14 Sch=sw[6]
set_property -dict { PACKAGE_PIN R13   IOSTANDARD LVCMOS33 } [get_ports { SW[7] }]; #IO_L5N_T0_D07_14 Sch=sw[7]
```

對應開發板上的PIN腳名稱

課堂練習範例程式碼

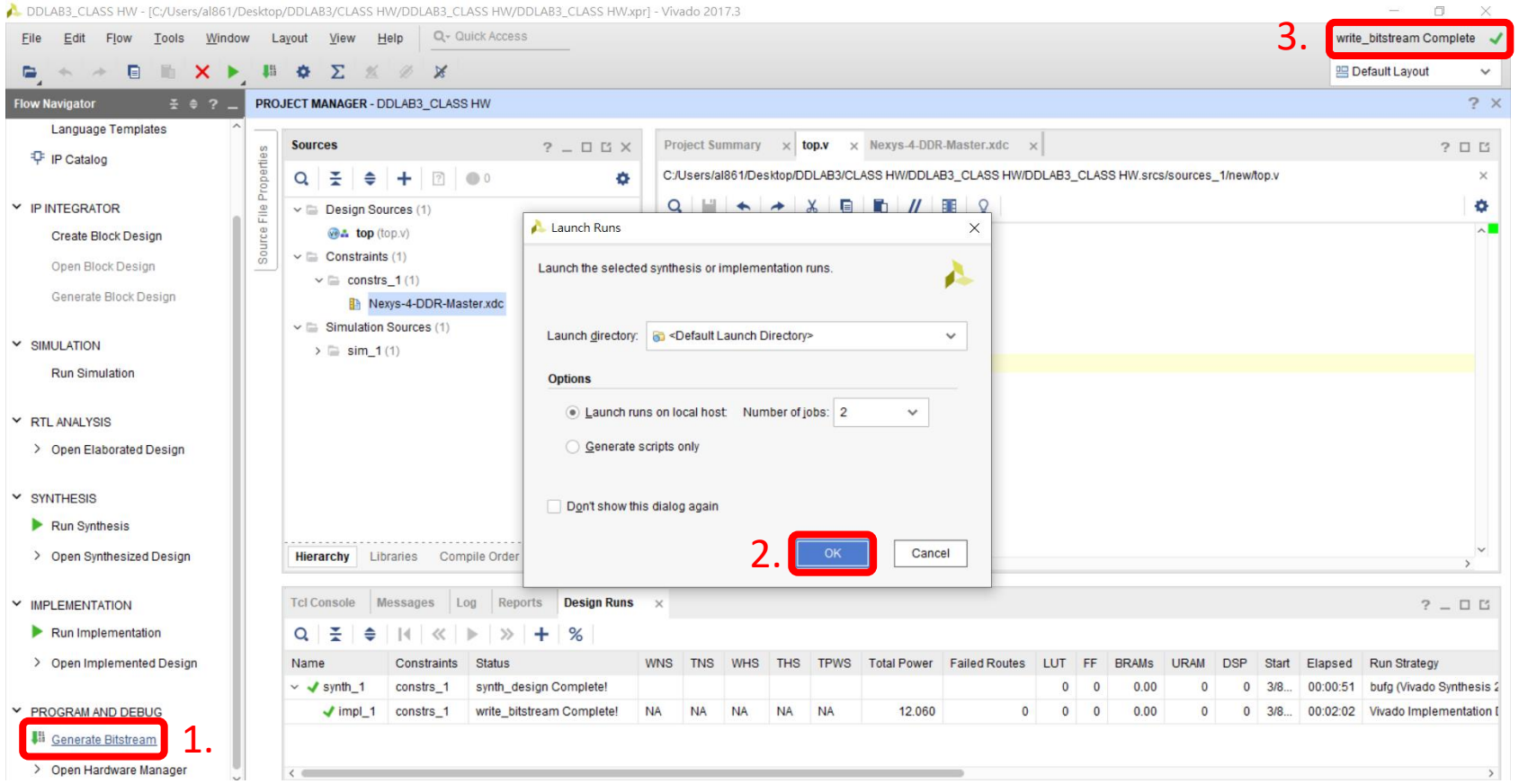
- 在左方欄位中的Design Source中找到top.v打開 -> 輸入範例程式碼後並存檔





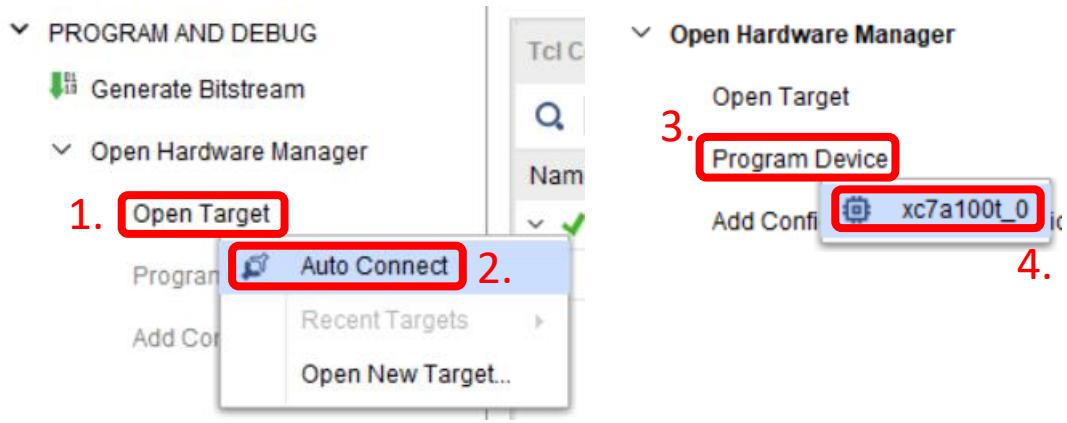
燒錄到FPGA驗證功能 (1/2)

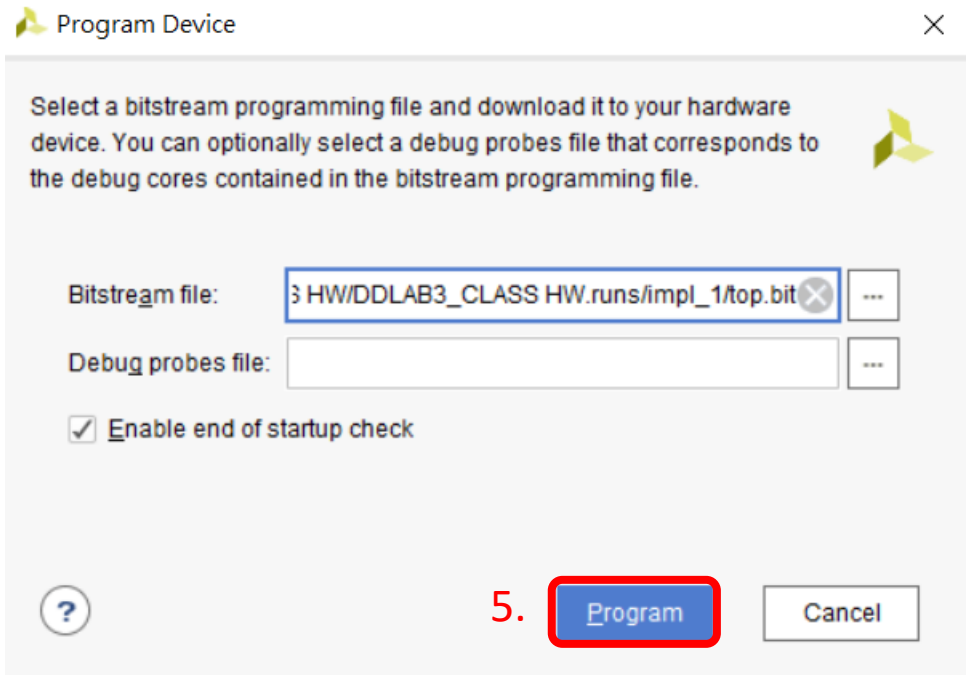
- 完成專案後將專案的電路燒錄到FPGA上驗證功能正確與否
  - 左下角欄位中選擇Generate bitstream -> OK -> 等待完成後右上角會出現成功訊息√



燒錄到FPGA驗證功能 (2/2)

- 打開Nexys4的電源 -> Open Target -> Auto Connect -> Program Device -> xc7a100t_0 -> Program
  - 燒錄上FPGA後確認switches是否可以控制對應的LEDs的亮滅

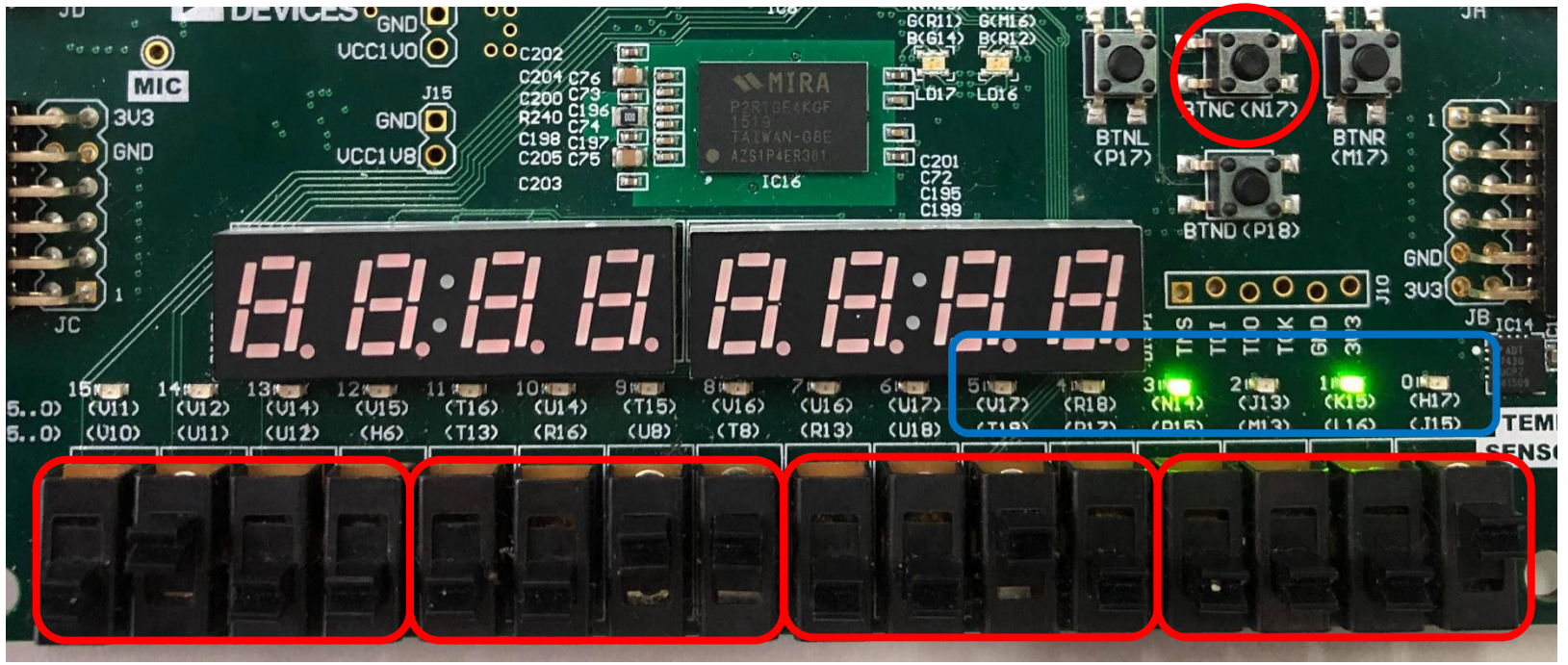




Lab作業

- 將Lab1作業四個4-bits的加法器在FPGA上實作，使用Nexys4開發板上從右到左每四個Switches當作一個input，當按下Button(N17)，就會將加法器四個input相加結果以binary形式更新到LEDs上，相加結果以6-bits來表示

按下Button即將相加結果更新



相加結果

Input d[3:0] Input c[3:0] Input b[3:0] Input a[3:0]

課程評分

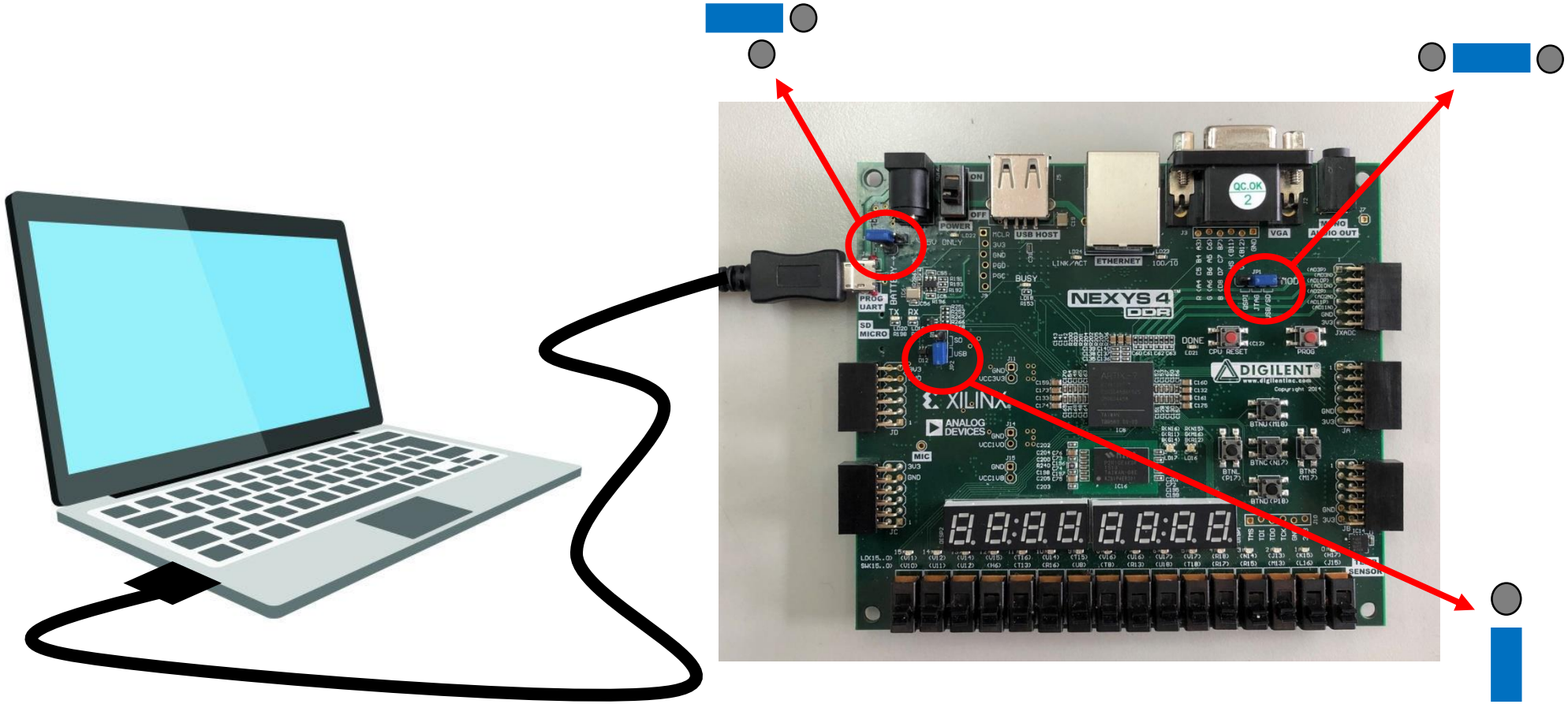
- Demo時間：2021.3.29(一)、4.7(三)，按照規定Demo時間自行前往Demo地點
- Demo地點：資工館501A
- 攜帶檔案：bitstream (.bit檔) (可以在創建專案的資料夾 -> .runs -> impl_1中找到)
- 課程評分方式
  - 加法器四個input相加結果正確，並可以透過按下Button將相加結果更新到LED燈上(100%)

附錄

- 實驗環境架設
- Vivado軟體安裝

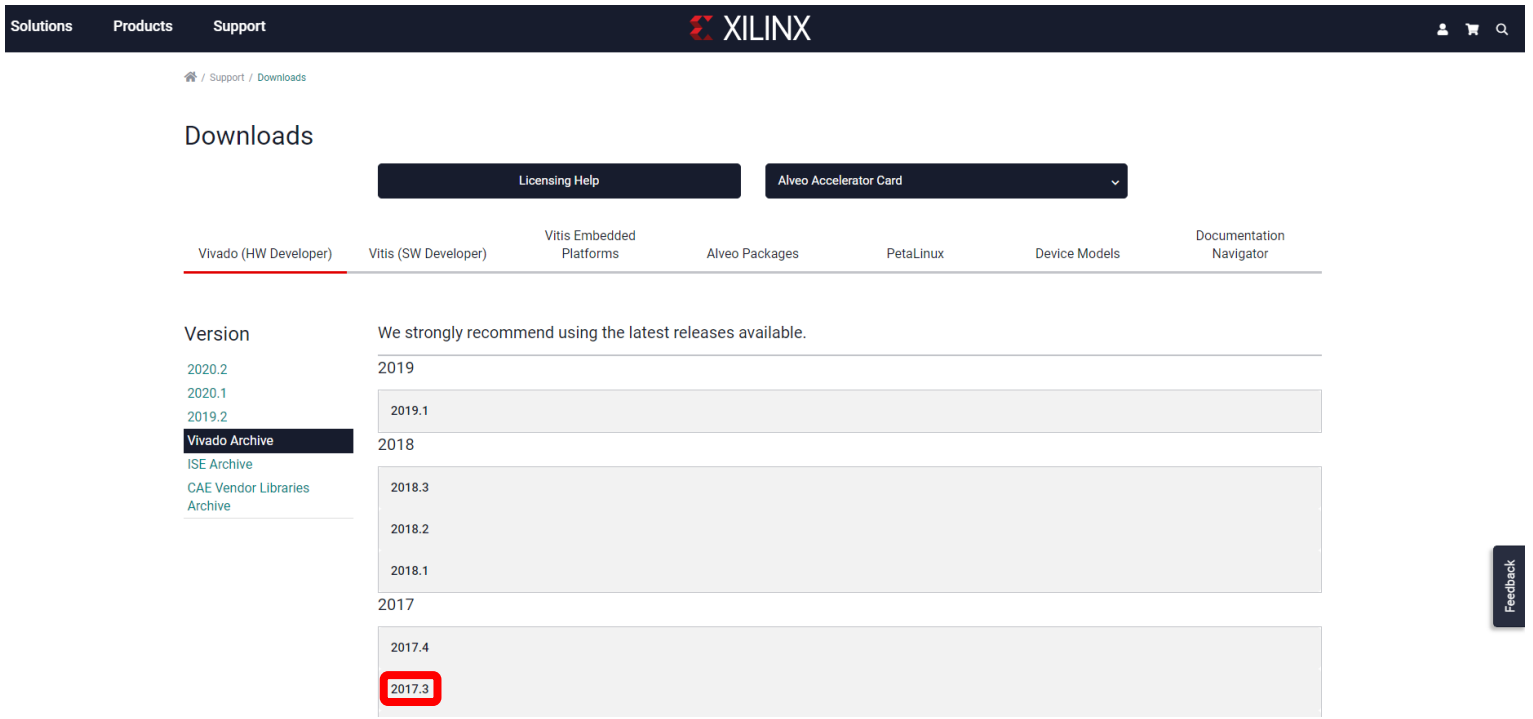
實驗環境架設

- 請同學們使用前請先檢查一下Nexys4 FPGA開發板上的3個Jumper是否與下圖一致，若有不同可能會造成Nexys4 FPGA開發板無法正常動作



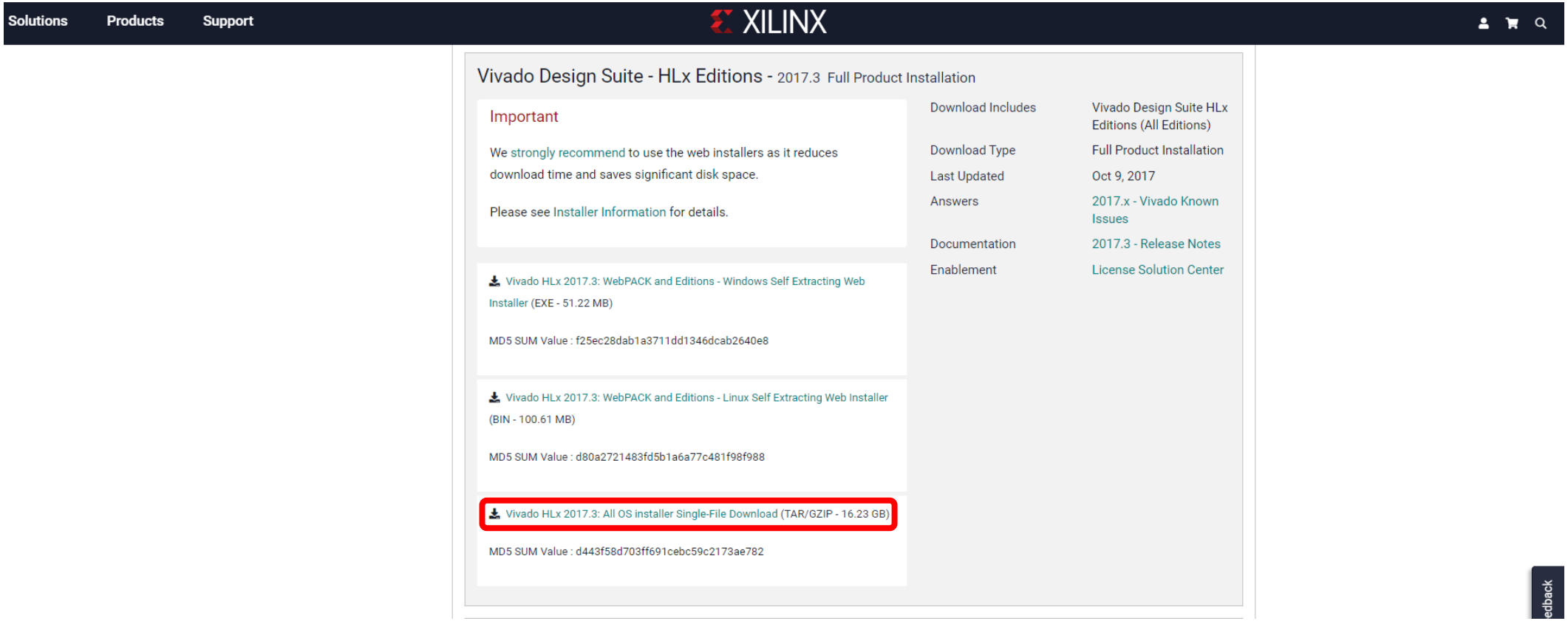
Vivado軟體安裝 (1/9)

- 下載網址超連結 -> https://www.xilinx.com/support/download/index.html/content/xilinx/en/downloadNav/vivado-design-tools/archive.html
- 選擇2017.3



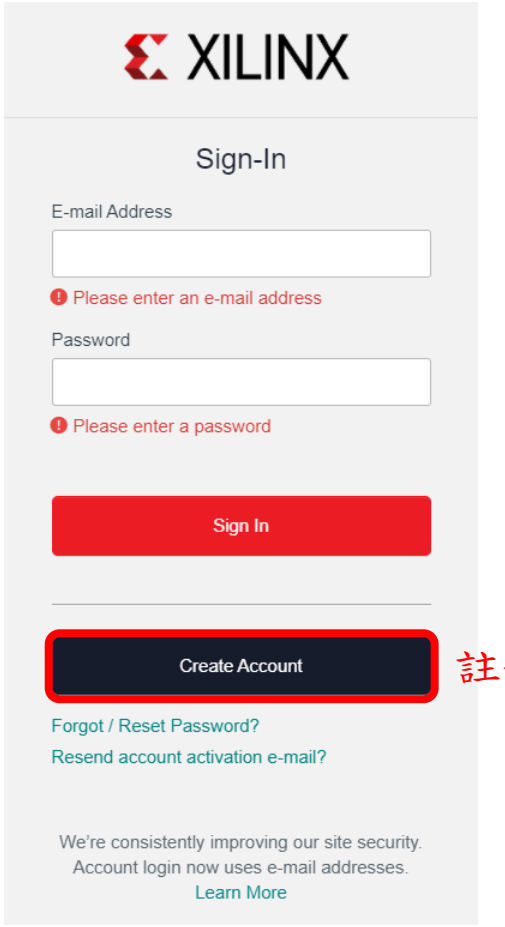
Vivado軟體安裝 (2/9)

- 選擇All OS版本

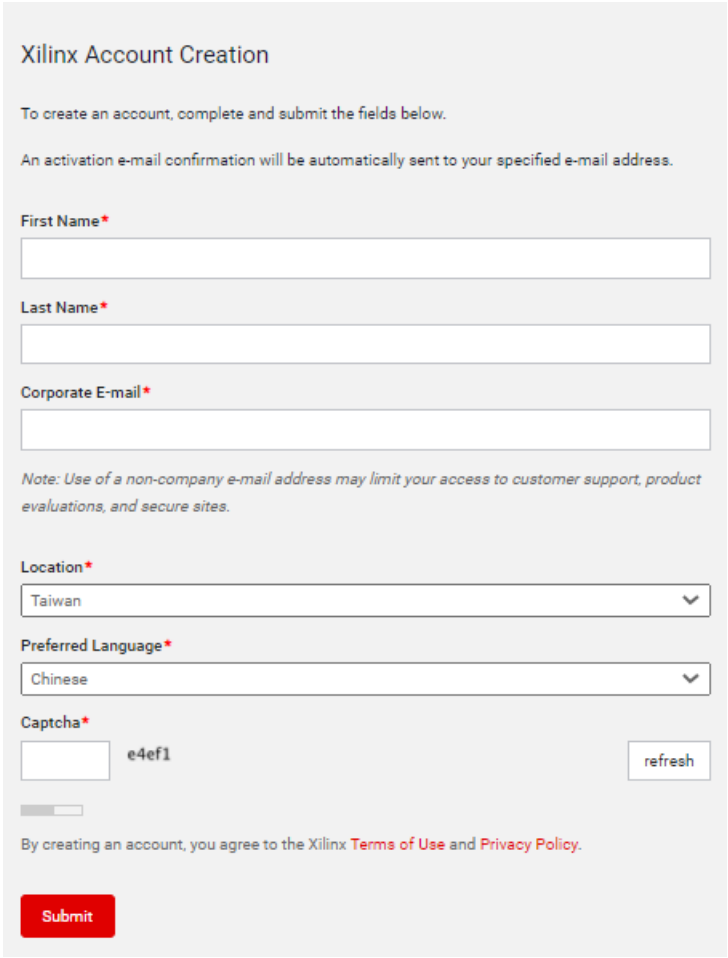


Vivado軟體安裝 (3/9)

- 註冊XILINX帳號 -> 填寫資料 -> E-mail認證

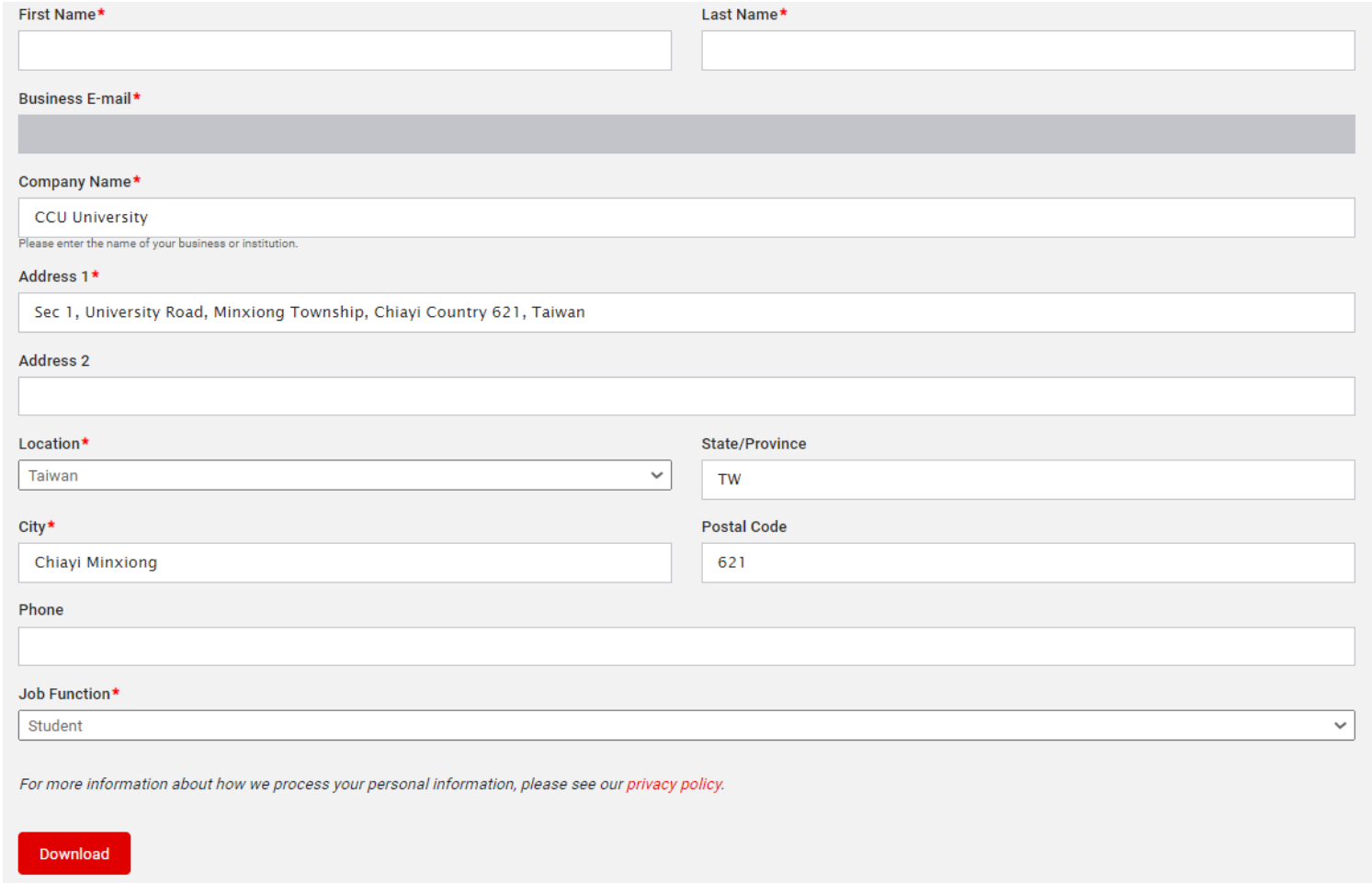


註冊XILINX帳號



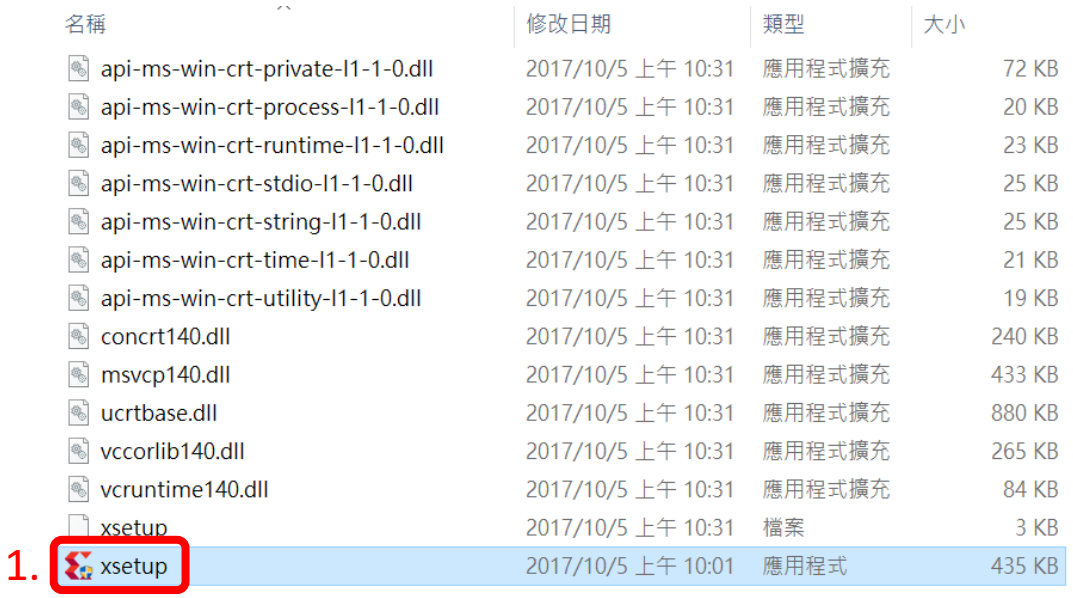
Vivado軟體安裝 (4/9)

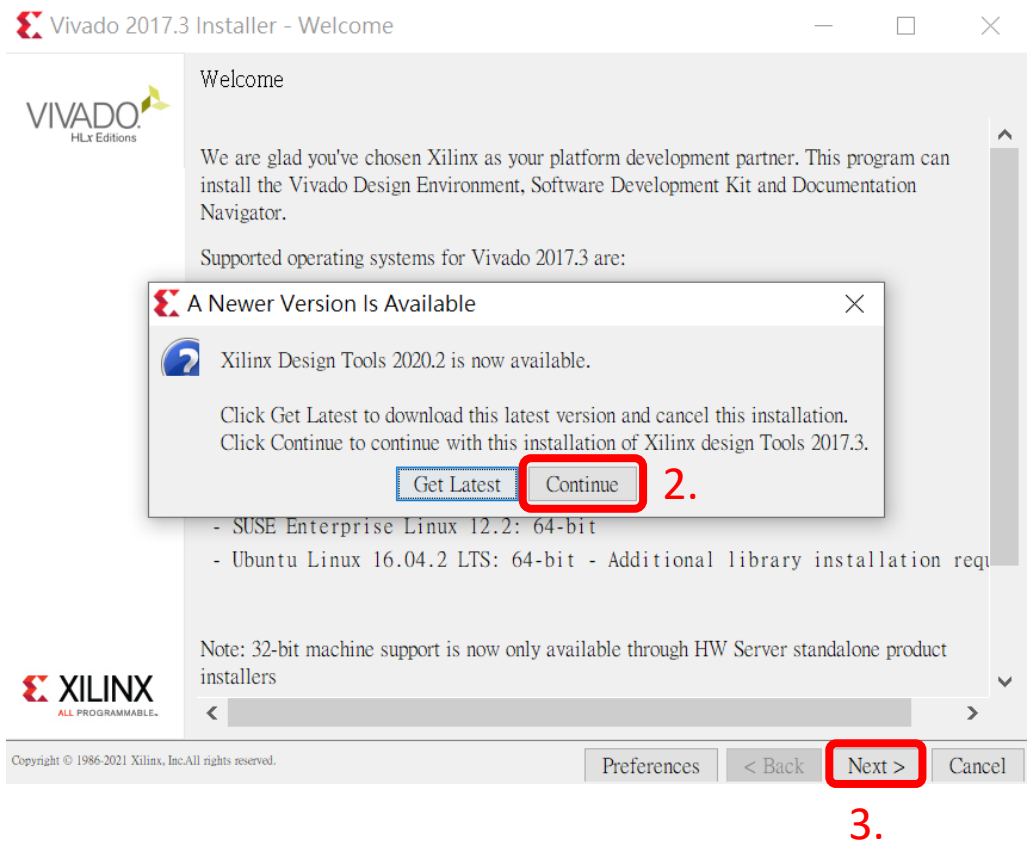
- 登入完成填寫資料後開始下載Vivado軟體



Vivado軟體安裝 (5/9)

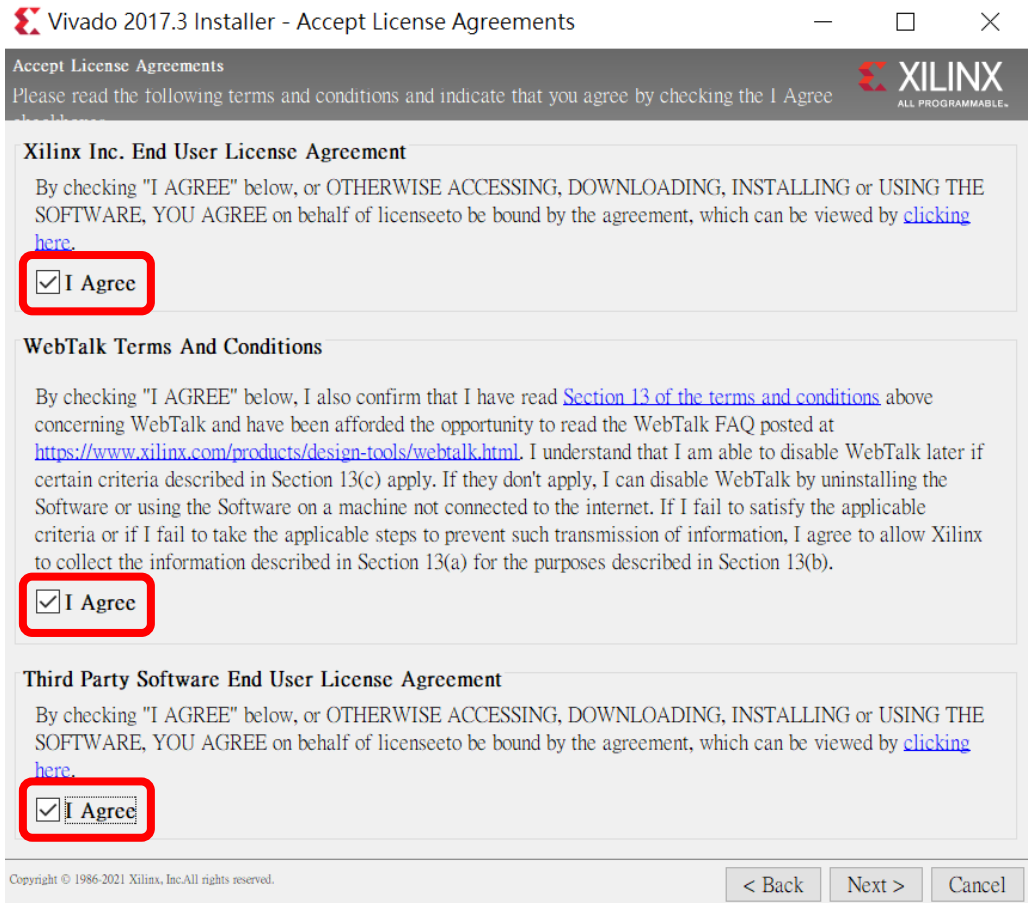
- 下載完成後解壓縮檔案 -> 點選xsetup -> Continue -> Next

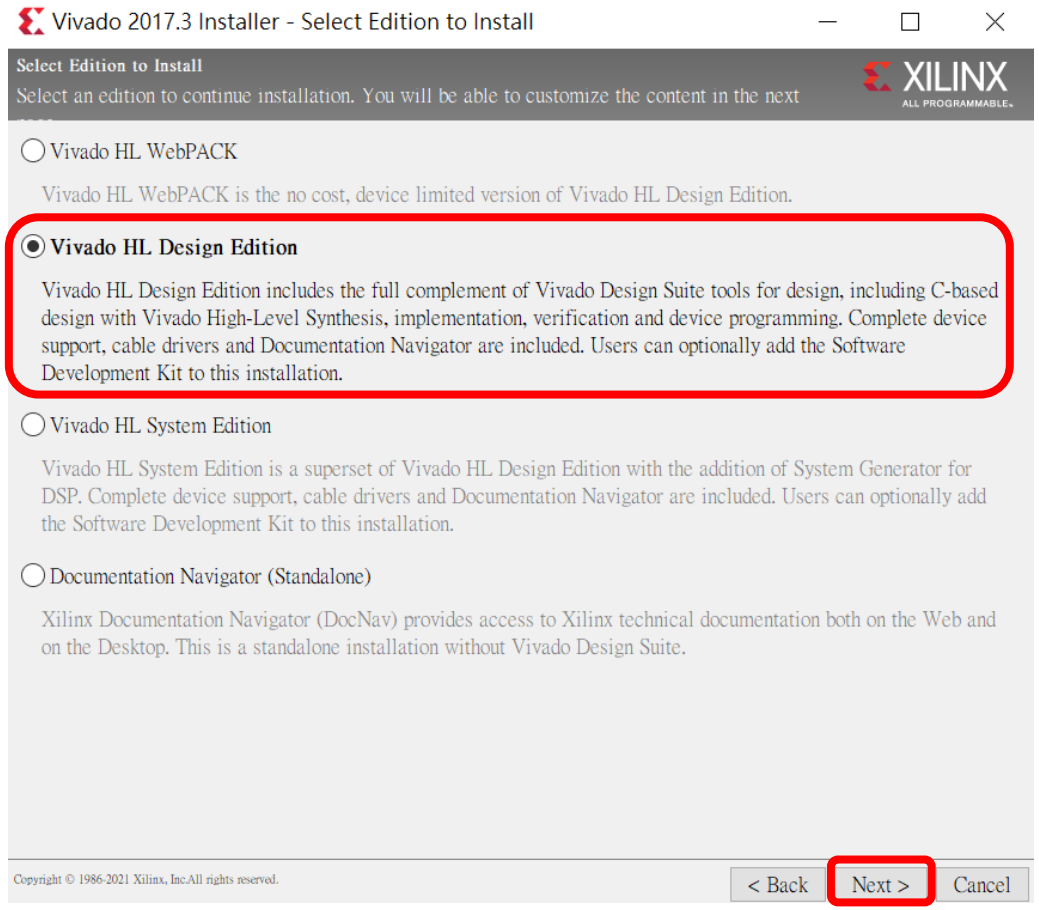




Vivado軟體安裝 (6/9)

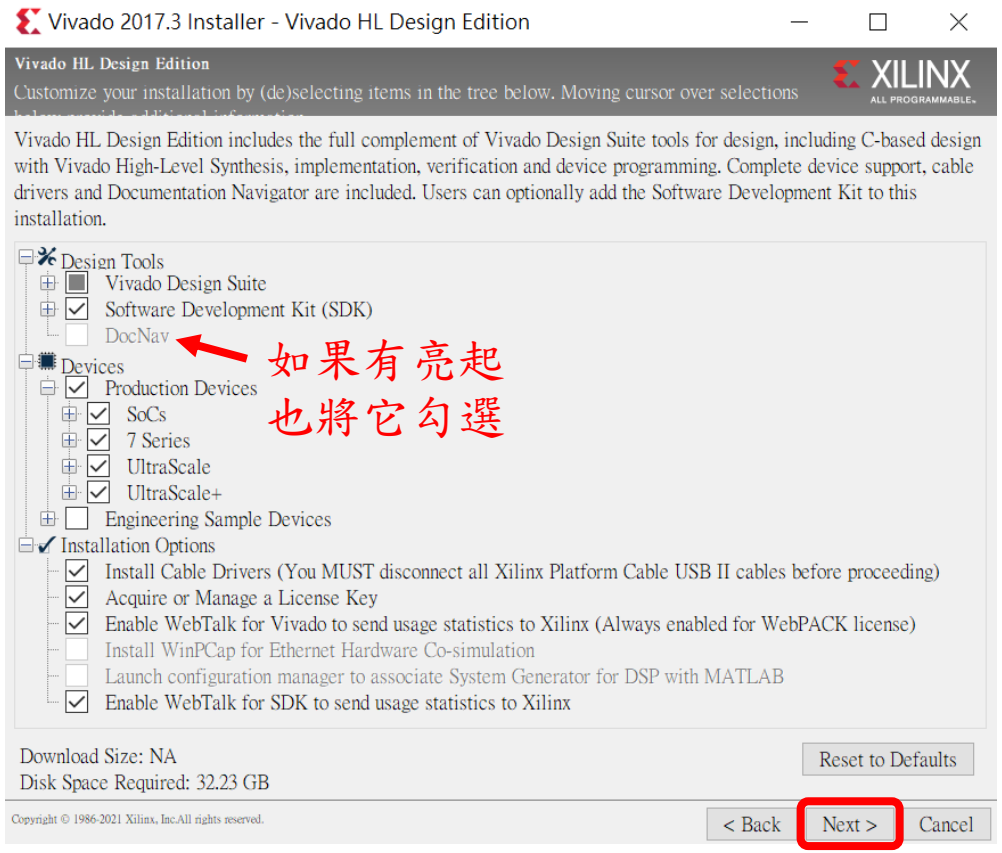
- 依照下圖紅框勾選 -> Next

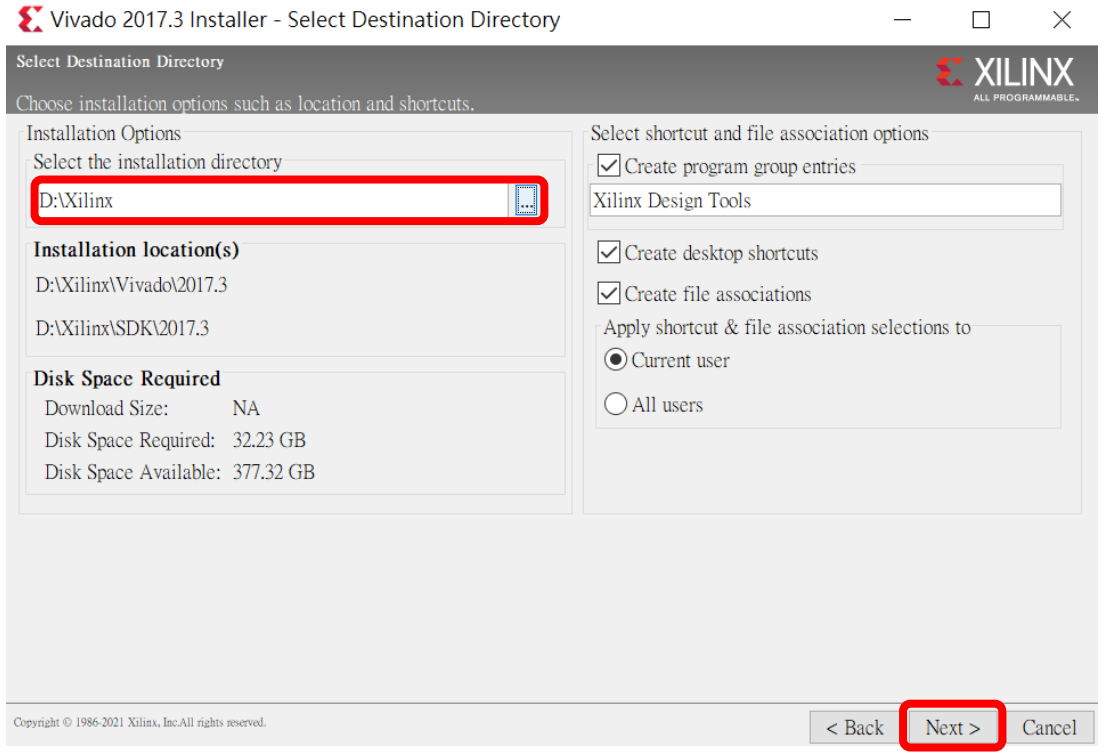




Vivado軟體安裝 (7/9)

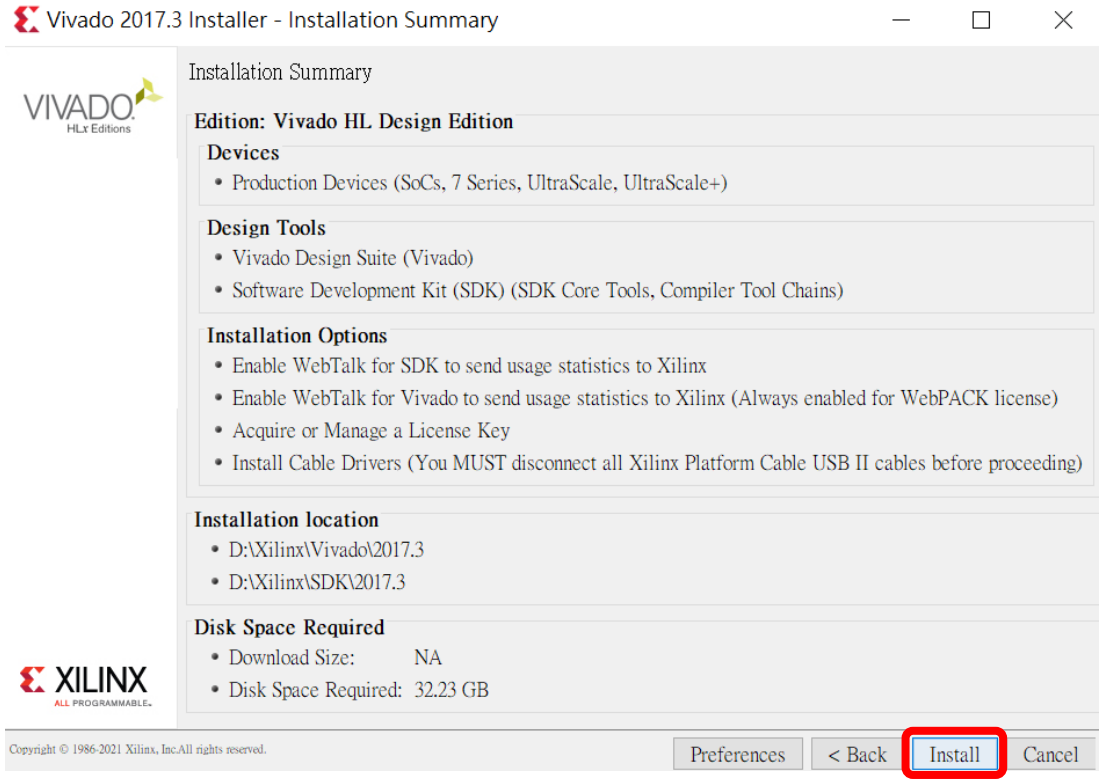
- 依照左圖勾選 -> Next -> 選擇安裝路徑 -> Next

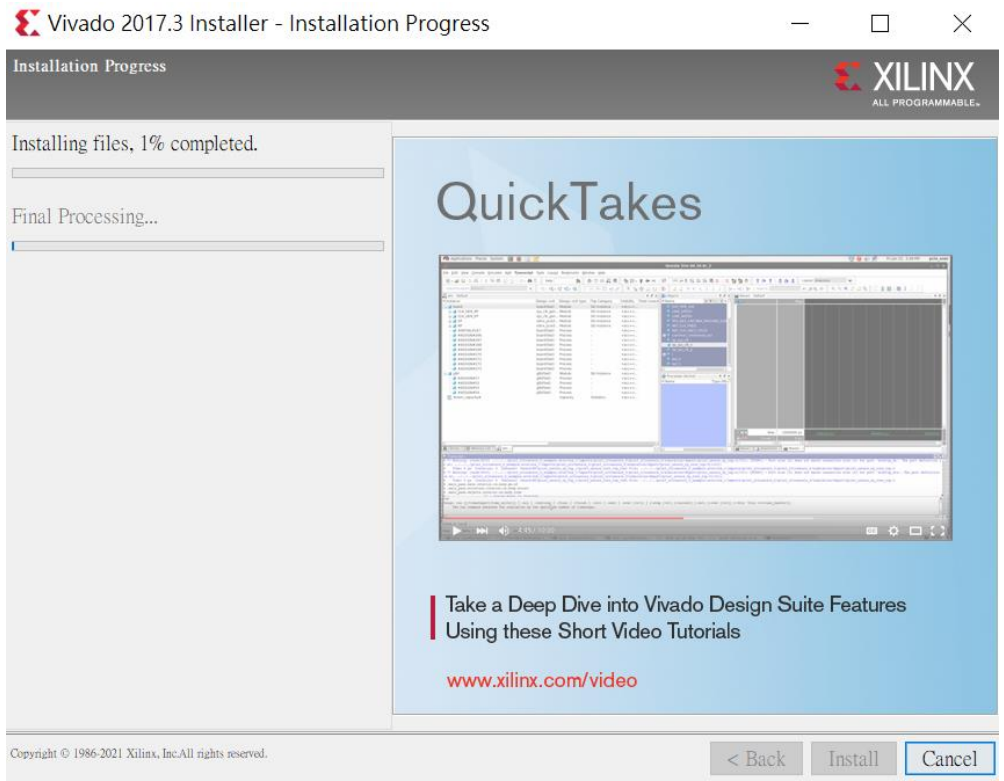




Vivado軟體安裝 (8/9)

- Next -> 等待安裝完成





Vivado軟體安裝 (9/9)

- 開啟Vivado軟體 -> Help -> Manage License -> Load License -> Copy License-> 選取vivado License資料夾中的xilinx_full.lic