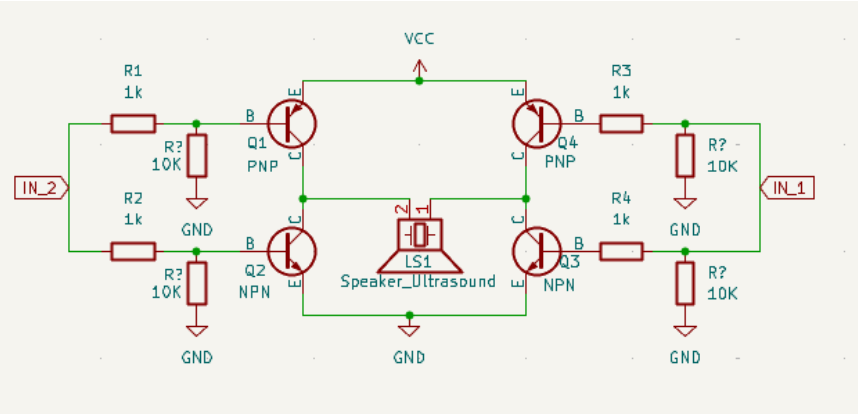
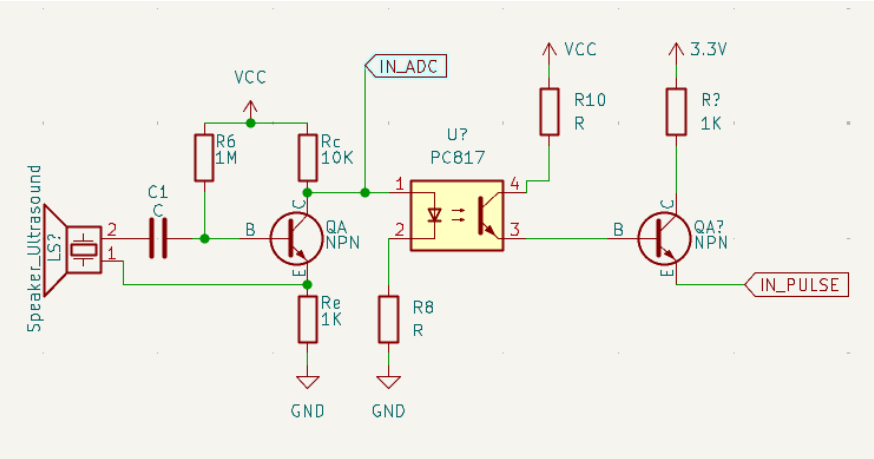
(Schematics)

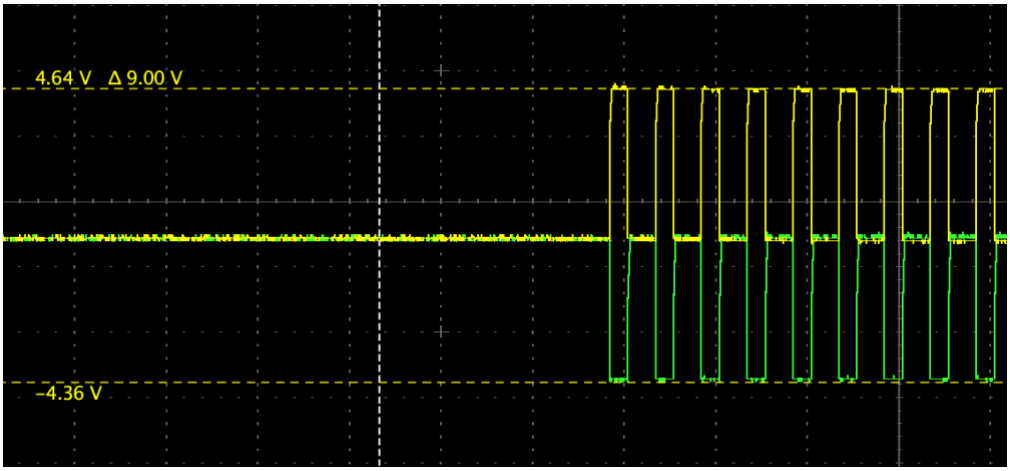
The H_bridge has 2 inputs which oscillate (1,0)(0,1) in (IN_1,IN_2) this allows 2 x source voltage as pulses. Works since PNP uses low to close and NPN as high so by suing potential dividers only need 2 input for reverse polarity from a given port.



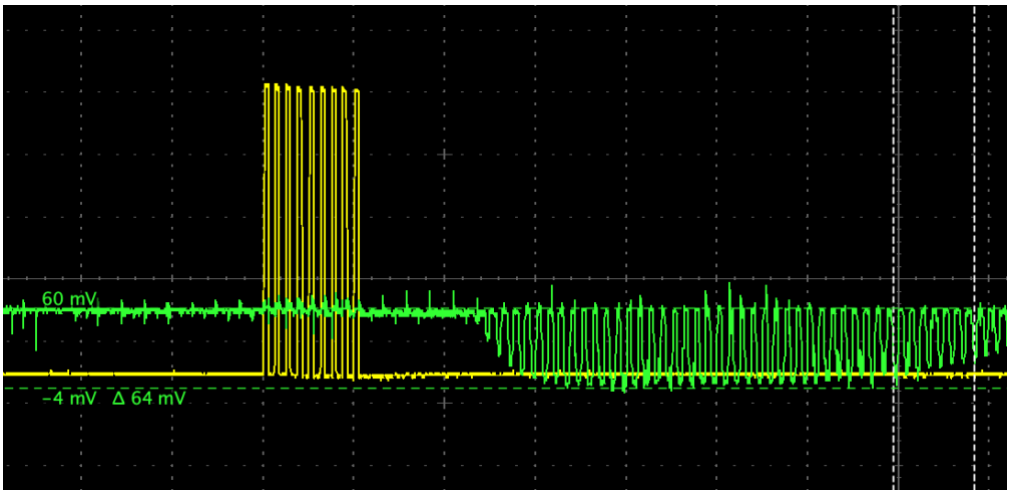
Output is at piezo, the amplifier stage has input PIEZO and output IN_ADC & IN_PULSE. The ADC input is for the amplified raw signal to ADC, the IN_PULSE is for GPIO setting. I used both in my test circuit.



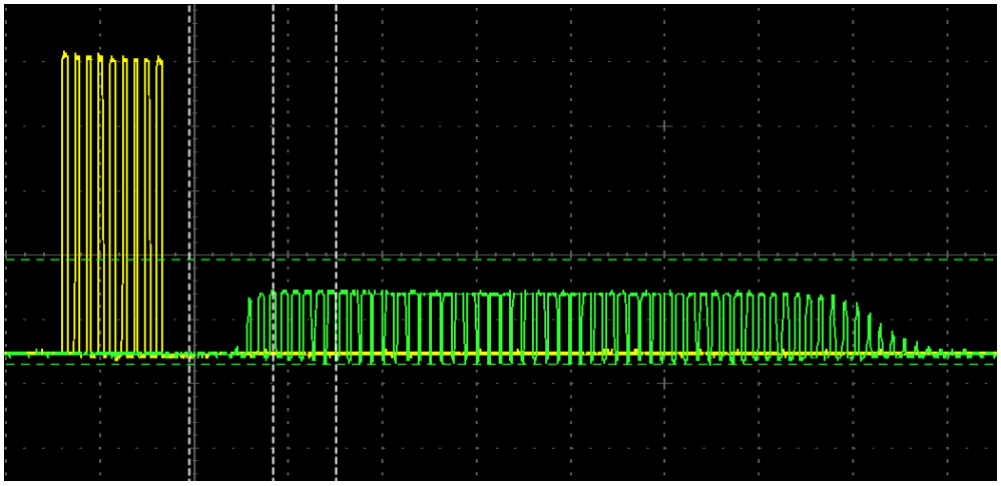
H_bridge output terminals to piezo transmitter:



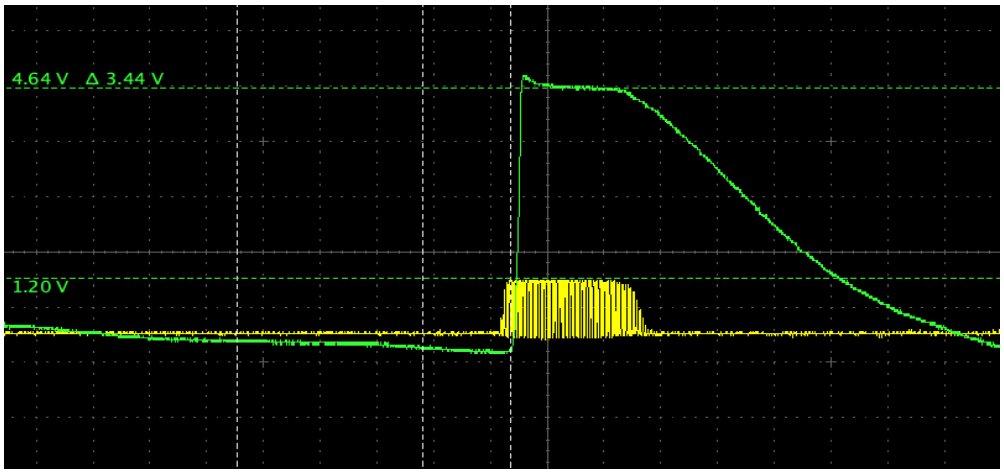
INPUT_PIEZO receiver: (60mv)



AMPLIFIED_OUPUT: (1.2V)

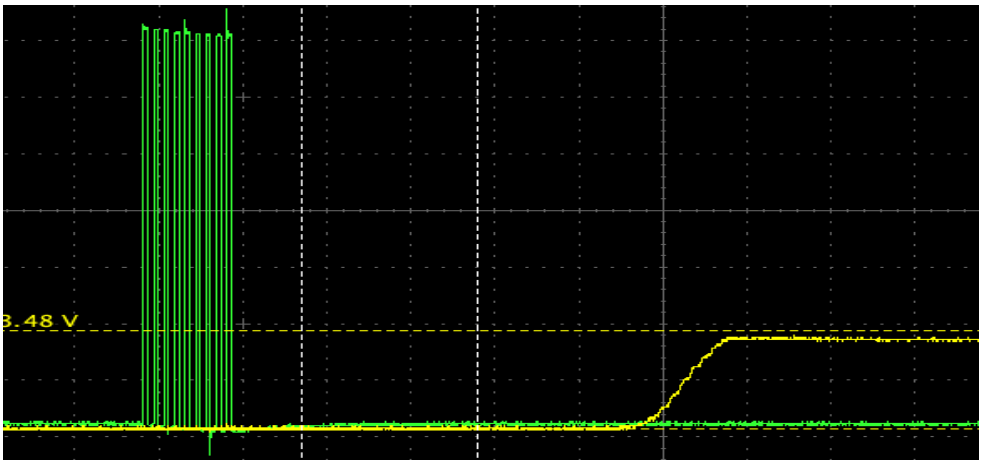


OPTO_OUTPUT: (4.6V)



The optocoupler is connected to VCC, the input and GND are between anode and cathode and output is connected to VCC, and to a logic NPN transistor base.

LOGIC_TRANSISTOR_OUTPUT: (3.3V)



The transistor output has its collector connected to 3.3V and emitter to GPIO In of Pico pulled down by a 10K resistor. The idea of using the transistor is to saturate the pulse at 3.3V and pull low below threshold to give a signal pulse with no noise at CMOS logic level.