TPD4E001-Q1 具有 1.5pF I/O 电容的 4 通道 ESD 保护阵列

1 特性

- 具有符合 AEC-Q100 标准的下列结果：
  - 器件温度等级 1：-40°C 至 +125°C 运行环境温度范围
  - 器件人体模型 (HBM) 静电放电 (ESD) 分类等级 3B
  - HBM 电平 15kV
  - 器件带电器件模型 (CDM) ESD 分类等级 C5
- IEC 61000-4-2 4 级 ESD 保护
  - ±8kV 接触放电
  - ±15kV 气隙放电
- IEC 61000-4-5 浪涌保护
  - 5.5A (8/20μs)
- 输入电容低至 1.5pF
- 最大泄漏电流低至 10nA
- 电源电压范围：0.9V 至 5.5V

2 应用

- 终端设备
  - 汽车音响主机
  - 汽车后座娱乐系统
  - 汽车后置摄像头系统
- 接口
  - USB 2.0
  - 以太网
  - 精密模拟接口

3 说明

TPD4E001-Q1 器件是一款低电容 TVS 二极管阵列，设计用于为通信线路中连接的敏感电子元件提供 ESD 保护。每个通道包含一对将 ESD 脉冲引导至 V_{CC} 或者 GND 的瞬态电压抑制二极管。根据 IEC 61000-4-2 国际标准规定，TPD4E001-Q1 可防止接触放电电压高达 ±8kV 和气隙放电高达电压 ±15kV 的 ESD 事件发生。该器件每通道的电容低至 1.5pF，因此非常适用于高速数据接口。低泄露电流（最大 10nA）确保了系统的最低功耗和模块接口的高精度。

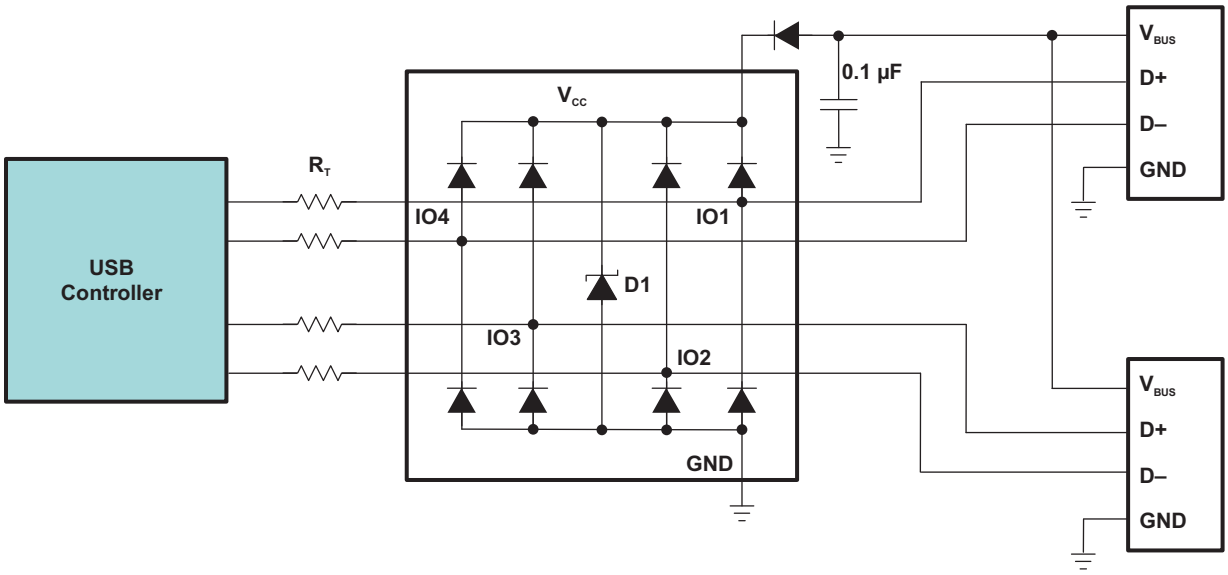
此外，此器件还适用于为使用 USB 2.0、以太网或高精度模拟接口的汽车音响主机、后座娱乐系统以及后座摄像机系统提供保护。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPD4E001-Q1	SOT-23 (6)	2.90mm x 1.60mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

典型电路原理图



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision C (June 2013) to Revision D **Page**

- 已添加 *引脚配置和功能*部分，*ESD 额定值*表，*特性 描述*部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1
- 已更改 器件 CDM ESD 分类等级，从 C4B 改为 C5 ... 1

Changes from Revision B (February 2012) to Revision C **Page**

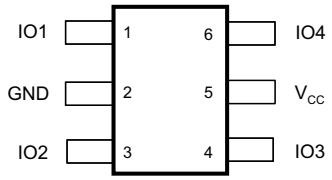
- Changed maximum I_{CC} supply current in Electrical Characteristics ... 4

Changes from Revision A (April 2013) to Revision B **Page**

- 已修改 说明 部分的文本 ... 1
- Revised Figure 2 graph ... 4
- Revised APPLICATION INFORMATION schematic ... 7

5 Pin Configuration and Functions

DBV Package
6-Pin SOT-23
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	2	GND	Ground
IO1	1	I/O	ESD-protected channel
IO2	3		
IO3	4		
IO4	6		
V_{CC}	5	I	Power-supply input. Bypass V_{CC} to GND with a 0.1-µF ceramic capacitor.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.3	7	V
V_{IO}	I/O voltage tolerance	–0.3	V_{CC} + 0.3	V
I_{PP}	Peak pulse current (Tp = 8/20 µs)(2)		5.5	A
P_{PP}	Peak pulse power (Tp = 8/20 µs)(2)		100	W
T_A	Free air operating temperature	–40	125	°C
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Non-repetitive current pulse 8/20 µs exponentially decaying waveform according to IEC 61000-4-5.

6.2 ESD Ratings: AEC Q100

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±15000	V
		Charged-device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 ESD Ratings: IEC 61000-4-2

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	±8000	V
		IEC 61000-4-2 air-gap discharge	±15000	

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_A	Free air operating temperature	–40		125	°C
V_{CC} pin	Operating voltage	0.9		5.5	V
IO1, IO2, IO3, IO4 pins	Operating voltage	0		V_{CC}	V

6.5 Thermal Information

THERMAL METRIC(1)		TPD4E001-Q1 DBV (SOT-23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	202.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	146.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	47.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	37.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	46.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.6 Electrical Characteristics

V_{CC} = 5 V ± 10%, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
I_{CC}	Supply current				1	200	nA
V_F	Diode forward voltage	I_F = 10 mA		0.65		0.95	V
V_{BR}	Breakdown voltage	I_{BR} = 10 mA		11			V
V_{CLAMP}	Clamping voltage	Surge strike(2) on IO pin, GND pin grounded, V_{CC} = 5.5 V, I_{PP} = 5.5 A	Positive transients		16		V
V_{RWM}	Reverse standoff voltage	IO pin to GND pin				5.5	V
I_{IO}	Channel leakage current	V_{IO} = GND to V_{CC}				±10	nA
C_{IO}	Channel input capacitance	V_{CC} = 5 V, bias of V_{CC}/2, f = 10 MHz			1.5		pF

(1) Typical values are at V_{CC} = 5 V and T_A = 25°C.
(2) Non-repetitive current pulse 8/20 µs exponentially decaying waveform according to IEC 61000-4-5.

6.7 Typical Characteristics

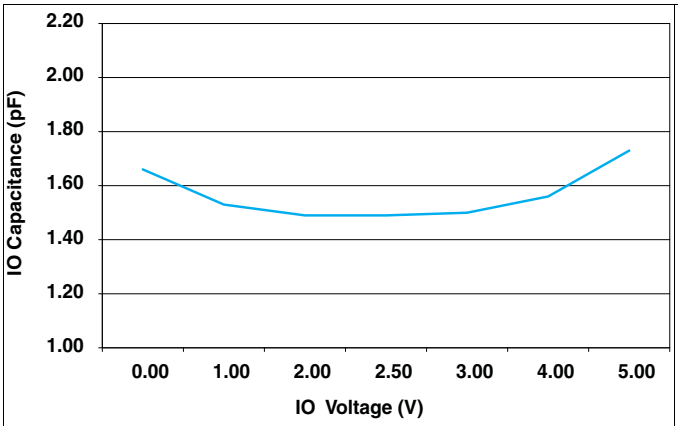


Figure 1. IO Capacitance versus IO Voltage (V_{CC} = 5 V)

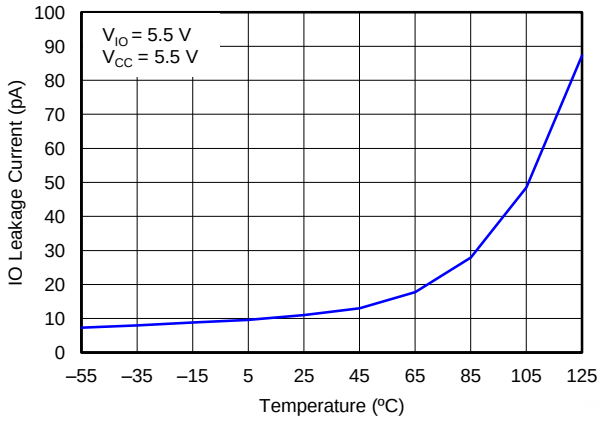


Figure 2. IO Leakage Current versus Temperature

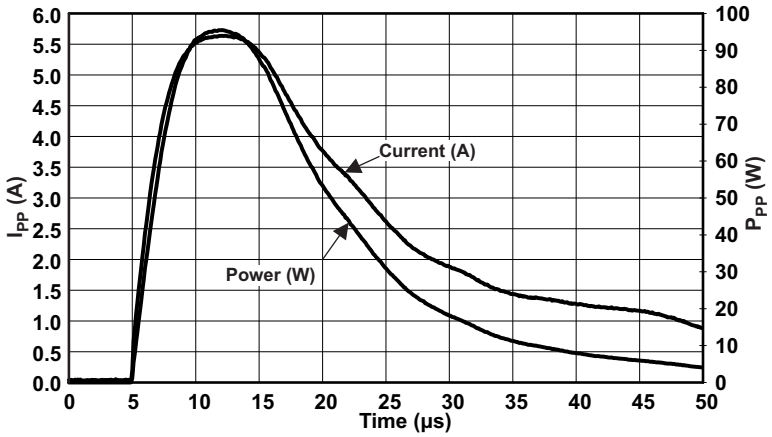


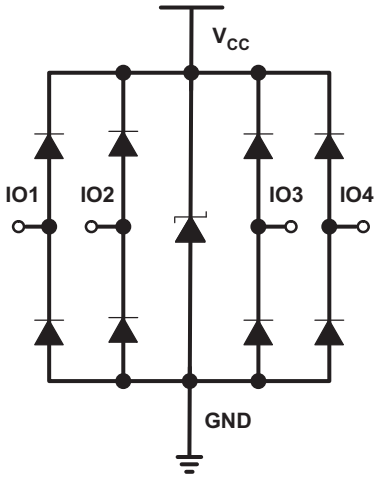
Figure 3. Peak Pulse Waveform, V_{CC} = 5.5 V

7 Detailed Description

7.1 Overview

The TPD4E001-Q1 device is a low-capacitance, TVS diode array designed for ESD protection in sensitive electronics connected to communication lines. Each channel consists of a pair of transient voltage suppression diodes that steer ESD pulses to V_{CC} or GND. The TPD4E001-Q1 device protects against ESD events up to ±8-kV contact discharge and ±15-kV air-gap discharge, as specified in IEC 61000-4-2 international standard. This device has a low capacitance of 1.5-pF per channel making it ideal for use in high-speed data interfaces. The low-leakage current (10 nA max) ensures minimum power consumption for the system and high accuracy for analog interfaces.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 AEC-Q100 Qualified

This device is qualified according to the AEC-Q100 standard. The device temperature rating is Grade 1 (–40°C to 125°C). The HBM Classification Level passed is 3B (> 8 kV). The CDM Classification Level passed is C5 (all pins 750 V to <1000 V).

7.3.2 IEC 61000-4-2 Level 4 ESD Protection

The device is specified at ±8-kV contact discharge and ±15-kV air gap discharge.

7.3.3 IEC 61000-4-5 Surge Protection

This device is rated to pass at least 5.5-A of peak pulse current according to the IEC 61000-4-5 (8/20-µs pulse) standard.

7.3.4 Low 1.5-pF Input Capacitance

This device has a typical capacitance of 1.5-pF on each of the four IO pins. This allows for high speed signals on the IO pins in excess of 1 Gbps.

7.3.5 Low 10-nA (Max) Leakage Current

This device is rated to have a maximum leakage current of 10-nA on each of the four IO pins.

7.3.6 0.9-V to 5.5-V Supply Voltage Range

This device is specified to operate with a supply voltage (on V_{CC}) between 0.9-V and 5.5-V to ensure sufficient signal integrity.

7.4 Device Functional Modes

The TPD4E001-Q1 device is a passive integrated circuit that triggers when voltages are above V_{BR} or below the lower diodes V_F (–0.6 V). During ESD events, voltages as high as ±8 kV (contact) can be directed to ground via the internal diode network. Once the voltages on the protected line fall below the trigger levels of TPD4E001-Q1 (usually within 10's of nano-seconds) the device reverts back to its high-impedance state.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPD4E001-Q1 device is a TVS diode array which is typically used to provide a path to ground for dissipating ESD events on high-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

8.2 Typical Application

For this design example, one TPD4E001-Q1 device is being used in a dual USB 2.0 application. This will provide a complete port protection scheme.

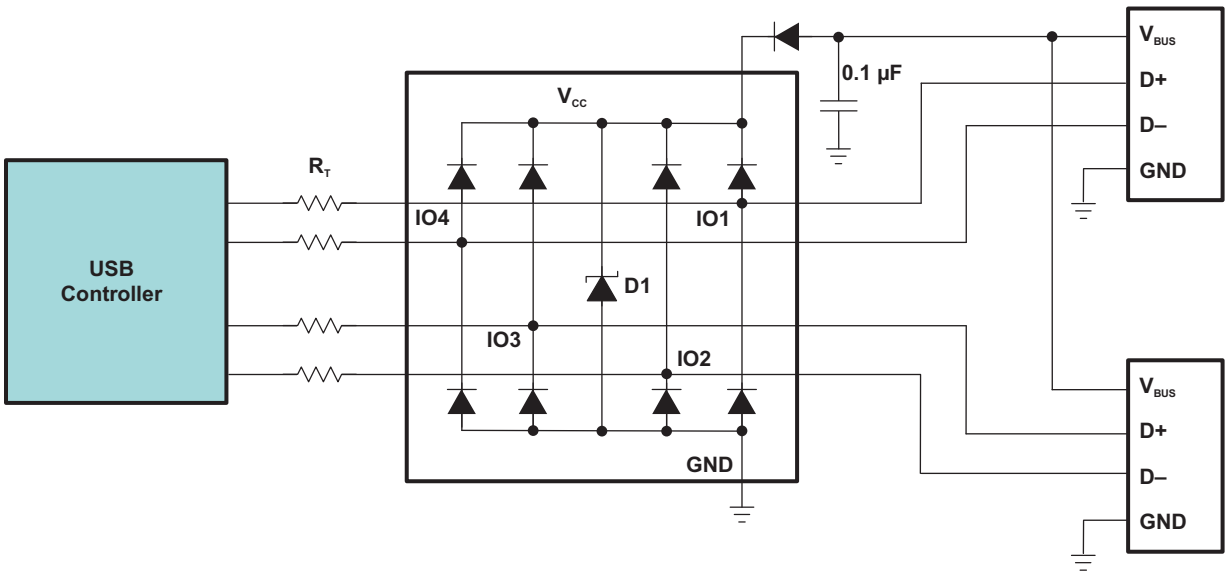


Figure 4. Typical Application Schematic

Typical Application (continued)

8.2.1 Design Requirements

For this design example, a single TPD4E001-Q1 device is used to protect all the pins on two USB2.0 connectors.

Given the USB application, known parameters are listed in the Table 1 table.

Table 1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on IO1, IO2, IO3, or IO4	0 V to 3.6 V
Voltage range on V_{CC}	0 V to 5.25 V
Operating Frequency on IO1, IO2, IO3, or IO4	240 MHz

8.2.2 Detailed Design Procedure

To begin the design process, some parameters must be decided upon; the designer needs to know the following:

- Signal range on all protected lines
- Operating frequency on all protected lines

8.2.2.1 Signal Range on IO1 Through IO4

The TPD4E001-Q1 device has 4 identical protection channels for signal lines. The symmetry of the device provides flexibility when selecting which of the 4 IO channels will protect which signal lines. Any IO will support a signal range of 0 to (V_{CC} + 0.3) V. Therefore, this device will support the USB 2.0 signal swing assuming V_{CC} is set appropriately.

8.2.2.2 Voltage Range on V_{CC}

The V_{CC} pin can be connected in one of two ways:

- If the V_{CC} pin connects to the system power supply, the TPD4E001-Q1 device works as a transient suppressor for any signal swing above V_{CC} + V_F. TI recommends a 0.1-μF capacitor on the device V_{CC} pin for ESD bypass.
- If the V_{CC} pin does not connect to the system power supply, the TPD4E001-Q1 device can tolerate higher signal swing in the range up to 10 V. Note that TI still recommends a 0.1-μF capacitor at the V_{CC} pin for ESD bypass.

If this pin is connected to the USB 2.0 V_{BUS} supply or left floating, the allowable signal swing is enough for a USB 2.0 application.

8.2.2.3 Bandwidth on IO1 Through IO4

Each IO pin on the TPD4E001-Q1 device has a typical capacitance of 1.5 pF. This capacitance is low enough to easily support USB 2.0 data rates.

8.2.3 Application Curve

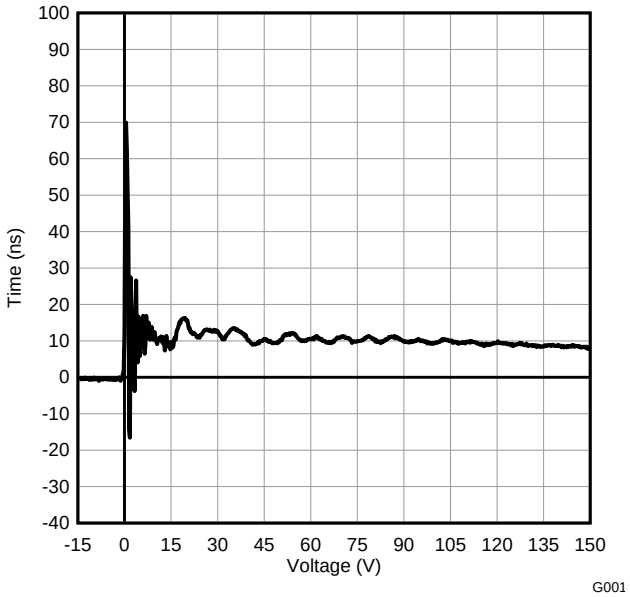


Figure 5. IEC 61000-4-2 Voltage Clamp Waveform +8kV Contact

9 Power Supply Recommendations

This device is a passive ESD protection device so there is no need to power it. Do not violate the maximum voltage specifications for each pin.

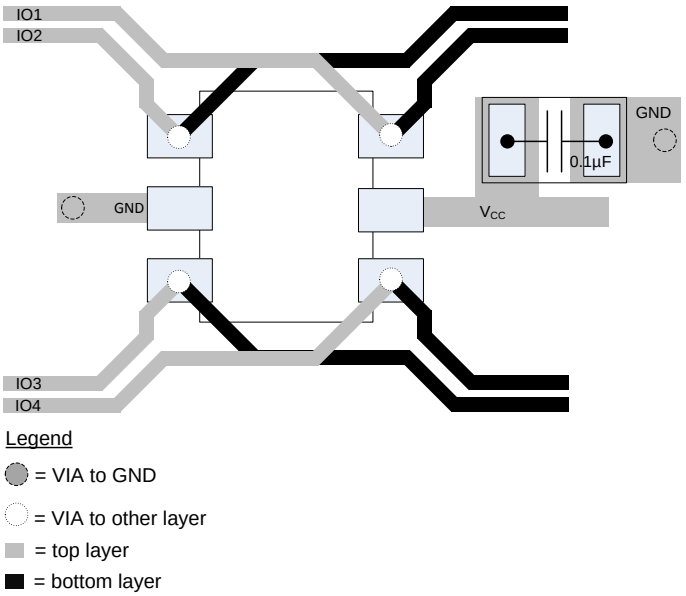
10 Layout

10.1 Layout Guidelines

When placed near the connector, the TPD4E001-Q1 device's ESD solution offers little or no signal distortion during normal operation due to low IO capacitance and ultra-low leakage-current specifications. The TPD4E001-Q1 device ensures that the core circuitry is protected and the system is functioning properly in the event of an ESD strike. For proper operation, observe the following layout and design guidelines:

- Place the TPD4E001-Q1 device solution close to the connector. This allows the device to take away the energy associated with ESD strike before it reaches the internal circuitry of the system board.
- Place a 0.1-μF capacitor very close to the V_{CC} pin. This limits any momentary voltage surge at the IO pin during the ESD strike event.
- Ensure that there is enough metallization for the V_{CC} and GND loop. During normal operation, the TPD4E001-Q1 device consumes nA leakage current. But during the ESD event, V_{CC} and GND may see 15 A to 30 A of current, depending on the ESD level. Sufficient current path enables safe discharge of all the energy associated with the ESD strike.
- Leave the unused IO pins floating.
- One can connect the V_{CC} pin in two different ways:
  a. If the V_{CC} pin connects to the system power supply, the TPD4E001-Q1 works as a transient suppressor for any signal swing above V_{CC} + V_F. TI recommends a 0.1-μF capacitor on the device V_{CC} pin for ESD bypass.
  b. If the V_{CC} pin does not connect to the system power supply, the TPD4E001-Q1 can tolerate higher signal swing in the range up to 10 V. Note that TI still recommends a 0.1-μF capacitor at the V_{CC} pin for ESD bypass.
- The optimum placement is as close to the connector as possible.
  – EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  – The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  – Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Example



11 器件和文档支持

11.1 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。要获得这份数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD4E001QDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AAXQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPD4E001-Q1 :

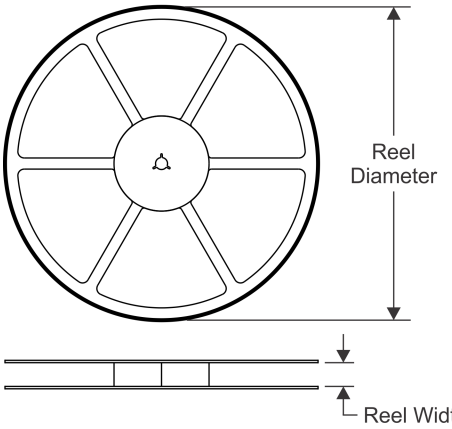
- Catalog: TPD4E001

NOTE: Qualified Version Definitions:

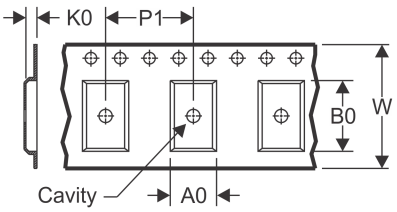
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

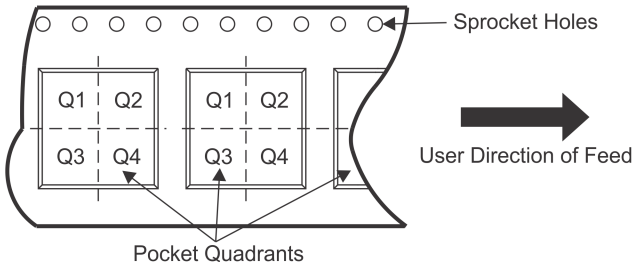


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

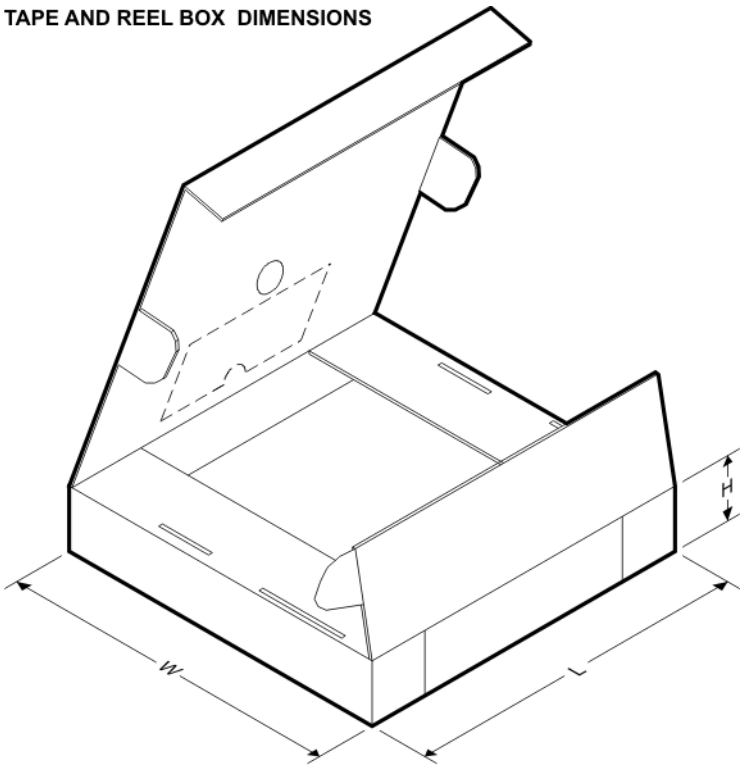
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD4E001QDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

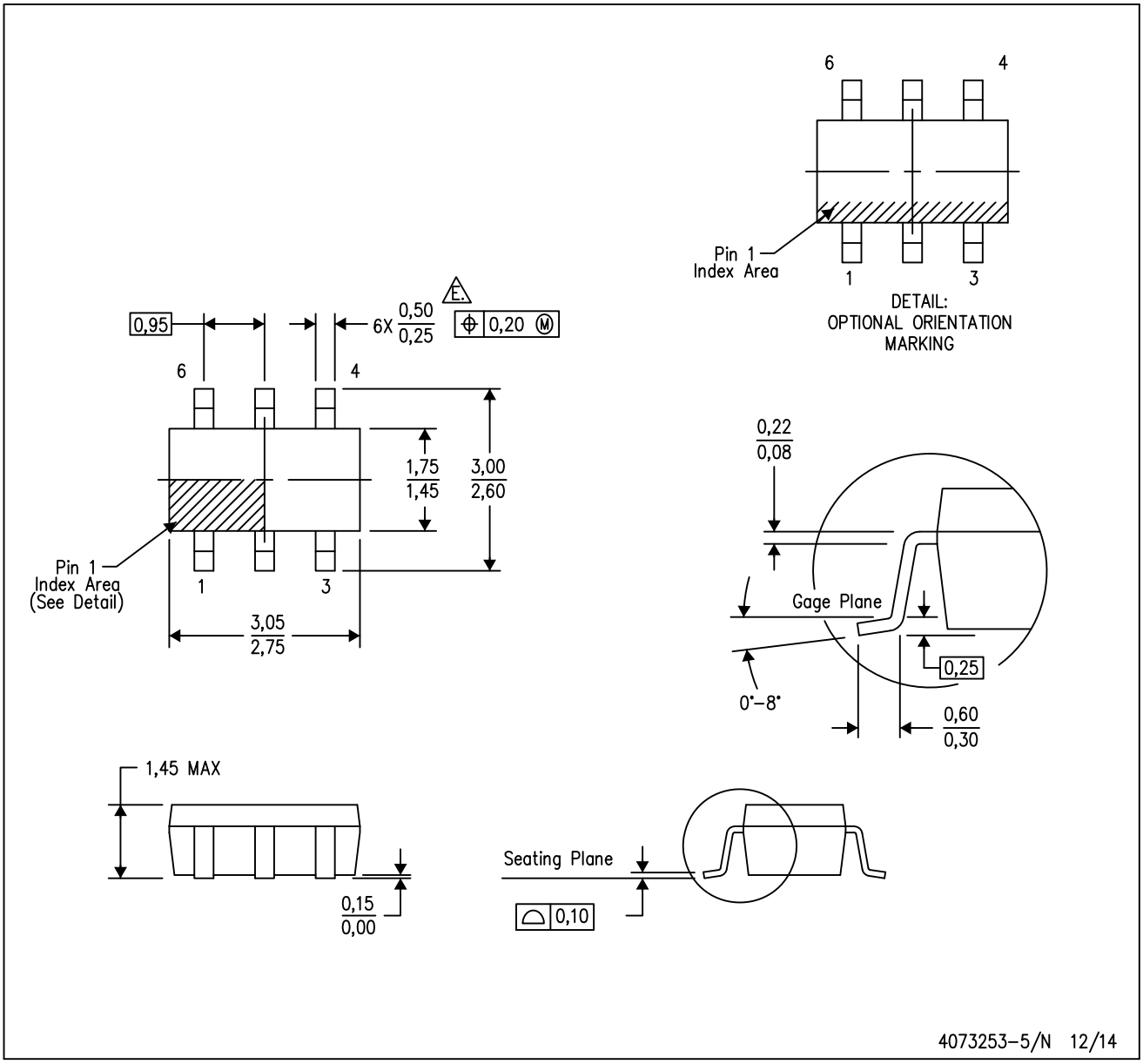
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

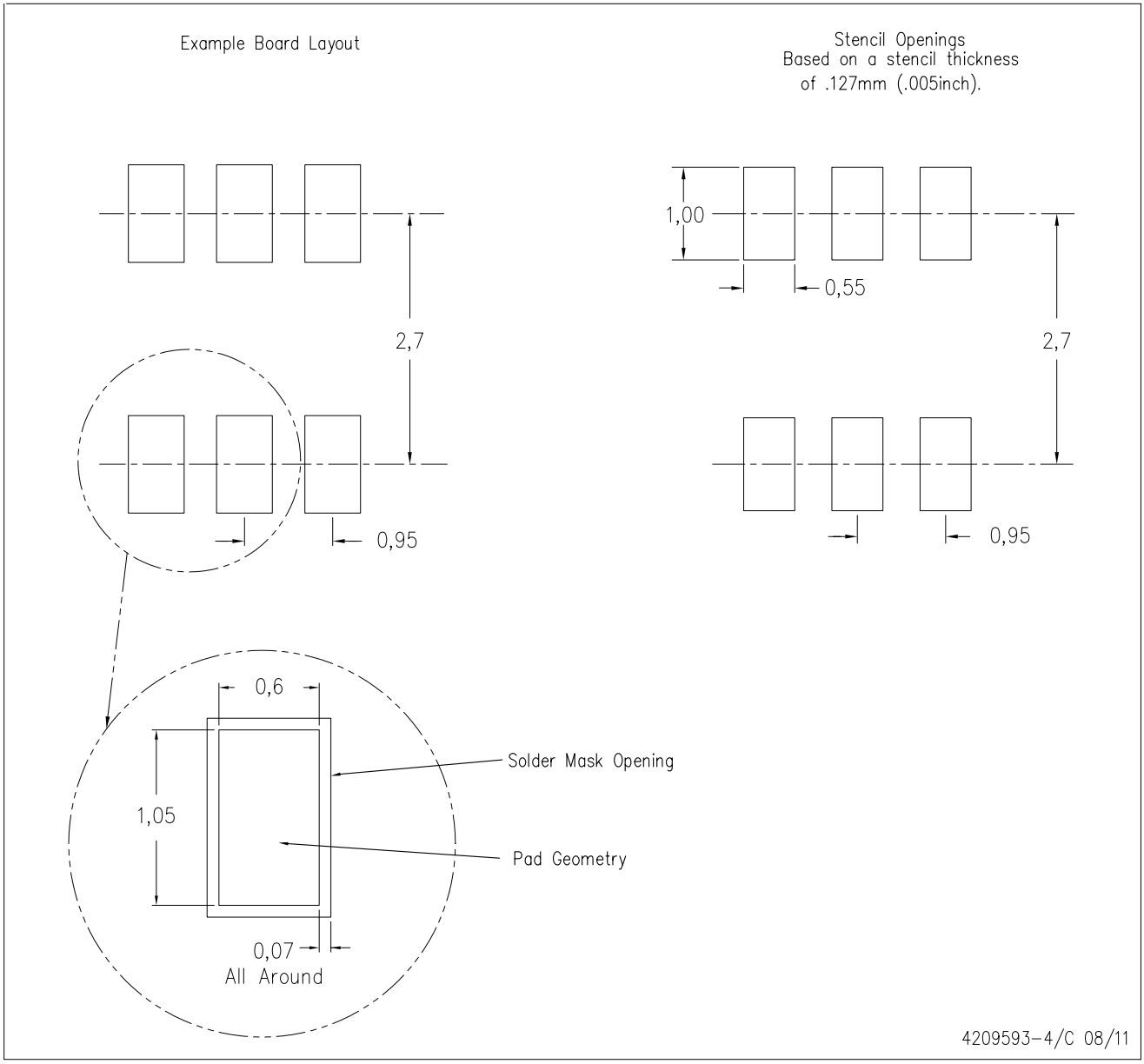
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD4E001QDBVRQ1	SOT-23	DBV	6	3000	180.0	180.0	18.0

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

DBV (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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