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North South University

Department of Electrical & Computer Engineering

Lab Report

Experiment No:	5
Experiment Title:	Design of a Register File
Course Code:	CSE332L
Section:	10
Course Name:	Computer Organization & Architecture Lab
Lab Group #:	03
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Date of Experiment:	19 September, 2023
Date of Submission:	26 September, 2023

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Objective:

① To design a register file that is 4 bit wide. Label properly the inputs / outputs / selections.

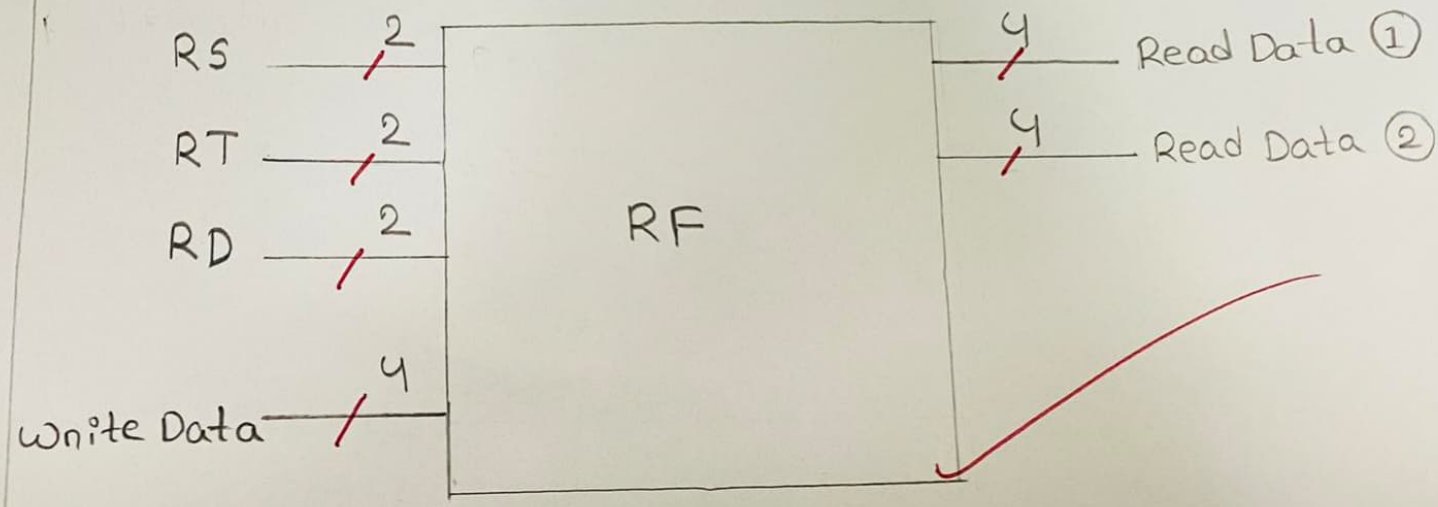
② To design the interfacing for reading data from any of those ~~resig~~ registers.

③ To design the interfacing for writing data to any of those registers. Make sure it has the write control signal.

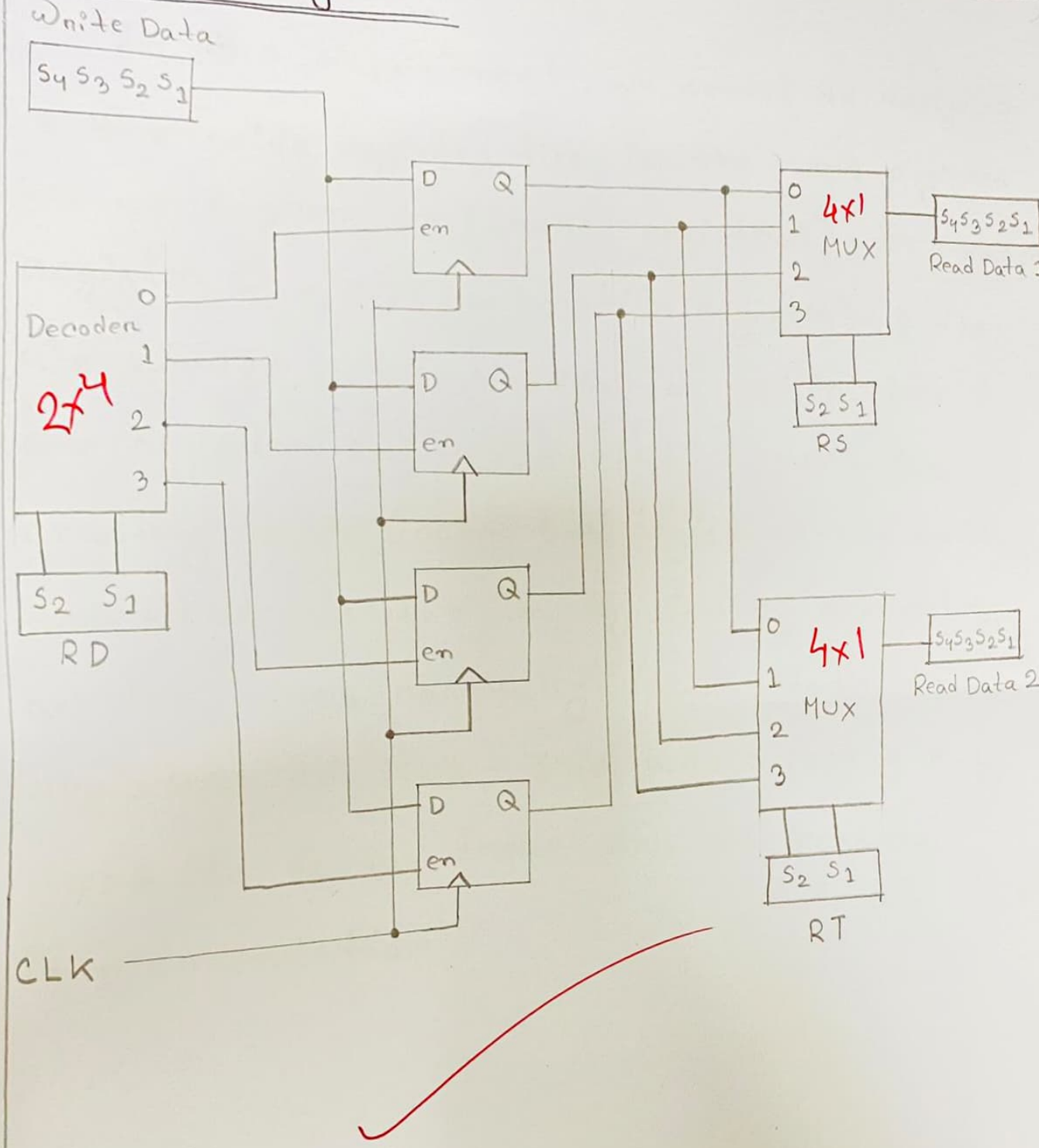
Equipments:

① Logisim software

Block Diagram:

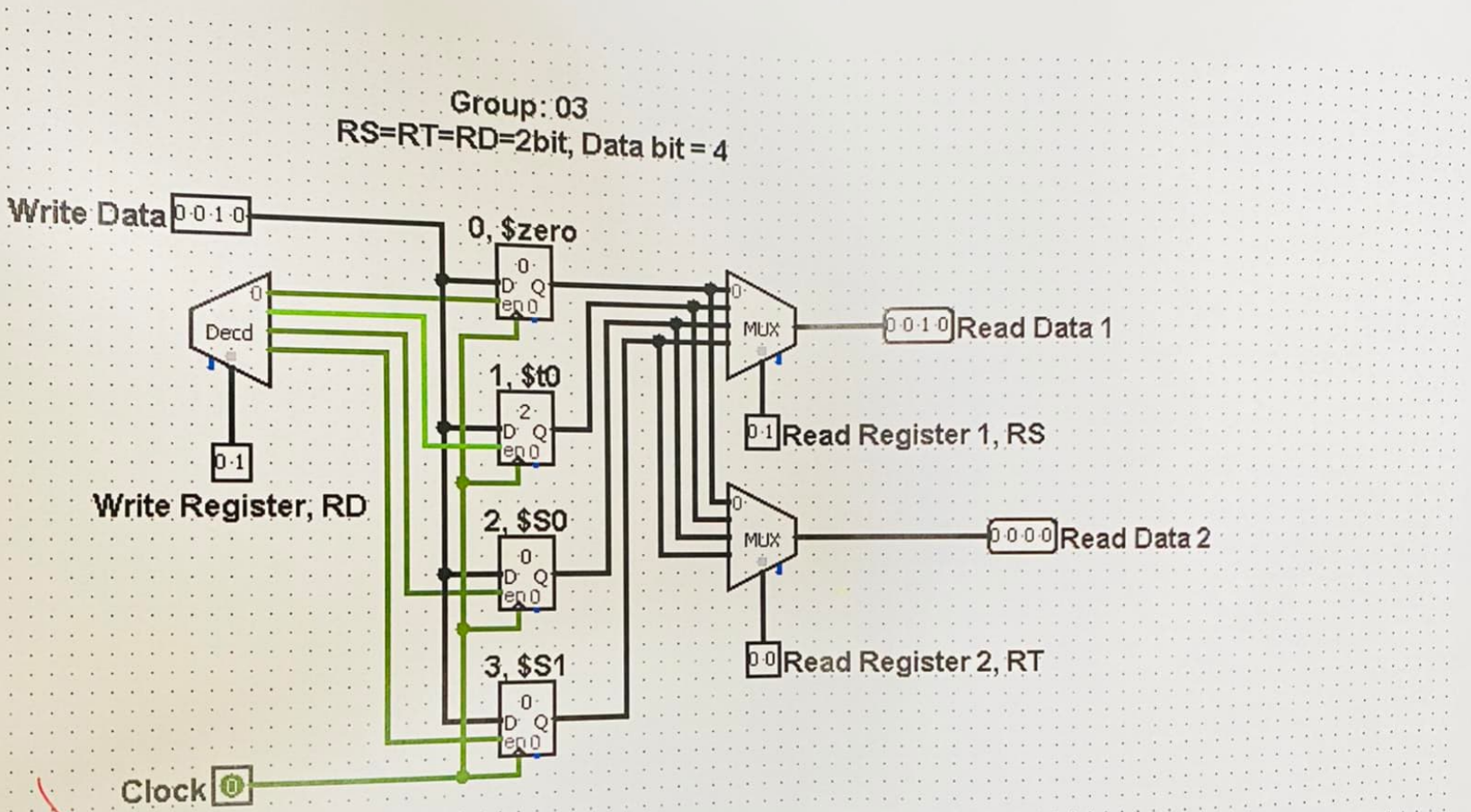


Circuit Diagram :



Discussion:

In this experiment, we needed to design a 4 bit wide register file. For the 4 bit register we were given RS (Source register 1) = RT (Source register 2) = RD (Destination register) = 2 bits. We needed 2x4 decoder for writing data in one register and we needed 2 MUXs for reading data from two registers. We built the whole circuit in logisim by connecting all the wires carefully from decoder to registers to MUX. This was a pretty easy task to do as there was no hardware implementation.


Group: 03
RS=RT=RD=2bit, Data bit = 4
Write Data
0 0 1 0
0, $zero
Decd
1, $t0
2, $S0
3, $S1
MUX
MUX
0 0 1 0
Read Data 1
0 1
Read Register 1, RS
0 1
Write Register, RD
0 0 0 0
Read Data 2
0 0
Read Register 2, RT
Clock