

Experiments Name: Introduction to Flip-Flops and Shift Registers.

Objective:

- Learn about the concept of states in digital logic and how Flip-Flop circuits can be used to store state information.
- Understand the internal logic of J-K Flip-Flops and implement one using basic logic gates.
- Understand the relationship between J-K, T and D Flip-Flops and observe the characteristics of all three.
- Implement a shift register using D Flip-Flops and analyze its operation.

Apparatus:

- 1x IC 7402 2-input NOR gates.
- 1x IC 4073 3-input AND gates.
- 1x IC 7404 Hex Inverter (NOT gates).
- 2x IC 7474 (D Flip-Flop).
- Trainer Board.
- Wires.

Theory:

Flip-Flops:

Flip flops are essential components in digital circuits for storing binary data. They have inputs, an output, and a clock input. The clock signal determines when the flip flop updates its state based on the inputs. Different types include D, JK, and T flip flops. They have two stable states, "set" and "reset." Flip flops are used in sequential circuits like registers, counters, and memory elements. They are crucial in applications such as computer processors, communication systems, and control systems, where synchronized data storage and manipulation are required.

JK, D ("Data" or "Delay") and T ("Toggle") are three common types of flip-flops used in digital logic circuits.

In case of the JK flip-flop (J=Set, K=Reset), the combination $J = 1, K = 0$ is a command to set the flip-flop (i.e., make the output, $Q = 1$); the combination $J = 0, K = 1$ is a command to reset the flip-flop ($Q = 0$); and the combination $J = K = 1$ is a command to toggle the flip-flop, i.e., change its output to the logical complement of its current value. Setting $J = K = 0$ maintains the current state.

Characteristic Table			Excitation Table			
J	K	Q_{next}	Q	Q_{next}	J	K
0	0	\bar{Q}	0	0	0	X
0	1	0	0	1	1	X
1	0	1	1	0	X	1
1	1	\bar{Q}	1	1	X	0

Table B.1: JK flip-flop: Characteristic and Excitation Tables

The T flip-flop changes state ("toggles") whenever the input T is high and the clock input is strobed. If the T input is low, the flip-flop holds the previous value when given a clock pulse. **Table B.2** shows the Characteristic Table and Excitation table for the T flip-flop.

Characteristic Table		Excitation Table		
T	Q_{next}	Q	Q_{next}	T
0	Q	0	0	0
		0	1	1
1	\bar{Q}	1	0	1
		1	1	0

Table B.2: T flip-flop: Characteristic and Excitation Tables

The D flip-flop captures the value of the D-input at a definite portion of the clock cycle (such as the rising edge of the clock). That captured value becomes the Q output. At other times, the output Q does not change. **Table B.3** shows the Characteristic Table and Excitation table for the T flip-flop.

Characteristic Table		Excitation Table		
D	Q_{next}	Q	Q_{next}	D
0	0	0	0	0
		0	1	1
1	1	1	0	0
		1	1	1

Table B.3: D flip-flop: Characteristic and Excitation Tables

Register:

A register is a digital circuit component used for storing and manipulating binary data. It consists of multiple flip flops connected. Registers can store multiple bits of data simultaneously and retain their values until updated. They are commonly used for temporary storage, data buffering, and data transfer between different parts of a digital system. Registers can be parallel-in-parallel-out (PIPO), parallel-in-serial-out (PISO), serial-in-parallel-out (SIPO), or serial-in-serial-out (SISO), depending on the arrangement of their inputs and outputs. Registers play a vital role in various applications, including arithmetic operations, memory units, and data processing systems.

A register that can shift its binary information either to its right or its left is called a shift register. The logical configuration of a shift register consists of a chain of flip-flops connected in cascade, with the output of one flip flop connected to the input of the next flip-flop. All flip-flops receive a common pulse which causes the shift from one stage to the next.

Circuit Diagram:

Give the pin number in every circuit left it for me.

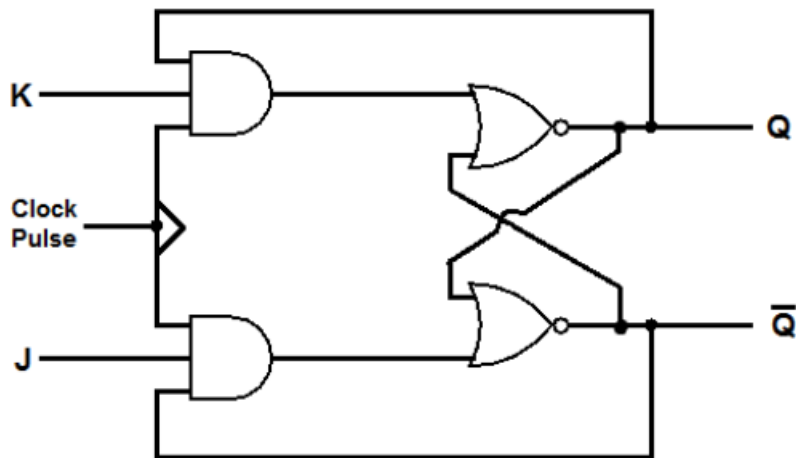


Figure D.1.1: JK Flip-Flop implemented using AND and NOR gates

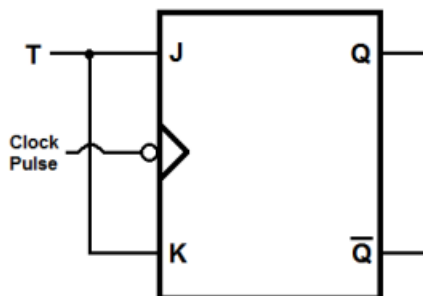


Figure D.2.1: T flip-flop constructed using JK flip-flop

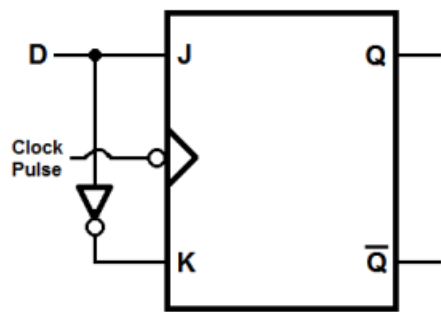


Figure D.2.2: D flip-flop constructed using JK flip-flop

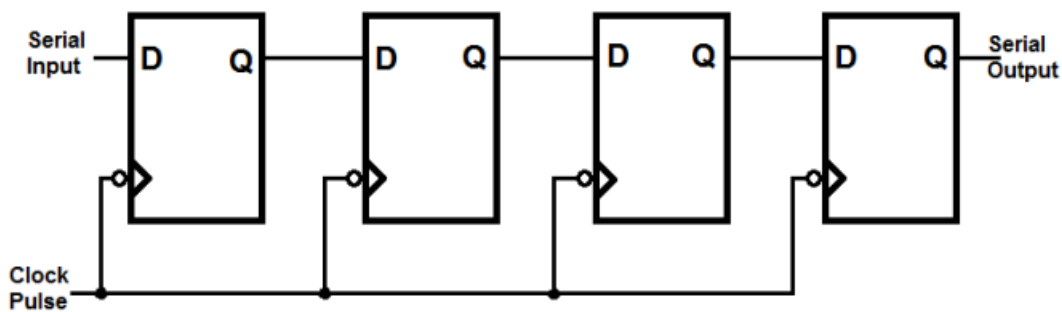


Figure D.3.1: Right Shift Register

Experimental Procedure:

Experiment-1:

- 01.** First, we construct the circuit for the J-K Flip Flops as the pin diagram shown in the Circuit Diagram Section (Fig D.1.1).
- 02.** After that, we complete the truth table (Table F.1.1) according to the characteristic of J-K Flip-Flops.
- 03.** Then we start to test our circuit according to the truth table. In each step we set the value for J and K and send one clock Pulse then we match it with the output of our truth table.
- 04.** Then test more as given bellow:
 - Set both J and K to 0.
 - Set J to 1 (keep K at 0).
 - Once again, set both J and K to 0.
 - Now, set K to 1 (keep J at 0).
 - Finally, set both J and K to 1.

Finally, we completed this experiment.

Experiment-2:

- 01.** For this experiment we just changed some connection of our previously built circuit for J-K.
- 02.** For making T Flip-Flop we just connect the K with J, so that input will be the same.
- 03.** Then we started to complete the truth table for T Flip Flop (Table F.2.1) by giving various input in J, given bellow:
 - a.** First, we set the input (T) to 0 and send several clock pulses. And found the output for each pulse is 0.
 - b.** Then, we set T to 1 and send one more clock pulse. We found output as 1.
 - c.** Then, we set T to 0 while the output is 1 and found that the output is 1.
 - d.** Then, we set T to 1 while the output is 1 and found that the output is 0.

Thus, our truth table follows the Excitation table of T Flip-Flops.

- 04.** Then we convert the T flip flop into D flip flop by adding a NOT gate between the connection from J to K.
- 05.** Then, we complete the truth table (Table F.2.2) for D flip flop by giving various input as given bellow:
 - a.** First, we give 0 to D and send several clock pulses. In each clock pulse we found the output 0.
 - b.** Then, we give 1 to D and send more clock pulse. In this case every clock pulse we found the output 1.
- 06.** Finally, we completed this experiment for T and D Flip-Flops.

Experiment-3:

- 01.** In this experiment, First, we complete the truth table for a Right Shift Register in Table F.3.1.
- 02.** Then we construct the truth table as the pin diagram shown in the Circuit Diagram section. We inactive all the Set and Reset Pin by giving a constant input of 1.
- 03.** After implementing it we started to test our circuit as the truth table.
- 04.** First, we gave an input of 1 and found the output of 1XXX.
- 05.** Then, we gave an input of 0 and found the output as 01XX. It looks, 1 is shifted by one digit right and 0 enter in the beginning.

06. Then, we gave an input of 1 and found the output as 101X. It's shifting right again.

07. After that, we gave an input of 0 and found the output of 0101. Finally, we completed this experiment of shift register.

Simulation:

Attached.

Experimental Data Table:

F.1 Experimental Data (JK Flip-Flop using AND and NOR gates):

J	K	Q	Q'
1	0	1	0
0	0	1	0
0	1	0	1
0	0	0	1
1	1	1	0
1	0	1	0
1	0	1	0
1	1	0	1

Table F.1.1

F.2 Experimental Data (T and D Flip-Flops using J-K Flip-Flops):

T	Q
0	0
1	1

Table F.2.1

D	Q
0	0
1	1

Table F.2.1

F.3 Experimental Data (Right shift register using D Flip-Flops):

States	Input	Output
Initial State	X	XXXX
T1	1	1XXX
T2	0	01XXX
T3	1	101XX
T4	0	0101

Table F.3.1

Results:

As our every truth table and output data matched with the characteristic table and Excitation table of J-K, T, D Flip-Flop, we can say that we successfully completed this experiment.

Questions and Answers (Q/A):

E.2: Difference between T and D Flip-Flops:

In D Flip-Flop whatever we give as input, output will be the same as input. On the other hand, T Flip Flop, a set of characteristics such as, if we give input 0 then the output will not change, it will be same as previous output. If we give input as 1 then the output will change like it will perform a toggle.

E.3.1:

Shift registers are digital components used in electronics to convert data between parallel and serial formats. They enable the efficient transfer of multiple bits of data in a sequential manner. With their clock-controlled shifting operation, shift registers can convert parallel data into a serial stream for transmission over serial communication channels. They play a crucial role in various applications, including serial communication interfaces, data transmission protocols, and storage systems. Shift registers simplify data transfer between devices with different data formats and optimize the utilization of communication channels.

E.3.2:

If the output of the last D Flip-Flop in the register was connected to the input of the first D Flip-Flop, then it will work as a Ring Counter. If the initial state is 0111 then the output in every clock pulse will be,

0111 (initial)

1011 (1st Clock Pulse)

1101 (2nd Clock Pulse)

1110 (3rd Clock Pulse)

0111 (4th Clock Pulse)

1011 (5th Clock Pulse)

Discussion:

From this experiment we learned a lot about the characteristic and Excitation table for J-K, T, and D Flip-Flops. We observe the behavior of each Flip Flops. We learn why we need these Flip Flop in digital logic. We learn to construct a register using D flip flop, also we built J-K flip flop using basic gates. We know the relation and difference between these three flip-flops. In this experiment we don't face any problems. We successfully completed this lab within the given time.

