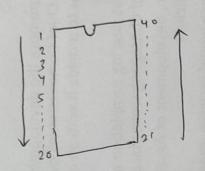
## CSE 331 /L-17/18.04.2024/

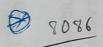
Interclacing



8086 > total 40 Pin

> no need to memorize, just understand the job done by each pin.

Book Reference: Intel Micropirocesson - Brey chapter-9 => Page - 321



Data Bus = 16 bit

Address Bus = 20 bit

Control Bus = x bit

36+x+ vec + 2 GND

AD = Address and Data

AD. - AD15 = Data + Address Bus merged

For separate the pin for address and data,

9086 used Buffer IC & Latch IC

yo pin IC+ Latch IC << 60 pin processor

→ in terms of cost and fabrication.

A16 - A19 > Address Pin + Status Pin

Difference between 8086 8 2088

- in Pata Pin - Pin number 34 and 28

BHF = Bus High Fnable

BHE=0 dark

darka bus = 16 bit

8 bit
Low

Work

BHE = 1
works as SZ

and data bus will be
used as normal

331 MN/MX

8686

8688

28- Pin Connection:

internal

memony/Device transfer

IO/M

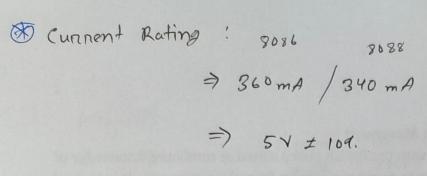
Clock Generation IC - 8284A for 8086

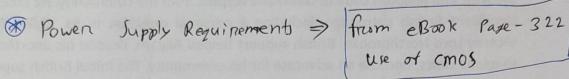
12 V on average

7 Signal will generate 19 - clock 22 - Ready 21 - Reset ) 0 = Stand by 1 = Busy Operating mode

1 Openating tempercuture:

32°F - 180°F → 0° c - 82.22° C





DC Characteristic!

20V | 1 Level

tru state
- high impedence state

O'8V

O level

1 Level

Input

o level

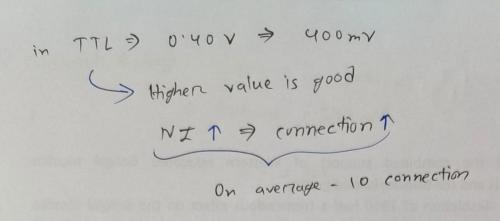
o level

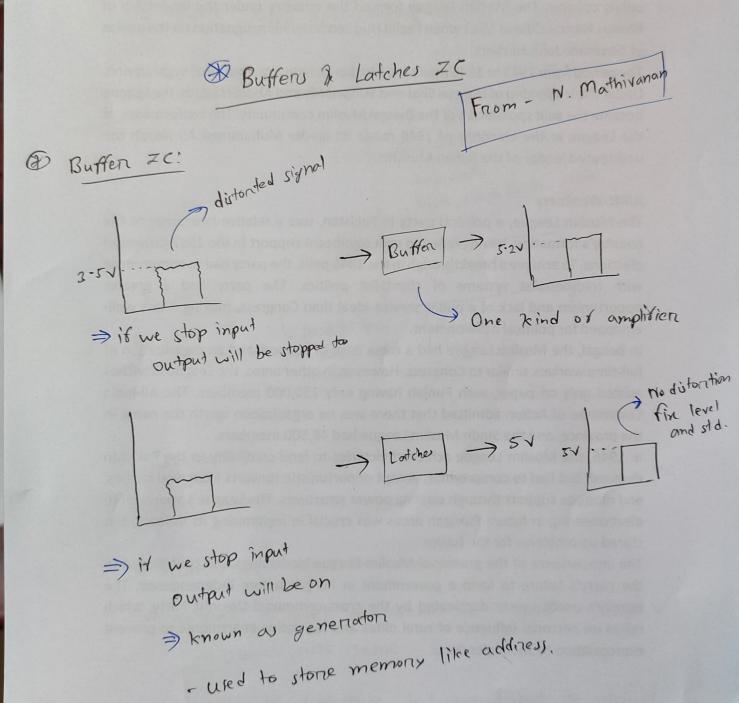
₩ TTL > Transiston trunsiston logic

-in output 0 level maximum is 0:40 V others are same

Noice îmmunity => différence between input to output in o level.

8086/8088 => 0:35 N = 350 mV





For long distance connection, we need to use butter ze.

(8)

0 level => will activate the butter

- two pant:

- unidirectional buffer

- Bi-directional buffer

1 level > will activate the concuit.

if enable pin = 0; will activate the ZC  $DZR = 1 \Rightarrow A_0$  will activate,  $B_0$  will be output

DZR=0 => B. will activate, A. will be output.

De Latches:

wed D. flip flop + amplifier

regenerate to signal will give sv G= Pulse/Clock