CSE 331 / L-19 / 27.04.2024 /

* Any input 0 ~~will~~ NAND will be 1

$\overline{RD}$ = Read Data

$\overline{WD}$ = Write Data

$\overline{INTA}$ = Interrupt acknowledge

always 1

0 = NAND = 1 = Normal operation of chip

1 = NAND = 0 = all pin 0

OR = 0 ($\overline{CS}$ = 1)

Ready = 1

$\overline{CS} = \overline{RD}$ (Need to be same input)

$RDY_1 = 1$

$AEN_1 = 0$

READY = 1

* Changing on $\overline{RD}$ will change the output of READY, but it will effect after some time, not immediate. So, the current cycle will be consider as the normal operation. Value is changing almost immediate but ~~the CLK pulse~~ will ~~be~~ effect from next pulse.

* One pulse wait, connection will be on second Pin

2 pulse ⇒ 3rd Pin

T_{w_6} ⇒ 6w

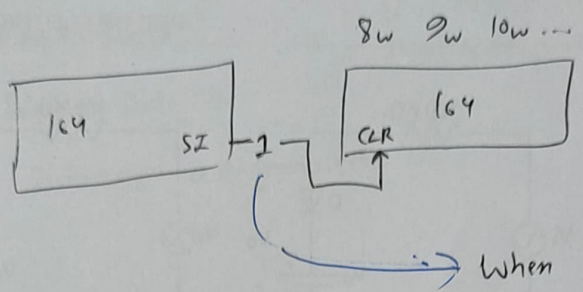
* Ensure that, make your microprocessor in wait stay unless and until about 600ns to 800ns

T_3 to T_4

T_{w3} wait pulse need to generate.

* T_{w_9} is not possible from this circuit.

So, if we need to wait upto T_{w_9} then we need to add another shift register 164 in parallel.



→ When all the pin is 1 and changing to 0 after full cycle, SI will be 1, for some time.

One Question in next Exam Must

* RAM & ROM

$\overline{CE}$ ⇒ Chip enable

$\overline{OE}$ ⇒ Output enable

$\overline{WE}$ ⇒ Write enable only for RAM

$D_0 - D_7$ = 8bit Data bus

$A_0 - A_{14}$ = 15 bit address

$= 2^{15}$

$= 32700$

$= 32K$ - 8bit/1byte

$= 32KB$

$= 32k \times 8$ bit

$= 32k \times 1$ byte → Standard

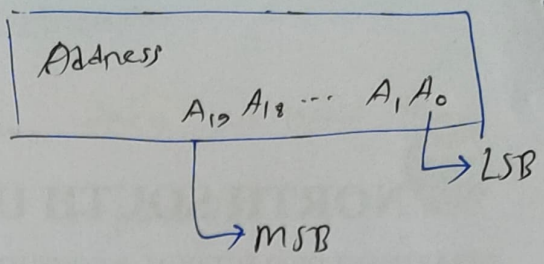
* For RAM,

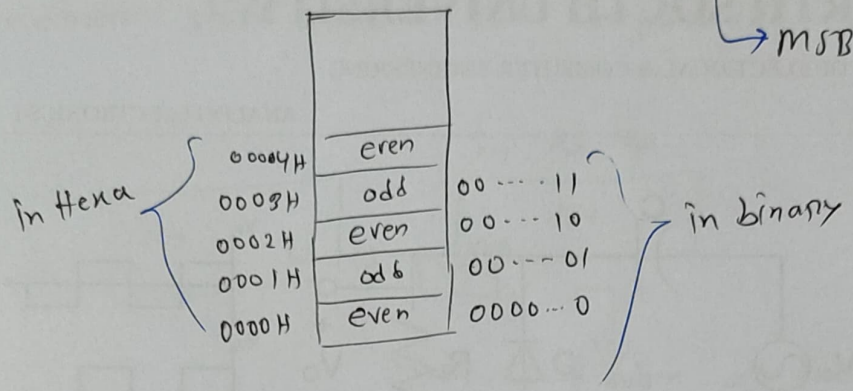
memory space $= 2^{12} = 4096$

$= \frac{4096}{1024} = 4k \times 1$ byte

$= 4k \times 8$ bit

✳ Memory bank:





LSB in binary,

0 = even ⇒ even addressed in Lower Bank

1 = odd ⇒ Upper bank

$A_1 - A_{19}$ connected in Both bank

A_0 – is the LSB decide the even or odd bank

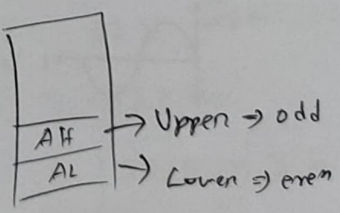
↳ 0 ⇒ activate even bank

Data bus $D_0 - D_7$ connected in ~~both~~ lower bank

$D_8 - D_{15}$ connected in higher bank

✳ Recall data insertion in Memory

MOV [BX], AX ⇒



A_0	$\overline{BHE}$	
0	1	Lower bank
1	0	Higher bank
0	0	Both
1	1	None

Not Possible according to structure

$\overline{BHE}$ = Bus High Enable

– when active, then $D_8 - D_{15}$ need to read

↳ Connected with upper bank

✳ At a time 16 bit data bus not used. Either lower 8 bit or upper 8 bit.

3.17 two 6212 8 RAM

one input in OR gate is 0.

A_0 and $\overline{BHE}$ decides which RAM need to be active

74138 ⇒ MUX

$A_{15} - A_{17}$ ⇒ selection Pin

$A_{15} - A_{19} = 0$

$0 \leftarrow A_{18}$ — $\overline{G2A}$

$1 \leftarrow A_{19}$ — $\overline{G2B}$

Total address = 00000 H – 07FFF H

$A_{19} - A_{16}$ $A_{19} - A_{16}$ $A_{15} - A_{12}$

0111 ⇒ 7