

SOP:

Using the first Canonical form we get,

$$a = A'B'C'D' + A'B'CD + A'BCD + A'BCD'$$

$$b = A'B'C'D' + A'B'CD + A'BCD + A'BCD'$$

$$c = A'B'C'D' + A'B'CD + A'B'CD + A'BCD + A'BCD' + A'BCD$$

$$d = A'B'C'D' + A'B'CD + A'BCD + A'BCD'$$

$$e = A'B'C'D' + A'B'CD + A'BCD' + A'BCD + A'BCD' + A'BCD + AB'C'D' + AB'CD + AB'CD' + AB'CD$$

$$f = A'B'C'D' + A'B'CD + A'B'CD + A'BCD + A'BCD + A'BCD + AB'C'D' + AB'CD + AB'CD'$$

$$g = A'B'C'D' + A'B'CD + AB'C'D' + A'B'CD + A'B'CD + A'BC'D' + A'B'C'D + A'BCD + A'BCD + A'BCD + A'BCD + A'BCD + A'BCD + AB'CD$$

$$h = A'B'C'D'$$

Here,

~~$$a = m_0 + m_3 + m_5 + m_7 + m_{10}$$~~

~~$$b = m_0 + m_3 + m_5 + m_{10}$$~~

~~$$c = m_0 + m_1 + m_3 + m_5 + m_8 + m_9$$~~

~~$$d = m_2 + m_5 + m_7 + m_{10}$$~~

~~$$e = m_0 + m_1 + m_2 + m_5 + m_6 + m_7 + m_8 + m_9 + m_{10} + m_{11}$$~~

~~$$f = m_0 + m_1 + m_2 + m_3 + m_5 + m_7 + m_8 + m_9 + m_{10}$$~~

$$g = m_0 + m_1 + m_2 + m_3 + m_4 + m_5 + m_6 + m_7 + m_8 + m_9 + \\ m_{10} + m_{11}$$

$$h = m_{12}$$

Let,

$$x = m_0 + m_3 + m_5$$

$$y = m_1 + m_8 + m_9$$

$$z = m_7 + m_{10}$$

$$u = m_2 + m_5$$

$$v = m_6 + m_{11}$$

Therefore,

$$a = x + z$$

$$b = x + m_{10}$$

$$c = x + y$$

$$d = z + u$$

$$e = d + y + v + m_0$$

$$f = c + z + m_2$$

$$g = f + v + m_4$$

$$h = m_{12}$$

Circuit Diagram: Attached

Simulation: Attached

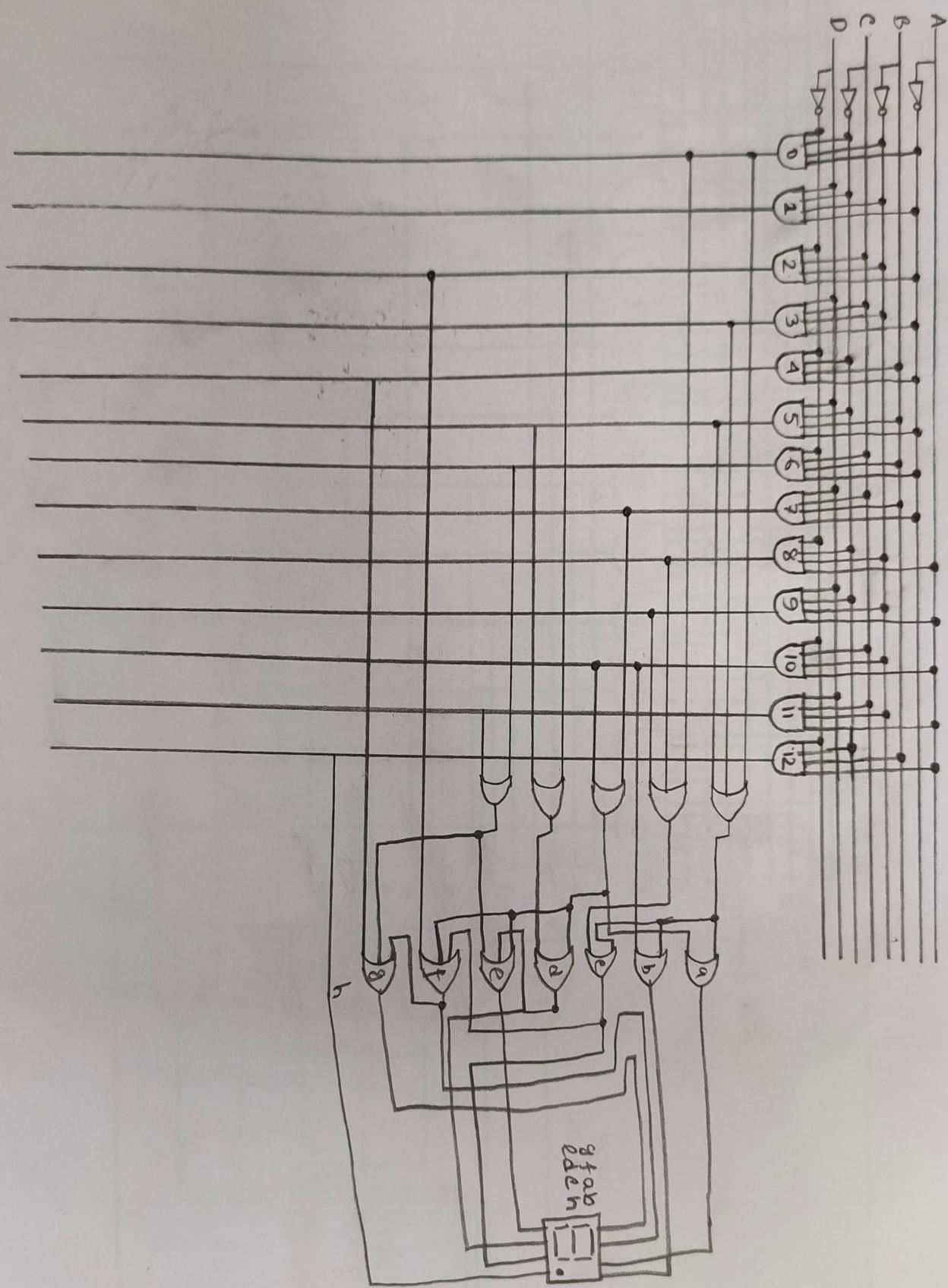
Cost Analysis:

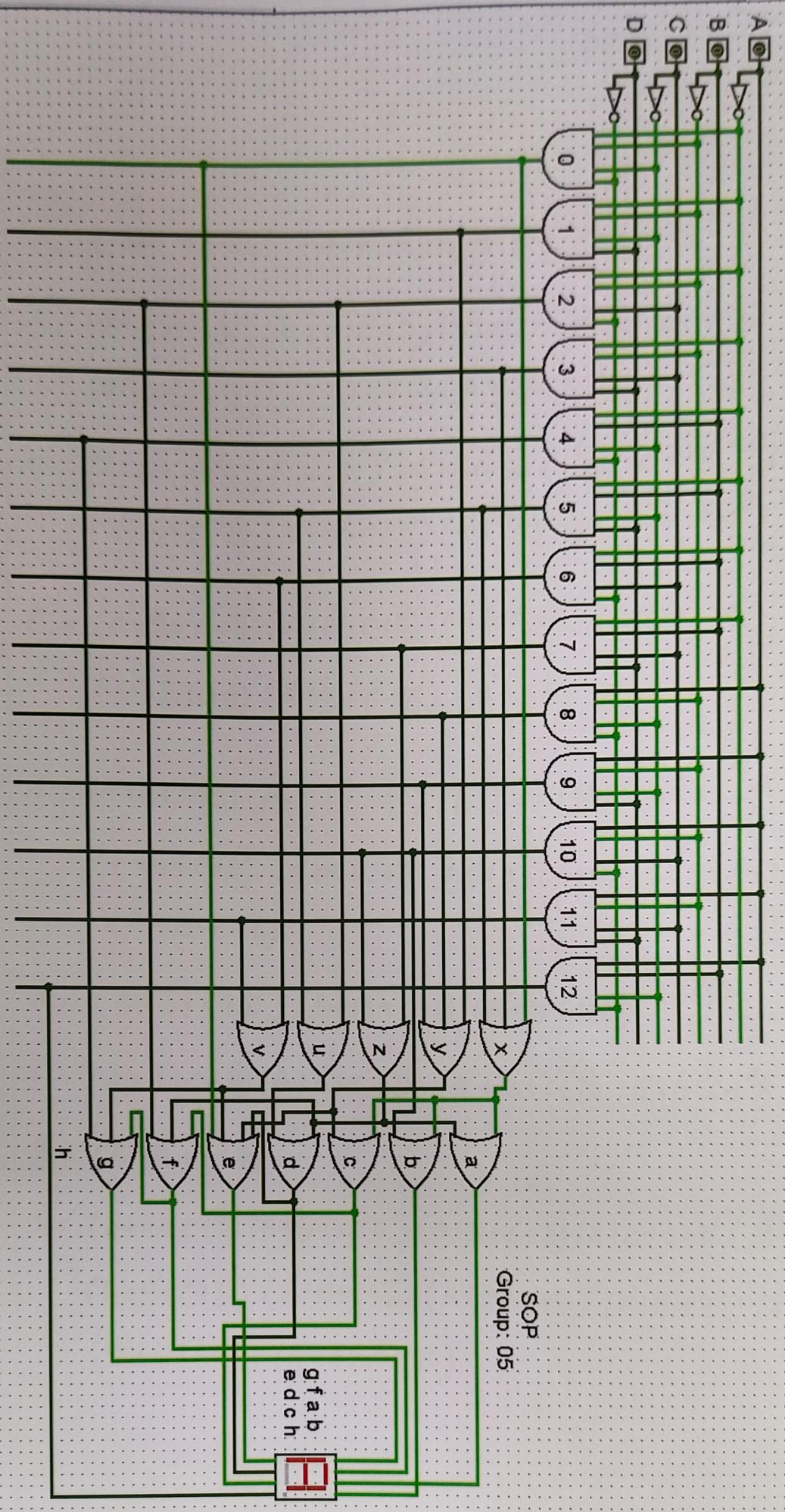
IC Name	Required Gates	Quantity	Price(BDT)
IC 7404 Hex Inverters (NOT Gate)	4	4	25.00
IC 7432 Quadruple 2-inp. OR Gate	8	2	50.00
IC 7408 Quadruple 2-inp AND Gate	12	3	75.00
IC 4075 Triple 3-input OR Gate	5	2	60.00
IC 4073 Triple 3-input AND Gate	14	5	150.00
7 segment Display	10	1	15.00
470 Ohm Resistor	1	12	12.00
Wires	145	145	362.50
Battery + Connector + Regulator			109.00
Bread Board		3	450.00
Total Cost			BDT 1308.50

Procedure:

01. First, we form the equation using 1<sup>st</sup> Canonical form.
02. Then, we implement the 13 min terms first. So that we can reuse them.
03. Then, we make some branches for reducing the IC. We take some common main terms that were used for at least two equations.
04. After that, we just follow the equation and construction the circuit according to the respective IC's pin Diagram.
05. We just connect the min terms using OR IC.
06. It requires the maximum IC, but it was working perfectly too.

SOP





P.S.:

Using the second canonical form we got,

$$a = (A+B+C+D') (A+B+C'+D) (A+B'+C+D) (A'+B+C+D) \\ (A'+B+C+D') (A'+B+C'+D) (A'+B'+C+D)$$

$$b = (A+B+C+D') (A+B+C'+D) (A+B'+C+D) (A+B'+C'+D') \\ (A'+B+C+D) (A'+B+C+D') (A'+B+C'+D) (A'+B'+C+D)$$

$$c = (A+B+C'+D) (A+B+C+D) (A+B'+C+D) (A+B'+C'+D') \\ (A'+B+C+D) (A'+B+C'+D) (A'+B+C+D)$$

$$d = (A+B+C+D) (A+B+C+D') (A+B+C'+D) (A+B'+C+D) \\ (A+B'+C'+D) (A'+B+C+D) (A'+B+C+D') (A'+B+C'+D) \\ (A'+B'+C+D)$$

$$e = (A+B+C'+D') (A+B'+C+D) (A'+B'+C+D)$$

$$f = (A+B'+C+D) (A+B'+C'+D) (A'+B+C+D) (A'+B'+C+D)$$

$$g = (A'+B'+C+D)$$

$$h = (A+B+C+D) (A+B+C+D') (A+B+C'+D) (A+B'+C+D') (A+B'+C+D) \\ (A+B'+C+D') (A+B'+C+D) (A+B'+C'+D) (A'+B+C+D) (A'+B+C+D') \\ (A'+B+C'+D) (A'+B+C'+D')$$

Here,

$$a = (M_1)(M_2)(M_4)(M_6)(M_8)(M_9)(M_{11})(M_{12})$$

$$b = (M_1)(M_2)(M_4)(M_6)(M_7)(M_8)(M_9)(M_{11})(M_{12})$$

$$c = (M_2)(M_4)(M_6)(M_7)(M_{10})(M_{12})(M_{12})$$

$$d = (M_0)(M_1)(M_3)(M_4)(M_6)(M_8)(M_9)(M_{11})(M_{12})$$

$$e = (M_3)(M_4)(M_{12})$$

$$f = (M_4)(M_6)(M_{11})(M_{12})$$

$$g = (M_{12})$$

$$h = (M_0)(M_1)(M_2)(M_3)(M_4)(M_5)(M_6)(M_7)(M_8)(M_9)(M_{10})$$

Let,

$$x = (M_4)(M_6)$$

$$y = (M_{11})(M_{12})$$

$$z = (M_8)(M_9)$$

$$u = (M_1)(z)$$

$$v = (M_2)(x)$$

$$\omega = (M_7)(M_{10})$$

$$m = (M_0)(M_3)$$

therefore,

$$a = (u)(v)(y)$$

$$b = (a)(M_7)$$

$$e = (v)(\omega)(y)$$

$$d = (m)(u)(f)$$

$$e = (M_3)(M_4)(M_{12})$$

$$f = (x)(y)$$

$$g = (M_{12})$$

$$h = (m)(u)(v)(M_5)(w)(M_{11})$$

Circuit Diagram : Attached

Simulation : Attached

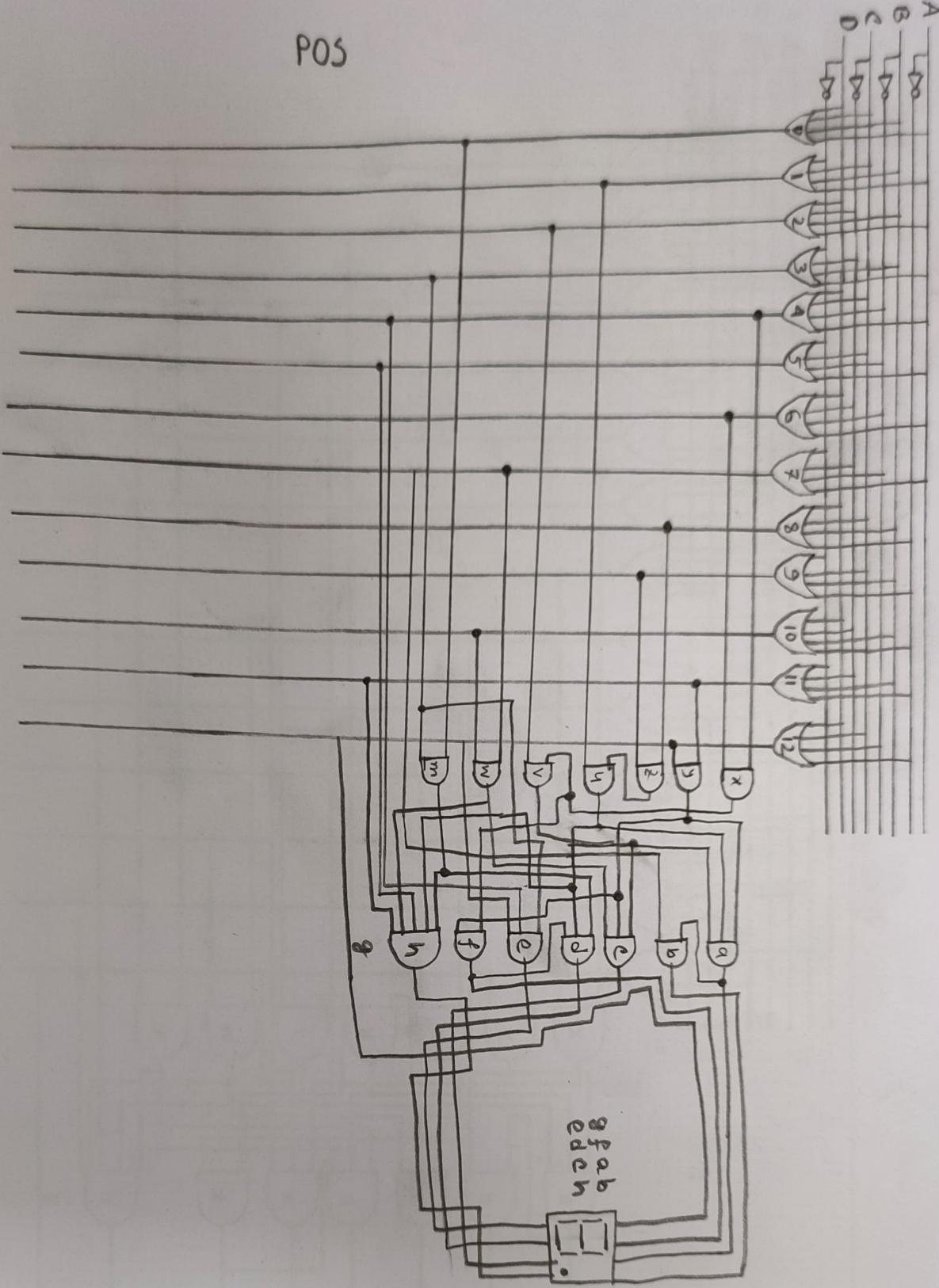
Cost Analysis :

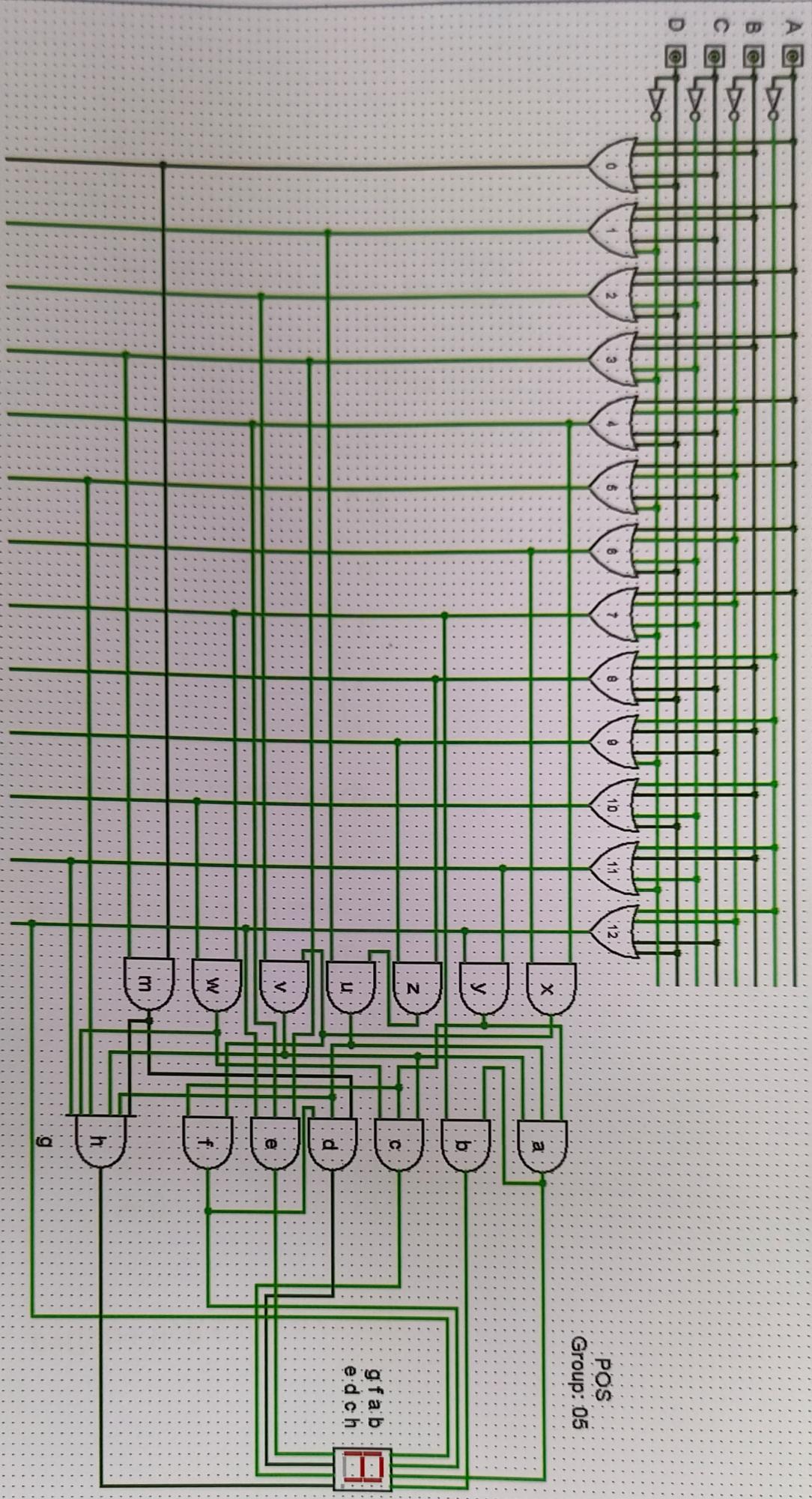
IC Name	Required Rates	Quantity	Price (BDT)
IC 7404 Hex Inverters (NOT gate)	4	1	25
IC 7432 Quadruple 2-inp OR Gate	12	3	75
IC 7408 Quadruple 2-inp. And Gate	10	3	75
IC 4075 Triple 3-input OR Gate	14	5	150
IC 4073 Triple 3-input And Gate	6	2	60
7 segment Display	10	1	15
470 ohm Resistor	1	12	12
Wires	154	154	385
Battery + Connector + Regulator			109
Bread Board		3	450
Total cost			1356 F

procedure :

01. First, we form the equation using the 2nd canonical form.
02. Then, implement the 13 maxterms using OR IC. Connect all the pins according to the pin Diagram. We can now reuse them as many times we need.
03. After that we take some common maxterms which are used in at least two equations. Make them a single branches and use them in two equations. It reduces the gate requirement.
04. Then we connect the max terms according to the 2nd canonical form using the AND IC.
05. After that we connect with the LED using the pin diagram shown in simulation.
06. Finally, our circuit was working perfectly.

POS





K-Map:

Using the 1<sup>st</sup> Canonical Form we get,

$$a = m_0 + m_3 + m_5 + m_7 + m_{10}$$

Map				
$\bar{C}\bar{D}$	$\bar{C}D$	$CD$	$C\bar{D}$	
$\bar{A}\bar{B}$	1	0	1	0
$\bar{A}B$	0	1	1	0
$A\bar{B}$	0	x	x	x
$A\bar{B}$	0	0	0	1

$$a = BD + A'CD + ACD' + A'B'C'D'$$

$$b = m_0 + m_3 + m_5 + m_{10}$$

Map				
$\bar{C}\bar{D}$	$\bar{C}D$	$CD$	$C\bar{D}$	
$\bar{A}\bar{B}$	1	0	1	0
$\bar{A}B$	0	1	0	0
$AB$	0	x	x	x
$A\bar{B}$	0	0	0	1

$$b = BC'D + ACD' + A'B'C'D' + A'B'CD$$

$$C = m_0 + m_1 + m_3 + m_5 + m_8 + m_9$$

Map

	$\bar{C}\bar{D}$	$\bar{C}D$	$CD$	$C\bar{D}$
$\bar{A}\bar{B}$	1	1	1	0
$\bar{A}B$	0	1	0	0
$A\bar{B}$	0	X	X	X
$AB$	1	1	0	0

$$C = BC' + C'D + A'B'D$$

$$d = m_2 + m_5 + m_7 + m_{10}$$

Map

	$\bar{C}\bar{D}$	$\bar{C}D$	$CD$	$C\bar{D}$
$\bar{A}\bar{B}$	0	0	0	1
$\bar{A}B$	0	1	1	0
$A\bar{B}$	0	X	X	X
$AB$	0	0	0	1

$$d = BD + B'C'D'$$

$$e = m_0 + m_1 + m_2 + m_5 + m_6 + m_7 + m_8 + m_9 + m_{10} + m_{11}$$

Map

	$\bar{C}\bar{D}$	$\bar{C}D$	$CD$	$C\bar{D}$
$\bar{A}\bar{B}$	1	1	0	1
$\bar{A}B$	0	1	1	1
$A\bar{B}$	0	X	X	X
$AB$	1	1	1	1

$$e = B'C' + AB' + CD' + BD$$

$$f = m_0 + m_1 + m_2 + m_3 + m_5 + m_7 + m_8 + m_9 + m_{10}$$

Map

	$\bar{C}D$	$\bar{C}D$	$CD$	$CD$
$\bar{A} \bar{B}$	1	1	1	1
$\bar{A} B$	0	1	1	0
$A \bar{B}$	0	x	x	0
$A \bar{B}$	1	1	0	1

$$f = BC' + BD' + AD$$

$$g = m_0 + m_1 + m_2 + m_3 + m_4 + m_5 + m_6 + m_7 + m_8 + m_9 + m_{10} + m_{11}$$

Map

	$\bar{C}D$	$\bar{C}D$	$CD$	$CD$
$\bar{A} \bar{B}$	1	1	1	1
$\bar{A} B$	1	1	1	1
$A \bar{B}$	0	x	x	x
$A \bar{B}$	1	1	1	1

$$g = A' + B'$$

$$h = m_{12}$$

Map

	$\bar{C}D$	$\bar{C}D$	$CD$	$CD$
$\bar{A} \bar{B}$	0	0	0	0
$\bar{A} B$	0	0	0	0
$A \bar{B}$	1	x	x	x
$A \bar{B}$	0	0	0	0

$$h = AB$$

Therefore,

$$a = BD + A'CD + AC'D' + AB'C'D'$$

$$b = BC'D + AC'D' + A'B'C'D' + A'B'CD$$

$$c = B'C' + C'D + A'BD$$

$$d = BD + B'C'D'$$

$$e = BC' + AB' + CD' + BD$$

$$f = B'C' + B'D' + A'D$$

$$g = A' + B'$$

$$h = AB$$

Circuit Diagram: Attached

Simulation: Attached

Cost Analysis:

IC Name	Required Gates	Quantity	Price
IC 7404 Hex Inverters (NOT gates)	4	1	BDT 25.00
IC 7432 Quadruple 2-input OR gates	4	1	BDT 25.00
IC 7408 Quadruple 2-input AND gates	12	3	BDT 75.00
IC 4075 Triple 3-input OR gate	6	2	BDT 60.00
IC 4073 Triple 3-input AND gate	3	1	BDT 30.00
7 Segment Display	10	1	BDT 15.00
470 ohm Resistor	1	12	BDT 12.00
Wires	97	97	BDT 242.00
Battery + Connector + Regulation			BDT 109.00
Bread Board		2	BDT 300.00
Total cost			BDT 893.50

procedure:

01. First, we form the equation for every segment using the first canonical form.

02. Then, we draw the K-map, find out the best group combinations.

03. From every group which inputs are unchanged, we take them and form a new shortest equation.

04. After that, we started to build the circuit.

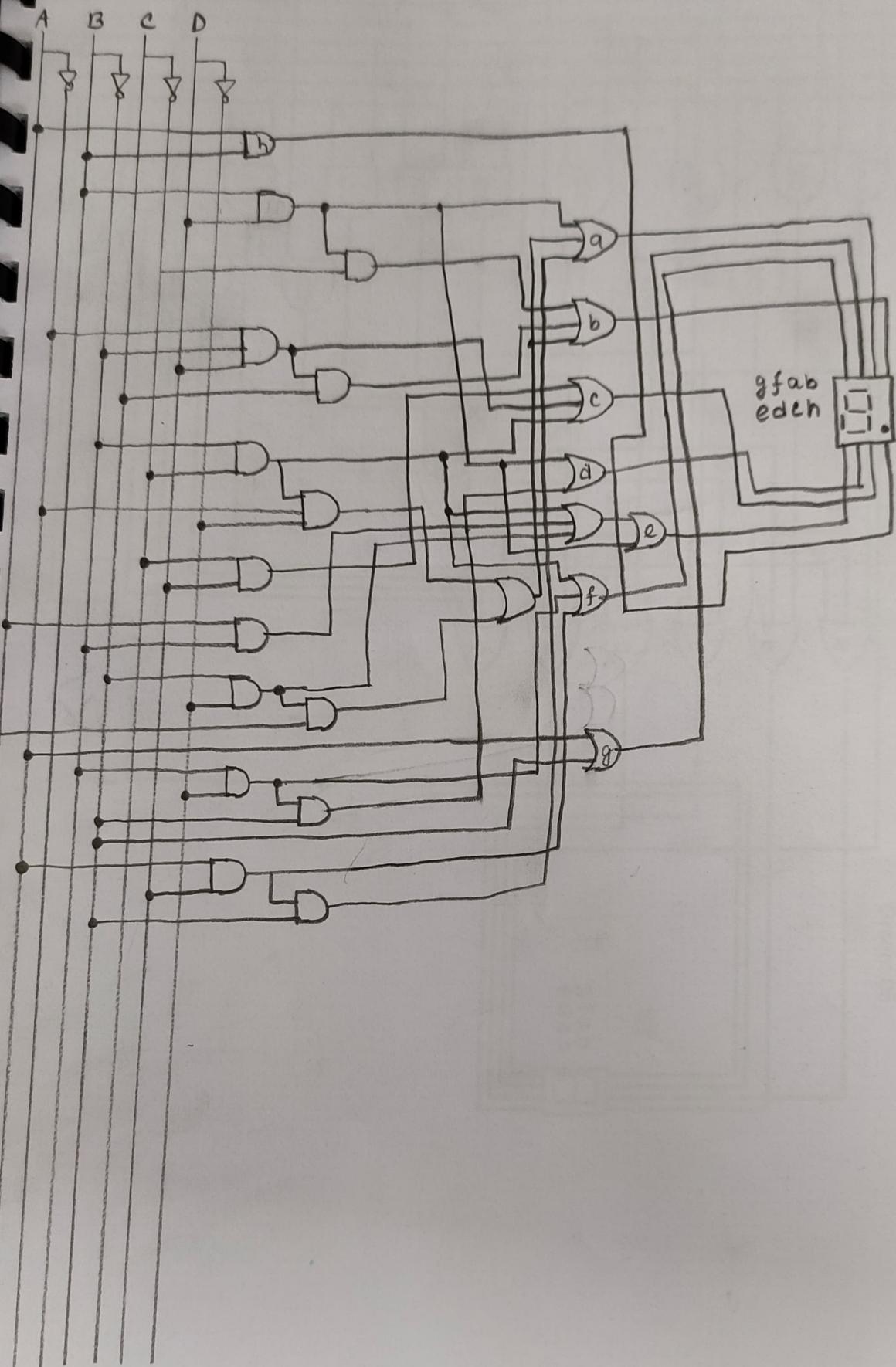
Before we started, we saw that there is some min term that are used at least twice.

05. So, we decided to build them first and reuse them, so that we can reduce the gate count.

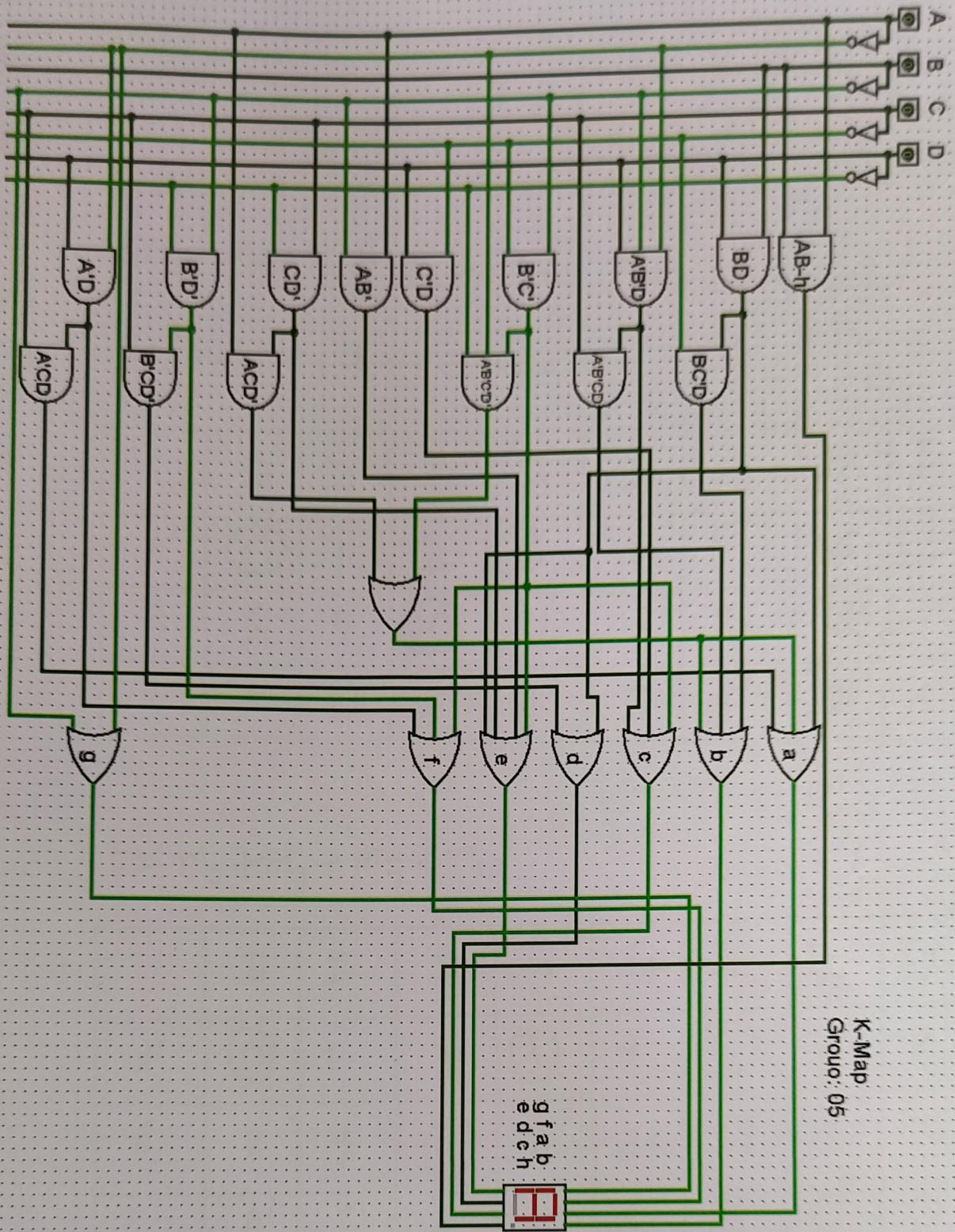
06. Then, we constructed the according the respective pin diagram.

07. It takes less gates than Boolean algebra.  
And it was working perfectly.

# K-MAP



K-Map  
Group: 05



MUX:

Using the 1st Canonical Form we get,

$$a = m_0 + m_3 + m_5 + m_7 + m_{10}$$

	$I_0$	$I_1$	$I_2$	$I_3$	$I_4$	$I_5$	$I_6$	$I_7$
$A'$	0	1	2	3	4	5	6	7
$A$	8	9	10	11	12	13	14	15
	$A'$	0	$A$	$A'$	0	$A'$	0	$A'$

$$b = m_0 + m_3 + m_5 + m_{10}$$

	$I_0$	$I_1$	$I_2$	$I_3$	$I_4$	$I_5$	$I_6$	$I_7$
$A'$	0	1	2	3	4	5	6	7
$A$	8	9	10	11	12	13	14	15
	$A'$	0	$A$	$A'$	0	$A'$	0	0

$$c = m_0 + m_1 + m_3 + m_5 + m_8 + m_9$$

	$I_0$	$I_1$	$I_2$	$I_3$	$I_4$	$I_5$	$I_6$	$I_7$
$A'$	①	②	2	③	4	⑤	6	7
$A$	⑧	⑨	10	11	12	13	14	15
	1	1	0	$A'$	0	$A'$	0	0

$$d = m_2 + m_5 + m_7 + m_{10}$$

	$I_0$	$I_1$	$I_2$	$I_3$	$I_4$	$I_5$	$I_6$	$I_7$
$A'$	0	1	②	3	4	⑤	6	⑦
$A$	8	9	⑩	11	12	13	14	15
	0	0	1	0	0	$A'$	0	$A'$

$$e = m_0 + m_1 + m_2 + m_5 + m_6 + m_7 + m_8 + m_9 + m_{10} + m_{11}$$

	$I_0$	$I_1$	$I_2$	$I_3$	$I_4$	$I_5$	$I_6$	$I_7$
$A'$	①	②	②	3	4	⑤	⑥	⑦
$A$	⑧	⑨	⑩	⑪	12	13	14	15
	1	1	1	$A$	0	$A'$	$A'$	$A'$

$$f = m_0 + m_1 + m_2 + m_3 + m_5 + m_7 + m_8 + m_9 + m_{10}$$

	$I_0$	$I_1$	$I_2$	$I_3$	$I_4$	$I_5$	$I_6$	$I_7$
$A'$	0	1	2	3	4	5	6	7
$A$	8	9	10	11	12	13	14	15
	1	1	1	$A'$	0	$A'$	0	$A'$

$$g = m_0 + m_1 + m_2 + m_3 + m_4 + m_5 + m_6 + m_7 + m_8 + m_9 + m_{10} + m_{11}$$

	$I_0$	$I_1$	$I_2$	$I_3$	$I_4$	$I_5$	$I_6$	$I_7$
$A'$	0	1	2	3	4	5	6	7
$A$	8	9	10	11	12	13	14	15
	1	1	1	1	$A'$	$A'$	$A'$	$A'$

$$h = m_{12}$$

	$I_0$	$I_1$	$I_2$	$I_3$	$I_4$	$I_5$	$I_6$	$I_7$
$A'$	0	1	2	3	4	5	6	7
$A$	8	9	10	11	12	13	14	15
	0	0	0	0	$A$	0	0	0

According to the truth table, g and h are inverted. So, we can use a NOT gate in the output of g to reduce one MUX IC for h.

Circuit Diagram: Attached.

Simulation: Attached.

Cost Analysis:

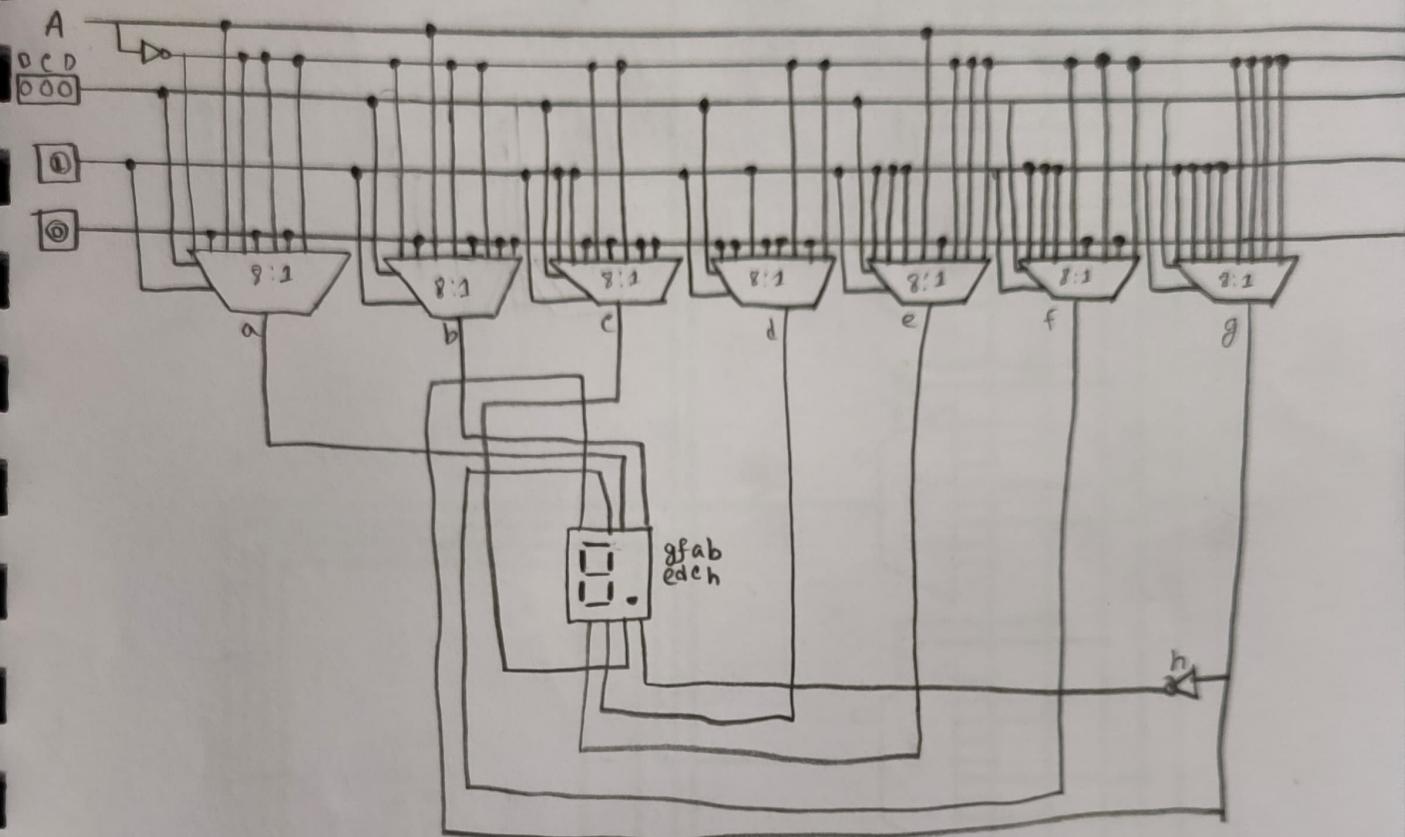
IC Name	Required Gates	Quantity	Price
IC 7404 Hex Inverters (NOT gates)	2	1	BDT 25.00
IC 74151 8:1 Line MUX	15	7	BDT 210.00
7 Segment Display	10	1	BDT 15.00
470 Ohm Resistors	1	12	BDT 12.00
Wires	127	127	BDT 317.50
Battery+Connectors+Regulators			BDT 109.00
Bread Board		2	BDT 300.00
Total Cost			BDT 988.50

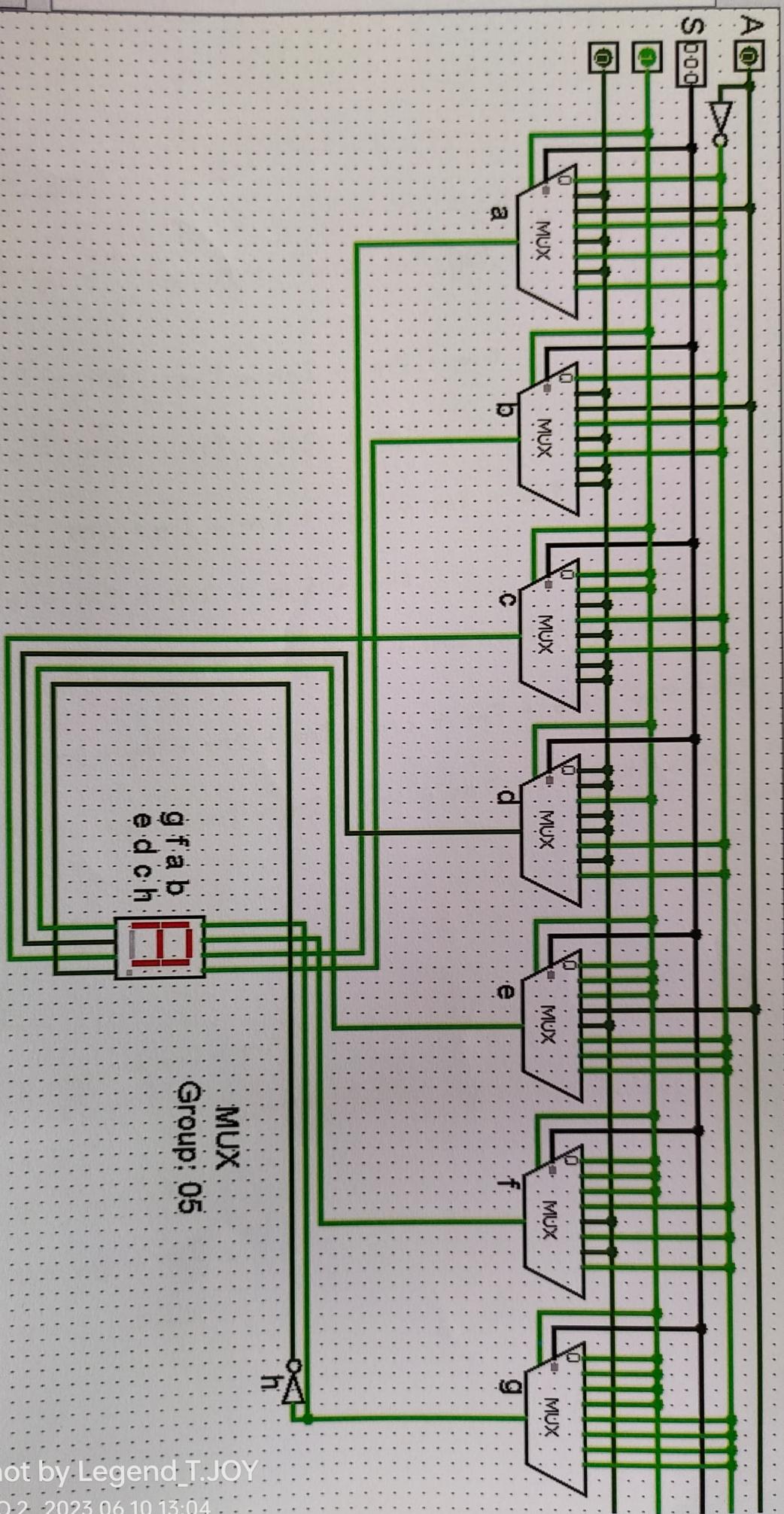
VII

procedure :

01. We select A as input and B, C, D as selection Data.
02. Then, we draw the table and give the number of the min term.
03. After that, we just circle the selected min term.
04. Then in every column we check the circle count.
05. If there was one circle, we take the input as the now header of that circle. If there were two circles, we take the input as 1. If no circle, then 0.
06. After that we started to construct the circuit using MUX.
07. We need one mux IC for every segment. As we have extra NOT gate, we reduce the last Mux IC.
08. According to the respective pin diagram we connect all the pins and complete our circuit.
09. It takes average IC, but it was also working perfectly.

# MUX





Decoder:

Using 1<sup>st</sup> Canonical Form we get,

$$a = m_0 + m_3 + m_5 + m_7 + m_{10}$$

$$b = m_0 + m_3 + m_5 + m_{10}$$

$$c = m_0 + m_1 + m_3 + m_5 + m_8 + m_9$$

$$d = m_2 + m_5 + m_7 + m_{10}$$

$$e = m_0 + m_1 + m_2 + m_3 + m_5 + m_6 + m_8 + m_9 + m_{10} + m_{11}$$

$$f = m_0 + m_1 + m_2 + m_3 + m_5 + m_7 + m_8 + m_9 + m_{10}$$

$$g = m_0 + m_1 + m_2 + m_3 + m_4 + m_5 + m_6 + m_7 + m_8 + m_9 + m_{10} + m_{11}$$

$$h = m_2$$

Let,

$$x = m_0 + m_3 + m_5$$

$$y = m_1 + m_8 + m_9$$

$$z = m_7 + m_{10}$$

$$u = m_2 + m_5$$

$$v = m_6 + m_{11}$$

Therefore,

$$a = n + z$$

$$b = n + m^0$$

$$c = n + y$$

$$d = z + u$$

$$e = d + y + v + m^0$$

$$f = c + z + m^2$$

$$g = f + v + m^4$$

$$h = m^12$$

Circuit Diagram: Attached.

Simulation: Attached.

Cost Analysis:

IC Name	Required Gates	Quantity	Price
IC 7408 Quadruple 2-Input AND	8	2	50
IC 4073 Triple 3-Input AND	5	2	60
IC 74154 4:16 Line Decoder	1	1	75
7 Segment Display (Anode)	1	1	15
470-n Resister	5	1	5
Wires	69	1	173
Battery + Connection + Regulation			109
Breadboard large 830 Pin		1	150
Total Cost			637 TK

## Procedure:

01. First, we form the equation for every segment using 1st Canonical form.

02. Then, we take some common minterms and build some branches. So that we can reuse them.

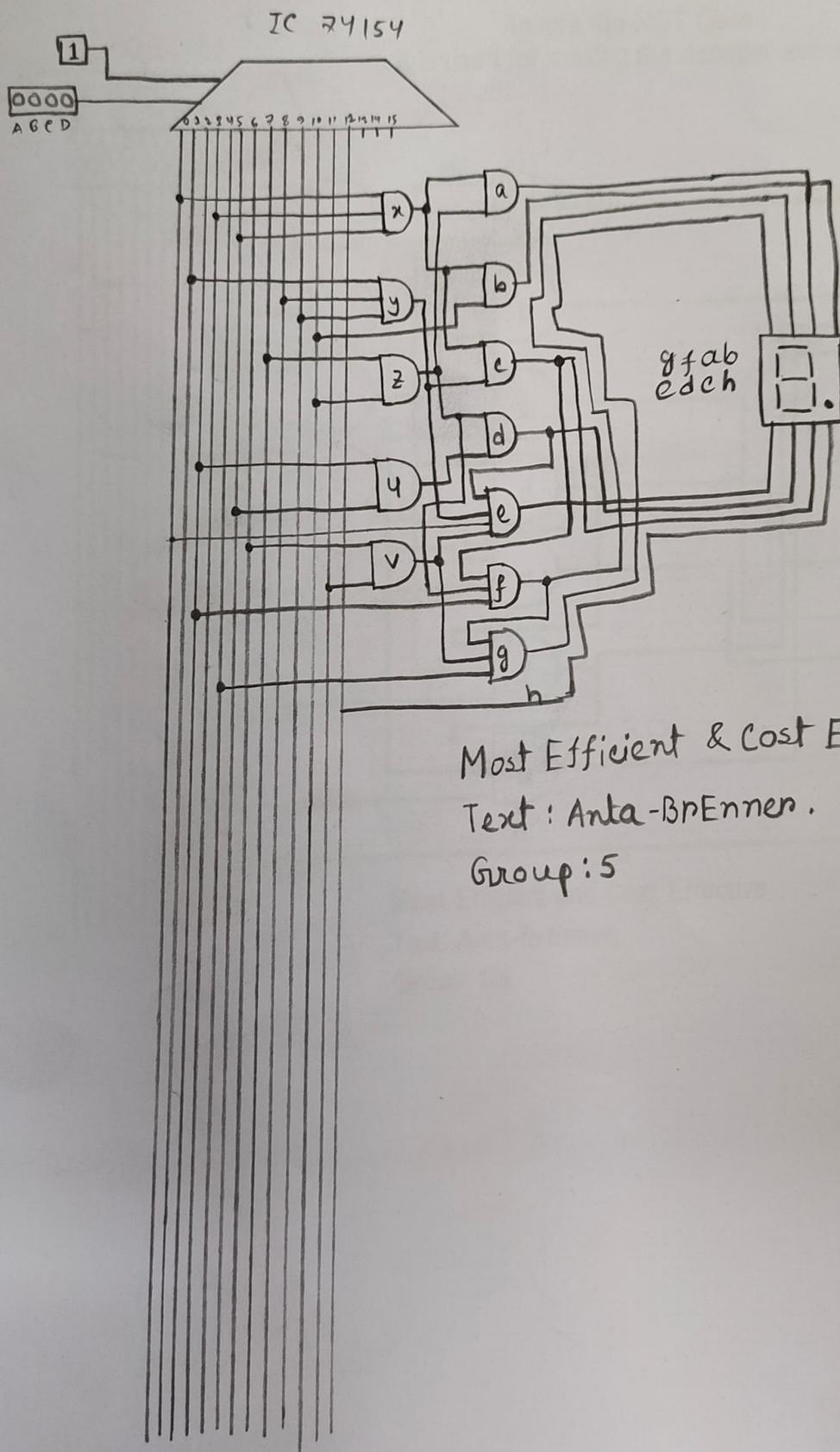
03. As Decoder is active low, which gives us 0 on selected data.

04. So, we decided to use AND IC to construct the circuit. We just replace the OR IC with AND.

05. According to the pin diagram, we connect all the required wires and complete the circuit.

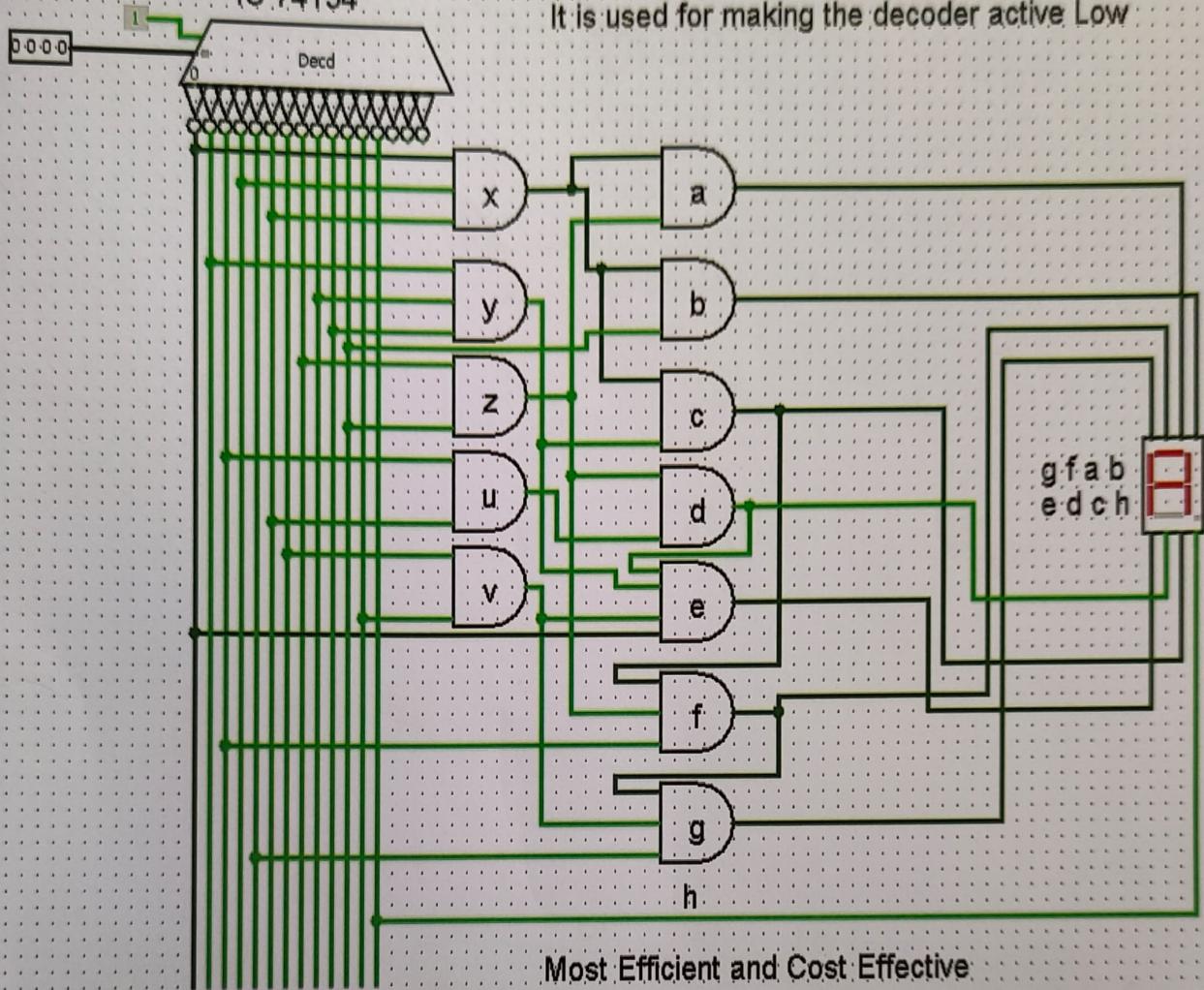
06. It requires less IC than others and it was working perfectly.

# DECODER



IC 74154

Ignore the NOT Gate  
It is used for making the decoder active Low



Most Efficient and Cost Effective

Text: Anta-BrEnner.

Group: 05

## J-K Flip-Flop:

K-Map using the state table:

		Map				
		00	01	11	10	
$Q_3 Q_2$	$Q_1 Q_0$	00	1	X	X	1
		01	1	X	X	1
11	0	0	0	0	0	
10	1	X	X	1		

$$J_0 = Q_3' + Q_2'$$

		Map				
		00	01	11	10	
$Q_3 Q_2$	$Q_1 Q_0$	00	X	1	1	X
		01	X	1	1	X
11	X	0	0	0	0	
10	X	1	1	X		

$$K_0 = Q_3' + \cancel{Q_2} Q_2'$$

Map

	00	01	11	10
00	0	1	X	X
01	0	1	X	X
11	0	0	0	0
10	0	1	X	X

$$J_1 = Q_3' Q_0 + Q_2' Q_0$$

	00	01	11	10
00	X	X	1	0
01	X	X	1	0
11	X	0	0	0
10	X	X	1	0

$$K_1 = Q_3' Q_0 + Q_2' Q_0$$

Map

$Q_3 Q_2$	$Q_1 Q_0$	00	01	11	10
00	00	0	0	1	0
01	01	x	x	x	x
11	11	x	0	0	0
10	10	0	0	1	0

$$J_2 = Q'_2 Q_1 Q_0$$

$Q_3 Q_2$	$Q_1 Q_0$	00	01	11	10
00	00	x	x	x	x
01	01	0	0	1	0
11	11	1	0	0	0
10	10	x	x	x	x

$$K_2 = Q'_3 Q_1 Q_0 + Q_3 Q'_1 Q_0$$

		Map			
		00	01	11	10
$Q_3 Q_2$	00	0	0	0	0
	01	0	0	1	0
	11	x	0	0	0
	10	x	x	x	x

$$J_3 = Q'_3 Q_2 Q_1 Q_0$$

		Map			
		00	01	11	10
$Q_3 Q_2$	00	x	x	x	x
	01	x	x	x	x
	11	1	0	0	0
	10	0	0	0	0

$$K_3 = Q_2 Q_1 Q'_0$$

All in one place:

$$J_0 = Q'_3 + Q'_2$$

$$\bar{0} K_0 = Q'_3 + Q'_2$$

$$J_1 = Q'_3 Q_0 + Q'_2 Q_0$$

$$K_1 = Q'_3 Q_0 + Q'_2 Q_0$$

$$J_2 = Q'_2 Q_1 Q_0$$

$$K_2 = Q'_3 Q_1 Q_0 + Q'_3 Q_1 Q'_0$$

$$J_3 = Q'_3 Q_2 Q_1 Q_0$$

$$K_3 = Q_2 Q_1 Q'_0$$