L-10 / 14.03.2024 / Quiz-1

CSE 331 / L-11 / 16.03.2024

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Page-178

Division Instruction:

DIV ⇒ unsigned

IDIV ⇒ signed

DZV BL
↳ Divison 8 bit (Byte Division)
then, dividened will be 16 bit, AX

BL) AX (Q = AL

R = AH

DIV BX → Word Division

BX) DX - AX (Q = AX

R = DX

DX = 0000H
AX = 0005H
BX = 0002H

DZV BX
2) 5 (2
4
1

AX = 0002H
DX = 0001H

99/

DX = 0000H ⇒ 0 5
AX = 0005H ⇒ 5
BX = FFFEH = 65534/-2

DZV ⇒ AX = 0000H
DX = 0005H

IDIV ⇒ AX = FFFEH
DX = 0001H

* 2's /

AX = 00FB H = 251

BL = FF H ⇒ 255/-1

DZV ⇒ AL = 00H
AH = FB H

IDZV ⇒ AL = FF05H → Divide Overflow
AH = 00H

* Divide Overflow ⇒ if result or remainder doesn't fit in AX or DX, then divide overflow.

* Sign Extention:

if DX = ?
AX = known
} need to extend sign.

CBW ⇒ convert Byte to Word
CWD ⇒ convert Word to Double Word

for unsigned ⇒ DX will fill by 0000H

for signed ⇒ DX will fill by the sign bit of AX.

* For higher version:

MOVZX ⇒ for unsigned data
MOVSX ⇒ for signed data

Exercise ~~Ex~~ Important
One Question must in the next exam

Lecture Slide - 5-6

B. Brey
Chapter-5

Arithmetic and Logic Instruction:

Addition:

- addition are not allowed for memory to memory and segment register.

⇒ Three type of addition available

(i) Just Add ⇒ ADD

(ii) Add with carry ⇒ ADC

(iii) Increment ⇒ INC

⇒

ADD CX, BX

⇒ CX = ~~CX~~ CX + BX

ADC CX, BX

⇒ CX = CX + BX + C (C → carry flag)

INC CX

⇒ CX = CX + 1H

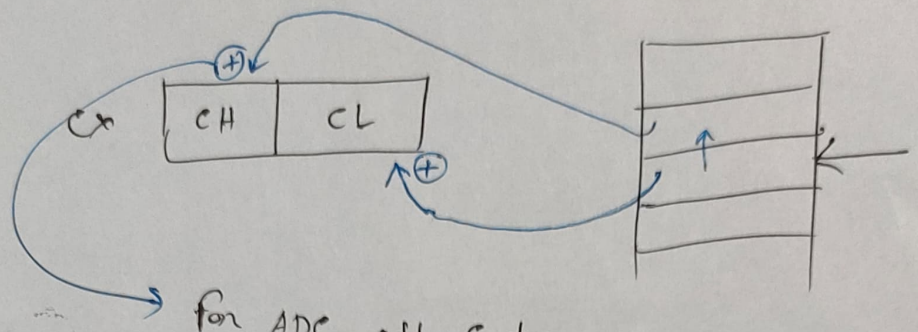
1H in Decimal 1

Question Pattern:

A Complete the ADD operation and explain flag register. ⇒ Slide-8

ADD CX, [BX] ⇒ Register indirect mode

⇒



for ADC, add C too

Slide - 6, 10, 11, 13, 15, 16 ⇒ Example

✱ After ADD operation,

Flag register ⇒ S, Z, C, A, P, O

changes according to the result.

✱ For INC, if the destination/source referred to memory, then size of data must need to declare.

INC BYTE PTR[BX]

✱ Subtraction:

- same as Addition

SUB CX, BX ⇒ CX = CX - BX

SBB CX, BX ⇒ CX = CX - BX - C

DEC CX ⇒ CX = CX - 1H

Slide - 17, 20, 22, 23 ⇒ Example

SUB ⇌ SBB

#connection

Comparison:

- Only one instruction, where destination operand never changes.
- used for conditional jump operation. CMOV or JMP
- flag bits will change according to the result of ~~the~~ subtraction between two operand.

CMP AX, BX → changes the flag bits.

⇒ AX - BX = Result

Slide - 25,

Multiplication & Division:

- we already covered MUL, IMUL, DIV, IDIV.

Here one special case is Immediate mode.

Slide - 27, 28

- 16-bit multiplication available in 80186
- must be in signed multiplication
- three operand

MUL AX, BL, 3H → immediate data as multiplier

↑ 16-bit destination Register

↳ Register/memory location as multiplicand

⇒ For division:

- imediate mode not available
- two kind of error → attempt to divide by zero
  → divide overflow

} Generate interrupt and show error message

slide - 35, 39,

⇒ Use of Remainder of a division

- could be used to round up the quotient on dropped to truncate the quotient.
- can also be converted to a fractional remainder.

Page - 40 Done

L-12 / 21.03.2024

No class

No content