



North South University
Department of Electrical & Computer Engineering
LAB REPORT- 06

Course Code: CSE 231L

Course Title: Digital Logic Lab

Section: 08

Lab Number: 06

Experiment Name: Introduction to Multiplexers and Decoders.

Multiplexers and Decoders

Experiment Date: 08 May 2023

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Submitted by Group Number: 05

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Submitted To: Pritthika Dhar

Experiments Name: Introduction to Multiplexers & DecodersObjectives:

- Understand the concept of Multiplexing in the context of digital logic circuits.
- Learn about the internal logic of digital multiplexers.
- Implement digital logic functions using multiplexers.
- Observe and analyze the operations of the 3 to 8 Line Decoder.

Apparatus:

- 1x IC 7404 Hex Inverter (NOT gates).
- 2x IC 4073 3-Input AND gates.
- 1x IC 7432 2-Input OR gates.
- 1x IC 74151 (8:1) Multiplexer.
- 1x IC 74138 (3:8 Line Decoder).
- Trainer Board.
- Wires.

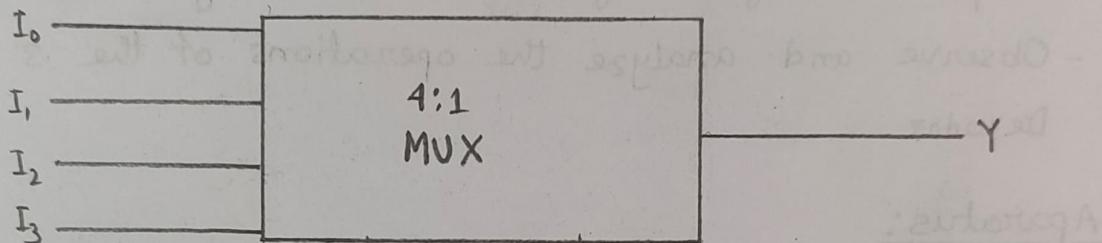
Theory:

Multiplexer: A multiplexer, also known as a "MUX", is a digital electronic device that allows multiple digital signals to be transmitted over a single communication channel or line. It selects one of ~~the~~ many input signals and forwards the selected input to a single output line.

Multiplexers are commonly used in digital systems such as computers and telecommunications networks, where multiple signals need to be transmitted over a single line. They are also used in various other applications,

such as in digital audio and video system, where multiple data channels need to be transmitted over a limited bandwidth.

A block diagram and truth table for a 4:1 Multiplexer (4 inputs and 1 output) is given below:



S_1 S_0

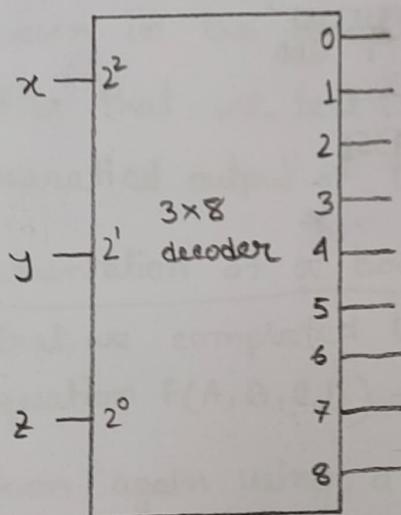
S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

Output Equation:

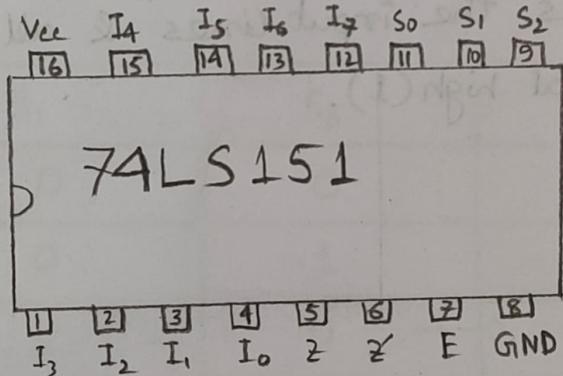
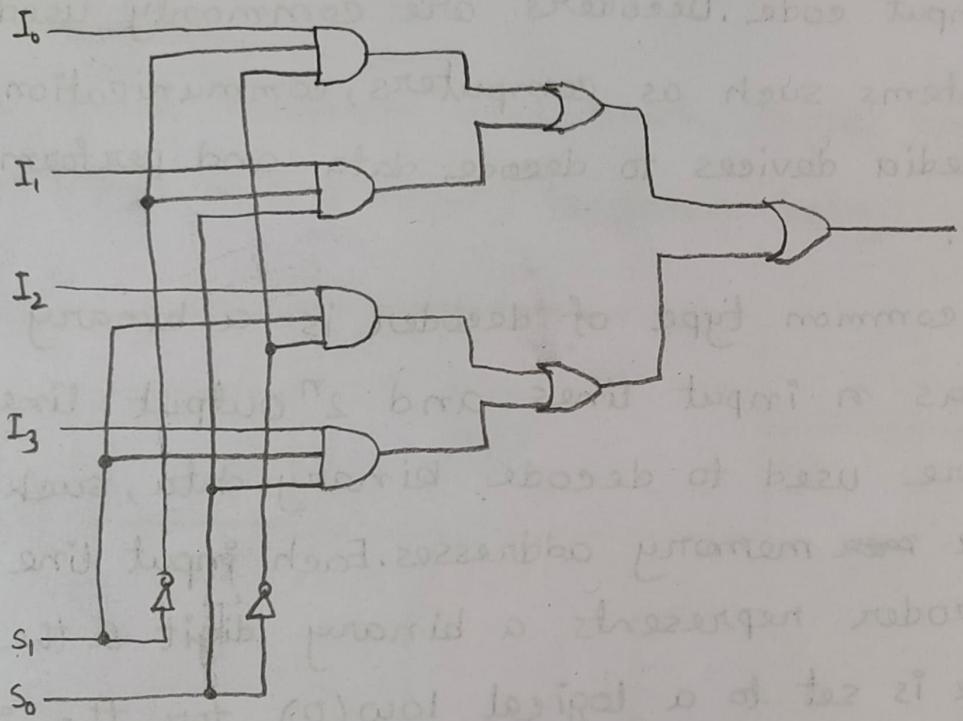
$$Y = I_0 S_1 S_0 + I_1 S_1 S_0 + I_2 S_1 S_0 + I_3 S_1 S_0$$

Decoder: A decoder is a digital electronic device that takes an input code and produces one or more outputs based on the input code. Decoders are commonly used in digital systems such as computers, communication systems & multimedia devices to decode data and perform various operations.

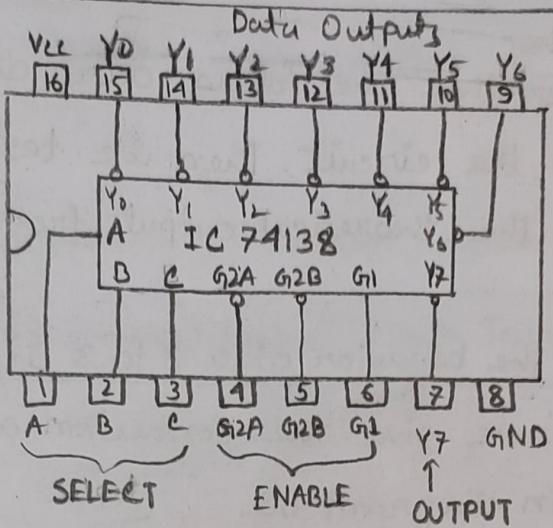
The most common type of decoder is a binary decoder, which has n input lines and 2^n output lines. Binary decoders are used to decode binary data, such as digital signals or ~~mem~~ memory addresses. Each input line of a binary decoder represents a binary digit & the corresponding output line is set to a logical low(0) for the input code that matches the input lines & all other output lines are set to a logical high(1).



Circuit Diagram:



Pinout of IC 74151



Experimental Procedure:

1:1 Multiplexer using basic logic gates:

1. First we complete the truth table for the given equation,
 $F(A, B, C) = \sum(0, 2, 3, 6)$
2. Then, determine the inputs for I_0 to I_3 using a short table method. After that we start to build the circuit shown in the circuit diagram.
3. After that we test the practical output with the theoretical output of the data table.

Implementation of a Boolean function using 8:1 Multiplexers:

1. First, we completed the truth table for the given equation $F(A, B, C, D) = \sum(1, 2, 3, 6, 9, 12, 13)$ on Table F.2.1.
2. Then again using a table method we determine the inputs for I_0 to I_7 . In this case we use A, B, C as the selection inputs S_2, S_1, S_0 respectively. Then we draw the IC diagram with pin ~~diagram~~ details in figure F.2.1.

3. After

3. After that we follow our drawn figure F.2.1 & build the circuit. Then we test our circuit with the theoretical output from table F.2.1.

Analyzing the behavior of a 3 to 8 Line Decoder (IC 74138):

1. First, we give the connection as shown in the Figure of Pin diagram B3.
2. Then, we give the connection high to G_{1A} and low to both G_{1B} & G_{2B} .
3. Then we connect the input A, B, C to the pin 1, 2, 3 respectively.
4. Then we test our circuit and write down the output value on Table F.3.1.

Simulation:

Attached.

Experimental Data Table

Experimental Data (Implementing a Boolean function using a 4:1 MUX)

A	B	C	F(Theoretical)	Data Table
0	0	0	1	
0	0	1	0	$I_0 = \bar{C}$
0	1	0	1	
0	1	1	1	$I_1 = 1$
1	0	0	0	
1	0	1	0	$I_2 = 0$
1	1	0	1	
1	1	1	0	$I_3 = \bar{C}$

Table F.1.1

Experimental Data (Implementing a Boolean function using an 8:1 MUX IC)

A	B	C	D	F(Theoretical)	Data Inputs
0	0	0	0	1	$I_0 = 1$
0	0	0	1	1	
0	0	1	0	0	$I_1 = D$
0	0	1	1	1	
0	1	0	0	0	$I_2 = \bar{D}$
0	1	0	1	0	
0	1	1	0	0	$I_3 = D$
0	1	1	1	1	
1	0	0	0	0	$I_4 = D$
1	0	0	1	1	
1	0	1	0	1	$I_5 = \bar{D}$
1	0	1	1	0	
1	1	0	0	0	$I_6 = 0$
1	1	0	1	0	
1	1	1	0	1	$I_7 = 1$
1	1	1	1	1	

Table F.2.1

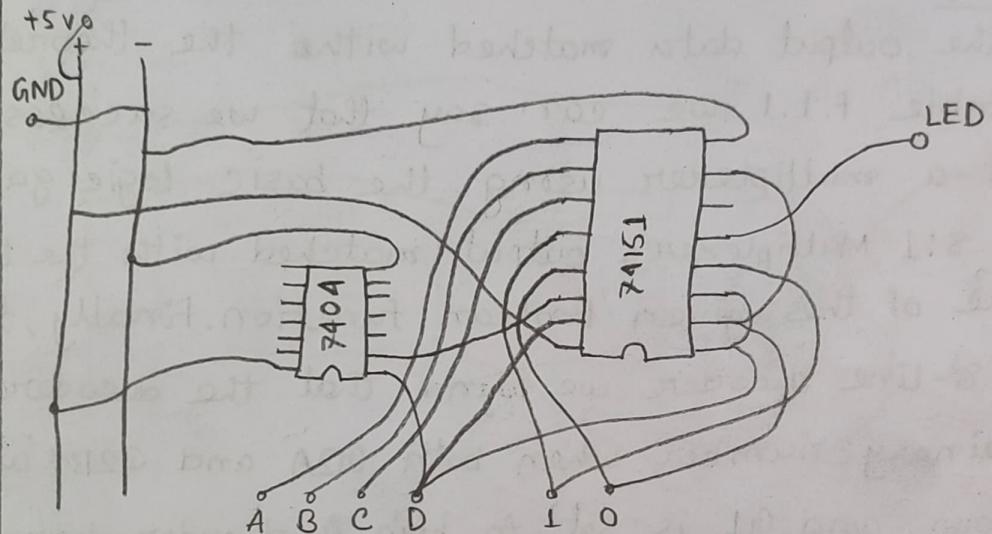


Figure F.2.1

Experimental Data (3 to 8 Line Decoder)

Enable Inputs		Select Inputs			Outputs							
G1	G2	C	B	A	Y ₀	Y ₁	Y ₂	Y ₃	Y ₄	Y ₅	Y ₆	Y ₇
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

Table F.3.1

Results:

As the output data matched with the theoretical data on table F.1.1, we can say that we successfully build a multiplexer using the basic logic gates. Also, our 8:1 Multiplexer's output matched with the theoretical value of the given Boolean function. Finally, from the 3 to 8-line decoder we found that the decoder decodes the binary number when both G2A and G2B are set to low and G1 is set to high, & decoder behaves like an active low decoder.

Question & Answers (Q/A):

E.1: Simulation attached with the report.

E.2: IC diagram for the implementation of the following function using IC 74151

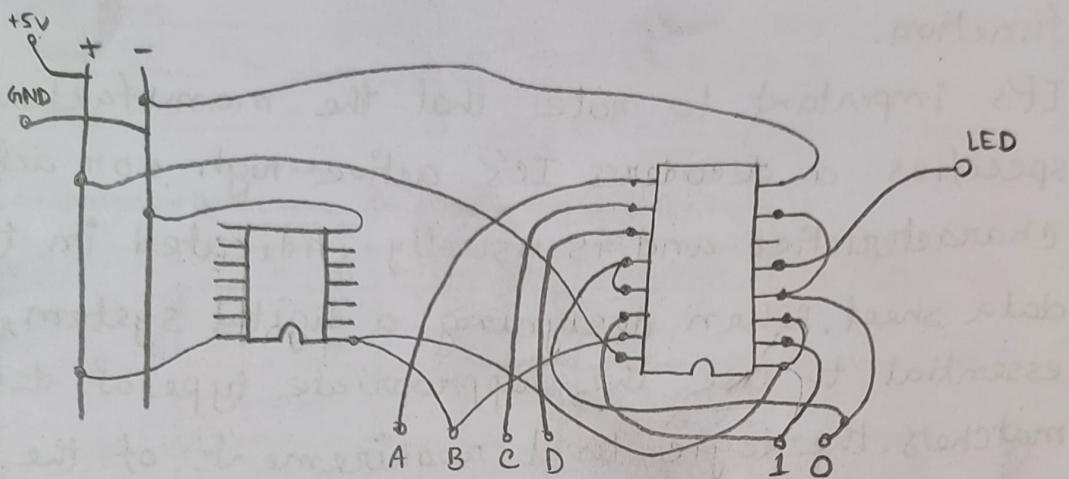
$$\text{Equation: } F(A, B, C, D) = \sum(1, 2, 3, 6, 9, 12, 13)$$

Selection Inputs are A, C, D.

Table:

	l_0	l_1	l_2	l_3	l_4	l_5	l_6	l_7
\bar{B}	0	1	2	3	8	9	10	11
B	4	5	6	7	12	13	14	15
Inputs	0	B'	1	B'	3	1	0	0

Diagram:



E.3:

The terms "active-high" and "active-low" are used to describe the behavior of digital electronic devices with respect to their input & output signals.

Active High: An active high device gives output as high voltage (1); if there are multiple output pins, others pin will give low voltage output.

Active Low: Active low device gives output as low voltage (0); if there are multiple outputs pins, others pin will give higher voltage output.

In a decoder IC, the output signals are usually active-low, meaning they are at a logical-low level when the corresponding input code is detected. The output signals are typically connected to other components in a digital system, such as a memory

chip or a microcontroller, to enable the desired function.

It's important to note that the manufacturer specifies a decoder's IC's active-high or active-low characteristic and is usually indicated in the data sheet. When designing a digital system, it's essential to use the appropriate type of decoder that matches the logic level requirements of the system.

Discussion: After completing these three experiments we completely understood the concept of ~~Multiplexer~~ Multiplexer and decoder. We learnt about the logic behinds a multiplexer and learnt to build multiplexer with basic logic gates. We also learnt to implement digital logic functions using multiplexer. We also observed the behavior of a 3 to 8 Line decoder. We can also implement a Boolean function using decoder with the help of some AND Gates (for active low decoder). As before in this experiment we again face problems with the NOT IC. It's always crash during experiments. After changing, we successfully built our circuits. We ~~before~~ also face problems with multiplexer. We know multiplexer will enable by input high, but ~~the~~ our multiplexer was enabling on low input. Finally, we complete our experiment successfully.

F. Data Sheet:

Instructor's Signature:

Group: 05	Date: 08/05/2023
Section: 8	Report:

F.1 Experimental Data (Implementing a Boolean function using a 4:1 MUX):

A	B	C	F (Theoretical)	Data Inputs	F (Practical)
0	0	0	1	$I_0 = \bar{C}$	
0	0	1	0		
0	1	0	1	$I_1 = 1$	
0	1	1	1		
1	0	0	0	$I_2 = 0$	
1	0	1	0		
1	1	0	1	$I_3 = \bar{C}$	
1	1	1	0		

Table F.1.1

F.2 Experimental Data (Implementing a Boolean function using an 8:1 MUX IC):

A	B	C	D	F (Theoretical)	Data Inputs	F (Practical)
0	0	0	0	1	$I_0 = 1$	
0	0	0	1	1		
0	0	1	0	0	$I_1 = D$	
0	0	1	1	1		
0	1	0	0	0	$I_2 = 0$	
0	1	0	1	0		
0	1	1	0	0	$I_3 = D$	
0	1	1	1	1		
1	0	0	0	0	$I_4 = D$	
1	0	0	1	1		
1	0	1	0	1	$I_5 = \bar{D}$	
1	0	1	1	0		
1	1	0	0	0	$I_6 = 0$	
1	1	0	1	0		
1	1	1	0	1	$I_7 = 1$	
1	1	1	1	1		

Table F.2.1

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08/05/23.

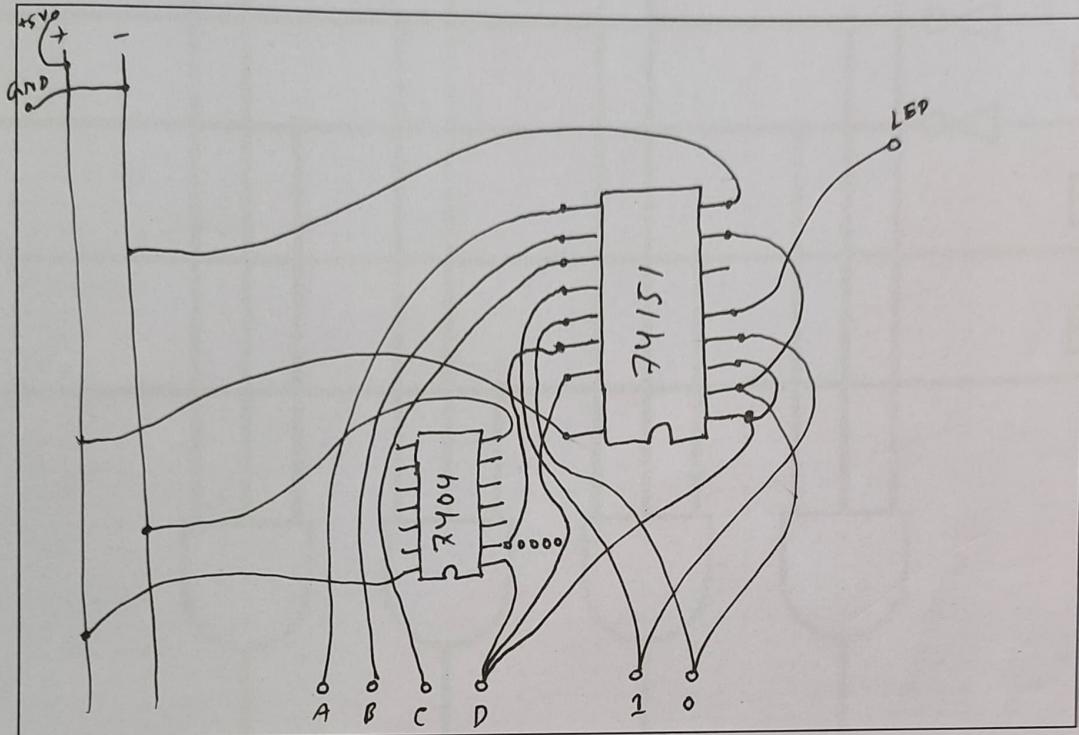


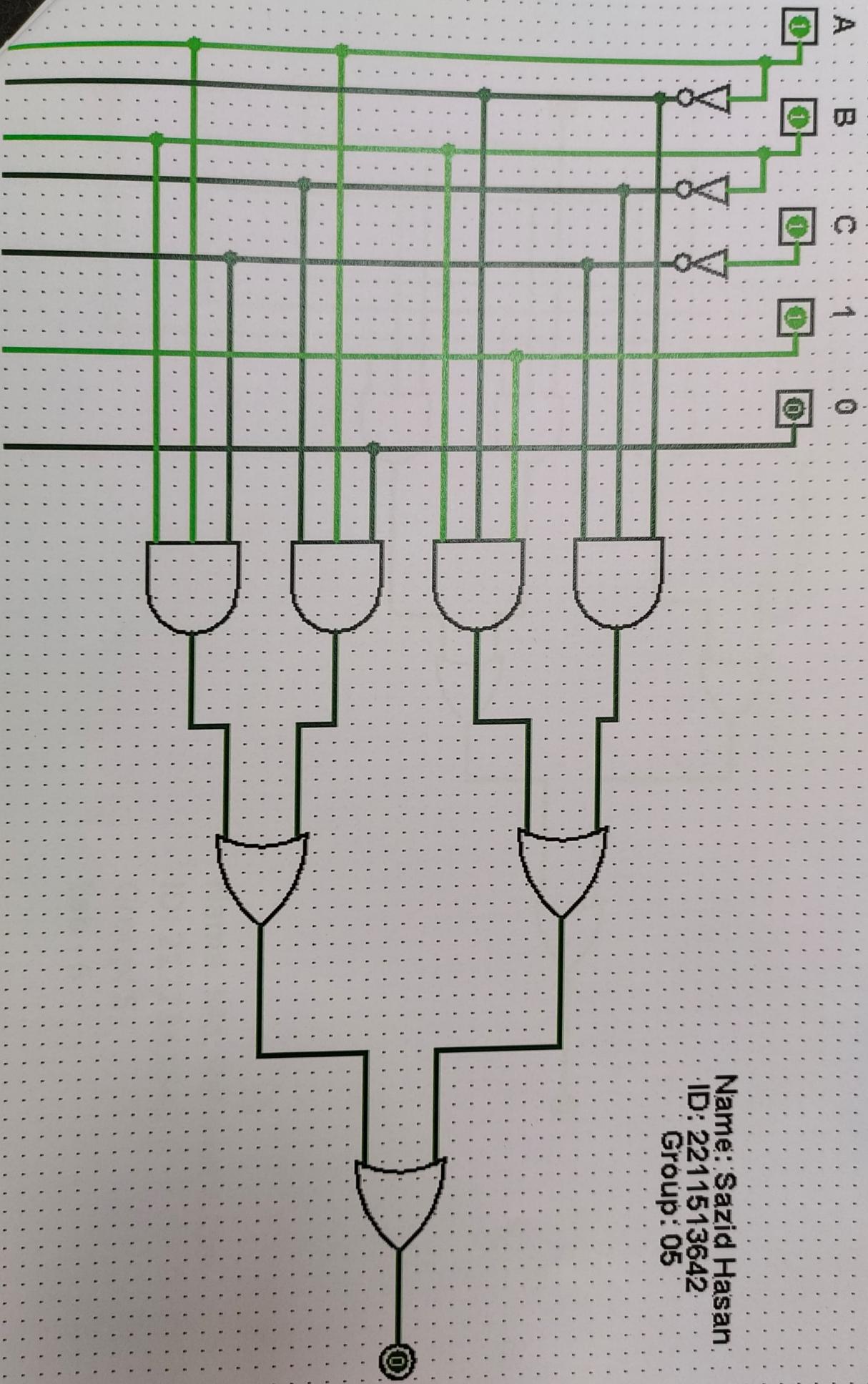
Figure F.2.1

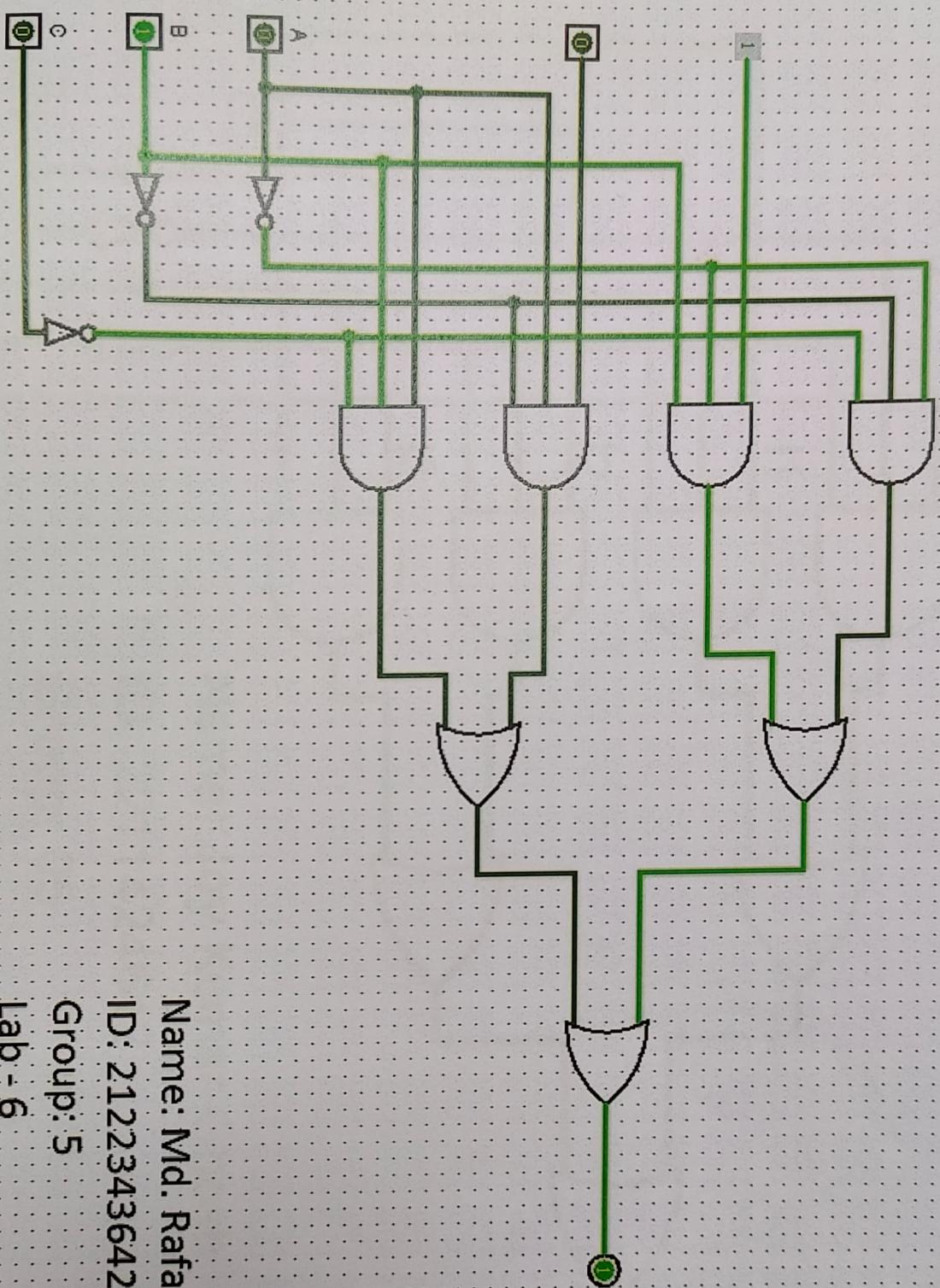
F.3 Experimental Data (3 to 8 Line Decoder):

Enable Inputs		Select Inputs			Outputs							
G1	G2	C	B	A	Y ₀	Y ₁	Y ₂	Y ₃	Y ₄	Y ₅	Y ₆	Y ₇
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

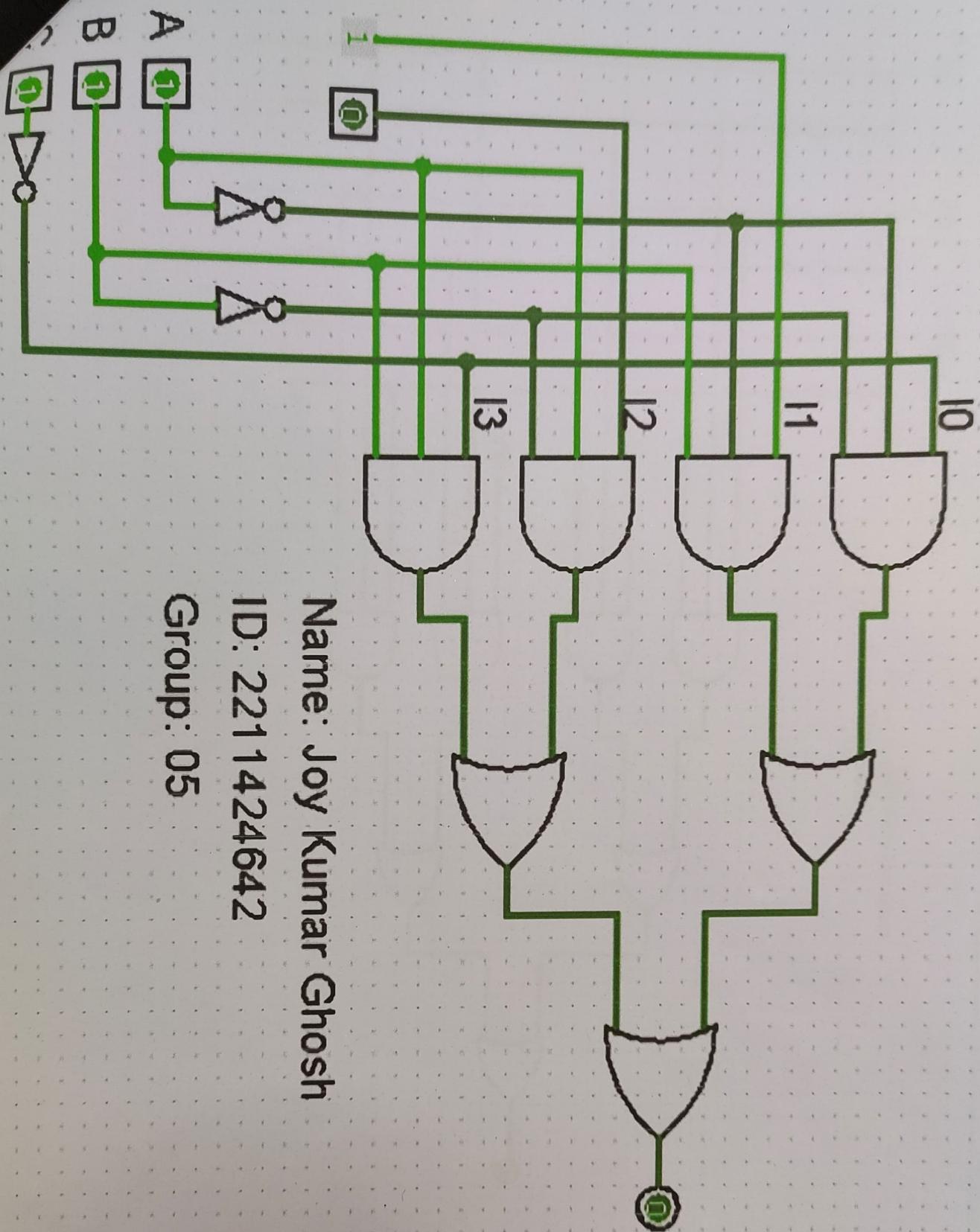
Table F.3.1

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11/05/23
Bonus → 1





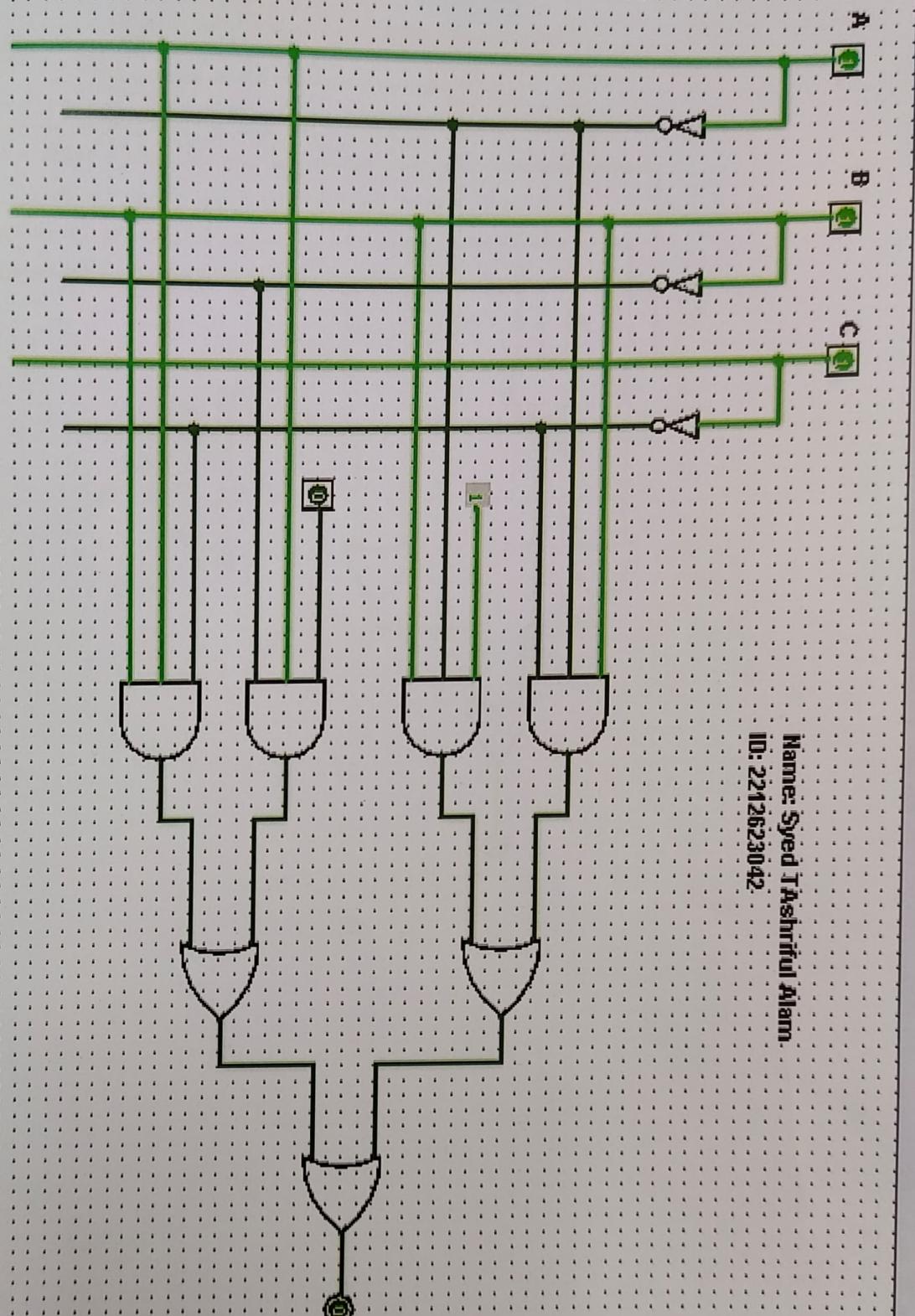
Name: Md. Rafawat Islam
ID: 2122343642
Group: 5
Lab - 6



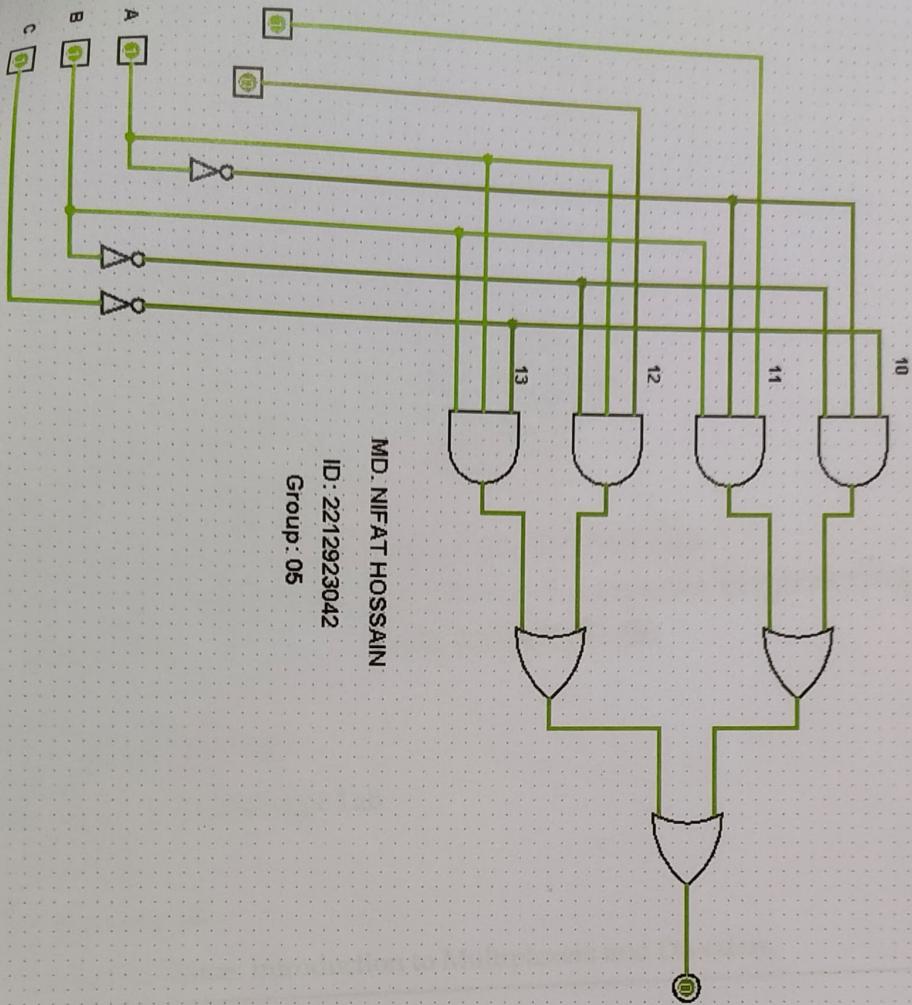
Name: Joy Kumar Ghosh

ID: 2211424642

Group: 05



Name: Syed Tashriful Alam
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MD. NIFAT HOSSAIN

ID: 2212923042
Group: 05

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