BOLD and Underline Word should be written with color pen. Use pencil margin, Page number with color pen, all drawing with pencil, table body with pencil but text will be ball pen.

<u>Experiment Name:</u> KCL, Current Divider Rule with Parallel and Ladder Circuit.

<u>Objectives:</u>

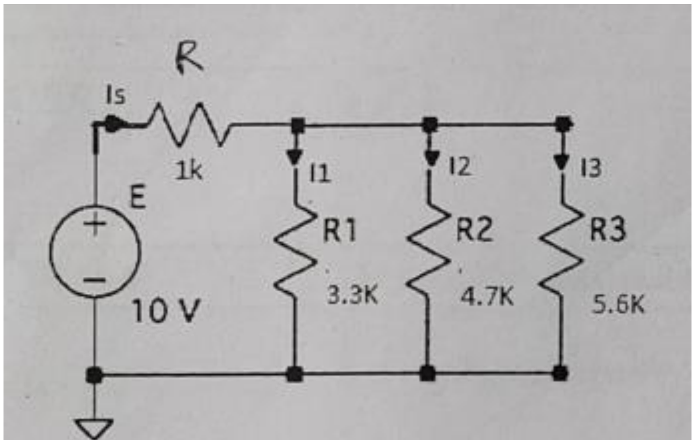
- Learn how to connect parallel circuit on a breadboard.
- Validate the current divider rules.
- Verify Kirchhoff's current law.
- Verify KCL and KVL in ladder circuit.

<u>Apparatus:</u>

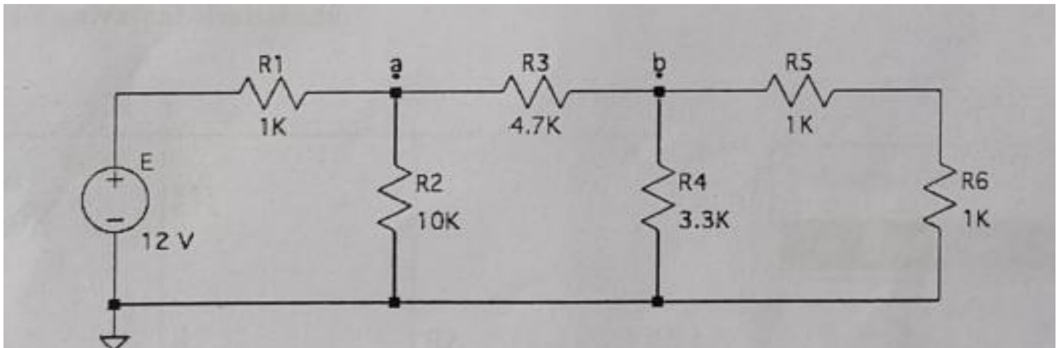
- Breadboard
- Resistors (1 KΩ, 3.3 KΩ, 4.7 KΩ, 5.6 KΩ, 10 KΩ)
- Digital Multimeter (DMM)
- DC Power Supply
- Wires

<u>Circuit Diagram:</u>

Update the resistors with measured Value and Source Voltage



Circuit 1



Circuit 2

Update the resistors with measured Value and Source Voltage

Data Table:

Table 1:

26/0

Experimental readings				Theoretical values			
I_S	I_{R1}	I_{R2}	I_{R3}	I_S	I_{R1}	I_{R2}	I_{R3}
4.05	1.78	1.23	1.05	4.15	~~4~~ 1.82	1.25	1.08

% Error			
I_S	I_{R1}	I_{R2}	I_{R3}
2.41	2.20	1.6	2.78

Table 2:

I_S	4.05	Is Total Current equal to sum individual current?
Sum of individual Current ($I_{R1} + I_{R2} + I_{R3}$)	4.06	Approximately Equal

Table 3:

Experimental Req	Theoretical Req	% Error
~~2.54~~ 2.42	2.41	0.41

Calculation (Theoretical Values):

Here,
R_1, R_2 and R_3 are in parallel ~~connection~~ connection.

$$\therefore R_T' = \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right)^{-1}$$

$$= \cancel{\frac{1}{0.986}}$$

$$= \left(\frac{1}{3.247} + \frac{1}{4.720} + \frac{1}{5.520}\right)^{-1}$$

$$= \cancel{1.426\,k\Omega}\ 1.427\ k\Omega$$

R & R_T' are in ~~series~~ seriese connection:

$$\therefore R_{eq} = R + R_T'$$
$$= 0.986 + 1.427$$
$$\cancel{= 2.42\ k\Omega}$$
$$= 2.413\ k\Omega$$

$$\therefore I_s = \frac{10}{2.413} = 4.15\ A$$

$$\therefore I_1 = \frac{I_s R_T'}{R_1} = \frac{4.15 \times 1.427}{3.247} = 1.82\ A$$

Error Calculation:

$$I_s = \left| \frac{\text{Theoretical } I_s - \text{Measured } I_s}{\text{Theoretical } I_s} \right| \times 100\%$$

$$= \left| \frac{4.15 - 4.05}{4.15} \right| \times 100\%$$

$$= 2.41\ \%$$

$$I_{R_1} = \left| \frac{1.82 - 1.78}{1.82} \right| \times 100\%$$

$$= 2.20\ \%$$

$$R_{eq} = \left| \frac{2.41 - 2.42}{2.41} \right| \times 100\%$$

$$= 0.41\ \%$$

Table 4:

Component	Voltage (V)	Current (mA)
E	12.06 (V)	2.58 mA
R1(1k) (0.99 kΩ)	2.57	2.58 mA
R2 (9.78 kΩ)	9.46	0.97
R3 (4.64 kΩ)	7.42	1.61
R4 (3.22 kΩ)	1.98	0.62
R5 (0.99 kΩ)	0.99	1.00
R6 (0.98 kΩ)	0.96	1.01

Table - 5

Theoretical Values & % of Error

Component	Voltage (V)	% of Error	Current (mA)	% of Error
E	12		2.58	0%
R1 (0.99 kΩ)	2.55	0.78%	2.58	0%
R2 (9.78 kΩ)	9.49	0.32%	0.97	0%
R3 (4.64 kΩ)	7.47	0.67%	1.61	0%
R4 (3.22 kΩ)	1.96	1.02%	0.61	1.64%
R5 (0.99 kΩ)	0.98	1.02%	0.99	1.01%
R6 (0.98 kΩ)	0.97	1.03%	0.99	2.02%

Calculation (Theoretical Values):

$$R_T = R_1 + \left(R2 \parallel \left(R3 + \left(R_4 \parallel \left(R_5 + R6\right)\right)\right)\right)$$

$$= R_1 + \left(R2 \parallel \left(R_3 + \left(R_4 \parallel 1.97\right)\right)\right)$$

$$= R_1 + \left(R2 \parallel \left(R_3 + \left(\frac{1}{3.22} + \frac{1}{1.97}\right)^{-1}\right)\right)$$

$$= R_1 + \left(R2 \parallel \left(R_3 + 1.22\right)\right)$$

$$= R_1 + \left(R2 \parallel 5.86\right)$$

$$= R_1 + \left(\frac{1}{9.78} + \frac{1}{5.86}\right)^{-1}$$

$$= R_1 + 3.665$$

$$= 0.99 + 3.665$$

$$= 4.66 \; k\Omega$$

$$\therefore I_S = \frac{12}{4.66} = 2.58\ mA$$

$$\therefore I_{R1} = I_S = 2.58\ mA$$

$$\therefore V_{R1} = I_{R1} \cdot R1 = 2.58 \times 0.99 = 2.55\ V$$

$$\therefore I_{R2} = \frac{3.665 \times 2.58}{9.78} = 0.97\ mA$$

$$\therefore V_{R2} = 0.97 \times 9.78 = 9.49\ V$$

$$\therefore I_{R3} = \frac{3.665 \times 2.58}{5.86} = \cancel{2.04\ mA}\ 1.61\ mA$$

$$\therefore V_{R3} = 1.61 \times 4.64 = 7.47\ V$$

$$\therefore I_{R4} = \frac{1.61 \times 1.22}{3.22} = 0.61\ mA$$

$$\therefore V_{R4} = 0.61 \times 3.22 = 1.96\ V$$

$$\therefore I_{R5} = \frac{1.61 \times 1.22}{1.97} = 0.99\ mA$$

$$\therefore V_{R5} = 0.99 \times 0.99 = 0.98\ V$$

$$\therefore I_{R6} = I_{R5} = 0.99\ mA$$

$$\therefore V_{R6} = 0.99 \times 0.98 = 0.97\ V$$

Error Calculation:

$$\text{Error of } I_{R4} = \left| \frac{0.61 - 0.62}{0.61} \right| \times 100\%$$

$$= 1.64\%$$

$$\text{Error of } V_{R4} = \left| \frac{1.96 - 1.98}{1.96} \right| \times 100\%$$

$$= 1.02\%$$

Graph:

N/A

Result Analysis:

After completing this experiment, we found that in every node sum of the entering current and the sum of the leaving current are the same. We also found that in every closed loop sum of the voltage rise and voltage drop is approximately zero. That means we verify the KCL and KVL in our ladder circuit.

Questions and Answers:

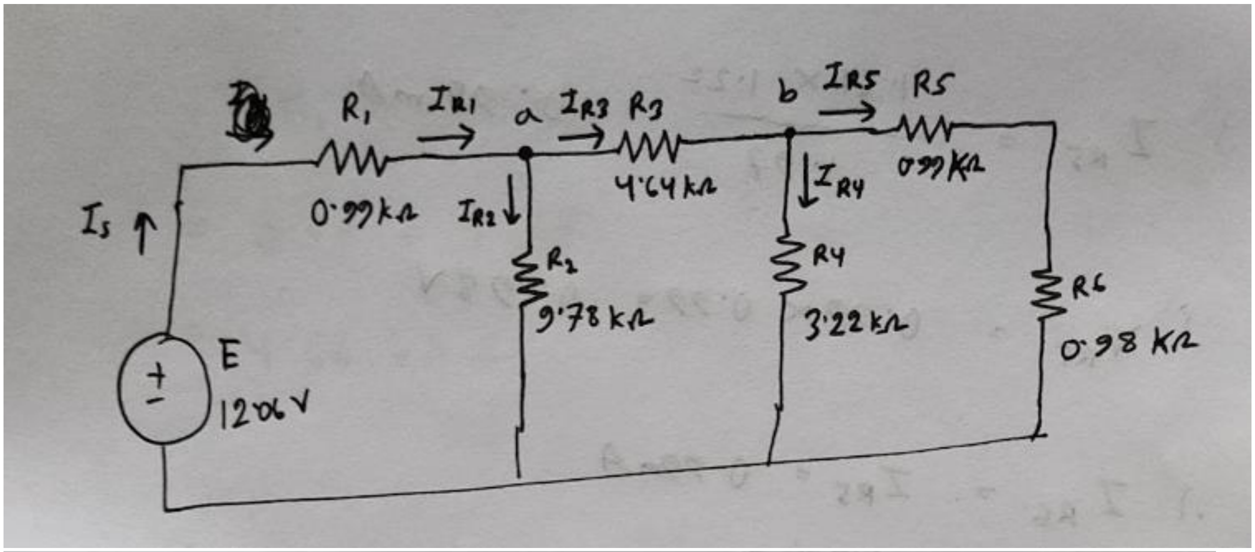
01. KCL:

Kirchhoff's Current Law (KCL) states that the algebraic sum of currents entering and leaving any node in an electrical circuit is always zero. In other words, the total current flowing into a node must be equal to the total current flowing out of that node.

This law is based on the principle of conservation of charge, which states that charge cannot be created or destroyed, but can only be transferred from one location to another. Thus, any current that enters a node must eventually leave that node to maintain the balance of charge in the circuit.

KCL can be expressed mathematically as:
$\sum i = 0$
where $\sum i$ is the algebraic sum of currents entering and leaving a node and is equal to zero.

02. ..



in node a,

$$I_{R1} = I_{R2} + I_{R3}$$

$$\Rightarrow 2.58 = 0.97 + 1.61$$

$$\therefore 2.58 = 2.58$$

in node b,

$$I_{R3} = I_{R4} + I_{R5}$$

$$1.61 = 0.62 + 1.00$$

$$\therefore 1.61 \approx 1.62 \text{ (Approximately Equal)}$$

According to the Kirchhoff's Current Law, entering current is equal to the leaving current. Here for node a and b, entering current and the leaving current are the same. Hence, in node a and b it follows KCL.

03. ..

3)

Calculation already showed.

From Table-1:

Source Current, $I_s = 4.05 \text{ mA}$

Sum of individual Current,

$$I_{R1} + I_{R2} + I_{R3} = (1.78 + 1.23 + 1.05)$$
$$= 4.06 \text{ mA}$$

Here,

entering current, $= 4.05 \text{ mA}$

leaving current $= 4.06 \text{ mA}$

They are approximately equal.

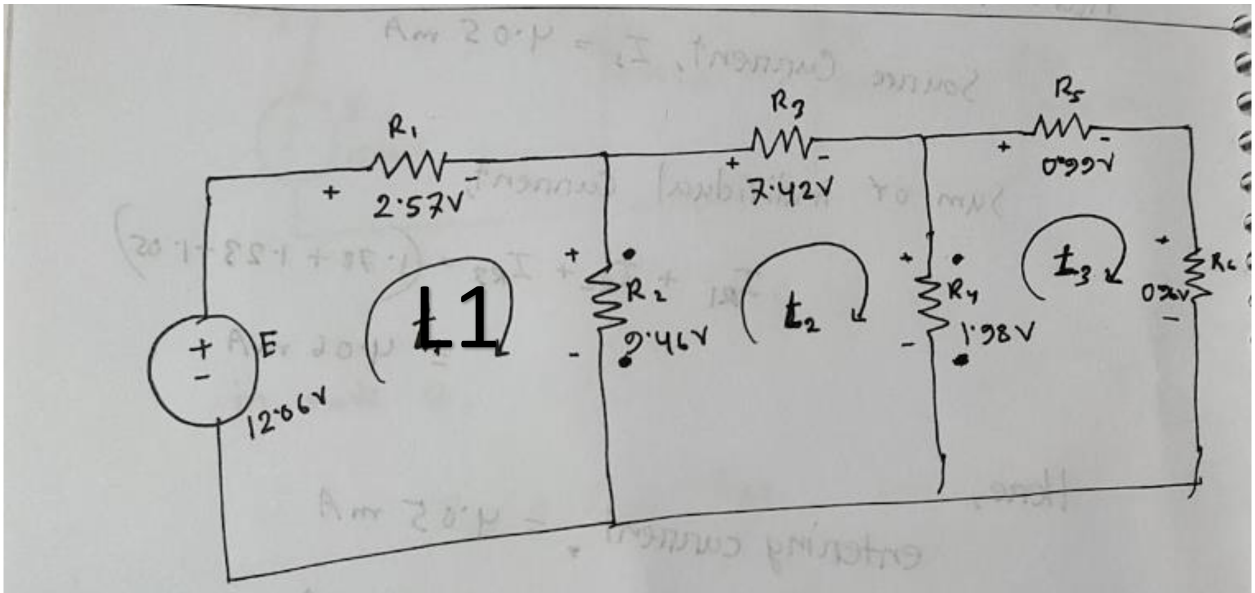
According to the Kirchhoff's Current Law, entering current is equal to the leaving current.

Hence, our circuit follows KCL.

04. Already Showed in Data Table Section.

05. Already Showed in Data Table Section.

06. …



Loop-1:

$$E - V_{R1} - V_{R2} = 12.06 - 2.57 - 9.46$$
$$= 0.03 \approx 0$$

Loop-2:

$$V_{R2} - V_{R3} - V_{R4} = 9.46 - 7.42 - 1.98$$
$$= 0.06 \approx 0$$

Loop-3 :

$$V_{R4} - V_{R5} - V_{R6} = 1.98 - 0.99 - 0.96$$
$$= 0.03 \approx 0$$

According to Kirchhoff's Voltage Law (KVL), the sum of all voltages around any closed loop in an electrical circuit is always zero. In other words, the algebraic sum of all the voltage drops and gains around a closed loop must be equal to zero.
In Loop 1, 2, and 3, here sum of the voltage raise and voltage drop is approximately zero.
Hence, we can say that our circuit follows KVL.

Discussion:

This experiment taught us to connect a parallel circuit on a breadboard. We also verify KCL and KVL in a ladder circuit. In this experiment, we face some difficulties in current measurement on circuit 1. DMM shows us too much less current than the theoretical value. Then we tried to solve this problem and found that a wire was slightly broken, and the current measurement was not accurate. After changing the wire, we get the correct result. In the ladder circuit, we don't face any difficulties and complete it at first.

Attachment:

01. Signed Data Table.
02. Simulation using Multisim.