North South University
Department of Electrical and Computer Engineering
CSE231L: Digital Logic Design Lab

Project Title: 7 Segment Display

Requirements:

1. Project Report.
2. Software Implementation.
3. Hardware Implementation.

Phase 1: Combinational part

Project Report:

- Truth Table
- Boolean Algebra (Solve it)
- Using NAND gates (Solve it)
- Using NOR gates (Solve it)
- Using SOP and POS (Solve it)
- K- map (Solve it)
- Using MUX and Decoder
- Mention the cost

Software Implementation: Implement All the mentioned (above) circuits in Logisim and choose the optimized one and explain why it is optimized. (briefly)

Hardware Implementation: Now implement the chosen optimized circuit in Hardware.

Phase 2: Sequential part

Project Report:

- Truth Table, Excitation Table, Characteristics Table
- Solve it Using J-K Flip Flop.
- Solve it Using T Flip Flop.
- Solve it Using D Flip Flop.
- Mention the cost

Software Implementation: Implement All the mentioned (above) circuits in Logisim and choose the optimized one and explain why it is optimized. (briefly)

Hardware Implementation: Now implement the chosen circuit in Hardware.

Seven-Segment Display (Groupwise):

Group No:	Display
1	St-Hopper-01.
2	BiLly-Dacre02
3	JonathanB-03.
4	Nancy-nAtaLia
5	Anta-BrEnNer.
6	6-Lucas_2006.
7	Joyce-Byers07
8	Erica-Priah08