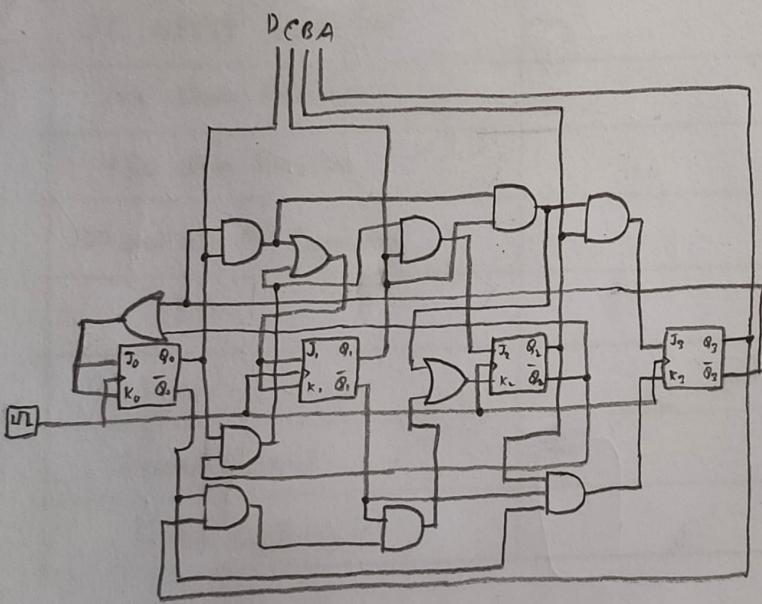


Circuit Diagram :



Simulation: Attached.

Cost Analysis:

IC Name	Required Gates	Quantity	Price
IC 7432 Quadruple 2-input OR gates	3	1	BDT 25
IC 7408 Quadruple 2-input AND gates	8	2	BDT 50
IC 7476 Dual J-K Flip Flop	4	2	BDT 100
IC NE555 Timer IC		1	BDT 25
10k Ohm Resistor		2	BDT 5
470 Ohm Resistor		5	BDT 10
100 and 0.1 uF Capacitor		2	BDT 10
LED		5	BDT 10
Wires		25	BDT 62.50
Bread Board		1	BDT 150
Total Cost			BDT 447.50

Procedure:

01. First, we complete the state table using the excitation and characteristic table of J-k Flip Flop.
02. Then, we draw the k-Map for every input of J, and K.
03. From the k-Map we find out the best group combinations and form the shortest equation for inputs.

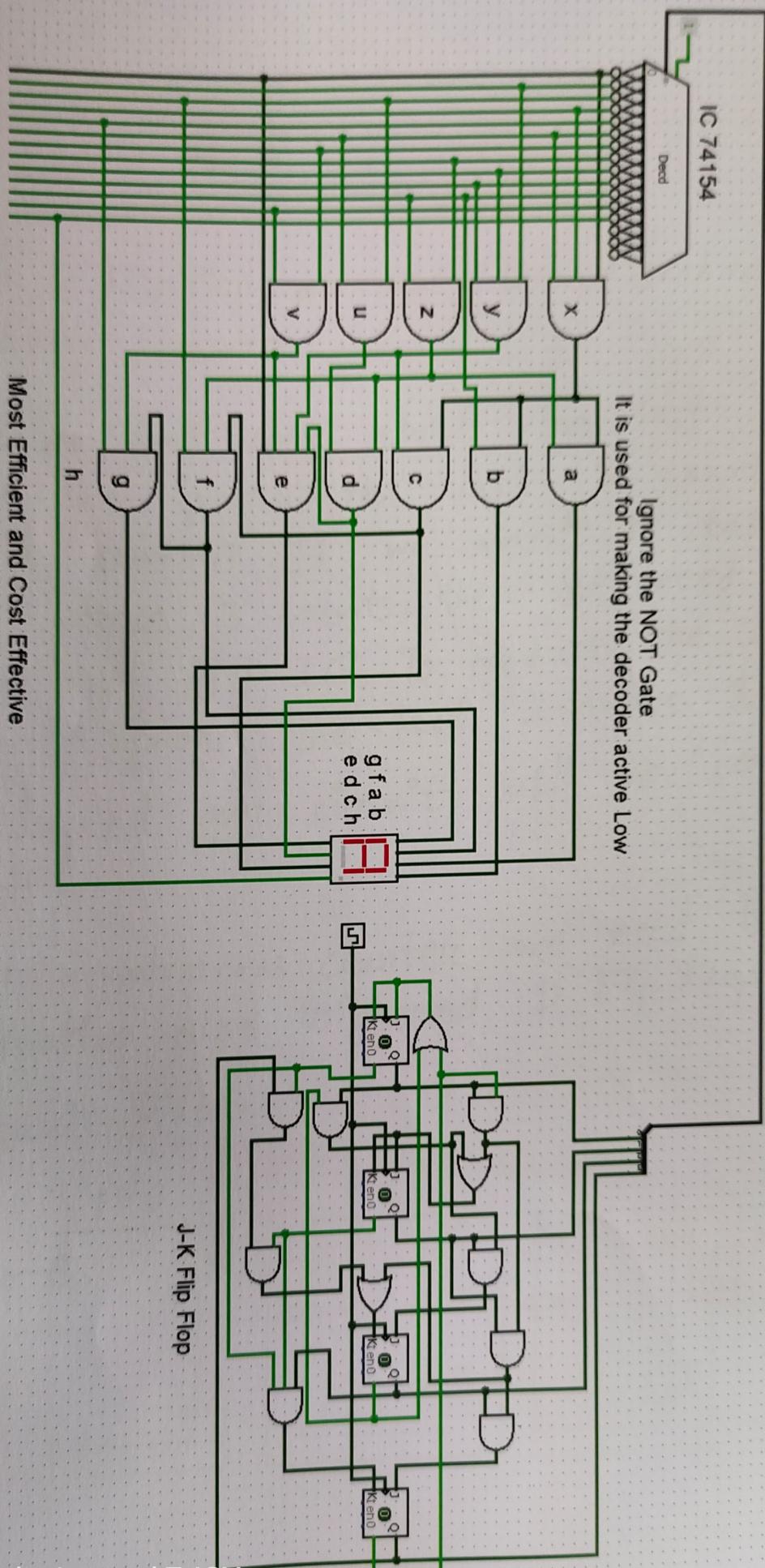
04. Then we draw the circuits diagram. We again we some branches for reducing the gate count.

05. After that, we started to construct the circuits according to the respective pin diagram.

06. Then we take the output from Q_3 , Q_2 , Q_1 , Q_0 and connect with our combinational circuit as respective A, B, C, D.

07. After giving every input perfectly, circuits were counting the sequence accurately.

08. It was a little bit complicated circuit but working well.



Most Efficient and Cost Effective
Text: Anta-BrEmmer.
Group: 05

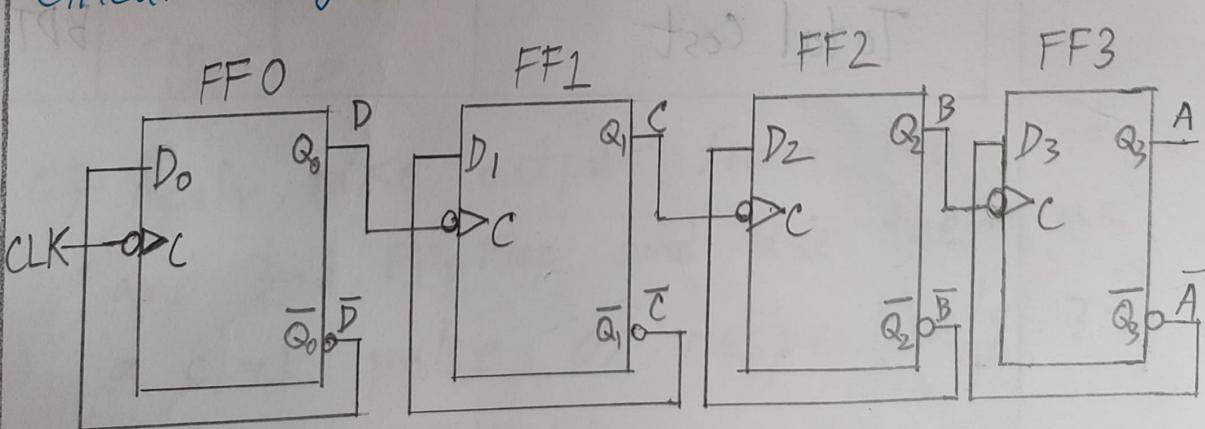
D Flip Flop

For D Flip Flop we use the asynchronous Binary Counter.

As we don't care about the last 3 counts, we can ignore the last 3 counts for this counter. If we want to take care of these 3 counts, then we need to add another AND IC. To reduce the IC, we just ignore the last 3 counts. In this case our circuit will be completely off.

For asynchronous counter we need to use negative edge triggered D Flip Flop.

Circuit Diagram:



Simulation: Attached.

Cost Analysis:

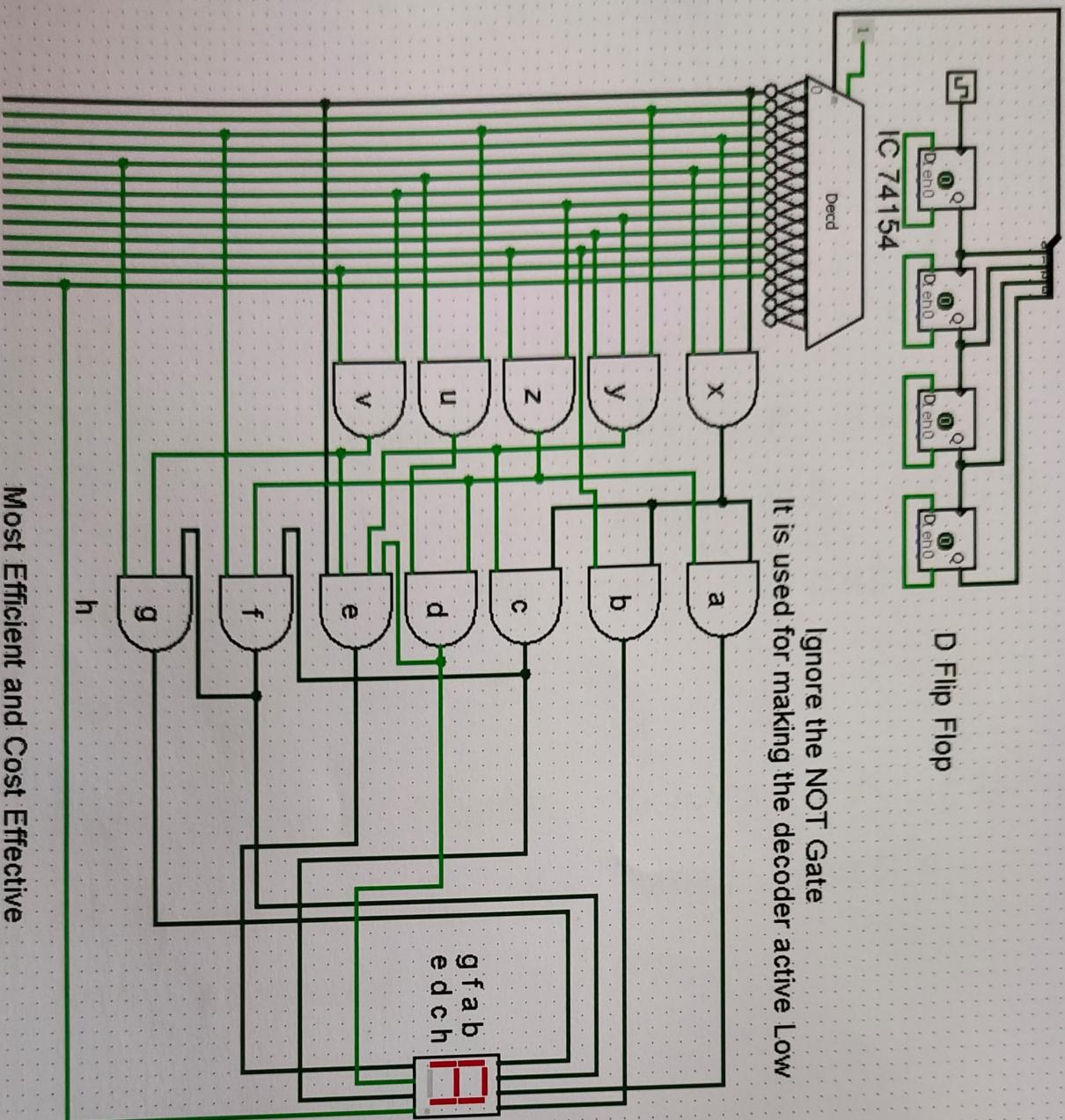
IC Name	Required Gates	Quantity	Price
IC 7474 Dual D FlipFlop	4	2	BDT 70.00
IC NE555 Timer IC	0	1	BDT 25.00
10K Ohm Resistor	0	2	BDT 5.00
470 Ohm Resistor	0	5	BDT 10.00
100 and 0.1 μ F capacitor		2	BDT 10.00
LED		5	BDT 10.00
Wires	0	25	BDT 62.50
Bread Board		1	BDT 150.00
Total Cost			BDT 342.50

Procedure:

01. For this asynchronous counter we just need 4 D Flip Flops.
02. First, we gave the connection to the V_{cc} and Ground.
03. Then, we gave the constant input of 1 to set and clear pin for inactive them.
04. After that, we connect every Q' to D.
05. Then, we gave the clock pulse to the 1st Flip Flop.
06. After that we take the output from the 1st Flip Flop and use it as a clock pulse for the 2nd Flip Flop.
07. Again, take output from the 2nd and 3rd Flip Flop and use them as a clock pulse of respectively 3rd and 4th Flip Flop.

08. Then we take the output from Q_3, Q_2, Q_1, Q_0 and connect with our combinational circuit as respective A, B, C, D.

09. It was working perfectly.



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Group: 05

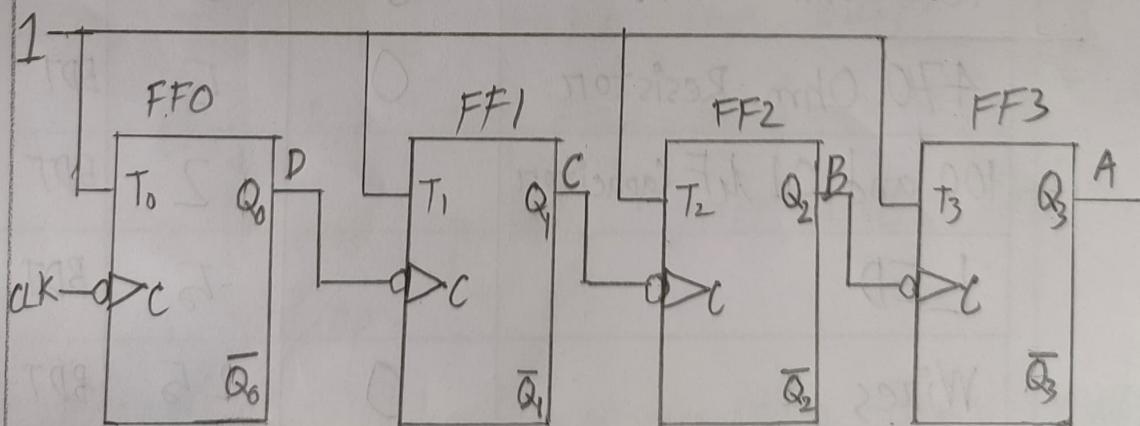
T(J-K) Flip Flop

When we give the same input in J and K, JK Flip Flop works like a T Flip-Flop. That is why we use JK Flip Flop to build this circuit. We just gave the same input in both J and K.

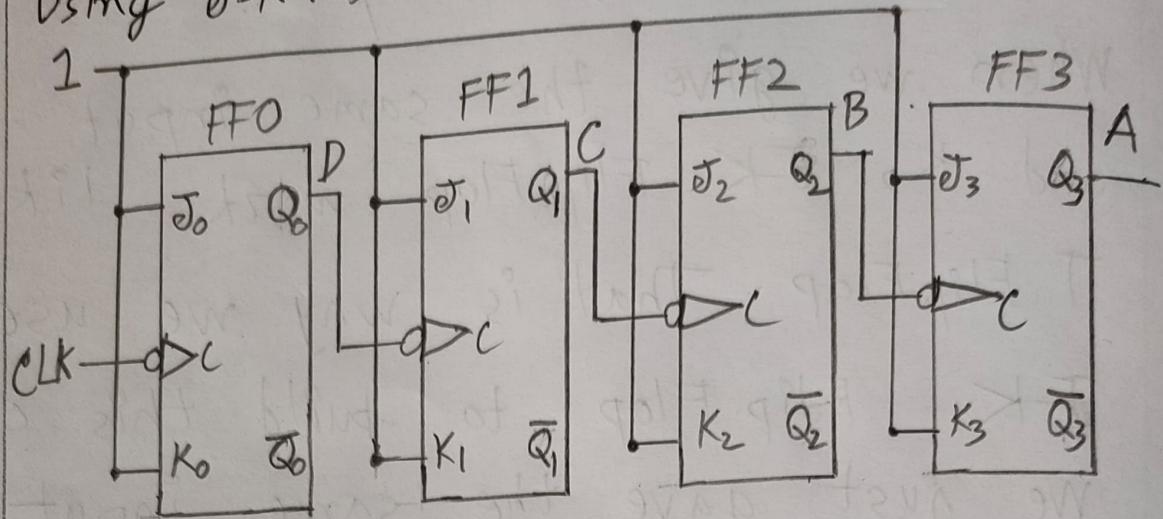
And we use Master-Salve JK Flip-Flop 7476, as it is the most stable and advanced Flip Flop.

Circuit Diagram:

Using T-Flip Flop:



Using J-K instead of T:



Simulation: Attached

Cost Analysis:

IC Name	Required Quantities	Quantity	Price
IC 7476 Dual JK Flip Flop	4	2	BDT 100.00
IC NE555 Timer IC	0	1	BDT 25.00
10K Ohm Resistor	0	2	BDT 5.00
470 Ohm Resistor	0	5	BDT 10.00
100 and 0.1 uF Capacitor		2	BDT 10.00
LED		5	BDT 10.00
Wires	0	25	BDT 62.50
Bread Board		1	BDT 150.00
Total Cost			BDT 372.50

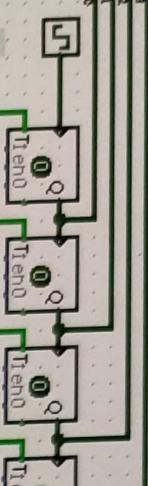
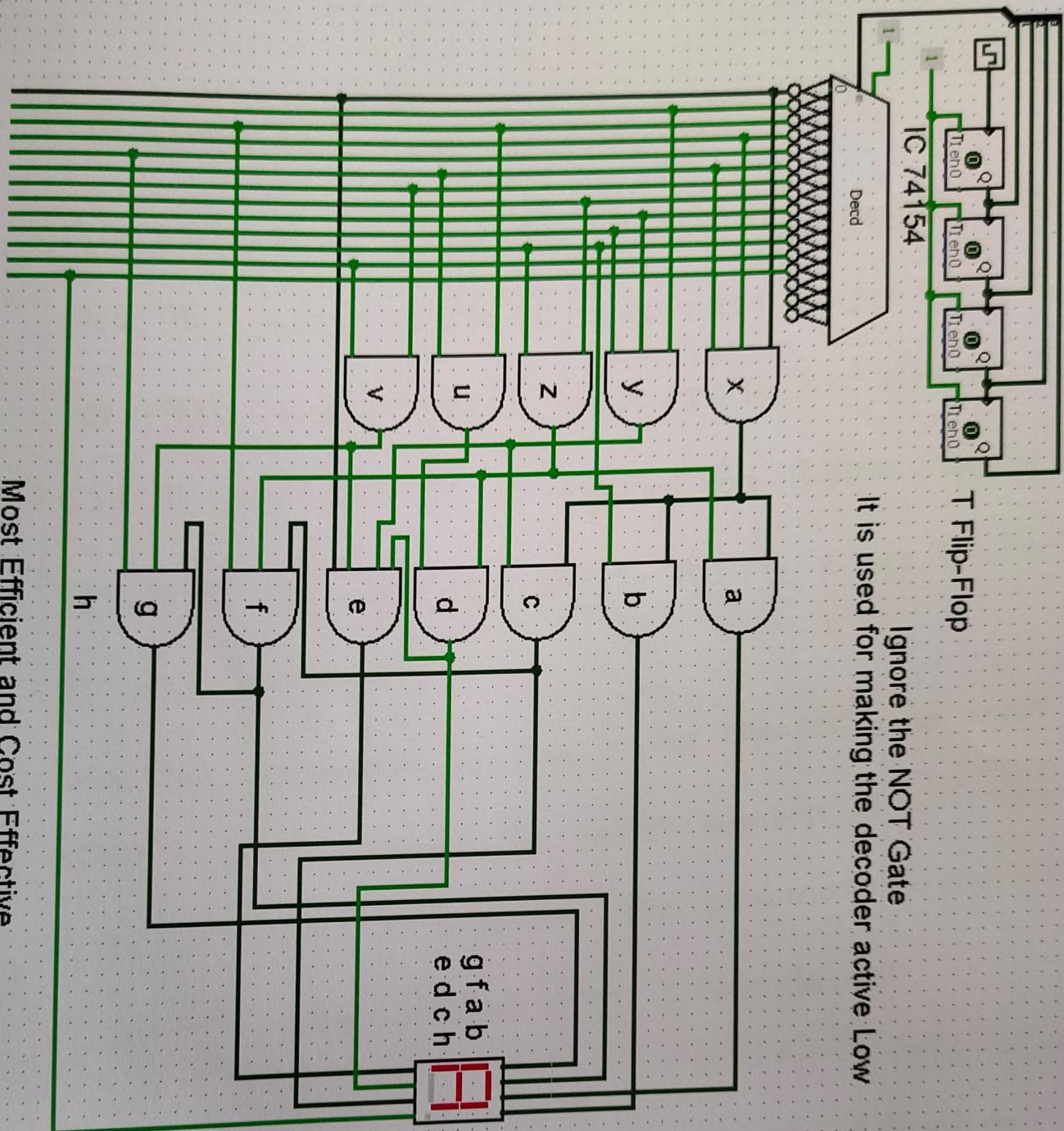
Procedure:

01. For asynchronous MOD 16 counter using T Flip Flop, first, we insert the J-K Flip Flop and gave the connection to the Vcc and Ground.
02. Then, we gave a constant input of 1 in every preset and reset pin for disabling them.
03. Then, we gave a constant input of 1 in every J and K. Now it will work like a T Flip Flop.
04. After that, we gave the clock pulse the 1st Flip Flop.
05. Then we take the output from the 1st Flip Flop and use it as a clock pulse for the 2nd Flip Flop.
06. After that we again take output from 2nd and 3rd Flip Flop and use

it as a clock pulse for the 3rd and 4th Flip Flop.

07. Then we take the output from Q_3, Q_2, Q_1, Q_0 and connect with our combinational circuit as respectively A, B, C, D.

08. It is costly little bit than D Flip Flop, but it was working perfectly and giving a very stable sequence.



Ignore the NOT Gate
It is used for making the decoder active Low

Most Efficient and Cost Effective

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Group: 05

Result Analysis:

Our cost analysis found that Boolean Algebra costs about 962 Tk, NAND 1,276 Tk, NOR 1,381 Tk, SOP 1,308 Tk, POS 1,356, K-Map 893 Tk, MUX 988 Tk, and Decoder 637 Tk only. And IC is required for Boolean Algebra 10x, NAND 13x, NOR 15x, SOP 13x, POS 14x, K-Map 8x, MUX 8x, and Decoder 5x.

From this information, Decoder is the cheapest and most efficient as it requires the lowest number of IC. For that, we decided to implement the combinational part of 7-segment display function using 16-line decoders.

In the sequential part, it was a little bit difficult to decide what should we use or not. In the cost analysis, we found that using J-K flip flop it was around 447 Tk and IC required 5x. In the D Flip Flop, cost was around 343 Tk and IC needs 2x only. In the T Flip Flop using J-K cost 372 Tk and IC needs 2x.

So, we can see that D flip flop and T flip flop IC count is the same. And cost difference is 30 Tk only. D flip flop sometime giving us glitch output, but T flip flop was working perfectly without any glitch. Between D and J-K Flip Flop, J-K Flip Flop is most stable than D. That's why we decided to implement the asynchronous MOD 16 counter using T Flip Flop.

Discussion:

From this project, we gained a lot of experience about combinational and sequential circuits. We can now build a synchronous and asynchronous counter. And using these counters, we can now build a combinational circuit that can show letters on a 7 segment display. We can construct a circuit that

minimize a circuit and choose an optimized one.

In this project, we face some problems regarding the LED and a branch of a function. First, we connected the LED without a resistor, and our LED was damaged for that. Then we used a resistor of 470 ohm, and that time LED was fine.

In the sequential part we experienced something like a horror incident. While we were trying to build the circuit using D flip flop, we used asynchronous clock pulse; in our circuit 1st flip flop giving constant output either 1 or 0. We used this output as a clock pulse for the 2nd flip flop, as 1st flip flop giving constant output, according to theory 2nd flip flop should not work, it should also give constant output. But the 2nd, 3rd, 4th flip flop was working perfectly in their position. Then we realize that it's a glitch. After

running in long term sometime its working perfectly sometimes not. Then we decided to implement using advanced J-K flip flop as it is the most stable flip flop. And finally, we successfully completed the project. It costs around 1010 Tk only, and it needs Rx with 100 wires.

Pricing Source:

- roboticsbd.com
- robodocbd.com

Contribution:

1. Joy Kumar Ghosh (2211412464):

- Hardware - Combinational (70%) and sequential (10%), timing circuit (100%).
- In Logisim - SOP, POS, MUX, Decoder, K-Map, J-K, D, T
- Report Full Draft in MsWord and concept and writing (5%)
- Solved POS, SOP, Decoders, J-K, T, D

02. Sazid Hasan (2211513642) :

- Hardware - Combinational (10%) & Sequential (90%) and Bug finder.
- Circuit Diagram drawing.
- Logisim - Boolean Algebra, NAND, NOR
- Report Writing (25%), Assist on Draft
- Solved Boolean Algebra, ~~NAND~~, NOR
- Understanding about whole project theory.

03. Syed Tarshriful Alom (2212623042) :

- Hardware - Observation.
- Report Writing (30%), Assist on Draft.
- Solved K-Map
- Understanding about whole project theory

04. Md. Rafawat Islam (2122343642) :

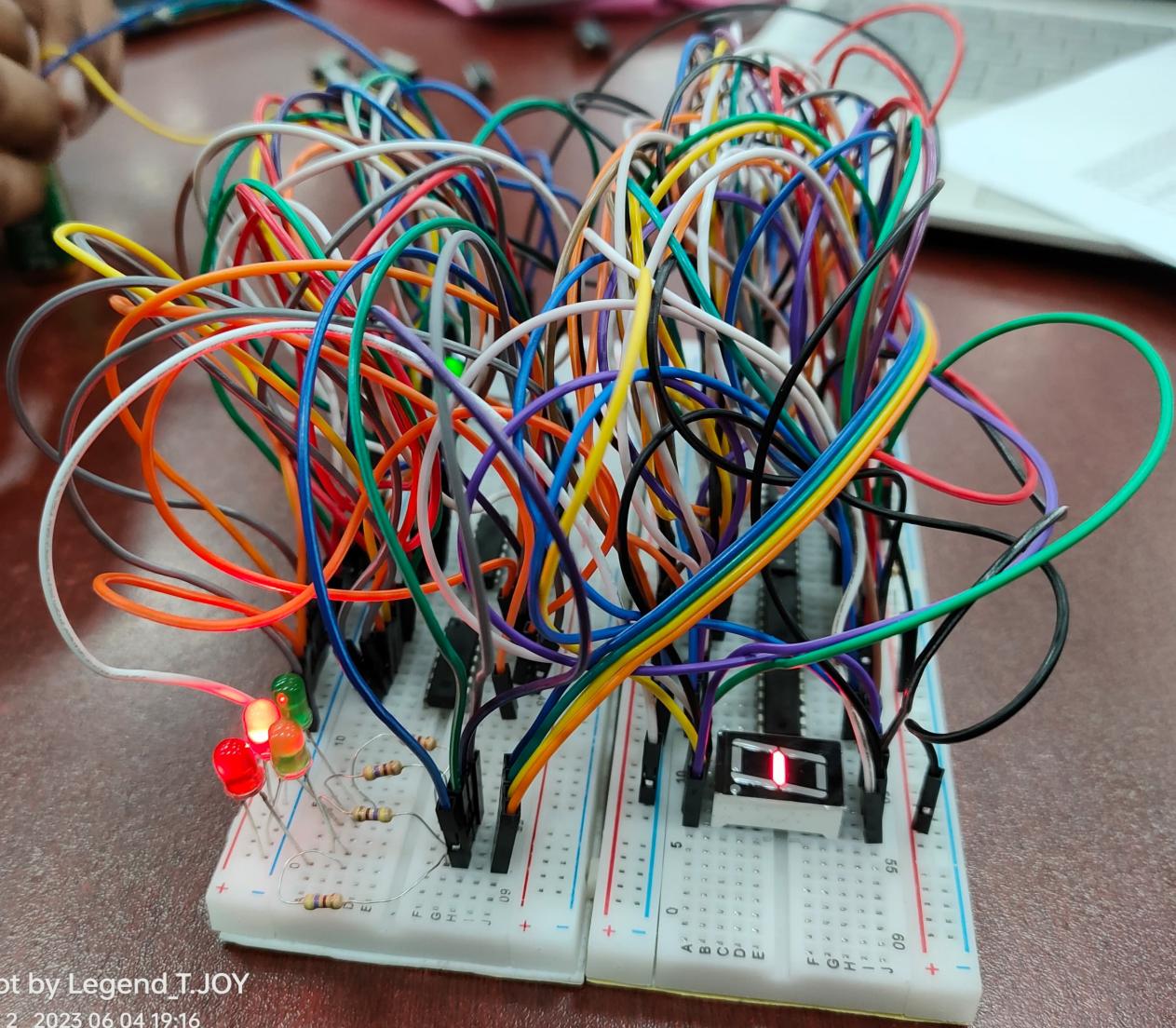
- Hardware - combinational (20%), Source converter (100%)
- Report Writing (20%)
- Solved MUX
- Understanding about whole project theory.

05. Md. Nifat Hossain (2212923042) :

- Hardware - Observation.
- Report Writing (20%), Assist on Draft.
- Solved J-K

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Understanding about whole project theory.

THANK YOU. ❤



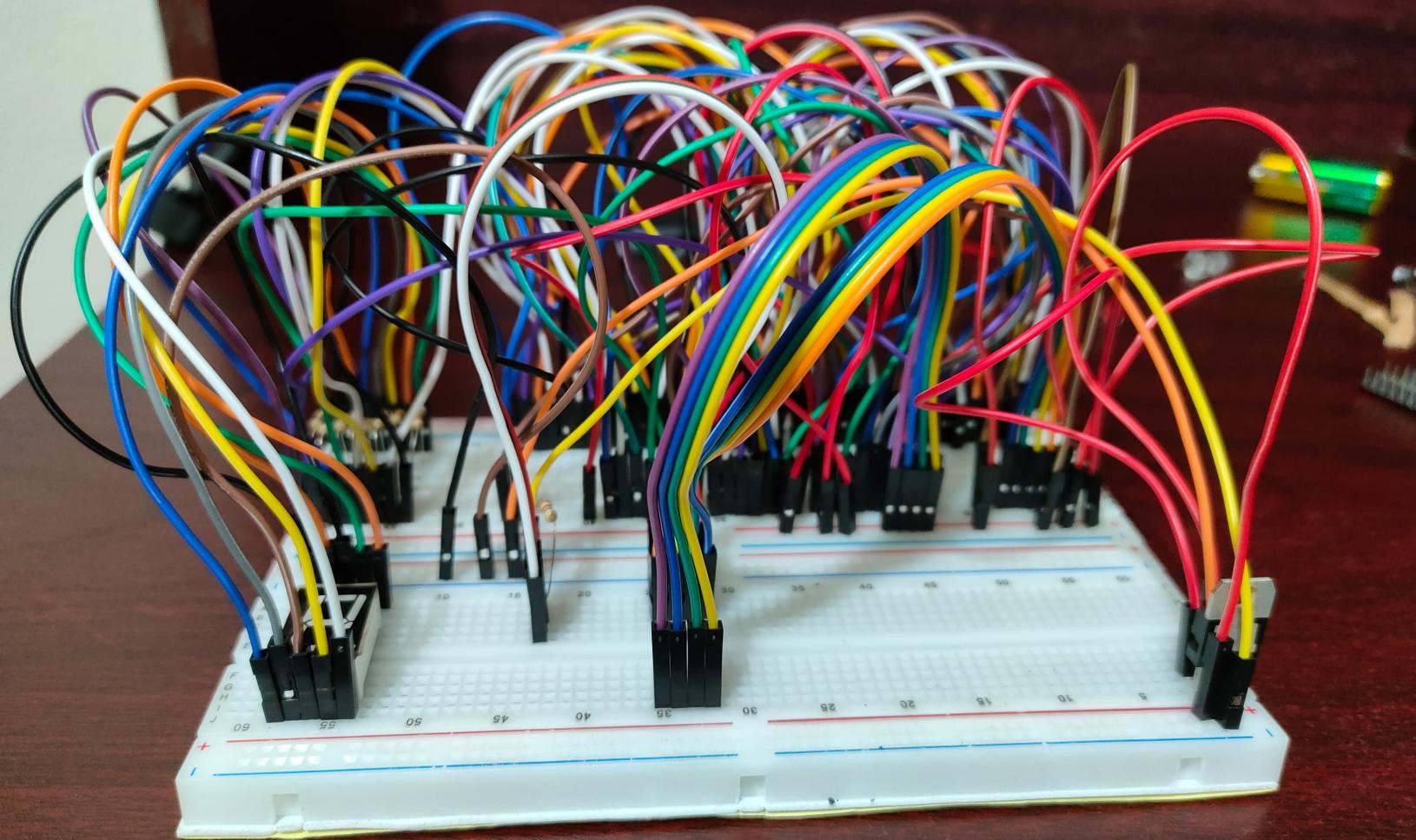
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