

**North South University**  
Department of Electrical & Computer Engineering  
**PROJECT REPORT**

Course Code: CSE 231L

Course Title: Digital Logic Lab

Section: 08

Project Part: Combinational & Sequential

Project Name: 7 Segment Display.

**Text: Anta-BrEnner.**

Date of Submission: 22 May 2023

Submitted by Group Number: 05

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Submitted To: Pritthika Dhar

Project Title: 7 segment Display.

Text: Anta-BrEnner.

### Objective:

- Gaining a practical understanding of combinational and sequential circuits.
- Design a synchronous and asynchronous counter circuits.
- Learn to display Letter on a 7 segment display with sequence.

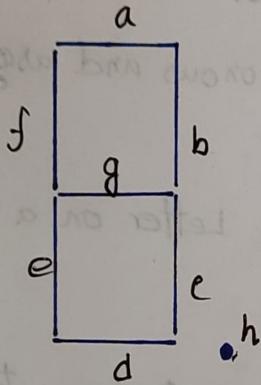
### Apperatus of Hardware Implementation :

- 1 x IC 74154 4:16 Line Decoder.
- 2 x IC 7408 Quadruple 2 input And gate.
- 2 x IC 4073 Triple 3-input And gate
- 2 x IC 7476 Master slave Dual JK FlipFlop.
- 1 x LM7805 5v Voltage regulator.
- 1 x Timer IC 555
- 1 x 7(seven) segment Display common node.
- 2 x 10K ohm resistor.
- 6 x 470 ohm resistor. (2V or 0V)
- 5 x LED
- 1 x 100  $\mu$ F capacitor.
- 1 x 0.1  $\mu$ F capacitor
- 1 x 9v Battery

- 100x Jumper Wires male to male
- 2 x 830 Pin Breadboard.

Theory:

7 segment Display:



Combinational Part:

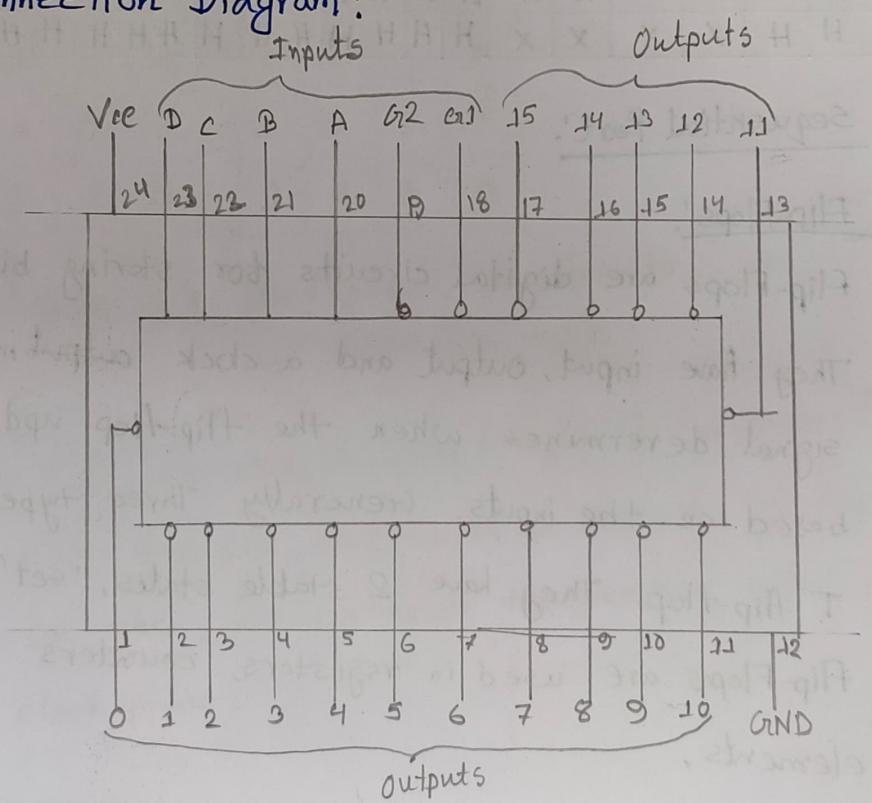
A decoder is a combinational circuit that converts binary information from  $n$ -input lines to a maximum of  $2^n$  output lines.

The 74154 is a 4:16 line decoder integrated circuit (IC) that is commonly used in digital circuits. It has 4 input lines (A, B, C, D) and 16 output lines (Y0 to Y15).

Each of this 4 line to 16-line decoders utilizes TTL circuitry to decode four binary coded inputs into one of sixteen manually exclusive outputs.

both the strobe inputs  $G_1$  and  $G_2$  are low. The demultiplexing function is performed by using the four input lines to address the output line, passing from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. These multiplexers are ideally suited for implementing high performance memory decoders. All inputs are buffered, and input clamping diodes are provided to minimize transmission line effects and simplify system design.

## Connection Diagram:



Function Table :

		Inputs				Outputs															
G1	G2	A	B	C	D	O	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	
L	L	L	H	L	L	H	A	H	H	L	H	H	H	H	H	H	H	A	H	H	
L	L	L	H	L	H	H	A	H	H	H	L	H	H	H	H	H	H	H	H	H	
L	L	L	H	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	
L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	
L	L	H	L	L	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	

### Sequential Part:

#### Flip-Flops:

flip-Flops are digital circuits for storing binary data.

They have input, output and a clock input. Clock signal determines when the flip-flop updates its state based on the inputs. Generally three types D, J-K or T flip-flop. They have 2 stable states, "set", "reset".

flip-Flops are used in registers, counters and memory elements.

$JK$ ,  $D$  ("Data" or "Delay") and  $T$  (toggle) are commonly used flip-flops in digital logic circuits.

In case of  $JK$  flip-flop ( $J=Set$ ,  $K=Reset$ ) the combination  $J=1, K=1$  is a command to toggle the flip-flop, the combination  $J=0, K=1$  is a command to reset the flip-flop, and the combination  $J=1, K=0$  is a command to set the flip-flop. Setting  $J=K=0$  maintains the current state.

Characteristic Table			Excitation Table			
$J$	$K$	$Q_n$	$Q$	$Q_n$	$J$	$K$
0	0	Q	0	0	0	X
0	1	0	0	1	1	X
1	0	1	1	0	X	1
1	1	$\bar{Q}$	1	1	X	0

Table B.1:  $JK$  flipflop : characteristic and Excitation table.

The  $T$  flipflop changes state ("toggles") whenever the input  $T$  is high and the clock input is stored. If the  $T$  input is low the flipflop holds the previous value when given a clock pulse.

Characteristic Table		Excitation Table		
T	$Q_{next}$	Q	$Q_n$	T
0	Q	0	0	0
1	$\bar{Q}$	0	1	1
		1	0	1
		1	1	0

Table B.2 : T-Flip-Flop characteristic and excitation table.

The D-FlipFlop captures the value of the D-input at a definite portion of the clock cycle (such as the rising edge of the clock). That captured value becomes the Q output. At other times, the output Q does not change.

Characteristic Table		Excitation Table		
D	$Q_{next}$	Q	$Q_n$	D
0	0	0	0	0
1	1	0	1	1

Table B.3 : D flipflop : characteristic and excitation table.

## Synchronous Counter:

It is a digital circuit composed of flip-flops and combinational logic, where the outputs depend not only on present inputs but also on the circuit's state. The flip flop serves as memory elements to store information.

In a synchronous sequential circuit a clock signal synchronizes the operations. On each clock edge, the inputs are sampled, and the outputs are updated based on a current state and the combinational logic. The state transition is governed by a set of logical equations that define the next state in terms of current state and inputs.

The circuit's behaviour can be described using a state diagram, which illustrates the various states and the transitions between them. The design process involves determining the required states, defining the state transition table, and deriving the logic equations for each flip-flop and output.

Synchronous sequential circuits are widely used in digital systems, such as microprocessor, memory units and communication protocols. They offer predictable

and reliable operation, allowing for precise control and synchronization in complex digital systems.

To analyze and design synchronous sequential circuits, we need to use state table and state diagrams. The state table shows how the state and output of sequential circuit changes with respect to the current state and input. State diagrams are simply graphical forms of state table. In this type of diagram a state is represented by a circle and the (clk-triggered) transitions between states are indicated by directed lines connecting the circles. The binary number inside each circle identifies the state of the flip-flop. The directed lines are labeled with two binary numbers separated by a slash. The first one is present state and second part is the output state.

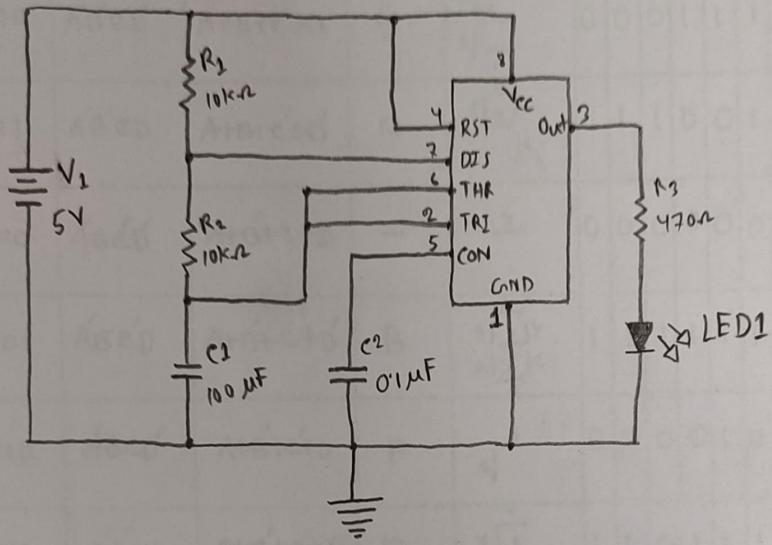
### Timer IC:

IC 555 also known as NE555 is a popular circuit used in wide range of operations. It operates as a versatile timer, providing precise timing function. The IC consists of comparators, flip-flops and a voltage

divider network. It can be configured in various modes, such as a stable, monostable, and bistable, depending on the external components connected to it.

In stable mode, it produces a single pulse of adjustable duration. With its simplicity, reliability and low cost, the 555 timer IC has become a fundamental component in many electric circuits, including timers, oscillators, pulse generators and LED flashers.

We use this IC as our clock pulse.



Circuit Diagram of NE555 IC

Time Calculation:

$$\text{High Time} = 0.693 (R_1 + R_2) * C$$

$$= 0.693 (10 * 10^3 + 10 * 10^3) * 100 * 10^{-6}$$

$$\approx 1.389 \text{ sec}$$

$$\text{Low Time} = 0.693 * R_2 * C$$

$$= 0.693 * 10 * 10^3 * 100 * 10^{-6}$$

$$= 0.693 \text{ sec}$$

$$\text{Total Time} = \text{High Time} + \text{Low Time} = 1.389 + 0.693 = 2.082 \text{ sec}$$

$$\text{Frequency} = \frac{1}{T} = \frac{1}{2.082} = 0.48 \text{ Hz}$$

## Truth Table of Combinational Part:

Truth Table for Sequential part:

Present State	Next state	$J_0$	$K_0$	$J_1$	$K_1$	$J_2$	$K_2$	$J_3$	$K_3$
0000	0001	1	X	0	X	0	X	0	X
0001	0010	X	1	1	X	0	X	0	X
0010	0011	1	X	X	0	0	X	0	X
0011	0100	X	1	X	1	1	X	0	X
0100	0101	1	X	0	X	X	0	0	X
0101	0110	X	1	1	X	X	0	0	X
0110	0111	1	X	X	0	X	0	0	X
0111	1000	X	1	X	1	X	1	1	X
1000	1001	1	X	0	X	0	X	X	0
1001	1010	X	1	1	X	0	X	X	0
1010	1011	1	X	X	0	0	X	X	0
1011	1100	X	1	X	1	1	X	X	0
1100	0000	0	X	0	X	X	1	X	1

Procedure:

Combinational Part:

01. First, we construct the truth table for our given text. There are 13 letters in our given text. That's why we take 4 inputs for ABCD for our truth table and the sequence 13, 14, 15 will be don't care.
02. In our Truth Table when input is 0000, letter A will display for that segment a, b, c, e, f, g will be 1 and others will be 0. We do it if ~~for~~ from sequence 0-12 and 13-15 are don't care.
03. Then we form the Boolean Equation for every segment using the principle of 1<sup>st</sup> Canonical form.
04. For Hardware implementation first we install the LM7805 5V Regulator on the breadboard. We connect the 9V Positive probe from the battery to the regulator pin 1 and ground to pin 2. & then take the 5V output from pin 3 and connect to breadboard positive line. Now it's ready for connecting IC.
05. Then we install the IC 74154 Decoder and give the GND connection on PIN 12 & the Vcc to pin ~~13~~ 24. For working as decoder, we give ground connection to pin 18 & 19. Then we connect our 4 inputs to pin 20, 21, 22, 23 as A, B, C, D. We use 470 Ohm resistor for giving the ground connection as input.
06. Then we take the output from pin 1-17 (except 12) and connect with 7408 and 4073 IC as the pin diagram given in attached simulation.
07. After that we install the 7-segments display common anode on the breadboard and give the positive connection through

a 470 Ohm resistor to the middle pin both side of the display. Then we connect the output for every segment to the corresponding pin as shown in the attached simulation & then we tested our full circuit and output was matched with our constructed truth table.

### Sequential Part:

01. For sequential part, first we construct the state table using J-K flip flop.  
Complete details given on the respective section of J-K Flip Flop.
02. After simulate, we find that it takes extra AND, and ORL.  
So we decided to use a asynchronous counter.
03. Then, we construct an asynchronous MOD 16 Counter using T(J-K) flip-flop.
04. First, we gave constant connection of 1 to each J & K also in the Reset & Preset Pin for deactivation.
05. Then we gave the Vcc and Ground connection to the respective pin.
06. After that, we connect the clock pulse to the J-K Flip-Flop.  
Then we take output from the  $Q_0$  and use it as a clock pulse for the 2<sup>nd</sup> flip-flop. As well as we take another output from  $Q_1$  &  $Q_2$  and use as clock pulse for the 3<sup>rd</sup> & 4<sup>th</sup> flip-flop.
07. Then we take output from  $Q_3, Q_2, Q_1, Q_0$  and connect with the decoder.
08. Then we run the circuit and test with respect to the truth table.

## Boolean Algebra

Using the 1st canonical form, we get,

$$\begin{aligned}a &= A'B'C'D' + A'B'CD + A'BC'D + A'BCD + AB'CD' \\&= A'B'CD + A'BCD + A'B'C'D' + A'B'C'D + A'B'C'D' + AB'CD' \\&= A'CD(B' + B) + A'C'(B'D' + BD) + B'D'(A'C' + AC) \\&= A'CD \cdot 1 + A'C'(B \odot D) + B'D'(A \odot C) \\&= A'CD + A'C'(B \odot D) + B'D'(A \odot C)\end{aligned}$$

$$\begin{aligned}b &= A'B'C'D' + A'B'CD + A'BC'D + AB'CD' \\&= A'B'C'D' + A'B'CD + A'B'C'D' + A'BC'D + A'B'C'D + AB'CD' \\&= A'B(C'D' + CD) + A'C'(BD' + BD) + B'D'(A'C' + AC) \\&= A'B'(C \odot D) + A'C'(B \odot D) + B'D'(A \odot C)\end{aligned}$$

$$\begin{aligned}c &= A'B'C'D' + A'B'C'D + A'B'CD + A'BC'D + AB'C'D + AB'C'D' \\&= A'B'C'(B'D' + D) + A'D(B'C + BC') + AB'C'(D' + D) \\&= A'B'C' \cdot 1 + A'B'C' \cdot 1 + A'D(B' \odot C) \\&= A'B'C' + AB'C' + A'D(B' \odot C) \\&= BC'(A' + A) + A'D(B' \odot C) \\&= BC' \cdot 1 + A'D(B' \odot C) \\&= BC' + A'D(B' \odot C)\end{aligned}$$

$$\begin{aligned}
 d &= A'B'CD' + A'BC'D + A'BCD + AB'C'D' \\
 &= A'B'C'D' + AB'C'D + A'BC'D + A'BCD \\
 &= B'C'D'(A'+A) + A'BD(C'+C) \\
 &= B'C'D \cdot 1 + A'BD \cdot 1 \\
 &= B'C'D + A'BD
 \end{aligned}$$

$$\begin{aligned}
 e &= (A+B+C'+D') (A+B'+C+D) (A'+B'+C+D) \\
 &= \overline{(A+B+C'+D')} \overline{(A+B'+C+D)} \overline{(A'+B'+C+D)} \\
 &= \overline{A'B'CD} + \overline{A'BC'D'} + \overline{ABC'D} \\
 &= \overline{A'B'CD} + \overline{BC'D'}(A+A) \\
 &= \overline{A'B'CD} + \overline{BC'D'}
 \end{aligned}$$

$$\begin{aligned}
 f &= (A+B'+C+D) (A+B'+C'+D) (A'+B+C'+D') (A'+B'+C+D) \\
 &= \overline{(A+B'+C+D)} \overline{(A+B'+C'+D)} \overline{(A'+B+C'+D')} \overline{(A'+B'+C+D)} \\
 &= \overline{A'BC'D'} + \overline{A'BCD'} + \overline{AB'CD} + \overline{ABC'D'} \\
 &= \overline{BC'D'}(A'+A) + \overline{A'BCD'} + \overline{ABC'D} \\
 &= \overline{BC'D'} + \overline{A'BCD} + \overline{ABC'D} \\
 &= \overline{BD'}(C'+A'C) + \overline{AB'CD} \\
 &= \overline{BD'}(A'+C') + \overline{ABC'D} \\
 &= \overline{BD'}(AC)' \cdot (A'+B+C'+D')
 \end{aligned}$$

$$g = A' + B' + C + D$$

$$= \overline{A' + B' + C + D}$$

$$= \overline{ABC'D'}$$

$$h = ABC'D'$$

Therefore,

$$a = A'CD + A'C'(B \odot D) + B'D'(A \odot C)$$

$$b = A'B'(C \odot D) + A'C'(B \odot D) + B'D'(A \odot C)$$

$$c = B'C + A'D (B' \odot C)$$

$$d = B'CD' + A'BD$$

$$e = \overline{A'B'CD + BC'D'}$$

$$f = BD \cdot (AC)' \cdot (A' + B + C' + D')$$

$$g = \overline{ABC'D'}$$

$$h = ABC'D'$$

Circuit Diagram: Attached.

Simulation: Attached.

## Cost Analysis

IC Name	Required Gates	Quantity	Price
IC 7404 Hex Inverters (NOT gates)	8	12	250 BDT
IC 7432 Quadruple 2-Input OR gates	4	1	25 BDT
IC 7408 Quadruple 2-Input AND gates	7	2	50 BDT
IC 4075 Triple 3-Input OR gates	3	1	30 BDT
IC 4073 Triple 3-Input AND gates	9	3	90 BDT
IC XXXX Quadruple 2-Input XNOR gates	4	1	25 BDT
7 Segment Display	10	1	15 BDT
470 Ohm Resistor	10	5	5 BDT
Wires	105	105	262 BDT
Battery + Connector + Regulator			109 BDT
Bread Board		2	300 BDT
Total Cost			961 BDT

(1)

## procedure :

01. First, we form the Boolean Equation by using the 1st Canonical form from the truth table.
02. Then, we apply various Boolean algorithms to reduce the gate requirements.
03. While we build the circuit diagram, we focus on the gate that can be reused by other equations. We build lots of branches first then use them multiple times. And we reduce to the minimum level.
04. According to the pin diagram of the respective IC we connect all the wires and build the circuit for our combinational part.
05. Then, we connect the LED using a 970 ohm resistor.
06. It requires lots of IC, but it works according our truth table.

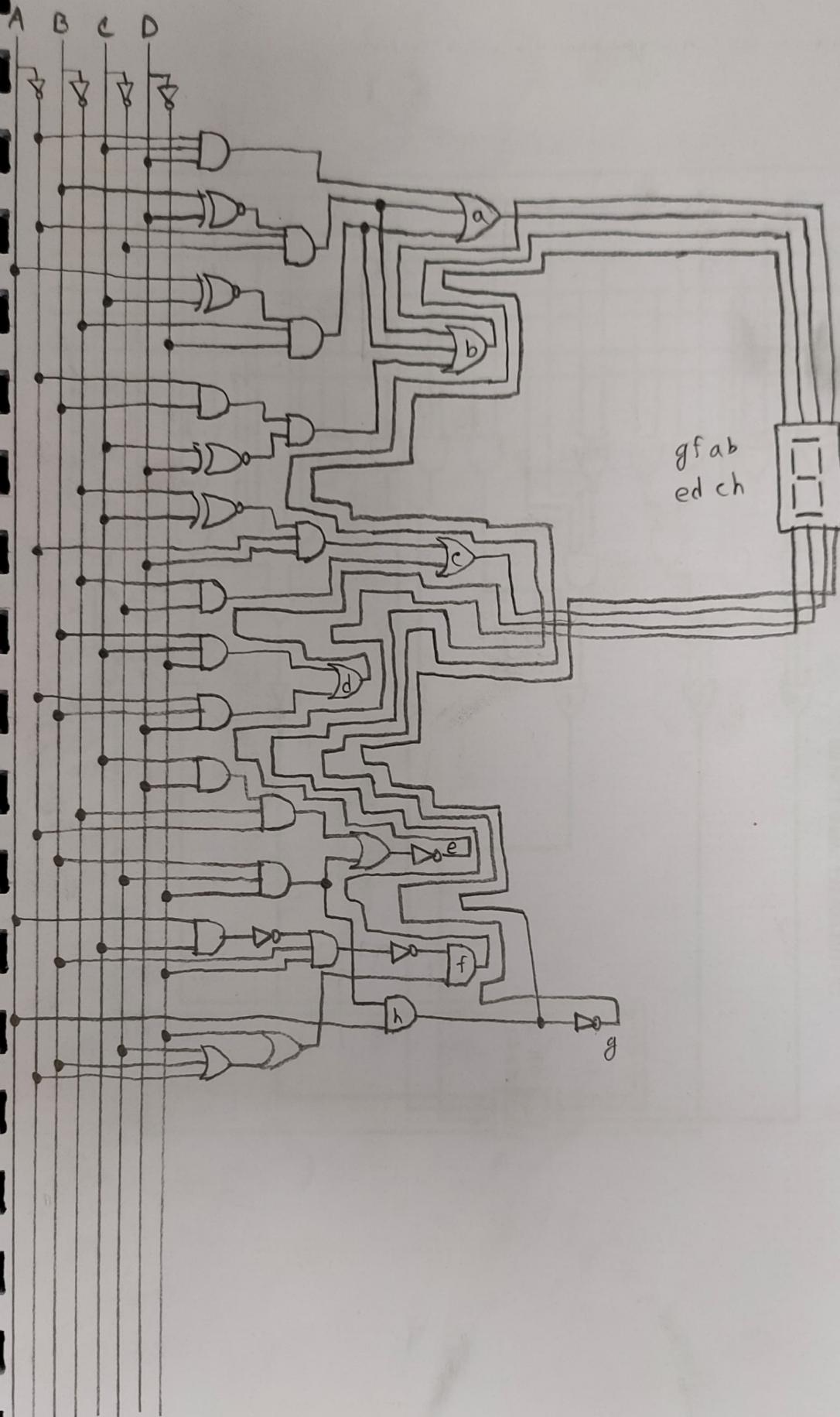
Circuit Diagram : Attached.

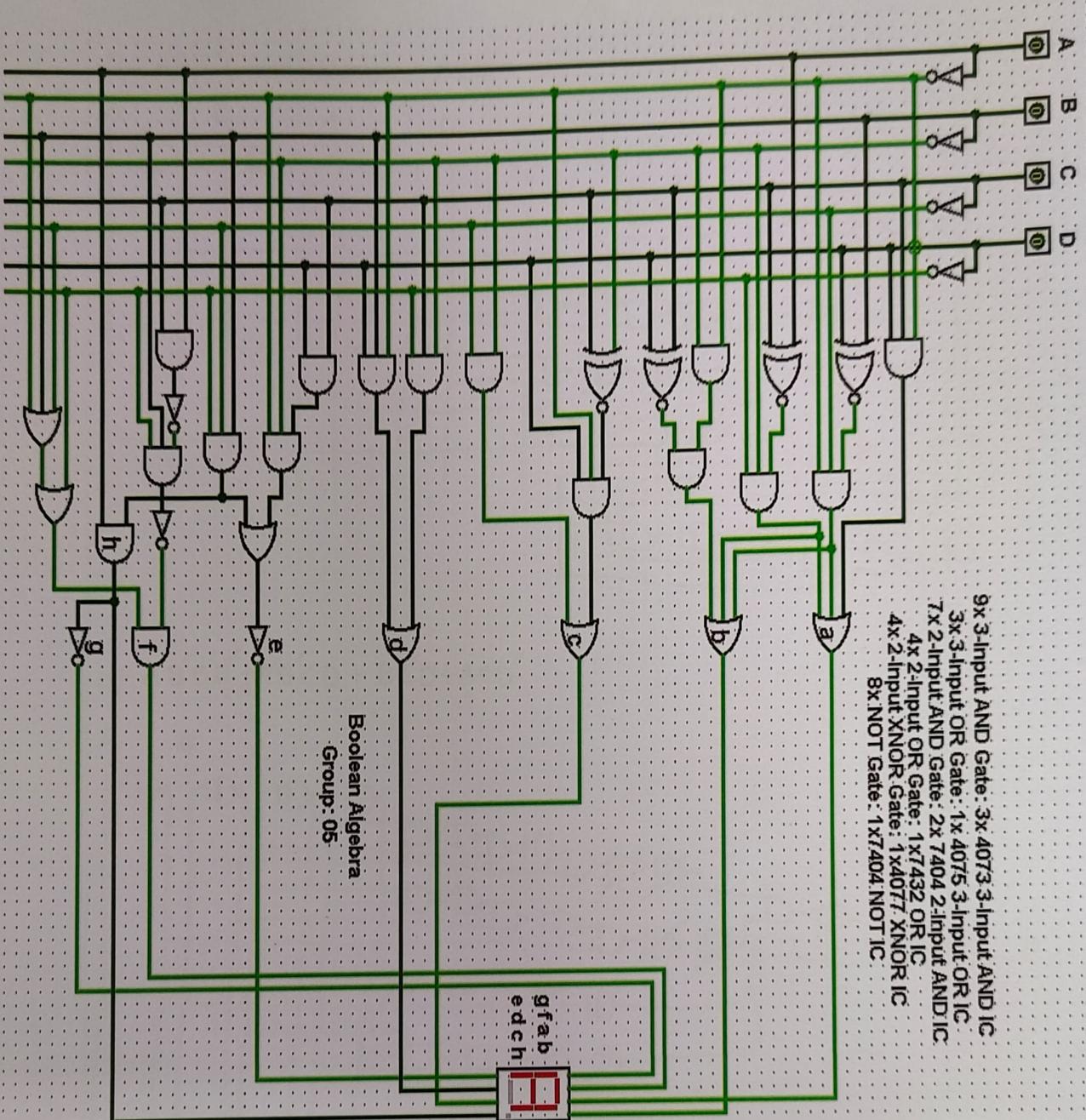
Simulation : Attached.

Cost Analysis :

IC Name	Required Gates	Quantity	price (BDT)
IC 7400 Quadruple 2-input NAND gates	51	13	325.00
7 Segment Display	10	1	35.00
970 ohm Resistor	1	12	12.00
Wires	146	146	365.00
Battery + Connector + Regulator			109.00
Bread Board		3	450.00
Total cost			1276.00

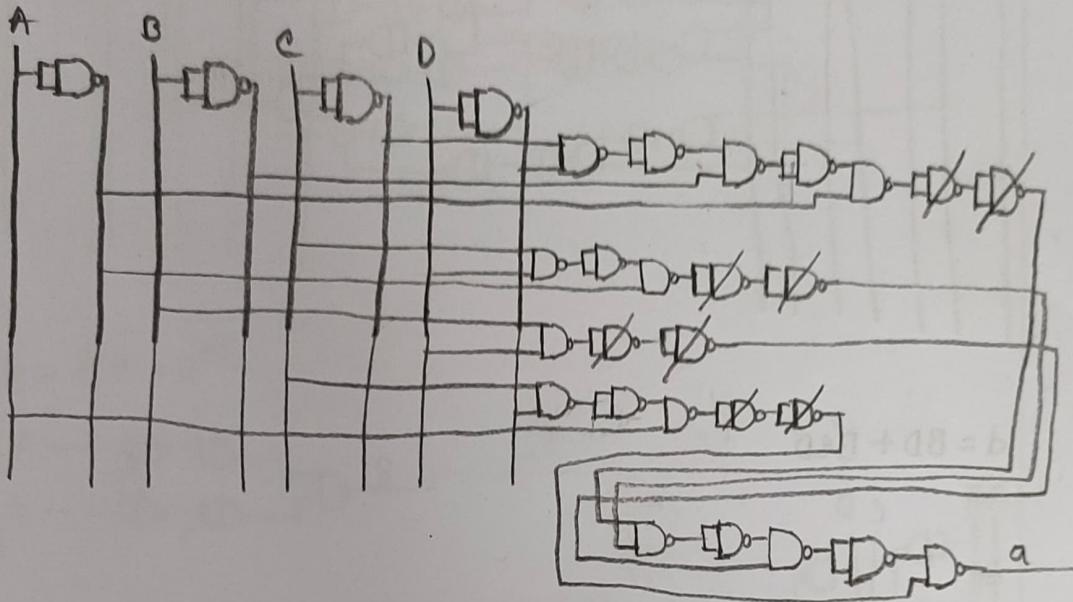
# Boolean Algebra



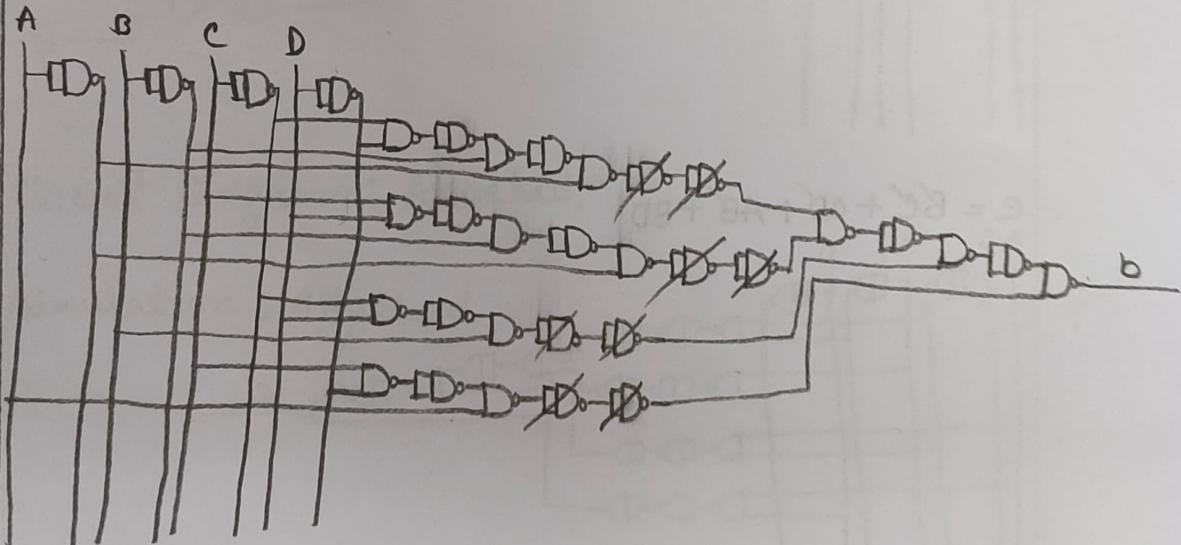


NAND

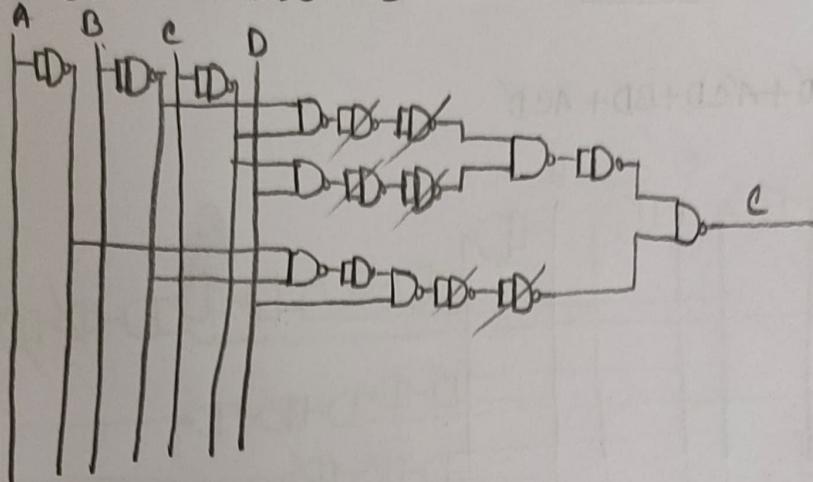
$$a = A'B'C'D' + A'CD + BD + ACD'$$



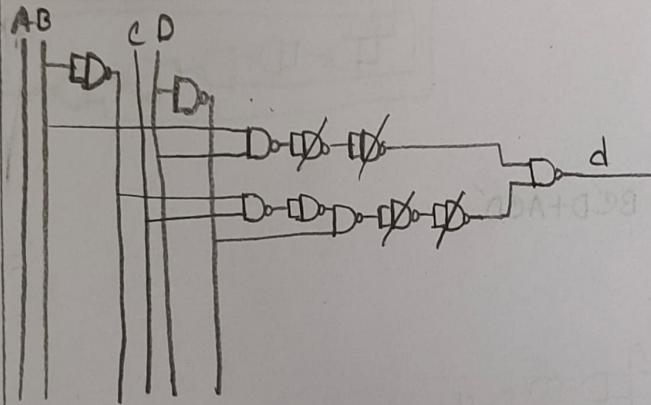
$$b = A'B'C'D' + A'B'CD + BC'D + ACD'$$



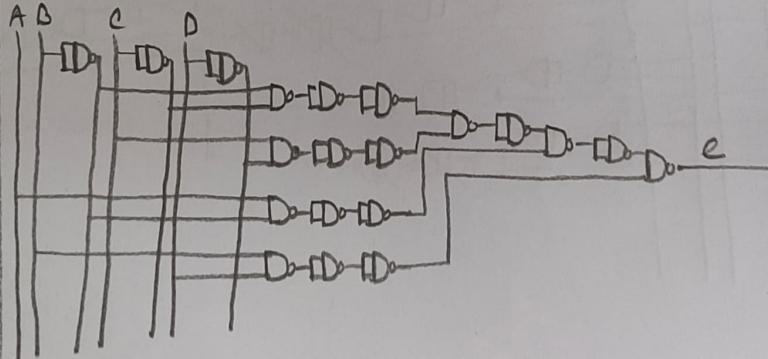
$$C = B'C' + C'D + A'B'D$$



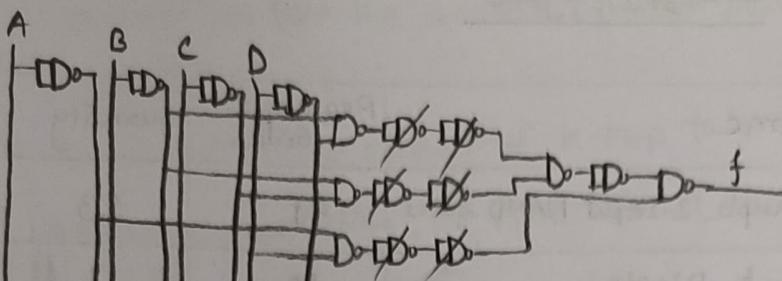
$$d = BD + BC'D'$$



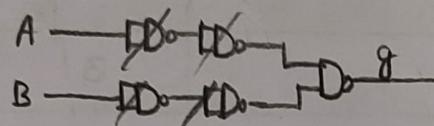
$$e = B'C' + CD' + AB' + BD$$



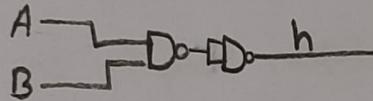
$$f = B'D' + B'C' + A'D$$



$$g = A'B + B'$$



$$h = AB$$



Circuit Diagram : Attached.

Simulation : Attached.

## Cost Analysis

IC Name	Required Gates	Quantity	Price
IC 7400 Quadruple 2-Input NAND gates	51	13	325 BDT
7 segment Display	10	1	15 BDT
470 Ohm Resistor		12	12 BDT
Wires	146	146	365 BDT
Battery + Connector + Regulator			109 BDT
Bread Board		3	450 BDT
Total Cost			1,276 BDT

beldatta : marginal tissue

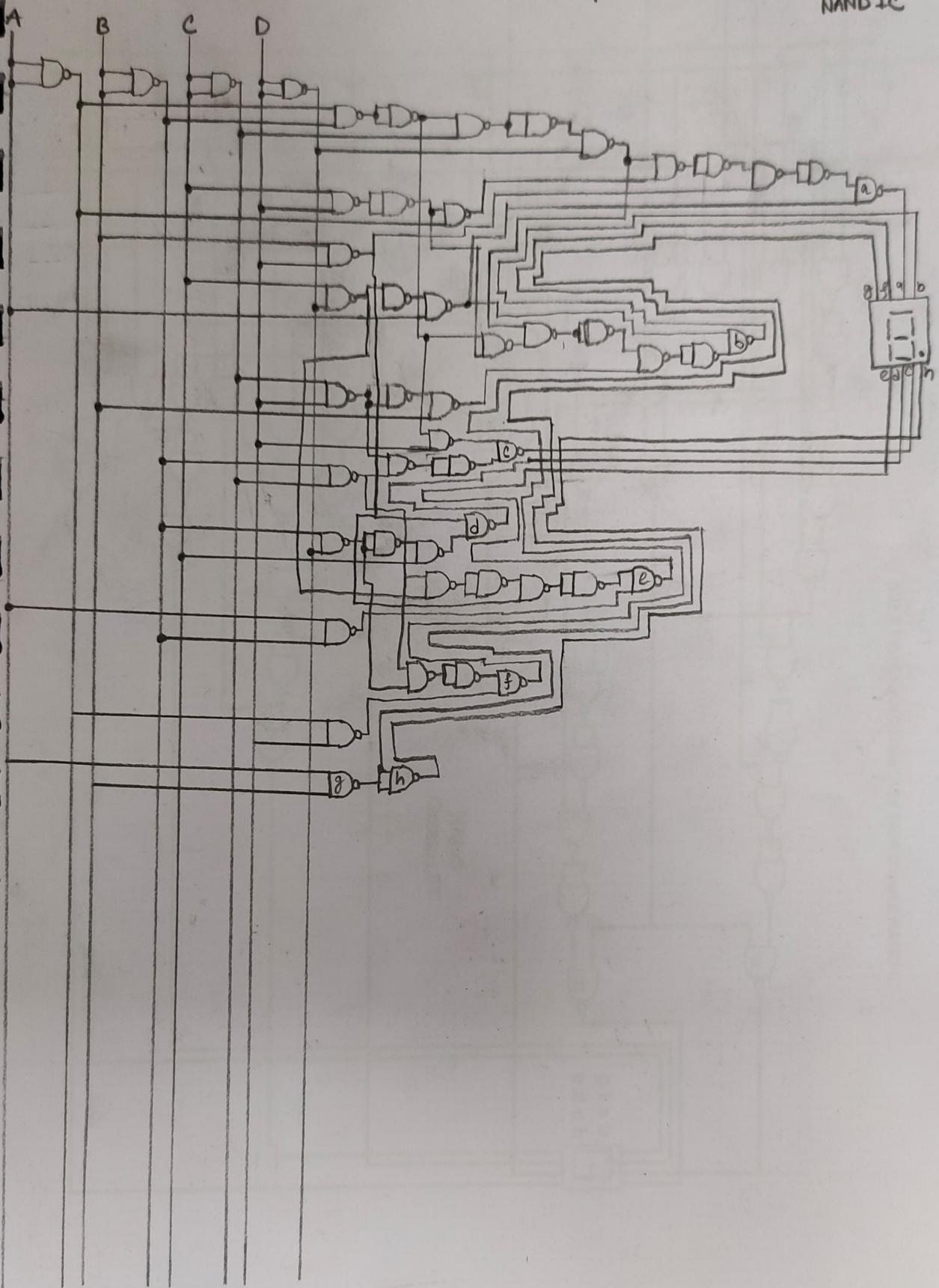
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### procedure :

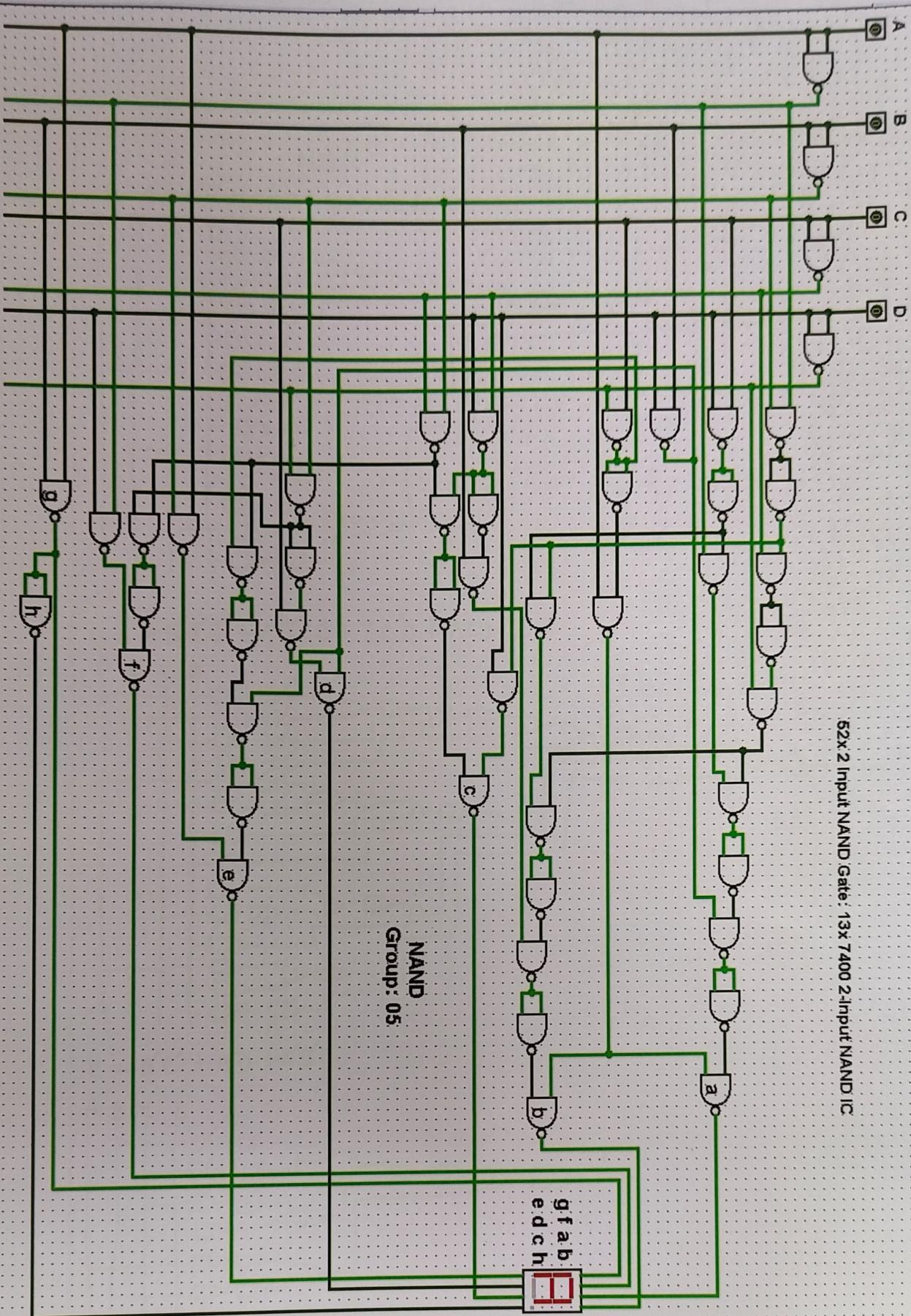
01. First, we take the shortest Equation possible from the K-Map Section.
02. We convert the circuit of K-map to a NAND Circuit.
03. After converting, we find lots of Invert Gate uses consequently.
04. Then, we remove the Invert Gate that was consequently connected from the circuit. This is called gate level minimization.
05. After that we redraw the circuit and implement the circuit using the respective IC's pin Diagram.
06. Then, we connect the LED using a 470 ohm resistor.
07. It also requires lots of gates, more than Boolean Algebra but it works fine.

# NAND

52x2 Input NAND Gate : 13x7400 2-Input  
NAND IC

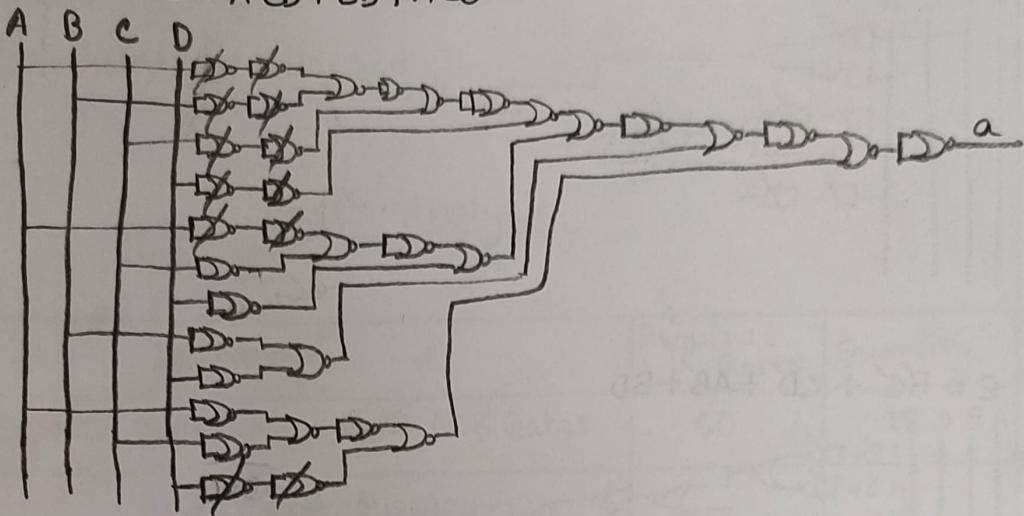


52x 2 Input NAND Gate: 13x 7400 2-Input NAND IC

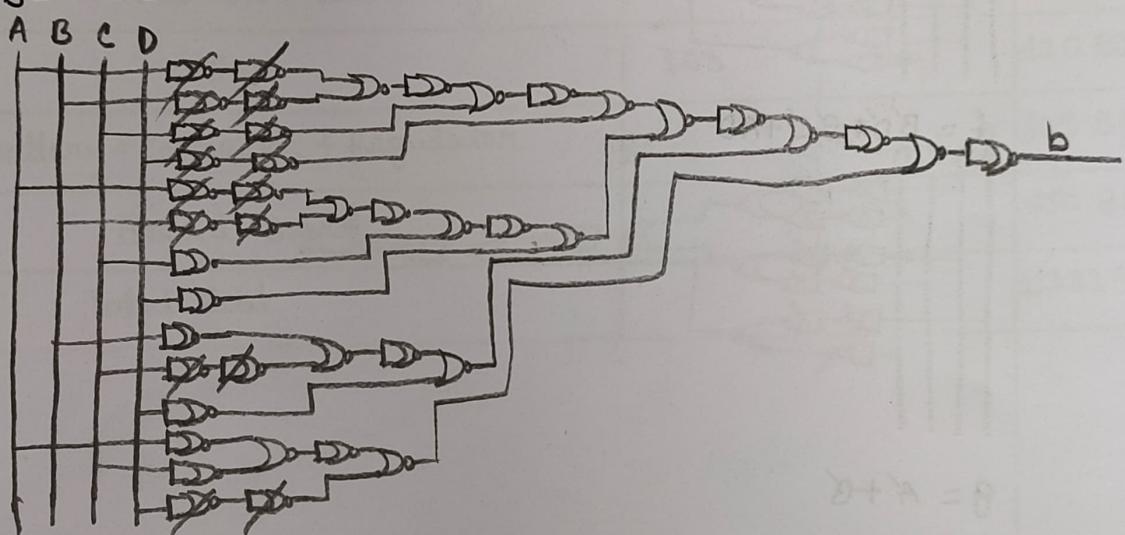


NOR

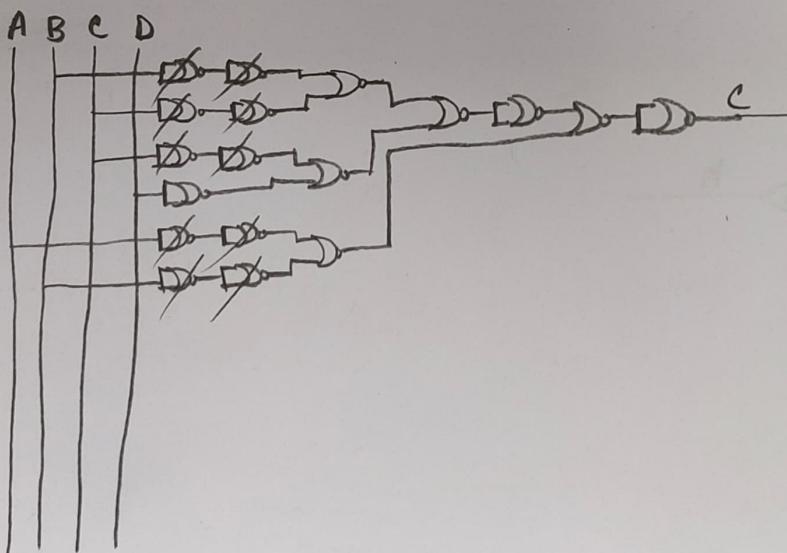
$$a = A'B'C'D' + A'CD + BD + ACD'$$



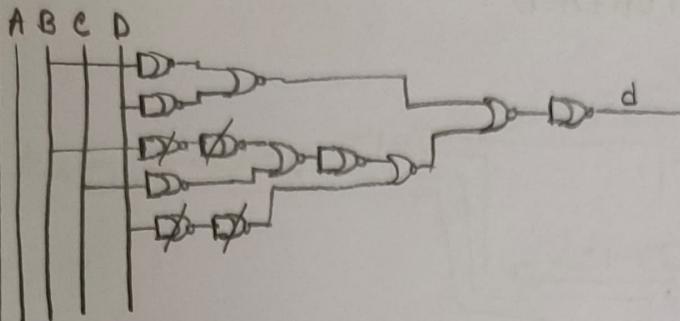
$$b = A'B'C'D' + A'B'CD + BC'D + ACD'$$



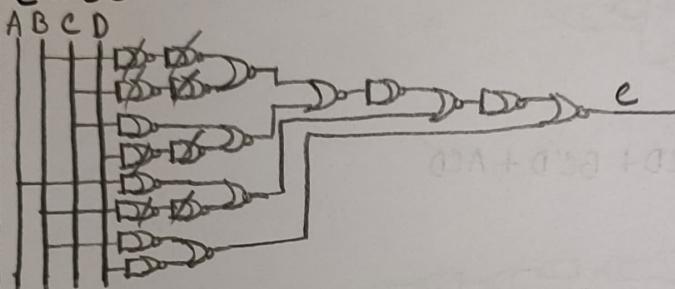
$$c = B'C' + C'D + A'B'D'$$



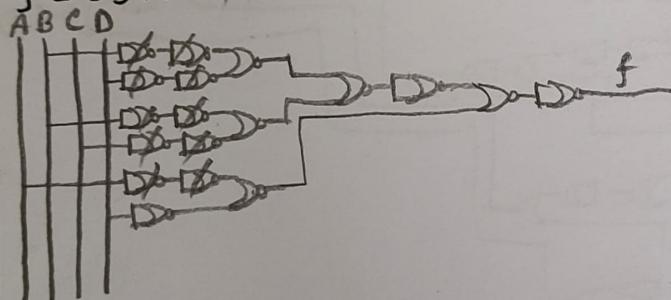
$$d = BD + B'CD'$$



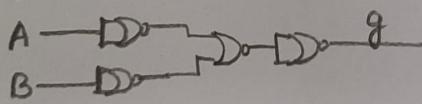
$$e = B'C' + CD' + AB' + BD$$



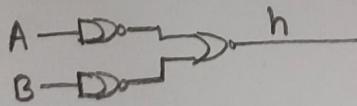
$$f = B'D' + B'C' + AD$$



$$g = A' + B'$$



$$h = AB$$



Circuit Diagram: Attached

Simulation: Attached

### Cost Analysis

IC Name	Required Gates	Quantity	Price
IC 7402 Quadruple 2-Input NOR Gates	60	15	375 BDT
7 segment Display		1	15 BDT
470 Ohm Resistor		12	12 BDT
Wires	168	168	420 BDT
Battery + Connector + Regulator			109 BDT
Bread Board		3	450 BDT
Total Cost			1,381 BDT

procedure :

01. Again, we copy the circuit of K-Map and Convert the circuit to a NOR circuit.

02. Hence, we also find some Invert gate connected consequently.

03. Again, we do the gate level minimization.

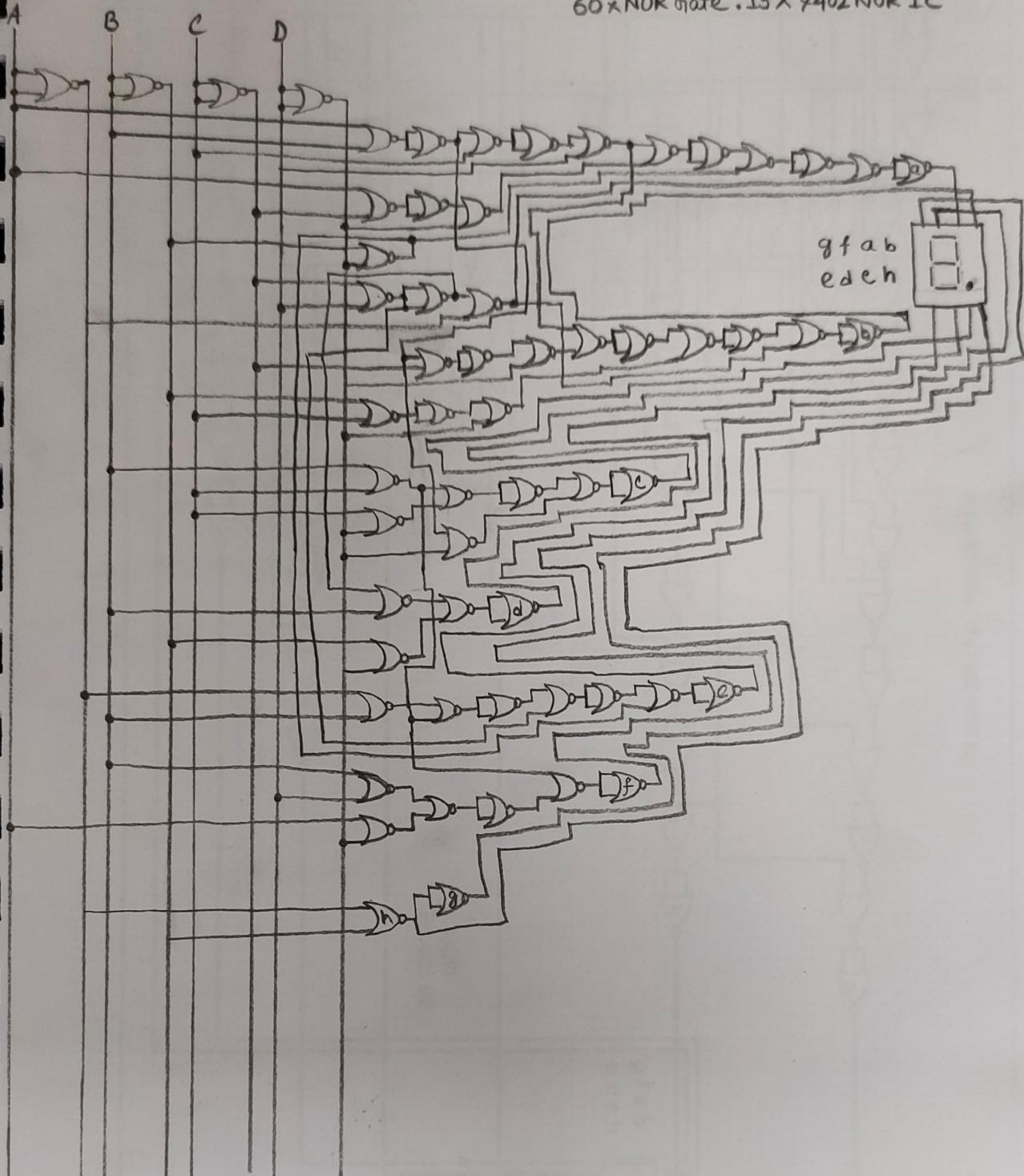
04. After that, we redraw the fresh circuit diagram and implement the circuit diagram using the respective IC's pin Diagram.

05. Then, we connect the LED using a 470 ohm resistor.

06. It also requires almost the same IC's as NAND circuit diagram. It was also working perfectly.

# NOR

60xNOR Gate : 15x 7402 NOR IC



60x NOR Gate: 15x 7402 NOR IC

