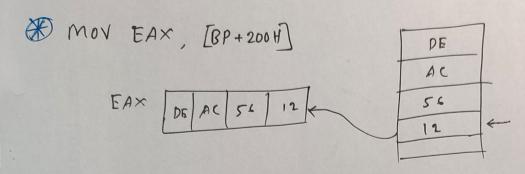
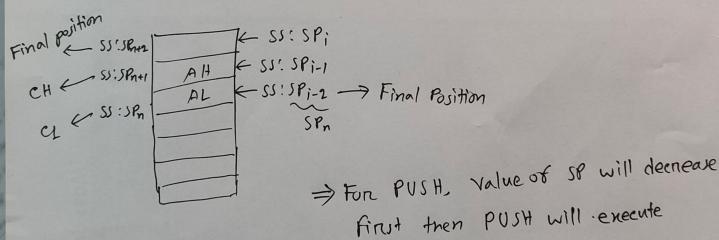
## CSF 33/ /L-6/29. 02.2024 /



Stack memony addressing mode:

- followed LIFO (last in, first out)



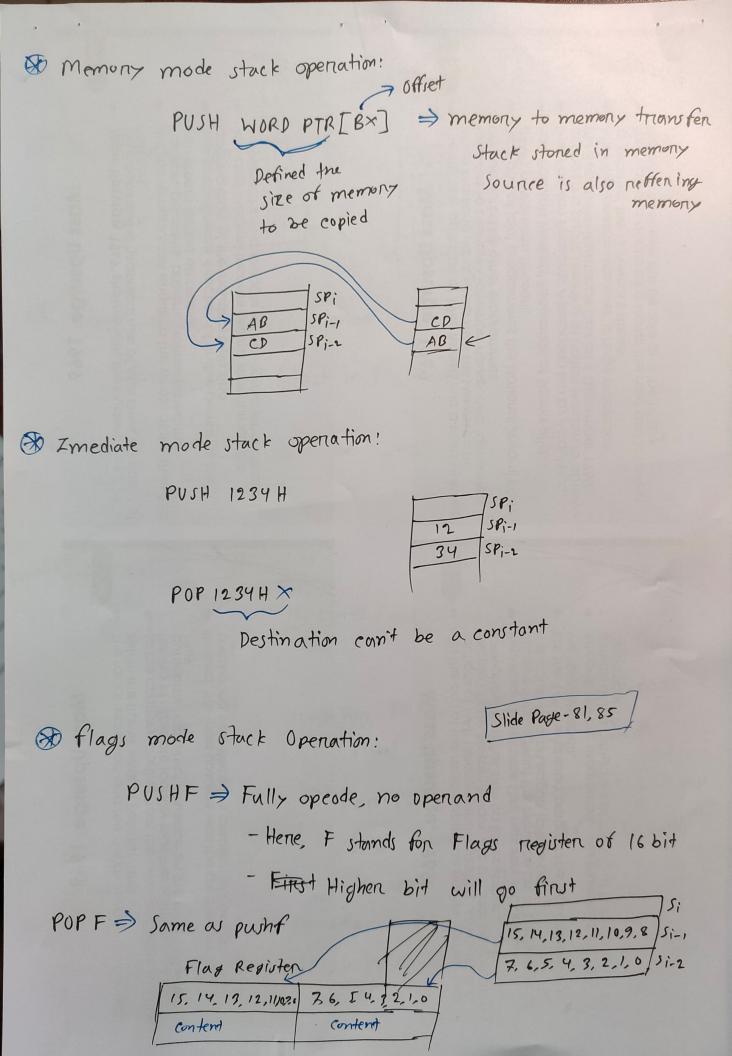
>> For POP, value val content will pop first, then value of SP will increase by 1.

Register mode stack operation!

⇒ PUSH BX | SpUSH CS ⇒ Highen bit will copied first then lower bit

POP CSX

Segment Register mode



All Register mode stack operation:

=> PUSHA

Push sequence

=> Ax, cx, Dx, Bx, SP, BP, SI, DI

=) POPA

pop sequence > Revenue of Push

Becameful about the final value of DJP

Let, initial value of SP = 2345 H

after PUSHA instruction,

value of SP will decrease by SPR-

value of JP will decrease 16 times. because of 8 register.

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Here 16 is decimal count
Remember, 0-9, decimal and
hera same. but after 9
in hera, it is A. So we
need to convent 16 to
heradecimal, which is 10.

: Final value of SP = (2345-10) H = 2335 H

Base prelative plus index - usefull for addressing two dimensional memory arms

Lecture Slide 4,5

Chapter - 4

Data movement instruction

## D LEA → Load Effective Address

- used to calculate the offset and stone it in a location.

LEA AX, NUMB
MOV AX, OFFSET NUMB

Both instruction do the same operation.

⇒ MOV BX, [DI] ⇒ copied the data stoned in a memony location reffered by the offset DI

=> LEA Bx, [DI] → copied the value on content of DI

Registers on the entire offset value inside the third bracket.

( LDS ) Load Data Segment

- do two operation at a time

MOV Bx, [DI]

MOV DS, [DI+2H]  $SB \times 34 12$   $SB \times 34 12$ 

MOV Bx, [SP] LSS Bx, [SP]
MOV Bxss, [SP+2H]

Shot by Logond T IOV