

North South University

Department of Electrical & Computer Engineering

Lab Report

Experiment No:

04

Experiment Title:

Design of a 4-bit Binary Up-Down counter.

Course Code:

CSE332L

Section:

10

Course Name:

Computer Organization & Architecture Lab

Lab Group #:

03

Written By:

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Objectives 8

(1) To build and understand the behaviour of an up/down counter

Equipments List &

- · Trainer Board
- · 10 7404, 7408 7432 7486 7474 (Notinate) (ANDMATE) (ORGATE) (XOTGATE) (D-FlipFlop)

 · Wires for connection
- · Power Supply

Block Diagram &

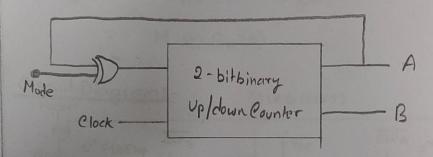
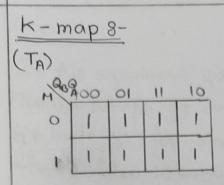
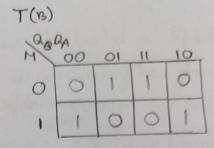


fig: Block diagram of 2-bit binary up/down counter.

Truth Tables

	0 (1)	-	and the second distriction of the second section of the section of the second section of the sect	A mark of the contraction of the	The same of the sa	
М	G _B (+)	Q _A (t)	QB(++1)	QA(++1)	TB	TA
0	0	0	0	1	0	1
0	0	A STATE OF THE STA	A COLUMN TO STATE	0	AT A DESCRIPTION OF THE PARTY O	CONTRACTOR CONTRACTOR CONTRACTOR
0	!	0			0	1
P			0	0		
1	0	0	1			
1	0		0	0	0	
1	1	0	0	1	1	1
1	11		11	0	0	1





Boolean Expression 3-

$$T_A = 1$$

$$T_B = \overline{H} G_A(t) + \overline{H} Q_A(t)$$

$$= \overline{H} \oplus Q_A(t)$$

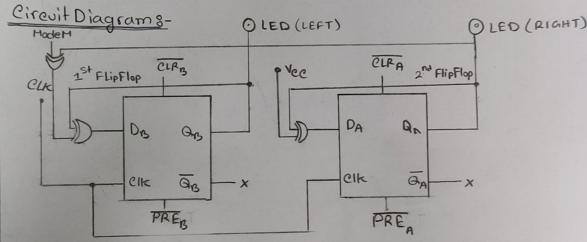
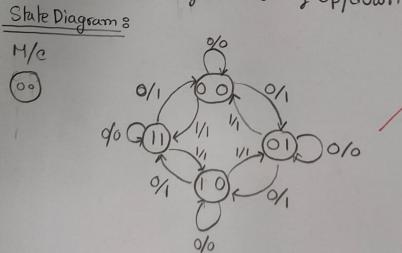


fig: 2-Bit Binary Up/down counter



Discussion:

In this experiment, we were to build a 24 bit-binary Up/down Counter but for the ease of understanding how the counter works we built a 2 bit-binary Up/down Counter. For this, we used the following ICs: IC7404 (NOT Gate), IC 7408 (AND-Gate), IC7432 (OR Gate), IC7486 (EXOR Gate) and Finally IC7474 (D-Flip Flop). This was a very straight forward circuit and was very easy to build. We didn't face any issues while implementing it. The experiment was successful.

