

BOLD and Underline Word should be written with color pen. Use pencil margin, Page number with color pen, all drawing with pencil, table body with pencil but text will be ball pen, write both side of page.

Experiment Name: Loading Effect of Voltage Divider Circuit.

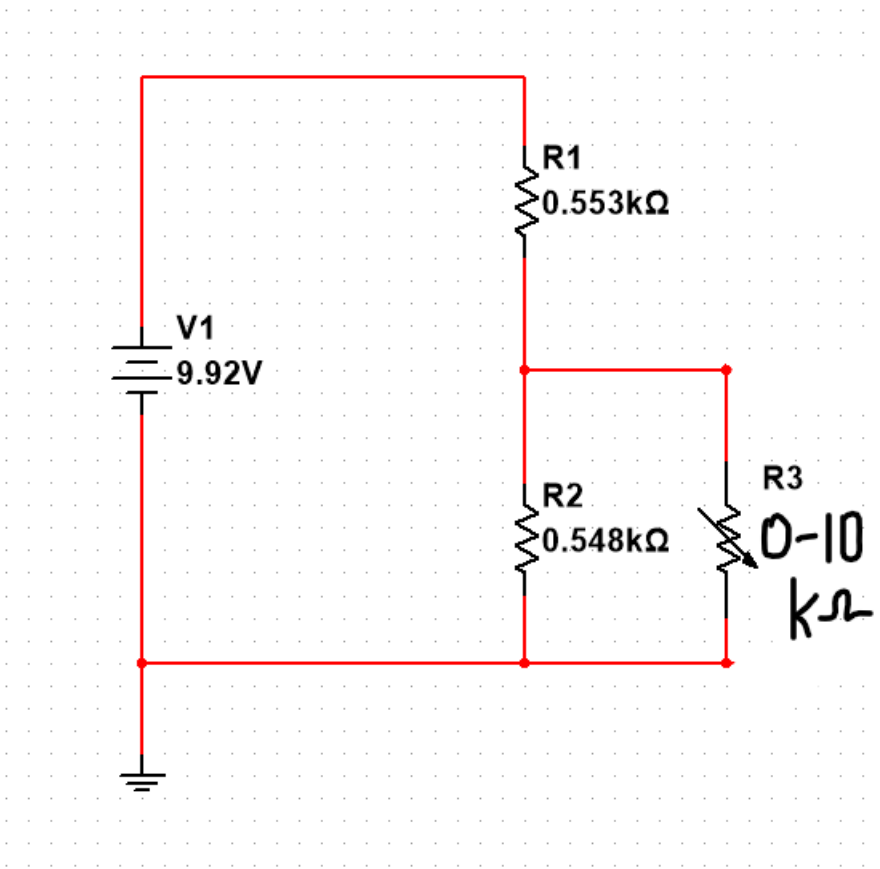
Objectives:

- To analyze how the voltage divider circuit behaves when there is no load resistance connected.
- Evaluate the performance of voltage divider circuit due to loading.

Apparatus:

- Breadboard
- Resistors (2x 560 Ω)
- Variable Resistor (0 - 10 k Ω)
- Digital Multimeter (DMM)
- DC Power Supply
- Wires

Circuit Diagram:



Data Table:

Table 1:

RL	Vout (Measured)	Vout (Calculated)	%Error
No resistor	4.91	4.94	0.61%
1k (1.01)	3.87	3.88	0.26%
4k (3.99)	4.60	4.62	0.43%
7k (6.99)	4.73	4.75	0.42%
10k (10.02)	4.80	4.81	0.21%

Theoretical Vout Calculation:

$$V_{in} = 9.92 \text{ V}$$

$$R_1 = 0.553 \text{ k}\Omega$$

$$R_2 = 0.548 \text{ k}\Omega$$

without load,

$$V_{out} = V_{in} \frac{R_2}{R_1 + R_2}$$

$$= 9.92 \times \frac{0.548}{(0.553 + 0.548)}$$

$$= 4.94 \text{ V}$$

$$\text{Error} = \left| \frac{4.94 - 4.91}{4.94} \right| \times 100\%$$

$$= 0.61\%$$

With Load,

When, $R_3 = 1.01 \text{ k}\Omega$

$$V_{out} = V_{in} \frac{(R_2 \parallel R_3)}{R_1 + (R_2 \parallel R_3)}$$

$$= 9.92 \times \frac{\left(\frac{1}{0.548} + \frac{1}{1.01} \right)^{-1}}{0.553 + \left(\frac{1}{0.548} + \frac{1}{1.01} \right)^{-1}}$$

$$= 3.88 \text{ V}$$

$$\text{Error} = \left| \frac{3.88 - 3.87}{3.88} \right| \times 100\%$$

$$= 0.26\%$$

When, $R_3 = 3.99 \text{ k}\Omega$

$$V_{out} = 9.92 \times \frac{\left(\frac{1}{0.548} + \frac{1}{3.99} \right)^{-1}}{0.553 + \left(\frac{1}{0.548} + \frac{1}{3.99} \right)^{-1}}$$

$$= 4.62 \text{ V}$$

$$\text{Error} = \left| \frac{4.62 - 4.60}{4.62} \right| \times 100\%$$

$$= 0.43\%$$

When $R_2 = 6.99 \text{ k}\Omega$ {Do it}

When $R_2 = 10.02 \text{ k}\Omega$ {Do it}

Graph:

N/A

Result Analysis:

After this experiment, we found that the voltage across a component suddenly drops whenever we add a resistor parallel to that component. Then, when we increase the resistor value, the total resistor increases, and the voltage rises. So, we can control the voltage of a component by adding a variable resistor parallel to that component.

Questions and Answers:

01. When there was no loading resistor in our circuit, V_{out} in R_2 was 4.91 volts. Whenever we add the variable resistor with a value of 1.01k Ohms in parallel, the total resistance at that point decreases, and the voltage drops to 3.87 volts. Then, when we increase the resistance of the loading resistor to 3.99 Ohms, the total resistance increases, and the voltage rises to 4.60 volts. As we connected the variable resistor in parallel connection, the total resistance of that point must be less than the lower resistor. In this case, the lower resistor is R_2 , so we can't get the previous voltage again, but we can control the voltage up to <4.91 volts. So, we can now control the voltage of R_2 by changing the value of the variable resistor.
02. All calculations showed in Data Table Section.
03. Our measured data and theoretically calculated data are approximately the same. We found a minimal margin of error of about 0.21-0.61% only. This error may happen due to wires resistance; variable resistors may increase by a bit of resistance. So, our voltage divider circuit supports the theory of the loading effect.

Discussion:

In this experiment, we analyze the voltage divider circuit behaves when there is a loading resistance connected in parallel connection. We saw how the voltage changes with the loading resistance value. Most importantly, we can now control the voltage of a component by adding a variable resistor in a parallel connection. In this experiment, we face some problems related to the variable resistor. To set its value at a particular point was too difficult; sometimes, it auto changed its resistance. We managed to keep it steady and completed the experiment within the time.

Attachment:

- 01.** Signed Data Table.
- 02.** Simulation using Multisim.