CSE 331 / L-18 / 25.04.2024 /

ALE = Address Latch Enable

* in Latch, G = Clock Pulse ↑

OE = 0, active

ALE = Clock Pulse ↑

for data make ALE = deactivate

* Buffer :

G = Data Enable pin = $\overline{DEN}$ = 0 for enable

DIR = Data transfer = DT/$\overline{R}$

↳ Receive

↳ microprocessor will receive

↓ microprocesor will transfer

* Address is generated by ALU, that's why there is no incomming address data.

* How many buffer and latches IC used and why? describe.

* Draw the simplified diagram of fully buffered 8086 & 8088.

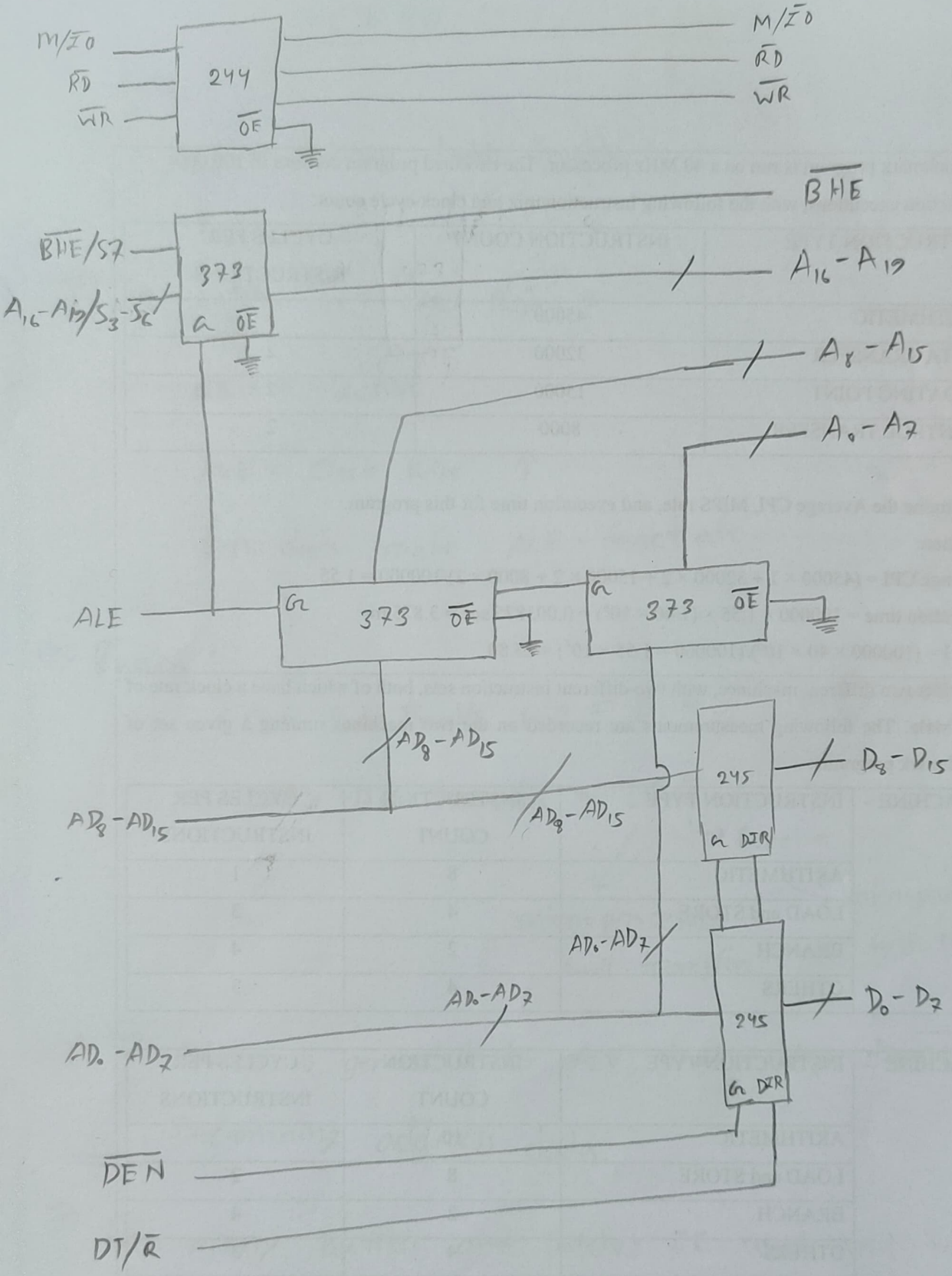


Fig.:- Simplified diagram of fully buffered 8086

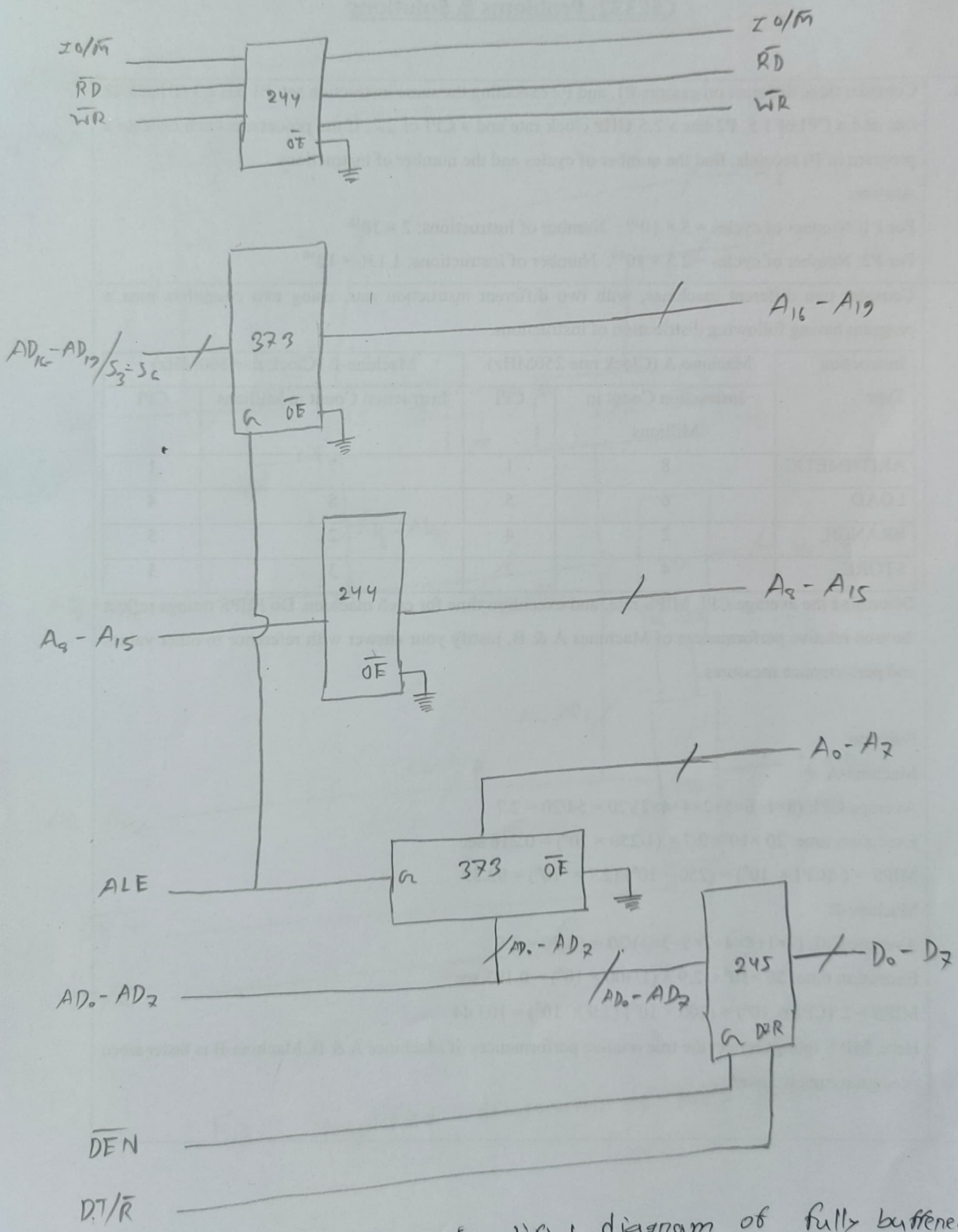


Fig.: Simplified diagram of fully buffered 8088

✱ 8284 IC

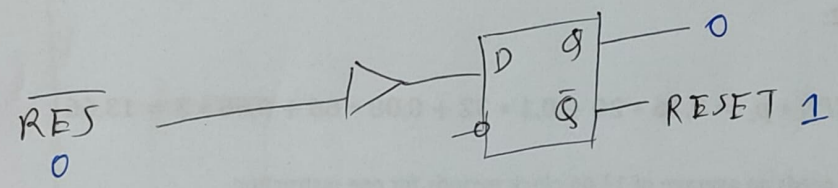
⇒ Clock Generator IC

⇒ Three output

- Reset
- Ready
- Clock → OSC, PCLK, CLK

EFI = External frequency input

✱ Reset Block:



✱ Clock Block:

Crystal Oscillator ⇒ 12 MHz
15 MHz → Divide by 3 ⇒ 5 MHz
20 MHz

PCLK = Peripheral Clock
divide by 2 ⇒ 2.5 MHz

F/C̄ ⇒ 1 ⇒ B will activate
0 ⇒ A will activate
} No need for 8086

↙ Frequency In

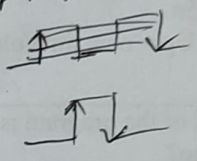
Ready Block:

RDY1 ⇒ 1	RDY2 ⇒ 1
$\overline{AEN1}$ ⇒ 0	$\overline{AEN2}$ ⇒ 0

Sync.

Async $\overline{ASYNC}$ ⇒ 1 ⇒ ⇒ single edge single pulse

⇒ 0, then D-flip-flop already 1



⇒ two edge one pulse

Async.

Draw the internal diagram of 8084 IC and explain. ***

Draw simplified write and read bus cycle for 8086/8088 and explain in brief. ***

164 ⇒ Shift Register

Tw ⇒ 1-7 ⇒ 200 - 1400 ns max wait

NAND=0; CLR ⇒ activate, all pin 0

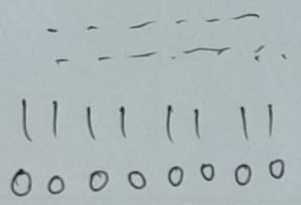
00000000

NAND=1; CLR = Deactivate

10000000

11000000

} Pen CLK



OR = 0 ; Ready = 0

OR = 1 ; Ready = 1

(*) Wait state generation timing of the circuit. ***

⇒ Draw & Explain in brief about input and output

How ~~out~~ output changing.