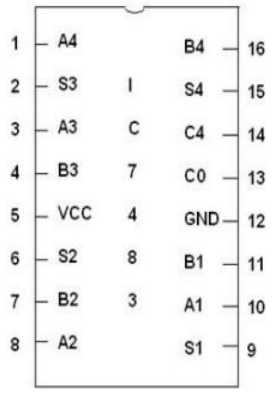
IC Number	IC Name	Input	Gate Count	Pin Details	
7400	NAND	2	4	1,2 = 3 4,5 = 6	9,10 = 8 12,13 = 11
7408	AND	2	4		
7432	OR	2	4		
7486	XOR	2	4		
7402	NOR	2	4	2,3 = 1 5,6 = 4	8,9 = 10 11,12 = 13
7404	NOT	1	6	1 = 2 3 = 4 5 = 6	9 = 8 11 = 10 13 = 12
4073	AND	3	3	1,2,8 = 9 3,4,5 = 6 11,12,13 = 10	
4075	OR	3	3		
7410	NAND	3	3	1,2,13 = 12 3,4,5 = 6 9,10,11 = 8	
7411	AND	3	3		

IC 7483 4-bit binary adder



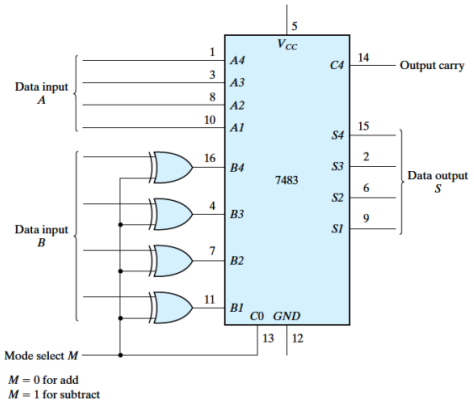


Figure D.1.1: 4-bit Adder-Subtractor

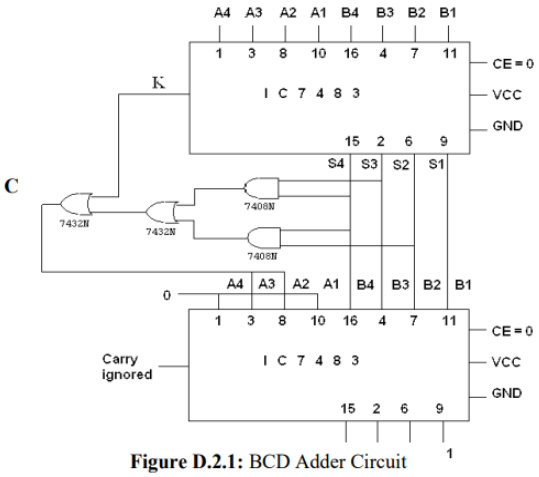


Figure D.2.1: BCD Adder Circuit

New Apparatus:

IC 74151 (8:1 Multiplexer):

The 74151 is a 16 pin IC which requires a Ground connection at pin 8 and V_{CC} at pin 16. Pins 4, 3, 2, 1 and 15, 14, 13, 12 are the inputs, pins 9, 10 and 11 are used to select a particular input and pin 5 is the output. Pin 6 is provides the inverse of the output at pin 5. An input at pin 7 is used to Enable the IC.

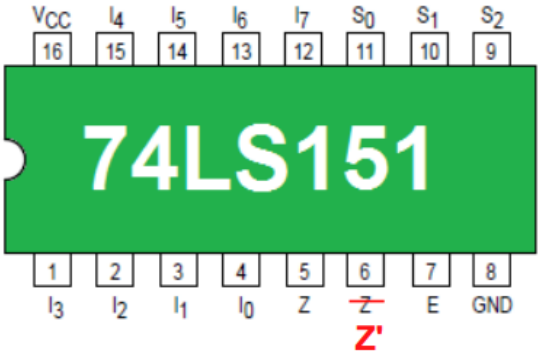


Figure B.3: Pinout of IC74151

IC 74138 (3 to 8 Line Decoder):

The 74138 is also a 16 pin IC which requires Ground at pin 8 and VCC at pin 16. Pins 15, 14, 13, 12, 11, 10, 9 and 7 are used as the outputs and pins 3, 2 and 1 are used to take input. A combination of the inputs at pins 6, 4 and 5 is used to enable the device. In order for the IC to function as intended, pin 6 (G1) must have a high value and both pins 4 and 5 (G2A and G2B) must have low values.

Unlike some of the other ICs used so far, the outputs of the 74138 IC are ACTIVE-LOW which means that they provide a 0 or LOW output when they are activated and a 1 or High output when they are inactive.

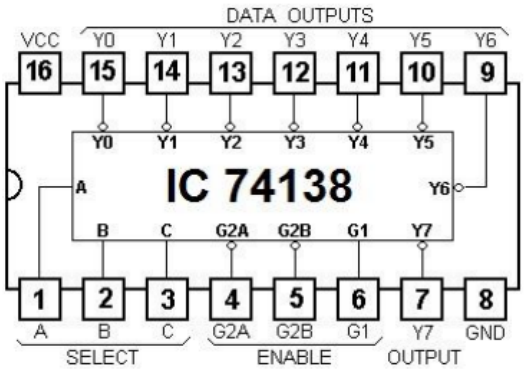


Figure B.4: Pinout of IC74138

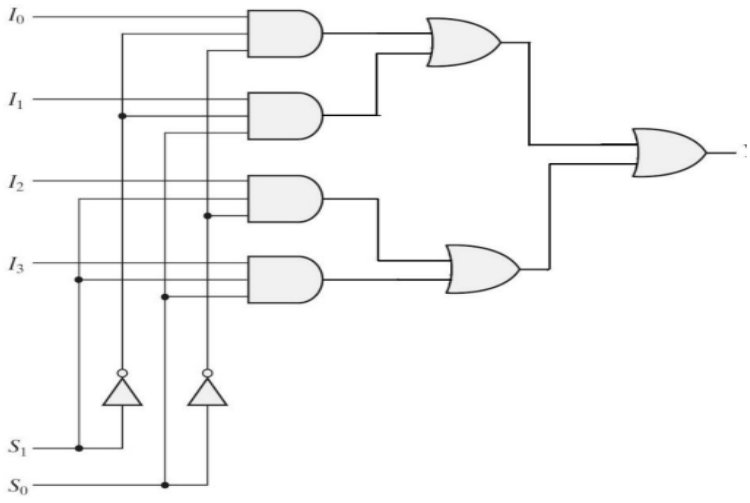
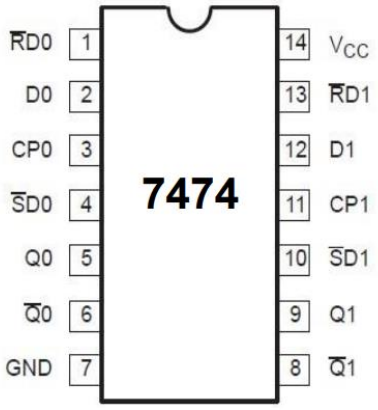


Figure D.1.1: 4:1 Multiplexer

IC 7474 (Dual D Flip-Flops):



PINS	DESCRIPTION
D0, D1	Data inputs
CP0, CP1	Clock inputs (active rising edge)
$\overline{SD}0$, $\overline{SD}1$	Set inputs (active low)
$\overline{RD}0$, $\overline{RD}1$	Reset inputs (active low)
Q0, Q1, $\overline{Q}0$, $\overline{Q}1$	Data outputs

Figure B.1: Pinout of IC7474

D.1 Procedure

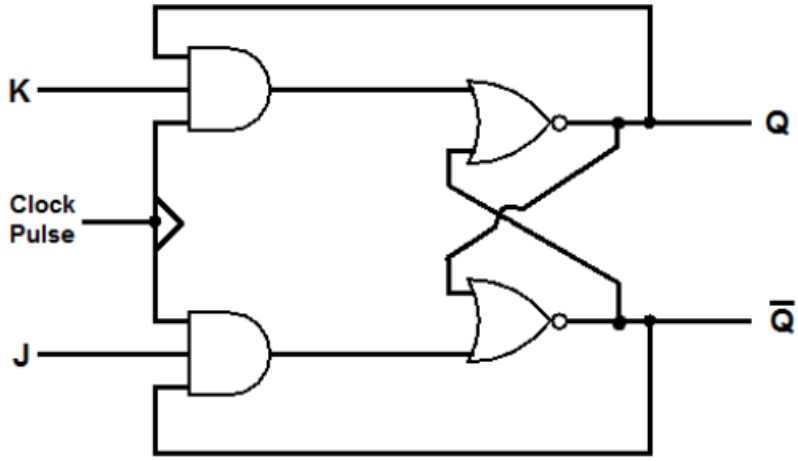


Figure D.1.1: JK Flip-Flop implemented using AND and NOR gates

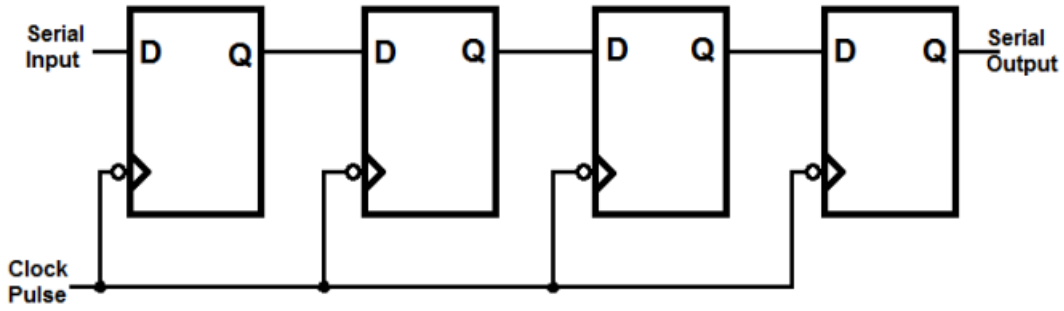


Figure D.3.1: Right Shift Register

IC 74107 (Dual JK Flip-Flops):

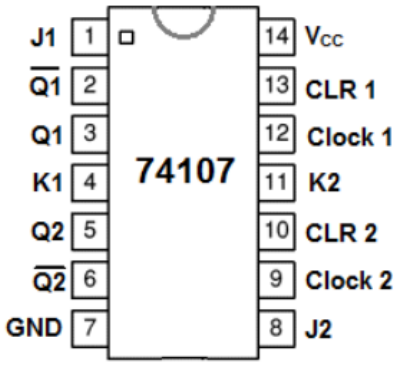


Figure B5: Pinout of IC74107

The 74107 is a 14 pin IC which requires a Ground connection at pin 7 and V_{CC} at pin 14. Pins 1 and 4 serve as the J and K inputs for the first Flip-Flop and pins 8 and 11 act as the J and K inputs for the second Flip-Flop. Pins 2 and 5 are the outputs of Flip-Flop 1 and Flip-Flop 2 respectively. Pin 12 is the clock input for the first Flip-Flop and pin 9 is the clock input for the second Flip-Flop. The CLR 1 and CLR 2 inputs (pin 13 and pin10, respectively) have to be supplied with logic 1 or 0 depending on the internal implementation of the paticular IC.