



North South University
Department of Electrical & Computer Engineering
LAB REPORT- 04

Course Code: CSE 231L

Course Title: Digital Logic Lab

Section: 08

Lab Number: 04

Experiment Name: BCD to Excess-3 Converter

Combinational Logic Design (K-Map)

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Submitted by Group Number: 05

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Experiment Name : Combinational Logic Design (K-map), BCD to Excess-3 converter.

Objective :

- Design a complete minimal combinational logic system from specification to implementation.
- Minimize combinational logic circuits using Karnaugh maps.
- Learn various numerical representation systems.
- Implement circuits using canonical minimal forms.

Apparatus :

- 1 x IC 7404 Hex inverters (NOT gates)

- 3 x IC 7411 Triple 3-input AND gates

- 1 x IC 4075 Triple 3-input OR gates

- 1 x IC 7032 Quadruple 2-input OR gates

- 3 x IC 7400 " " " NAND "

- 1 x IC 7410 Triple 3-input NAND "

- Trainer Board

- wires.

Theory :

BCD is a way of representing decimal numbers using binary

digits. In BCD, each decimal digit is represented by a four digit bit binary code. Allowing each BCD digits to

have one of 16 possible values (0000 to 1001) BCD is

commonly used in digital systems, where decimal

①

(Q8) (a) Arithmetic is required such as in calculators, counter and displays.

Excess-3 is a decimal code that represents decimal numbers using binary digits by adding 3 to the corresponding binary value of each decimal digit. Excess-3 is commonly used in digital systems where decimal arithmetic is required such as in calculators and digital displays.

A k-map is a diagram made up of squares, with each square representing one minterm of function that is to be minimized. In fact, it represents a visual diagram of all possible ways a function may be expressed in standard form. By recognizing various patterns, it is possible to derive alternative algebraic expressions for the same function, from which the simplest can be selected.

(2)

w	x	y	z	A	$wx \setminus yz$	00	01	11	10
0	0	0	0	1		m_0	m_1	m_3	m_2
0	0	0	1	1		$wxyz'$	$w'xy'z$	$w'x'yz$	$w'x'y'z'$
0	0	1	0	0		m_4	m_5	m_7	m_6
0	0	1	1	0		$w'xy'z'$	$w'xy'z$	$w'xyz$	$w'xyz'$
0	1	0	0	0	w	m_{32}	m_{33}	m_{15}	m_{14}
0	1	0	1	0		$wxy'z'$	$wxy'z$	$wxyz$	$wxyz'$
0	1	1	0	1		m_8	m_9	m_{11}	m_{10}
0	1	1	1	0		$wx'y'z'$	$wx'y'z$	$wx'yz$	$wx'yz'$
1	0	0	0	1					
1	0	0	1	1					

Figure B1.

Table: B1

$wx \setminus yz$	00	01	11	10
	m_0	m_1	m_3	m_2
00	1	1	0	0
	m_4	m_5	m_7	m_6
01	0	0	0	1
	m_{32}	m_{33}	m_{15}	m_{14}
	X	X	X	X
11				
	m_8	m_9	m_{11}	m_{10}
10	1	1	X	X

Figure B2

Figure B1 shows the minterm positions on the k-map, 4 input variables and 1 output variable.

Table B1 shows the truth table for the function.

$A = WX + XYZ' + WZ + X'Y'$ where $WXYZ$ goes from Binary 0 to 9.

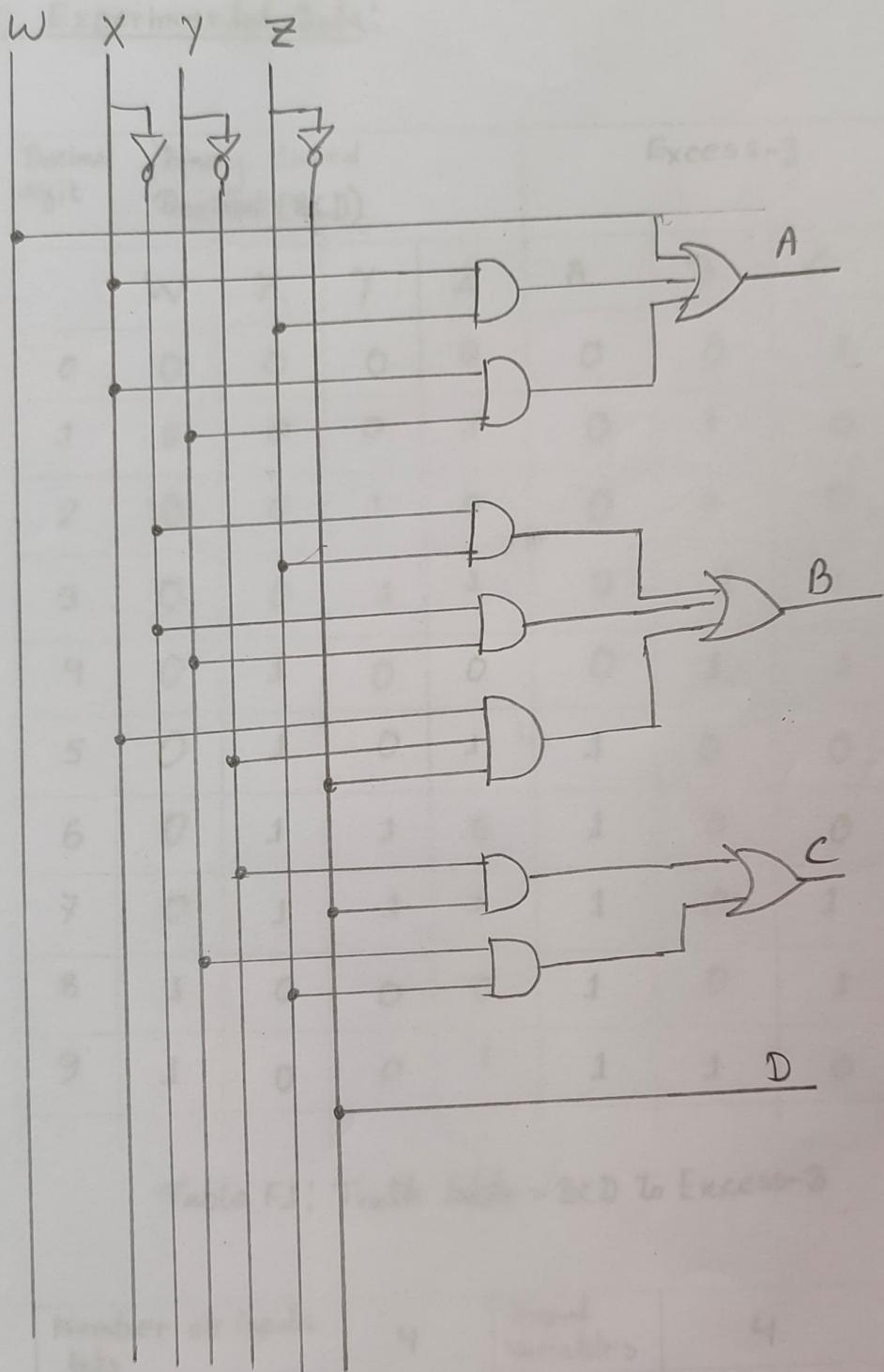
Figure B2 shows the k-map for the function. We can use the k-map to minimize the function to $A = X'Y' + XYZ'$

Experimental procedure:-

1. First we complete the truth table F1 for BCD to Excess-3 converter.
2. Then, we complete the k-Map for output of A, B, C and D to find the minimal 1st canonical functions.
3. After that we draw the circuit diagram with pin configurations in figure F2. Then we start to implement this circuit according to the drawing.
4. First, we implement for A and test it then B and so on. After that we connect 4 outputs at once and test it again.
5. Then we start to minimize the circuit diagram using nand universal gate. First, we draw the minimal circuit in figure F3 with pin configurations. Then we start to implement it.
6. Here, we also implement and test it one by one. After complete we connect 4 output at once and again test it.

(3)

Circuit Diagram



Number of inputs bits	Number of outputs bits	Total variables	Total variables	4
4	4	4	4	4

Truth Table and Analysis

F. Experimental Data:

Decimal digit	Binary Coded Decimal (BCD)				Excess-3			
	W	X	Y	Z	A	B	C	D
0	0	0	0	0	0	0	1	1
1	0	0	0	1	0	1	0	0
2	0	0	1	0	0	1	0	1
3	0	0	1	1	0	1	1	0
4	0	1	0	0	0	1	1	1
5	0	1	0	1	1	0	0	0
6	0	1	1	0	1	0	0	1
7	0	1	1	1	1	0	1	0
8	1	0	0	0	1	0	1	1
9	1	0	0	1	1	1	0	0

Table F1: Truth table - BCD to Excess-3

Number of inputs bits	4	Input Variables	4
Number of outputs bits	4	Output Variables	4

Table F2: System Analysis

$w \times$	$y \times z$	00	01	11	10
00	0	0	0	0	0
01	0	1	1	1	1
11	x	x	x	x	x
10	1	1	x	x	x

$$A = w + xz + xy$$

$w \times$	$y \times z$	00	01	11	10
00	0	1	1	1	1
01	1	0	0	0	0
11	x	x	x	x	x
10	0	1	x	x	x

$$B = \bar{x}z + \bar{x}y + xy\bar{z}$$

$w \times$	$y \times z$	00	01	11	10
00	1	0	1	0	0
01	1	0	1	0	0
11	x	x	x	x	x
10	1	0	x	x	x

$$C = \bar{y}\bar{z} + yz$$

$w \times$	$y \times z$	00	01	11	10
00	1	0	0	1	1
01	1	0	0	1	1
11	x	x	x	x	x
10	1	0	x	x	x

$$D = \bar{z}$$

Figure F1: k-maps

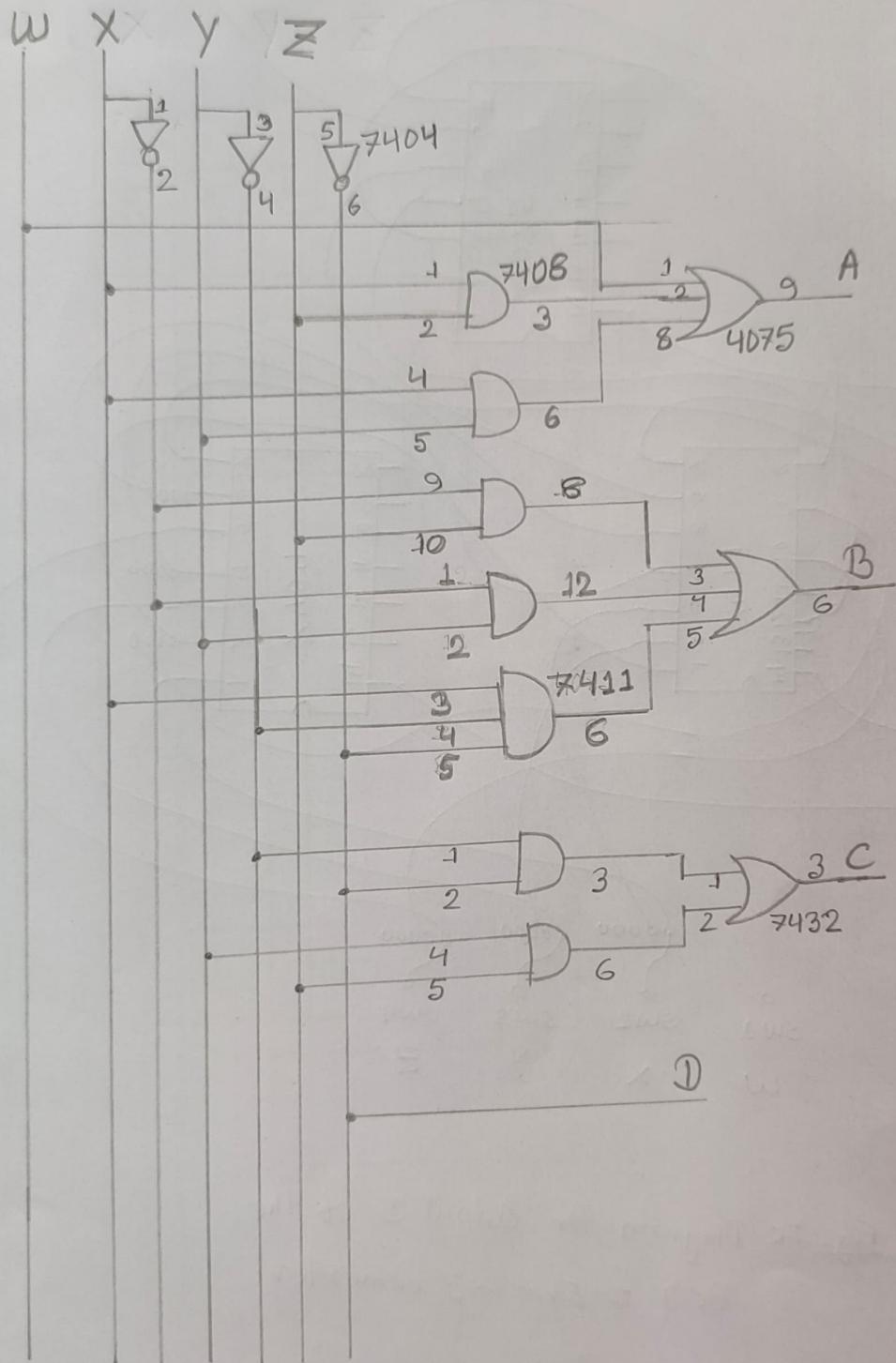


Figure F2: Minimal 1st canonical circuit of BCD to Excess-3 converter

Answer no - 1

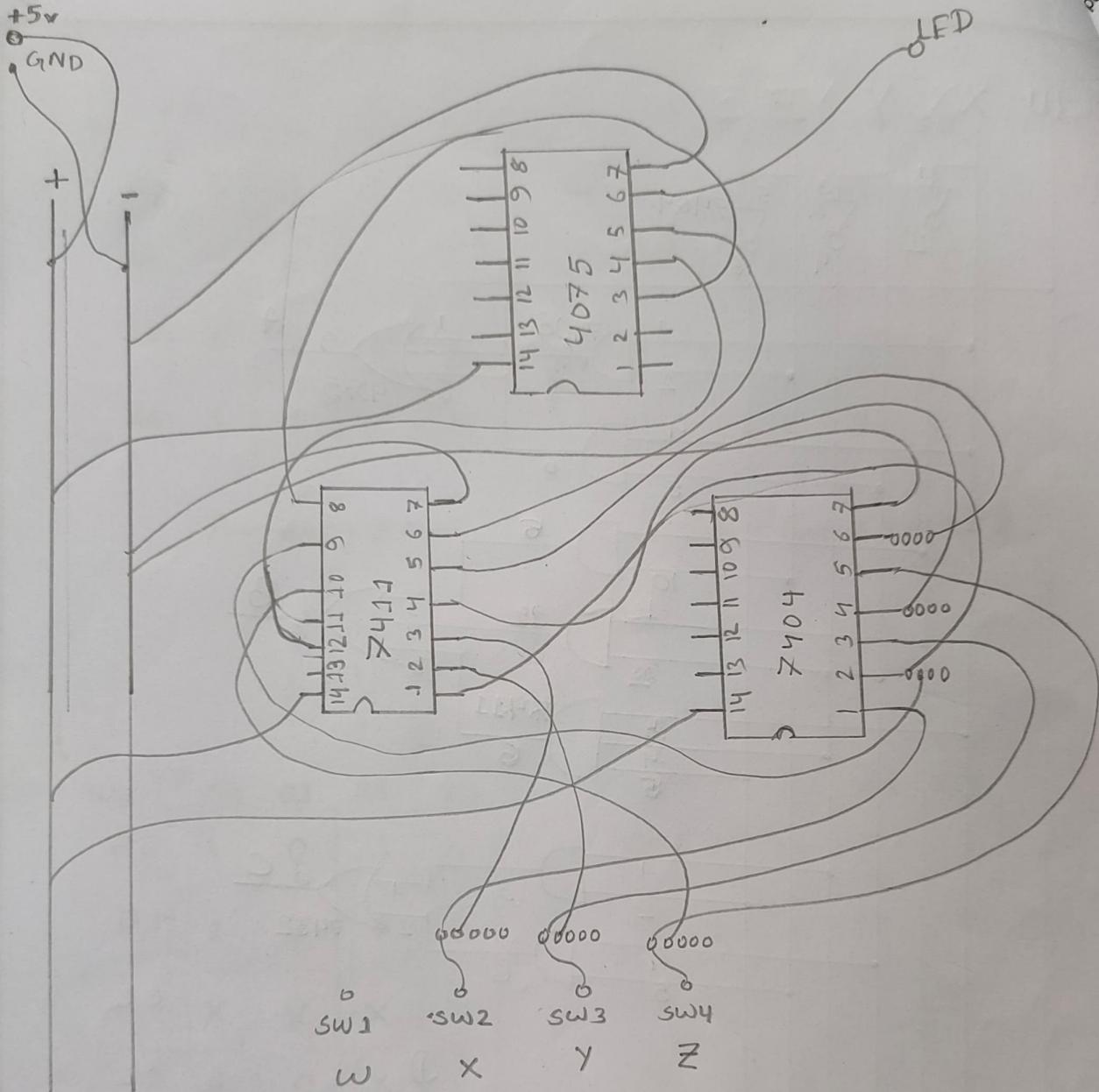


Fig:- Logic Diagram for Output B of the
BCD to Excess 3 converter

(6)

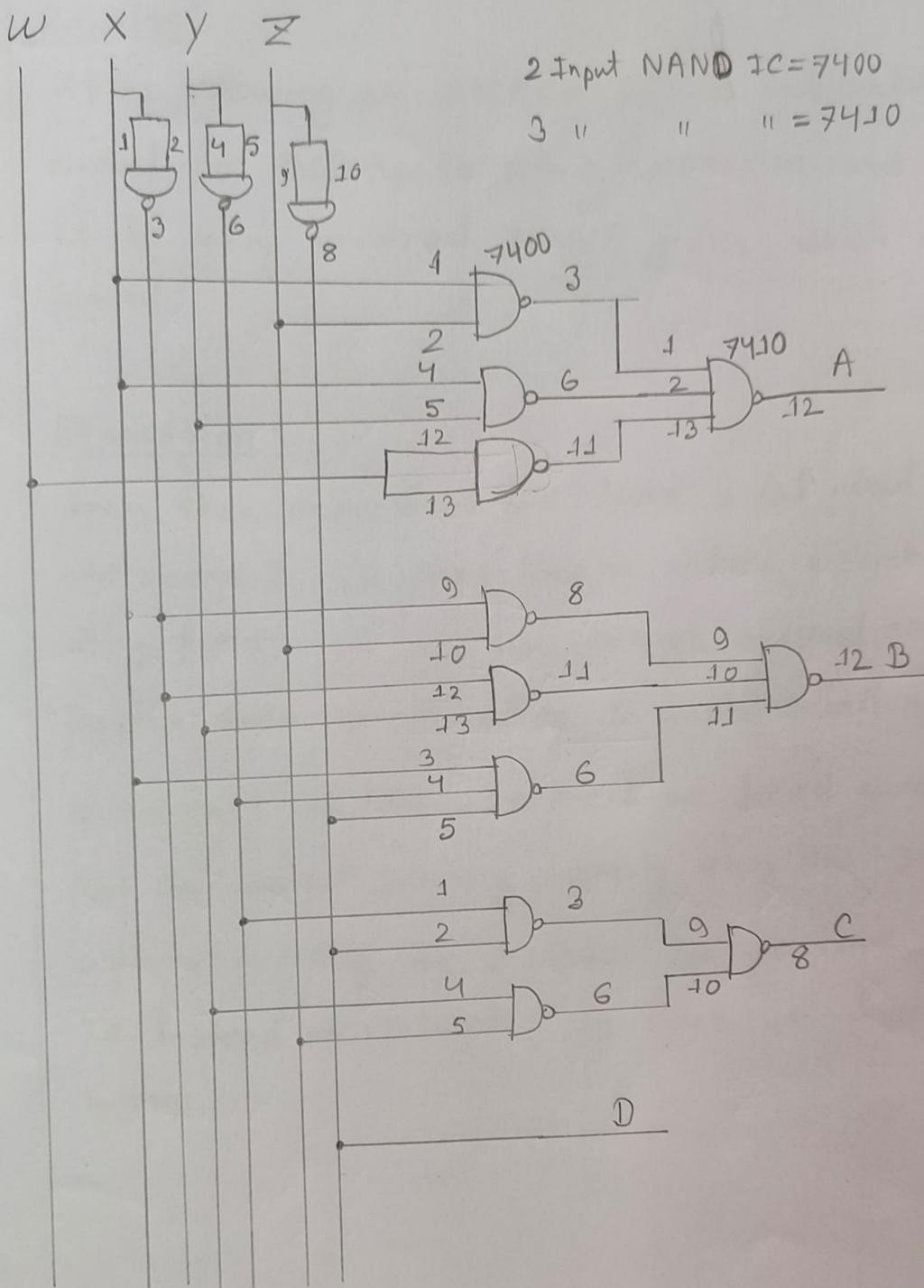


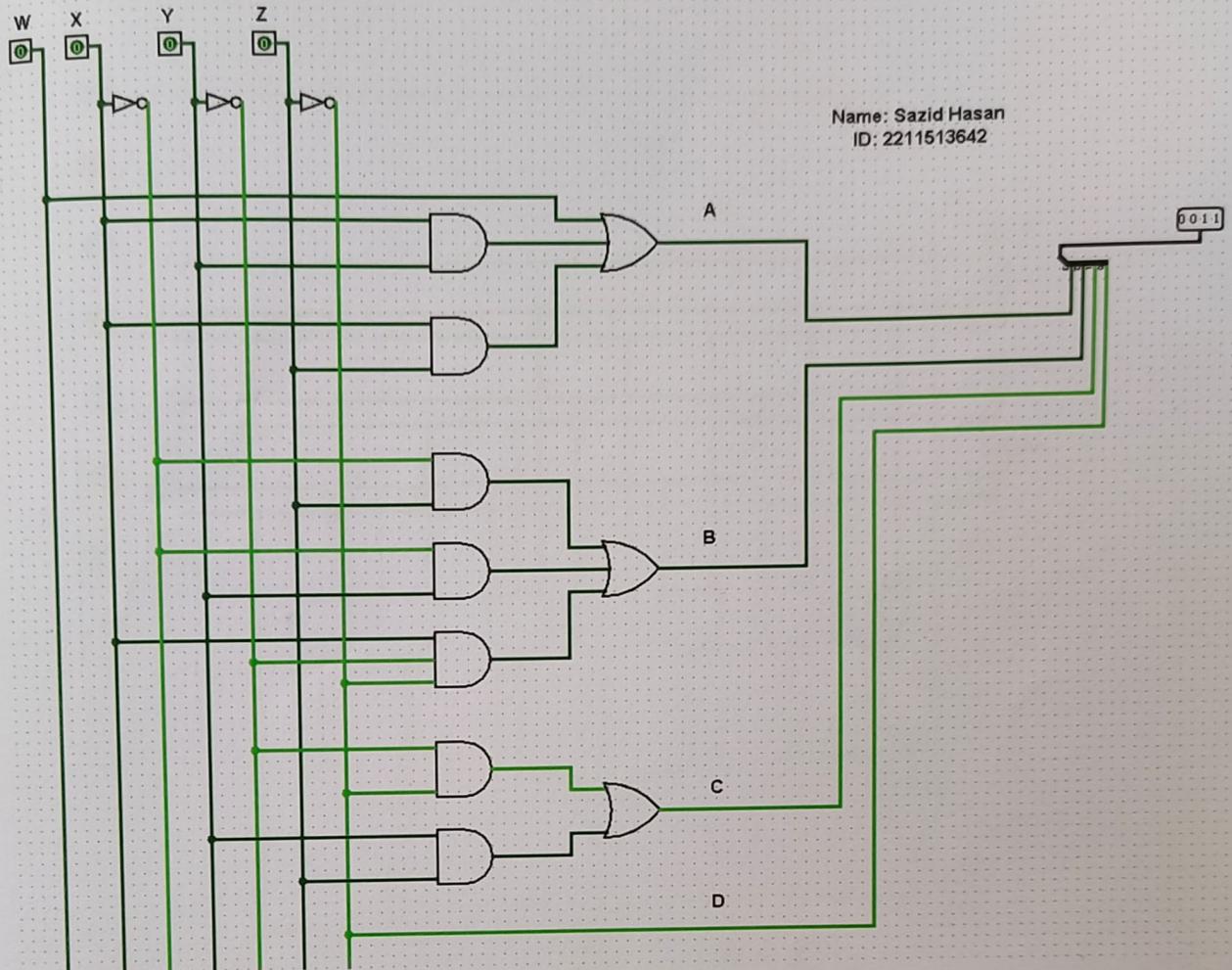
Figure F3: Minimal universal gate implementation of BCD to Excess-3 converter

Results:

After following all procedures, we successfully build the circuit of BCD to Excess-3 conversion and we also built it by using universal NAND gates, which reduces IC's count.

Discussion:

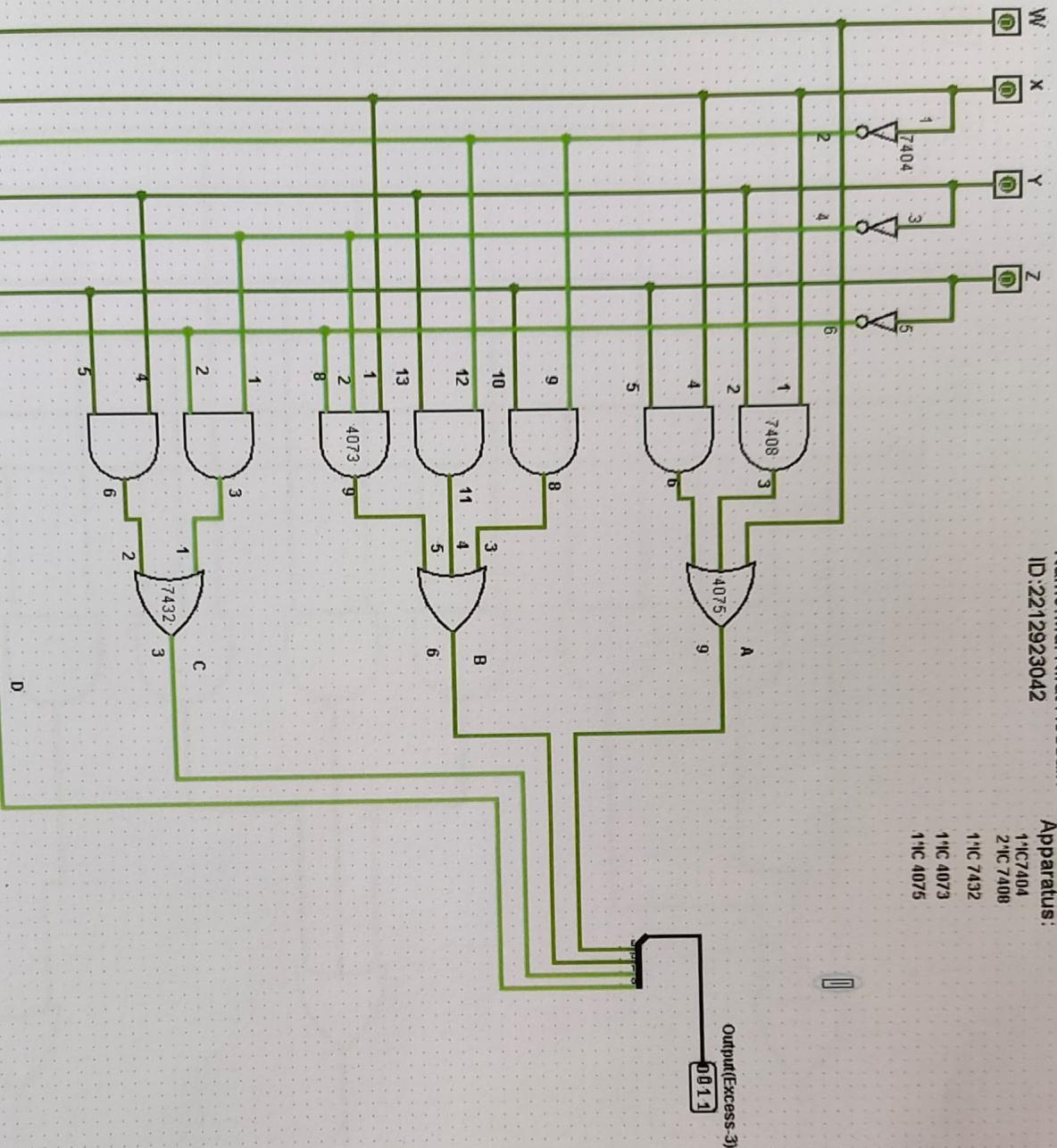
From this experiment we learn a lot about the k-map, BCD and excess-3. We learn how to reduce a combinational circuit using k-map. We can now design minimal combinational logic system from specification to implementation. During the first part of the experiment we faced some problems. Not IC was not working properly even the 3-input OR IC was not working for 2 inputs. So we have use 2 input OR IC instead of 3 input. In short, we learn a lot about k-map.



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Apparatus:

1'IC 7404
2'IC 7408
1'IC 7432
1'IC 4073
1'IC 4075



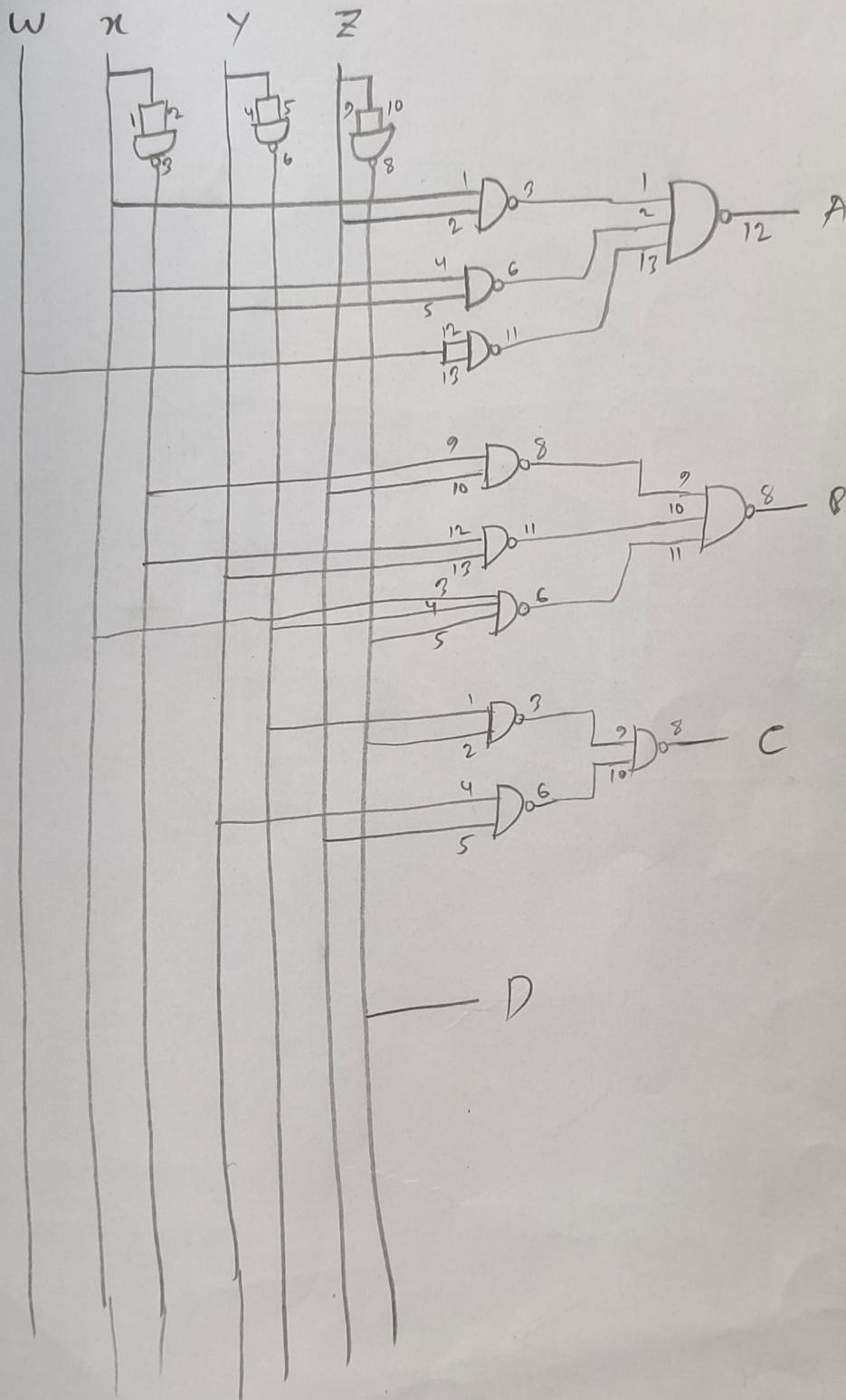


Figure F3: Minimal universal gate implementation of BCD to Excess-3 converter

Priyanka Dhar
13/03/23

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20/03/23
Bonus ↗ 2