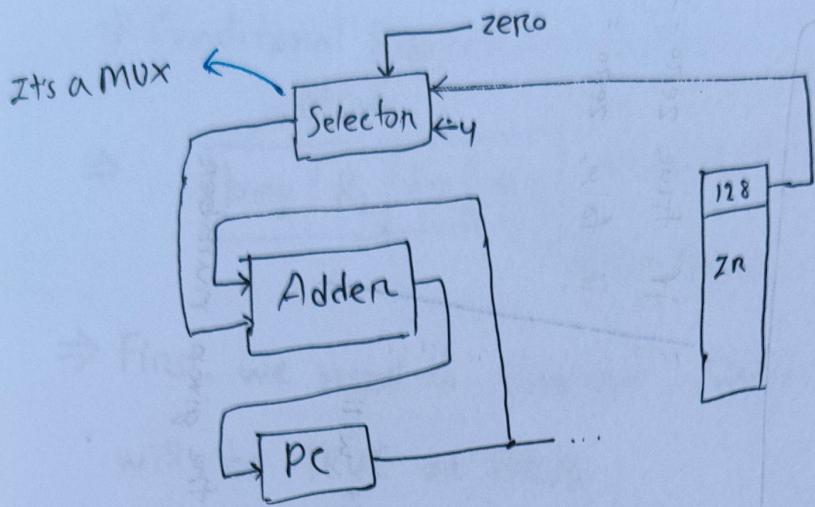


- ⊗ If condition is false, then there will be no action. Z<sub>t</sub> will execute next instruction.
- ⊗ When condition is True, PC will be updated by the given number
- And a few instruction will be skip.

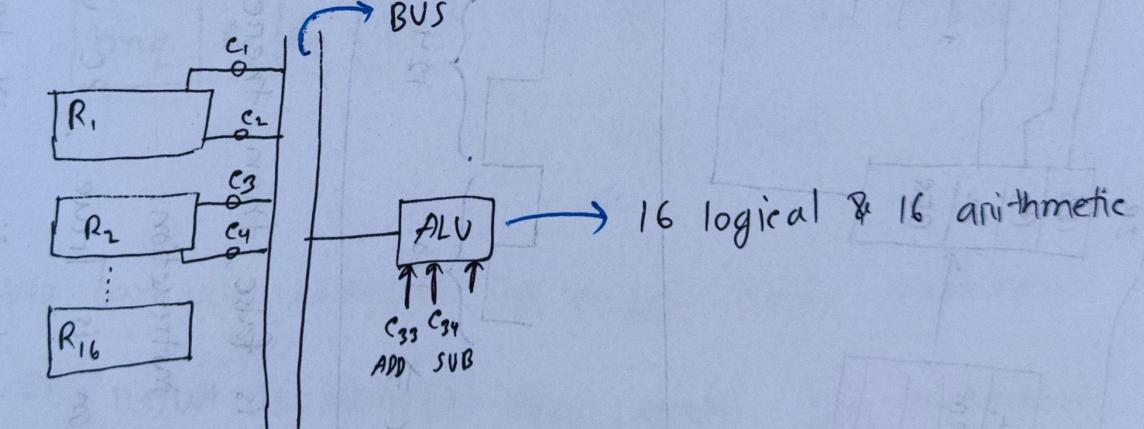
Alternative way: without AFerent ALU



Selection is MUX

L-22 / 09.10.2023

### Micro Programmed Control Unit



Left Right

26931-D  
26931-D  
26931-D

## Control Signal

## Micro Operation

c<sub>1</sub> → Transfer content of R<sub>1</sub> to Internal BUS

c<sub>2</sub> → " " " BUS to R<sub>1</sub>

c<sub>33</sub> → To select ADD operation

④ 128 Instruction, each instruction → a micro program.

⇒ Avg micro instruction is 8.

Each instruction =  $16 \times 2 + 16 + 16 + 2 + 20$

= 86 bit ⇒ in a single micro instruction

After Optimize ⇒  $10 + 5 + 1 + 20$   
= 36 bit

④ Micro Control memory =  $(128 \times 8 \times 36)$  bits

Write micro program for ADD R<sub>1</sub> R<sub>2</sub> M

⇒

1. Fetch:

- i. PC → Address (C<sub>67</sub>)
- ii. Read Control signal (C<sub>68</sub>)
- iii. Data BUS → Memory Data Register (C<sub>69</sub>)
- iv. Memory Data Register → Internal BUS (C<sub>70</sub>)
- v. Internal BUS → IR (C<sub>71</sub>)

Then, micro instruction will be

0 0 0 C<sub>71</sub> 0 0 0 ...  
0 0 0 C<sub>68</sub> 0 0 0 ...  
... 0 0 0 C<sub>69</sub> 0 0 0 ...

⇒ After optimize,  
step will be same,  
instruction bit will  
be reduce.

2. Decode:

- i. IR → CU

:

3. Register Read

⌚ Some Notes on todays picture,

⇒ in case of immediate mode the data may appear in any operand field.

⇒ Both operand field can't carry data at a single time.

L-23 / 11.10.2023

Midterm - Exam

L-24 / 16.10.2023

⌚ Pipeline Hazard

	1	2	3	4	5	6	7
I-1	IF	ID	ALU	MA	WR		
2		IF	ID	ALU	MA	WR	
3			IF	ID	ALU	MA	WR
4				IF	ID	ALU	MA
5					IF	ID	ALU
6						IF	ID
7							IF

**Seacal-D**

Calcium Carbonate (From Coral Source) and  
Vitamin D<sub>3</sub> (Colecalciferol)

**Seacal-DX**

Calcium Carbonate (From Coral Source)  
and Vitamin D<sub>3</sub> (Colecalciferol)

④ Instruction are independent

④ AVG CPI  $\approx 1$ ; Speed up  $\approx k$

④ If Instruction are not independent

⇒ Data Dependency

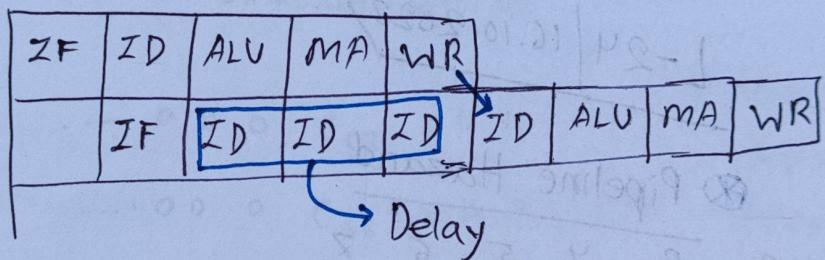
I-1: ADD R<sub>1</sub>, R<sub>2</sub> R<sub>3</sub>

I-2: SUB R<sub>4</sub> R<sub>3</sub> R<sub>5</sub>

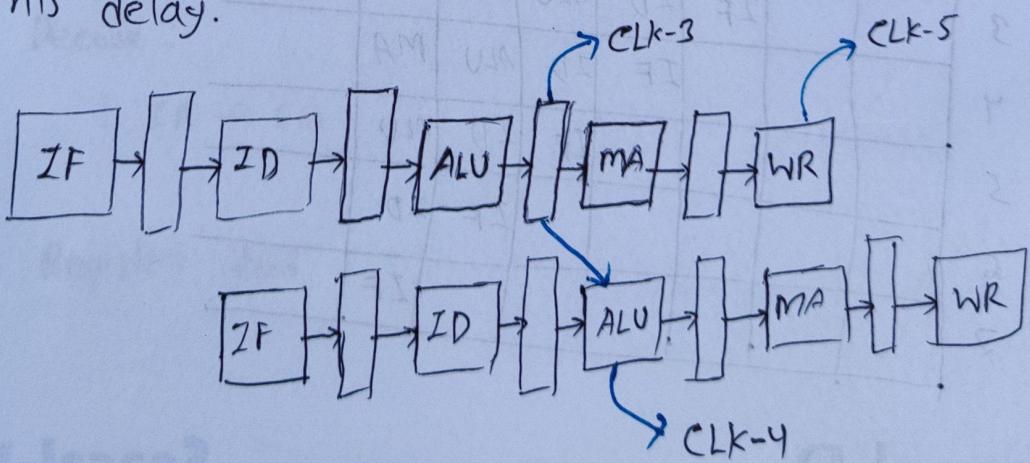
Result

Operand (Depends on 1<sup>st</sup> instruction)

Then,

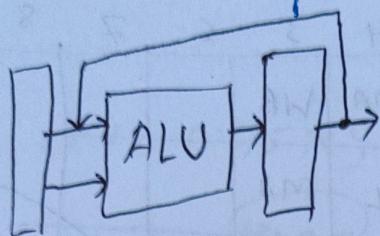


④ We need to redesign the Pipeline Path to reduce this delay.



We can easily transfer the result of ALU back to the ALU without any delay.

Modified Part only. known as forwarding



⊗ LOAD R<sub>1</sub>, R<sub>2</sub>(64) } Data dependency  
 SUB R<sub>2</sub> → R<sub>1</sub>, R<sub>3</sub>

1	2	3	4	5	6	7	8
ZF	ID	ALU	MA	WR			
IF	ID	ID	ID	ALU	MA	WR	

Delay, we need to reduce it.

Hence,

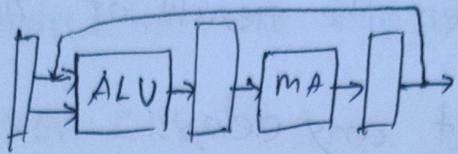
at CLK-4 ⇒ Data that need to store in R,  
 is available in MA buffer.

at CLK-3 ⇒ we need to read data.

we can transfer data from buffer to ALU

at CLK-4

we need to run ID. twtch.



## ⊗ Conditional Instruction:

	1	2	3	4	5	6	7	8
I-1	IF	ID	ALU	MA	WR			
2		IF	ID	AL	MA			
3			IF	ID	ALU			
4				IF	ID			
5					IF			
6								
7								
8								

Condition Evaluated

Must be Clean

Skip

Continue

Conditional Instruction  
True → 7  
False → Continue

L-24/

EISC

i i - - -

111

10.67 100%

Let,

$$\text{Total instruction} = \underline{100} + 75$$

$$\begin{aligned}\text{Average CPI} &= 0.75 \times 4 + 0.25 \times 5 \\ &= \underline{4.25}\end{aligned}$$

$$T = \frac{1}{f} = \frac{1}{4.25 \times 10^9} = \boxed{4.5 \text{ ns}}$$

$$\therefore \text{Single instruction processing time} = 4.25 \times 4.5 \\ = \boxed{19.125}$$

$$\begin{aligned}\text{Total} &= I \times \text{CPI} \times 4.5 \\ &= 100 \times 4.25 \times 4.5 = \boxed{1912.5 \text{ ns}}\end{aligned}$$

RISC

$$\text{Average CPI} = \underline{1.1}$$

$$\text{Single Time} = 4.5 \text{ ns}$$

$$\text{Total} = 175 \times 1 \times 4.5 = \boxed{787.5}$$

$$\text{Speed up} = \frac{1912.5}{787.5} =$$