Flag Register

ODITS Z'A'P'C

Parity ⇒

even = 1

odd = 0

Memory Address

CS ⇒ IP

SS ⇒ SP, BP

DS ⇒ Bx, DI, SI

ES ⇒ DI

Instruction List

↓PUSH Ax } SP

↑POP Cx

H, L

L, H

PUSHF | POPF

PUSHA | POPA

→ Ax, Cx, Dx, Bx, SP, BP, SI, DI

LEA Ax, variable name

LDS = Load Data Segment

LSS Bx, [SP]

LES

MOVSB/W/D/Q ⇒ SI, ~~DI~~

↳ Cx, D, REP

CLD = Clear D = 0

STD = Set D = 1

LODSB/W/D/Q ⇒ SI, AX

STOSB/W/D/Q ⇒ Ax, DI

INSB/W/D/Q ⇒ DI, Dx

OUTSB/W/D/Q ⇒ SI, Dx

XCHG = Exchange

XLAT ⇒ AL = [AL + Bx]

IN ⇒ AL, Dx

OUT ⇒ Dx, AL

CMP ⇒ Subtraction

$1000 = -2^3 = -8$

$\underbrace{-2^n \cdots 0 \cdots 2^n - 1}_{2^{n+1}}$

MUL / IMUL Bx

Dx-Ax = Ax · Bx

DIV / IDIV Bx

Ax = Dx-Ax / Bx

Dx = Remainder

CF/OF = 0, extend

1, not extend

CBW } for extend

CWD

ADD, ADC, INC

SUB, SBB, DEC

AND = Clear

OR = set

XOR = 1' compliment

= Clear

TEST = AND operation

- only Z flag

NOT = logical inversion

NEG = Arithmetic Inversion

BSF = Bit Scan Forward

→

BSR = Bit Scan Reverse

←

SHL Ax, 1

←

SHR

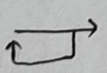
→

SAL ←

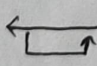
SAR

→

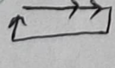
ROR Ax, 1



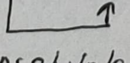
ROL



RCR



RCL



SCASB/W/D/Q ⇒ DI, Ax

CMPSB/W/D/Q ⇒ SI, DI

REPE / REPNE | D, Cx

Procedure

Name PROC NEAR/FAR

↑ Default

- - -

- - -

- - -

RET

name ENDP

MACRO

name MACRO Parameter

- - -

- - -

- - -

ENDM

Vector Table = 1KB

Interface

8086 vs. 8088

- Data Pin

- 34 & 28

- MAX{MIN}

→ BHE → M/IO

8284A ⇒ Clock generator

DC

input = 0·8 - 2·0

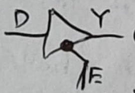
output = 0·45 - 2·4

TTL, output = 0·40 - 2·4

Noice = 0·8 - 0·45

74244 = one way buffer

74245 = Both way buffer

input  output

74373 = Latch

↳ D-flipflop + buffer

164 = shift register

Latch - 373

G = Clock = ALE

$\overline{OE}$ = fixed ground

Buffer - 245

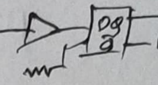
G = Data Enable = $\overline{DEN}$

DIR = DT/$\overline{R}$

Buffer - 244

$\overline{OE}$ = Output Enable

Reset-Block

$\overline{RES}$  RESET

Wait State Generator

RDY_1 = variable

$\overline{AEN_1}$ = 0

RDY_2 = 0

164 - SI = 1

$\overline{RD} = \overline{CS}$

ROM

$\overline{OE}$ = Output Enable

$\overline{CE}$ = Chip enable

RAM

$\overline{OE}$

$\overline{CE}$

$\overline{WE}$ = Write enable

Memory Bank

$A_{19} - A_1$ = Both

$D_{15} - D_8$ = Upper

$D_7 - D_0$ = Lower

$\overline{BHE}$ = upper

A_0 = Lower

Lower = even

upper = odd

74138 = MUX 8bit

139 = mux 4bit 2x

IC 138

CBA = Selection

G1 = 1

$\overline{G2A} = \overline{G2B} = 0$

RAM-Interface

- $\overline{OE} = \overline{MEMR}$ = All
- $\overline{WE} = \overline{MEMW}$ = All
- $\overline{CE}$ = OR ⇒ one = output of mux

another = $\overline{BHE}$ & A0

↓ upper ↓ Lower

EPROM-Interface

- $\overline{OE}$ =
- $\overline{CE}$ =

0 = even } Lower

1 = odd

2 = even } upper

3 = odd

$\overline{BHE}$ } odd EPROM

$\overline{MEMR}$

$\overline{MEMR}$ } even EPROM

A_0

$\overline{OE}$

$\overline{CE}$

↓

From mux

even = lower 8bit

odd = higher 8bit

PROM = OR } Programmable

PAL = AND

PLA = Both

DAC

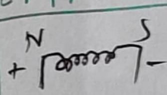
$I_T = \frac{V_{Ref}}{R \cdot 2^n}$ (total n num)

↙ in Binary multiply increasing

$V_0 = I_T \cdot R'$

$= \frac{V_{Ref} \cdot R'}{R \cdot 2^n}$ (+n)

Stepper Motor



ROL = Clock

ROR = Clock'

initial = 1100 1100

c c

PPI 8255A

$\overline{RD}$

$\overline{WR}$

A_1

A_0

Reset

$\overline{CS}$

Determine Address for port

Determine Control Word

0 = Reset

1 = set

$D_3 - D_1$ = for pin

1 = input

0 = output

Determined AND mask

Diagram Draw

8086 - Microprocessor

8088 - Microprocessor

244 - One way buffer

245 - two way buffer

373 - Latch

8284A - Clock Generator

164 - shift Register - Wait state diagram

139 - Mux 4 bit 2x

138 - Mux 8 bit

2732 - EPROM

62128 - RAM

AD558 - DAC (~~570~~)

16L8 - PLA

stepper Motor - Diagram

8255A - Pheripheral Device (Port Related)

8254 - Counter

Mode-0 = interrupt ⇒ Low - High

mode-1 = Retriggerable one shot (Handware ⇒ Low - High

Mode-2 = Continuous pulse ⇒ all high, last count low

Mode-3 = Square wave ⇒ half high - half low

Mode-4 = strobe ⇒ high - end one low

Mode-5 = strobe ⇒ just rising edge