Linh Nguyen

B04

ENCM 369 – Computer Organization

Lab 8

Ex. A) Part I

The critical path is from Q631:16 to the register R7, and the desired frequency for CLK is 3 GHz, therefore the desired period is Tc =

Part II

The short path is from Q631:16 to the register R7, which is just a 16-bit bus, therefore tcd = 0.

Ex C)

36.0 36.5 37.0 37.5 38.0 38.5 (ns)

lw $9, 20($8) | F | D | E | M | W |

or $10, $13, $11 | F | D | E | M | W

2. At t = 37.0 ns, it is at the end of the Fetch stage of the or instruction, so the PC gets 0x0040\_0138 which is the address of the NOP after or.

Just after t = 37.0 ns, InstrD gets the machine code for the or instruction: 0x01ab\_5025.

Just before t = 37.0 ns, RD1 and RD2 will have the source register values from the lw instruction; 0x1001\_0300 for RD1 and 0x0000\_0123 for RD2. The output of the Sign Extend will be the sign-extended offset of the lw instruction: 0x0000\_0018.

3. Just before t = 37.5 ns, RD1 and RD2 will have the source register values for the or instruction; 0x0000\_0025 for RD1 and 0x2233\_44c0 for RD2.

InstrD20:16 will have 010112 for $11 and InstrD15:11 will have 011012 for $13.

After t = 37.5 ns, the 32-bit ALU output is the sum of the offset and $8 from the lw instruction: 0x1001\_0318.

4. Just before t = 38.0 ns, the 32-bit ALU output is the OR of $11 and $13: 0x2233\_44e5.

WriteRegE4:0 is 010102, the destination register for the or instruction.

5. Just before t = 38.5 ns, ALUOutM is the OR result: 0x2233\_44e5 and WriteRegE4:0 is 010102 for the destination register for the OR instruction.

Ex D)

F

D

E

M

W

and $t0, $t1, $t2

F

D

E

M

W

add $s0, $s1, $t0

F

D

E

M

W

sw $t0, 12($sp)

F

D

E

M

W

lw $a0, 0($s0)

F

D

E

M

W

sub $t9, $s3, $s4

add $a1, $a0, $t9

F

D

E

M

W