Linh Nguyen

B04

ENCM 369 – Computer Organization

Lab 10

Ex. A)

|  |  |  |  |
| --- | --- | --- | --- |
| Address | Tag | Set | Action |
| 0x0040\_27b8 | 0x00402 | 494 | I-cache hit – no  I-cache update |
| 0x0040\_27bc | 0x00402 | 495 | I-cache miss – instruction 0x0240\_2021 is copied into instruction field in set 495, V-bit in that set is changed to 1, tag to 0x00402 |
| 0x0040\_27c0 | 0x00402 | 496 | I-cache miss – instruction 0x0c10\_0f50 is copied into instruction field in set 496, V-bit in that set is changed to 1, tag to 0x00402 |
| 0x0040\_17c0 | 0x00401 | 496 | I-cache miss – instruction 0x8c99\_0000 is copied into instruction field in set 496, V-bit in that set is changed to 1, tag to 0x00401 |
| 0x0040\_17c4 | 0x00401 | 497 | I-cache hit – no  I-cache update |
| 0x0040\_17c8 | 0x00401 | 498 | I-cache hit – no  I-cache update |
| 0x0040\_17cc | 0x00401 | 499 | I-cache hit – no  I-cache update |
| 0x0040\_27c4 | 0x00402 | 497 | I-cache miss – instruction 0x2652\_0004 is copied into instruction field in set 497, V-bit in that set is changed to 1, tag to 0x00402 |
| 0x0040\_27c8 | 0x00402 | 498 | I-cache miss – instruction 0x1653\_fffc is copied into instruction field in set 498, V-bit in that set is changed to 1, tag to 0x00402 |
| 0x0040\_27bc | 0x00402 | 495 | I-cache hit – no  I-cache update |
| 0x0040\_27c0 | 0x00402 | 496 | I-cache miss – instruction 0x0c10\_0f50 is copied into instruction field in set 496, V-bit in that set is changed to 1, tag to 0x00402 |
| 0x0040\_17c0 | 0x00401 | 496 | I-cache miss – instruction 0x8c99\_0000 is copied into instruction field in set 496, V-bit in that set is changed to 1, tag to 0x00401 |
| 0x0040\_17c4 | 0x00401 | 497 | I-cache miss – instruction 0x0019\_c023 is copied into instruction field in set 497, V-bit in that set is changed to 1, tag to 0x00401 |
| 0x0040\_17c8 | 0x00401 | 498 | I-cache miss – instruction 0xac98\_0000 is copied into instruction field in set 498, V-bit in that set is changed to 1, tag to 0x00401 |
| 0x0040\_17cc | 0x00401 | 499 | I-cache hit – no  I-cache update |
| 0x0040\_27c4 | 0x00402 | 497 | I-cache miss – instruction 0x2652\_0004 is copied into instruction field in set 497, V-bit in that set is changed to 1, tag to 0x00402 |
| 0x0040\_27c8 | 0x00402 | 498 | I-cache miss – instruction 0x1653\_fffc is copied into instruction field in set 498, V-bit in that set is changed to 1, tag to 0x00402 |
| 0x0040\_27cc | 0x00402 | 499 | I-cache miss – instruction 0x2414\_0000 is copied into instruction field in set 499, V-bit in that set is changed to 1, tag to 0x00402 |

Ex B)

Question 3:

31

15

14

5

4

2

1

0

17-bit search tag

10-bit set

3-bit block offset

2-bit byte offset



Each block has 1 V-bit, 17 tag bits, 8 data words x (32 bits/word) = 256 data bits

The total bits in each block is 1+17+256 = 274 bits/block and there are 1024 blocks.

Therefore, (274 bits/block) x (1024 blocks) = 280576 bits are needed for the whole cache.

Question 4:

0

2

43

16

15

6

5

3

28-bit search tag

10-bit set

3-bit block offset

3-bit byte offset

0

2

43

21

20

6

5

3

23-bit search tag

15-bit set

3-bit block offset

3-bit byte offset

1. Each block has 1 V-bit, 23 tag bits, 8 data words x (64 bits/word) = 512 data bits

The total bits in each block is 1+23+512 = 536 bits/block and there are 32,768 blocks.

Therefore, (536 bits/block) x (32,768 blocks) = 17,563,648 bits are needed for the whole cache.

Ex C) Part II

Output from heapsort\_trace.txt :

Linh Nguyen@Linh-the-Nguyen ~

$ ./sim2 < ENCM369/lab10/exC/heapsort\_trace.txt

64705 reads

57046 read hits

60419 writes

60387 write hits

overall miss rate: 6.1%

Output from mergesort\_trace.txt :

Linh Nguyen@Linh-the-Nguyen ~

$ ./sim2 < ENCM369/lab10/exC/mergesort\_trace.txt

104298 reads

99955 read hits

73410 writes

70863 write hits

overall miss rate: 3.9%

Comparing results from Part I and Part II:

Heapsort\_trace.txt:

Part I: overall miss rate: 11.9%

Part II: overall miss rate: 6.1%

mergesort\_trace.txt:

Part I: overall miss rate: 14.2%

Part II: overall miss rate: 3.9%

The cache with the four-word blocks (Part II) performs better than the cache with the single-word block (Part I), as it has a lower miss-rate even though both caches have the sae capacity of 4KB. The miss rate lowers as the block size increases from 1 word to 4, which suggests that both algorithms have significant special locality of reference in data access.

Part III

Output from heapsort\_trace.txt :

Linh Nguyen@Linh-the-Nguyen ~

$ ./sim3 < ENCM369/lab10/exC/heapsort\_trace.txt

64705 reads

64517 read hits

60419 writes

60419 write hits

overall miss rate: 0.2%

Output from mergesort\_trace.txt :

Linh Nguyen@Linh-the-Nguyen ~

$ ./sim3 < ENCM369/lab10/exC/mergesort\_trace.txt

104298 reads

103451 read hits

73410 writes

72945 write hits

overall miss rate: 0.7%