```
1 // Macros for message ASCII
   `define LF 10
 2
 3
   `define CR 13
   `define DOLLAR 36
 4
   `define COMMA 44
 6
   `define STAR 42
 7
 8
 9
   // Macro for message bits
   `define CHAR LENGTH 8
10
11
   // gpsdecode
12
13
   // -----
14 // Receives a NEMA message from the UART interface and decode it to signals
15
   // used by other modules
16 // Only cares about GPVTG message
   // Ready Valid& interface
17
18 //
19 // Inputs
20 // -----
21 // clk_i - Clock
22 // rst i - Reset
23 // [7:0] data i - ASCII char read from FIFO
24 // valid i - Input message is valid
25
   // ready_i - Next module is ready to receive data
26 //
27 // Outputs
28 // -----
29 //
30 // ready_o - Decoder is ready to receive a new message
31 // vkmh_o - Speed in km/h
32
33 // Example data from GPS
   // $GPVTG,0.00,T,,M,0.00,N,0.00,K,N*32\r\n
34
35
   //
   // TalkerID, course, Reference, Course, Reference, Speed, Unit (knot), Speed, Unit (km/h),
36
   Mode, Checksum, CR, LF
   // should get Speed before Unit (km/h)
37
38
39
   module gpsdecode(
40
41
       input [0:0] clk_i,
       input [0:0] rst i,
42
       input [7 :0] data i,
43
       // data from FIFO is valid
44
       input [0:0] valid_i,
45
       // next module is ready to receive data
46
       input [0:0] ready_i,
47
48
       // data is ready to be read
       output [0:0] ready o,
49
50
       output [0:0] valid_o,
       output [7:0] vkmh o
51
52 );
```

```
53
 54
 55
     logic [0:0] ready_r;
     logic [0:0] valid r;
 56
 57
     logic [7:0] vkmh_r;
 58
 59
     //
    // State machine
 60
 61
    //
    // 0 - Idle
                       // Wait for $
 62
     // 1 - MsgID
                       // Parse message ID, go to Continue if parsed as GPVTG. When msgidindex_r ==
 63
     3 and msgidmatch_r == 1, stay in msgID and go to field when msgidindex_r == 5. Else go to
    // 2 - Continue // Parse message until 7th comma
 64
     // 3 - Speed
                       // Parse Speed
 65
     // 4 - Done
                       // Done parsing speed, set valid_o to 1.
 66
 67
     typedef enum logic [2:0] {
 68
 69
         IDLE,
 70
         MSGID,
 71
         FIELD,
 72
         IGNORE,
 73
         DONE
 74
     } state_t;
 75
 76
     state t state r, state n;
 77
     logic [7:0] msgidindex_r;
 78
 79
     logic [7:0] commaindex r;
     logic [7:0] speedindex_r;
 80
 81
 82
     logic [0:0] msgidmatch_r;
 83
 84
      always_ff @(posedge clk_i) begin
 85
         if (rst_i) begin
 86
             state r <= IDLE;</pre>
 87
         end
 88
         else begin
 89
             state_r <= state_n;</pre>
 90
         end
 91
      end
 92
 93
      // state transitions
 94
 95
         always_comb begin
             if (rst_i) begin
 96
 97
                  state_n = IDLE;
 98
             end
 99
             else begin
100
                  case (state_r)
101
                      IDLE: begin
                          if (data i == "$") begin
102
                               state_n = MSGID;
103
104
                          end
105
                          else begin
106
                               state_n = IDLE;
107
                          end
```

```
108
                      end
109
                      MSGID: begin
                          if (msgidmatch_r == 1 && msgidindex_r == 5) begin
110
                               state n = FIELD;
111
112
                          end
                          else if (msgidmatch_r == 0 && msgidindex_r > 3) begin
113
114
                               state n = IGNORE;
115
                          end
116
                          else begin
117
                               state_n = MSGID;
118
                          end
119
                      end
120
                      FIELD: begin
121
                          if (speedindex_r == 3) begin
122
                               state n = DONE;
123
                          end
124
                          else begin
125
                               state n = FIELD;
126
                          end
127
                      end
                      IGNORE: begin
128
129
                          if (data_i == "$") begin
                               state n = MSGID;
130
131
                          end
132
                          else begin
133
                               state n = IGNORE;
134
                          end
135
                      end
136
                      DONE: begin
                          state_n = IDLE;
137
138
                      end
                      default : begin
139
                          state_n = IDLE;
140
141
                      end
142
143
144
                  endcase
145
             end
146
147
         end
148
149
150
     // msgindex logic
151
     // increment once whenever a new char is read (pulse of valid_i) when in msgid state
152
     always_ff @(posedge clk_i) begin
153
154
         if (rst_i) begin
155
             msgidindex_r <= 0;</pre>
156
         end
157
         else begin
158
             case (state_r)
159
                  IDLE: begin
160
                      msgidindex_r <= 0;</pre>
161
                 end
                 MSGID: begin
162
                      if (valid i) begin
163
```

```
164
                            msgidindex r \leftarrow msgidindex r + 1;
165
                        end
166
                        else begin
                            msgidindex_r <= msgidindex_r;</pre>
167
168
                        end
169
                   end
170
                   FIELD: begin
                        msgidindex_r <= 0;</pre>
171
172
                   end
                   IGNORE: begin
173
                        msgidindex_r <= 0;</pre>
174
175
                   end
176
                   DONE: begin
177
                        msgidindex_r <= 0;</pre>
178
                   end
179
                   default : begin
180
                        msgidindex_r <= 0;</pre>
181
                   end
182
               endcase
183
          end
184
     end
185
186
187
     // msgid match logic
188
     //
     // check at index 3 if the char is V
189
190
     // if it is, msgidmatch_r = 1
     // else msgidmatch_r = 0
191
192
193
     always_ff @(posedge clk_i) begin
194
          if (rst_i) begin
195
              msgidmatch_r <= 0;</pre>
196
          end
197
          else begin
198
               case (state_r)
199
                   IDLE: begin
200
                        msgidmatch_r <= 0;</pre>
201
                   end
202
                   MSGID: begin
203
                        if (msgidindex r == 3) begin
                            if (data i == "V") begin
204
205
                                 msgidmatch_r <= 1;</pre>
206
                            end
207
                            else begin
                                 msgidmatch_r <= msgidmatch_r;</pre>
208
209
                            end
210
                        end
211
                        else begin
212
                            msgidmatch_r <= msgidmatch_r;</pre>
213
                        end
214
                   end
215
                   FIELD: begin
216
                        msgidmatch_r <= 0;</pre>
217
                   end
                   IGNORE: begin
218
219
                        msgidmatch_r <= 0;</pre>
```

```
220
                   end
221
                   DONE: begin
222
                       msgidmatch_r <= 0;</pre>
223
                   end
                   default : begin
224
225
                       msgidmatch_r <= 0;</pre>
226
                   end
227
              endcase
          end
228
229
     end
230
231
232
233
234
235
236
     // commaindex logic
237
238
     always_ff @(posedge clk_i) begin
239
          if (rst_i) begin
240
              commaindex_r <= 0;</pre>
241
          end
242
          else begin
243
              case (state_r)
244
                   IDLE: begin
245
                       commaindex r <= ∅;
246
                   end
247
                   MSGID: begin
248
                       commaindex r <= ∅;
249
                   end
250
                   FIELD: begin
251
                       if (valid_i) begin
252
                       if (data_i == ",")
253
                       commaindex_r <= commaindex_r + 1;</pre>
254
                       end
255
                       else begin
256
                            commaindex_r <= commaindex_r;</pre>
257
                       end
258
                   end
259
                   IGNORE: begin
260
                        commaindex_r <= 0;</pre>
261
                   end
262
                   DONE: begin
263
                       commaindex_r <= 0;</pre>
264
                   end
                   default : begin
265
266
                       commaindex_r <= 0;</pre>
267
                   end
268
              endcase
269
          end
270
     end
271
272
273
     // speedindex logic
274
     always_ff @(posedge clk_i) begin
275
```

```
276
          if (rst i) begin
277
              speedindex r <= ∅;
278
          end
          else begin
279
280
              case (state_r)
                   IDLE: begin
281
                       speedindex_r <= 0;</pre>
282
283
                   end
284
                  MSGID: begin
285
                       speedindex_r <= 0;</pre>
286
                   end
287
                   FIELD: begin
288
                       if (valid_i) begin
                       if (commaindex_r == 7) begin
289
290
                            speedindex r \le speedindex r + 1;
291
                       end
292
                       end
293
                       else begin
294
                            speedindex_r <= speedindex_r;</pre>
295
                       end
296
                   end
297
                   IGNORE: begin
298
                       speedindex r <= 0;</pre>
299
                   end
300
                  DONE: begin
301
                       speedindex r <= 0;
302
                   end
                   default : begin
303
304
                       speedindex r <= ∅;
305
                   end
306
              endcase
307
          end
308
     end
309
310
     // speed logic
311
     logic [7:0] speed_r;
312
313
     always_ff @(posedge clk_i) begin
314
          if (rst_i) begin
315
              speed r <= 0;
316
          end
317
          else begin
              case (state_r)
318
319
                   IDLE: begin
                       speed_r \leftarrow 0;
320
321
                   end
322
                  MSGID: begin
323
                       speed_r <= 0;</pre>
324
                   end
325
                   FIELD: begin
326
                       if (valid_i) begin
327
                       if (commaindex_r == 7) begin
328
                            if (speedindex_r == 0) begin
329
                                case (data i)
                                "0" : speed_r <= 0;</pre>
330
                                "1" : speed_r <= 10;
331
```

```
"2" : speed_r <= 20;
332
                                "3" : speed_r <= 30;
333
                                "4" : speed_r <= 40;
334
                                "5" : speed_r <= 50;
335
                                "6" : speed_r <= 60;
336
                                "7" : speed_r <= 70;
337
338
                                "8": speed r <= 80;
                                "9" : speed_r <= 90;
339
340
                                default: speed r <= 0;</pre>
                                endcase
341
342
                           end
343
                           else if (speedindex r == 1) begin
344
                                case (data i)
345
                                "0" : speed_r <= speed_r + 0;</pre>
                                "1" : speed_r <= speed_r + 1;
346
                                "2" : speed r \le peed r + 2;
347
                                "3" : speed_r \leftarrow speed_r + 3;
348
                                "4": speed r \le speed r + 4;
349
                                "5" : speed_r <= speed_r + 5;
350
                                "6" : speed_r \leftarrow speed_r + 6;
351
                                "7" : speed_r <= speed_r + 7;
352
                                "8" : speed_r <= speed_r + 8;
353
                                "9" : speed_r <= speed_r + 9;</pre>
354
                                // this should handle empty msg
355
356
                                default: speed_r <= speed_r + 0;</pre>
357
                                endcase
358
                           end
359
                       end
360
                       end
                       else begin
361
362
                           speed_r <= speed_r;</pre>
363
                       end
364
                   end
365
                   IGNORE: begin
366
                       speed_r <= ∅;
367
                  end
368
                  DONE: begin
369
                       speed_r <= ∅;
370
                   end
371
                   default : begin
                       speed_r <= 0;</pre>
372
373
                   end
374
              endcase
375
         end
376
     end
377
378
379
380
381
     //
382
383
         always_ff @(posedge clk_i) begin
384
385
              if (rst_i) begin
386
                  ready r <= 0;
387
                  valid r \ll 0;
```

```
388
               end
389
               else begin
390
                   case (state_r)
                       IDLE: begin
391
392
                            ready_r <= 1;</pre>
393
                            valid_r <= 0;</pre>
394
                       end
395
                       MSGID: begin
396
                            ready_r <= 1;</pre>
397
                            valid_r <= 0;</pre>
398
                       end
399
                       FIELD: begin
400
                            if (speedindex_r == 3) begin
401
                            ready_r <= 0;
402
                            valid_r <= 1;</pre>
403
                            end
404
                            else begin
405
                            ready r <= 1;
406
                            valid_r <= 0;</pre>
407
                            end
408
                       end
409
                       IGNORE: begin
410
                            ready_r <= 1;</pre>
411
                            valid_r <= 0;</pre>
412
                       end
413
                       DONE: begin
                            ready_r <= 0;
414
415
                            valid_r <= 0;</pre>
416
                       end
417
                       default : begin
418
                            ready r <= 0;
419
                            valid_r <= 0;</pre>
420
                       end
421
                   endcase
422
              end
423
          end
424
425
          // outputs
426
427
          assign ready_o = ready_r;
428
429
          assign valid_o = valid_r;
          assign vkmh_r = speed_r;
430
431
          assign vkmh_o = vkmh_r;
432
433
434
435
     endmodule
```