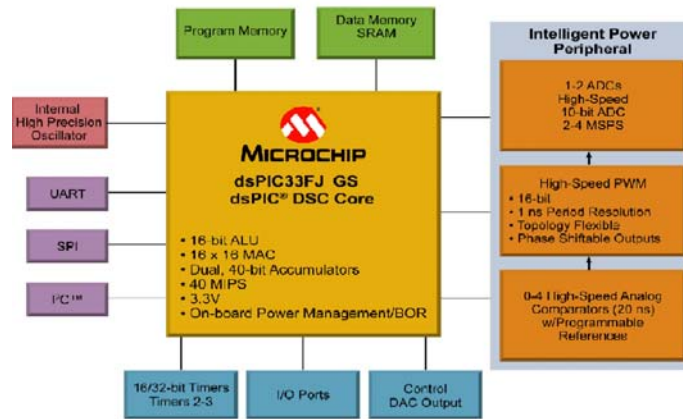


Introduction to the dsPIC® DSC SMPS (Part 2)

Welcome to part 2 of the Introduction to the SMPS dsPIC® DSC Web seminar, which covers the SMPS PWM module. My name is Alex Dumais and I am an Applications Engineer for Microchip.

dsPIC33F SMPS Family Block Diagram: Self-Contained SMPS Solution



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Introduction to dsPIC® DSC SMPS (part 2)

Slide 2

In part 1 of this two part Web Seminar, we covered the 10-bit high-speed ADC module and the high speed features of the SMPS dsPIC devices.

The processor, data ram, and program flash provide the zero wait state performance needed for SMPS applications.

In this Web Seminar, we will look at the high-Speed PWM module with 1 ns resolution. This family provides all of the expected microcontroller peripherals such as UART, SPI, I2C, timers, input capture, and output compares in addition to the SMPS peripherals.

The SMPS family incorporates a high accuracy (1%) internal RC oscillator that eliminates the need for an external crystal or oscillator for most applications.

The primary feature of this family are the SMPS peripherals: fast pwm with smps output modes, fast analog comparators, and a fast analog to digital converter with asynchronous input sampling capability.

Session Agenda

- **PWM modes and their applications**
- **PWM resolution**
- **External synchronization features**
- **Fault handling**

The agenda for this web seminar is:

- The PWM operating modes along with their typical usage
- The definition of resolution and why it is an important feature
- Presentation of the external features, including Fault handling and external synchronization

SMPS PWM Module

- **High resolution PWM: 1.04 ns resolution**
- **Up to 10 PWM modes of operation:**
 - Including Push-Pull, True Independent Output, and Center-Aligned
- **Individual dead-time values for each PWM:**
 - Positive and negative dead time
 - 1.04 nsec resolution
- **Extensive Fault handling capability**
- **Extensive ADC triggering options**

The primary feature of the SMPS PWM module is the very high resolution of 1 nsec. Most PWM modules designed for motor control typically have duty cycle resolutions between 10 to 25 nanoseconds.

Because SMPS applications have switching frequencies that are at least ten times that of motor control applications, the increase resolution is needed to minimize current ripple.

Motor control PWM modules are typically limited to generating complementary PWM outputs, and the PWM signals are either edge-aligned or center-aligned.

SMPS applications are more diverse, so the SMPS PWM module provides several different modes of operation.

The SMPS PWM module can provide unique dead-time values for each PWM output, and it has the capability to provide negative dead time.

Negative dead time is the forced overlap of the complementary PWM signals. This feature is required for some advanced SMPS designs.

To support the advanced sampling capabilities of the SMPS ADC, the SMPS PWM module provides ADC trigger generation logic for each PWM generator.

The SMPS PWM module has more sophisticated fault processing capability than what is found on motor control PWM modules.

What is PWM Resolution ?

!!!! High Resolution PWM is NOT a 16-bit PWM counter width !!!!

PWM Resolution = PWM Counter Frequency / PWM Output Frequency

Assume: PWM output frequency = 500 kHz

Example 1 : Let Counter frequency = 60 MHz

Therefore resolution = 1 part in 120 (about 7 bits)

Example 2 : Let Counter frequency = 1,000 MHz

Therefore resolution = 1 part in 2,000 (about 11 bits)

Many people are confused about the term “PWM Resolution”.

PWM resolution is NOT how wide a particular counter is, but it is how many counts (minimum possible pwm time slices) that can occur with a PWM cycle period. This resolution is usually specified in nanoseconds.

Another way to look at PWM resolution is to divide the PWM timebase counter frequency by the desired PWM output frequency.

Many typical PWM modules designed for motor control applications operate the PWM counter timebase at 60 MHz. If the desired pwm output frequency is 500 KHz, then the PWM resolution is 1 part in 120, or about 7 bits of resolution.

With the PWM counter operating at 60 MHz, the PWM's smallest time-slice is 16.6 nanoseconds.

If the timebase counter is operating at 1 GHz (1000 MHz), then the PWM resolution is about 11 bits when generating a 500 KHz PWM signal.



SMPS Applications Require High-Resolution PWM

If a PWM module cannot output a value that matches the Control Loop's calculated value, the control loop will dither between the two closest values to obtain the desired result.

Example:

The PWM can output values of 3 or 4, but the control loop needs 3.25.

The PWM will dither between the supported values to obtain desired result:

.... 3 3 3 4 3 3 3 4

This dithering is called "Limit Cycling" and causes ripple currents, and chaotic control loop behavior.

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Introduction to the dsPIC[®] DSC SMPS (part 2)

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If PWM modules do not have enough resolution, the control system (hardware or software) will dither the PWM outputs to achieve the desired average output.

In power supply applications, PWM dithering can create problems with ripple currents, and cause the control to enter a bad mode of operation called "Limit Cycling".

SMPS PWM Modes

- **Standard**
- **True Independent Output**
- **Complementary**
- **Redundant**
- **Center-Aligned**
- **Push-Pull**
- **Multi-Phase**
- **Variable Phase**
- **Current Reset**
- **Current Limit**

The SMPS PWM module provides a variety of PWM modes commonly used in SMPS applications:

STANDARD mode is the standard non-complementary output mode where one to two outputs provide the same PWM waveforms.

TRUE INDEPENDENT mode allows PWMxH and PWMxL to have different PWM periods as well as different duty cycles.

COMPLEMENTARY mode provides a PWM output signal on one pin, and the complement of the PWM signal is provided on the other output pin.

REDUNDANT mode provides the same PWMxH output signal to both PWMxH and PWMxL pins.

CENTER-ALIGNED mode provides a single PWM signal where half of the PWM period appears before a reference point, and the other half after the reference point.

PUSH-PULL mode provides a standard PWM signal on one output pin and then on the next cycle the PWM signal is outputted on the other pin, and then the process repeats.

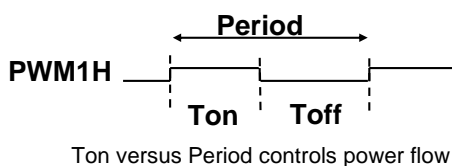
MULTI-PHASE mode allows multiple PWM generators to output PWM signals that are synchronized but phase shifted relative to each other.

VARIABLE PHASE mode is similar to MULTI-PHASE, but the phase relationships are constantly changing.

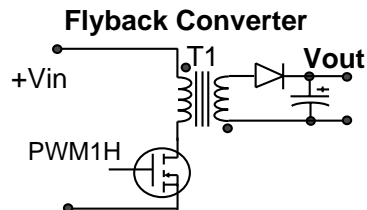
CURRENT RESET mode is a variable frequency mode where the user specifies an "ON" time, and an external signal or an internal analog comparator truncates the "OFF" time.

CURRENT LIMIT mode is a variation of STANDARD, COMPLEMENTARY, PUSH-PULL, MULTI-PHASE, and VARIABLE PHASE modes where an analog comparator or external signal truncates the PWM "ON" time on a

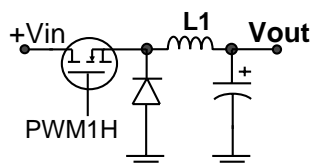
Buck, Boost, and Flyback Converters use Standard PWM



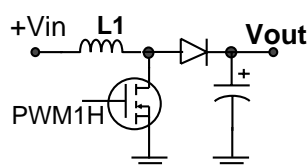
Ton versus Period controls power flow



Buck Converter



Boost Converter



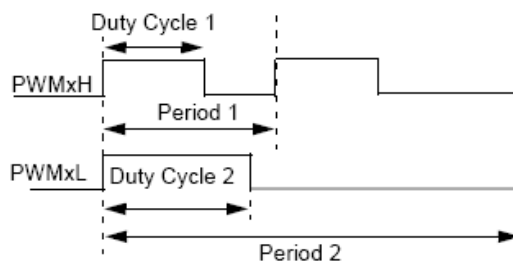
The STANDARD PWM mode is commonly used for asynchronously switched BUCK, BOOST, and Flyback converters.

This simple output mode requires only a single I/O pin, so it is useful in small package devices.

For Standard PWM mode, set the PMOD bits in the IOCONx register to use complementary, redundant, or true independent mode.

Set PENH bit in the IOCONx register to '1' to give the PWM module control of the PWMxH pin. PENL bit is set to '0' giving the GPIO ownership of that pin.

True Independent



- Independent time base mode (ITB = 1)
- Different duty cycles and periods between same PWM channel

In True Independent Output Mode, the PWM channel (PWMxH, PWMxL) can have different period values and different duty cycle values.

This provides two independent PWM signals.

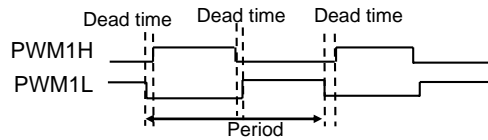
For True Independent Output Mode set the PMOD bits in the IOCONx register to '3'.

Set the ITB bit in the PWMCONx register to '1'.

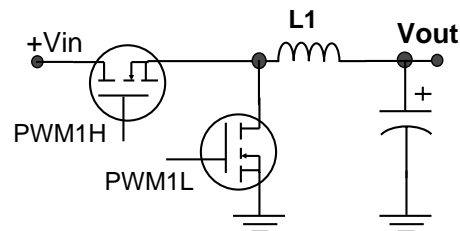
Configure the PHASEx/SPHASEx register and the PDCx and SDCx registers to the desired operating condition.

Set the PENH and PENL bits to '1' in the IOCONx register for PWM ownership.

Buck Converter with Synchronous Rectification Uses Complementary PWM Mode



Synchronous Buck Converter



COMPLEMENTARY PWM mode is typically used for synchronously switched BUCK converters.

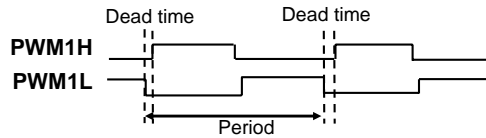
The complementary PWM output drives the synchronous rectifier (MOSFET).

Dead time is applied to eliminate shoot through.

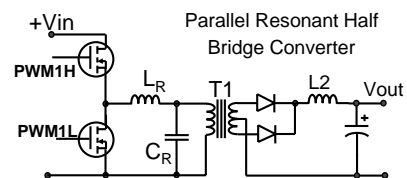
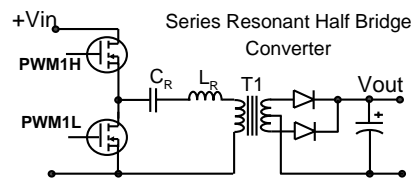
For Complementary mode, set the PMOD bits in the IOCONx register to '0';

Set PENH and PENL in the IOCONx register to '1' to give the PWM module control of the I/O pins.

Series and Parallel Resonant Half Converters Use Complementary PWM Mode



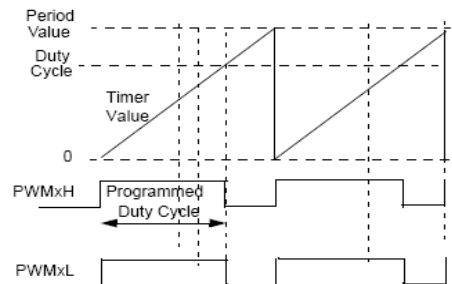
Note: This is 50% duty cycle Complementary mode PWM; the period (frequency) is varied to control power.



Note: C_R and L_R are the resonant elements

Resonant and Quasi-Resonant mode converters that are configured as Half-Bridge or Full-Bridge topologies typically use complementary output PWM mode.

Redundant



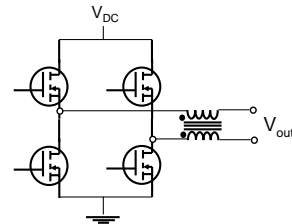
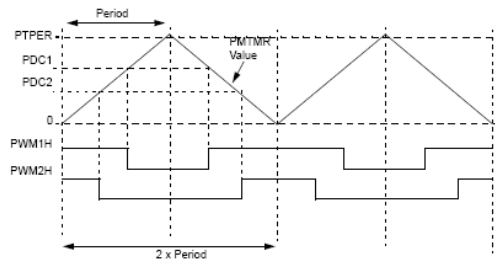
- **PWMxH signal an output for both PWM outputs (PWMxH and PWMxL)**

In Redundant output mode PWMxH and PWMxL are the same PWM signal (PWMxH).

To enable Redundant Output mode, set the PMOD bits in the IOCONx register to '1'.

Set PENH and PENL in the IOCONx register to '1' to give the PWM module control of the I/O pins.

Center-Aligned



Center-Aligned mode used for Inverters

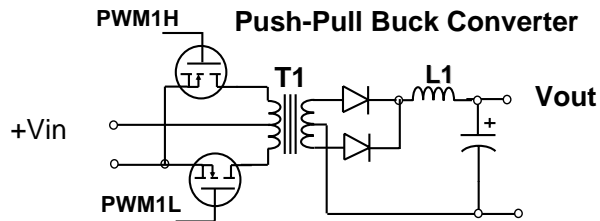
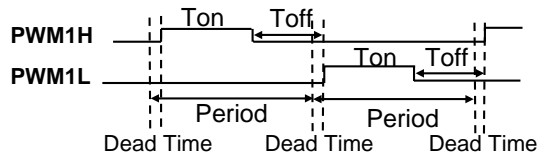
- CAM bit in PWMCON register set to '1'
- Independent Time Base mode (ITB = 1)

The Center-Aligned PWM waveforms align the PWM signals with respect to a reference point so that half of the PWM signal occurs before the reference point and the remaining half of the signal occurs after the reference point. Center-Aligned mode can be used with inverters to help reduce THD.

The Center-Aligned mode is enabled when the Center-Aligned Mode Enable (CAM) bit in the PWM Control (PWMCONx<2>) register is set.

When operating in Center-Aligned mode, the effective PWM period will be twice the value that is specified in the PHASEx registers because the independent time base counter in the PWM generator is counting up and then counting down during the cycle. The up/down count sequence doubles the effective PWM cycle period.

Push-Pull Converters Use Push-Pull PWM Mode



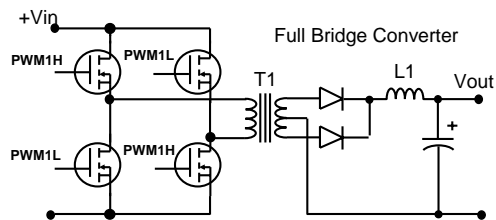
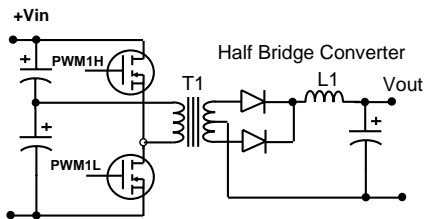
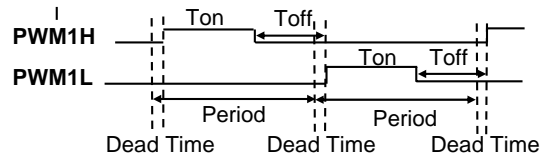
Push-Pull converters use Push-Pull mode!

In Push-Pull mode, the PWM outputs are alternately available on the PWMxH and PWMxL pins. For the first period, PWMxH is active and, in the next period, PWMxL is active.

For Push-Pull mode, set the PMOD bits in the IOCONx register to '2'.

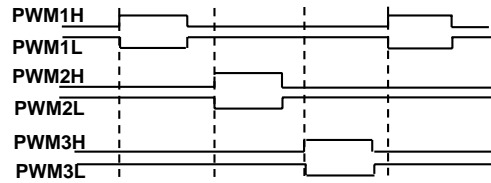
Set PENH and PENL in the IOCONx register to '1' to give the PWM module control of the I/O pins.

Half and Full Bridge Converters Use Push-Pull PWM Mode

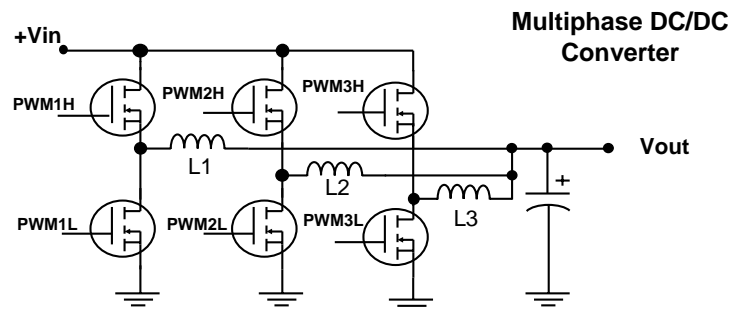


Both Half-Bridge and Full-Bridge converters can use Push-Pull Output mode.

Multi-Phase Converter Uses Multi-Phase PWM



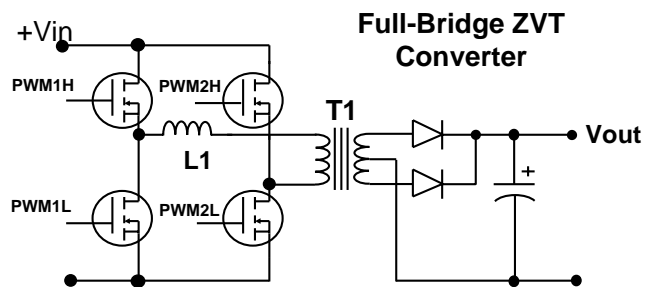
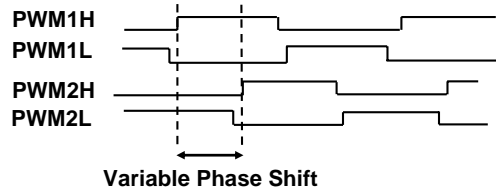
Note: Dead time not shown



The multi-phase converter is a set of buck converters parallel to each other but operating out of phase with each other. The phase offset is fixed by the circuit design.

Multi-phase converters may have two, three, four, or more phases. The phase offsets are setup to evenly distribute the phase shifts among the phases.

ZVT Converters Use Variable Phase PWM



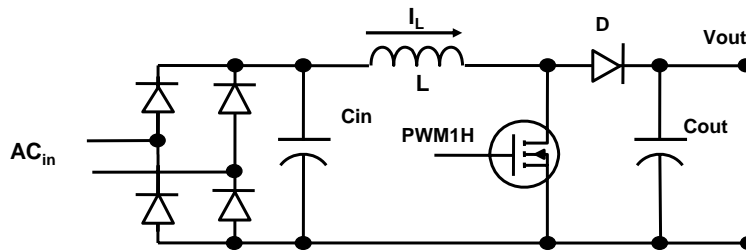
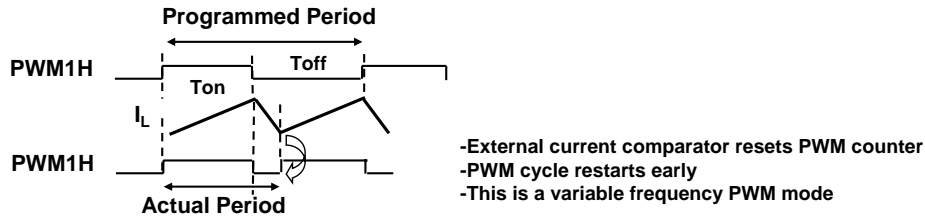
ZVT (Zero Voltage Transition) converters often use variable phase PWM.

Two PWM generators are used, and each PWM generator provides true and complement outputs.

The PWM duty cycle is usually set to 50%.

The power transfer control is obtained by varying the relative phase shift of the two PWM signals rather than varying the duty cycle.

Power Factor Correction Uses PWM Reset Mode



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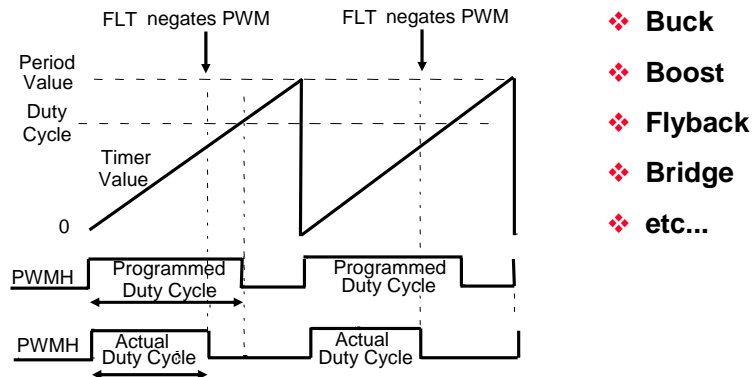
Slide 18

Some Power Factor Correction designs use PWM Reset mode where the PWM “off” time is truncated when an inductor current falls below a desired minimum.

A variation of the PWM reset mode that truncates the PWM “ON” time instead of the “OFF” time can be created by using the complementary output mode when the PWM Reset feature is enabled. The complementary output will provide the constant “OFF” time and variable “ON” time.

These modes are variable frequency modes.

Many Topologies Use Current Limit PWM Mode



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Many of the PWM modes can also use the cycle by cycle current limiting feature.

The current limit mode is typically used in a "Current Mode" control loop where the peak inductor current is monitored and limited.

Usually, an analog comparator monitors the inductor current and truncates the PWM "ON" time as input and output conditions change.

Using an analog comparator can greatly reduce the processor and ADC workload that otherwise would be encountered if the processor directly monitored peak inductor currents.

To be effective, the time from the peak current sensing occurs until the PWM signal is terminated (truncated) must be minimized.

The SMPS PWM and analog comparators have a delay from analog input to PWM output of 20 nanoseconds.



SMPS PWM Module External Synchronization Options

- The master PWM time base may be synchronized to external signals.
- The master PWM time base can generate an output signal to synchronize other devices.
- Multiple SMPS dsPIC® DSCs may be synchronized to control EMI issues in large systems.

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Introduction to the dsPIC® DSC SMPS (part 2)

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The SMPS dsPIC® DSC family features input and output synchronization capability.

The input synchronization feature enables an external signal to reset the master PWM time base. The time base reset function is edge sensitive (user selectable). The user programs the PERIOD register with a value slightly larger than the expected externally controlled period. If the SYNCI signal is not received due to noise or system failure, the PWM cycle will continue at the specified rate until new SYNCI signals are received.

The SYNCO output signal enables the dsPIC DSC to generate a pulse when the primary time base “rolls over” at the end of the specified PERIOD. The SYNCO signal may be used to synchronize other SMPS dsPIC DSCs or other control devices.

SMPS PWM Module Extensive Fault Handling Options

- Two independent Fault functions per PWM channel: Current Limit and Fault
- User selectable output states for Fault and current Limit
- Each PWM channel may select or share Fault pins
- Each PWM Fault input is configurable:
 - Latched or Cycle by Cycle
 - Digital or (Analog) Comparator
 - Polarity Selectable

The term “Fault” handling includes both cycle by cycle current limiting, as well as latching system fault conditions to shut down the PWM generation due to a fault in the end application (such as overload or short circuit).

Either the internal analog comparators or external circuitry may be used to control the operation of the PWM module.

Each PWM module has two “fault/current limit” inputs. These inputs may be shared among all of the PWM generators, or they can be independent.

Each fault/current limit input may be programmed for high or low active signal states.

The PWM outputs are user programmable in response to a current limit or a Fault input.



Key Support Documents

Microchip Web Sites: www.microchip.com/smcs
www.microchip.com/16-bit

For device data sheets, family reference manuals, and other related documents, please visit the following Microchip websites.

Thank You

Thank you for attending this Webinar

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