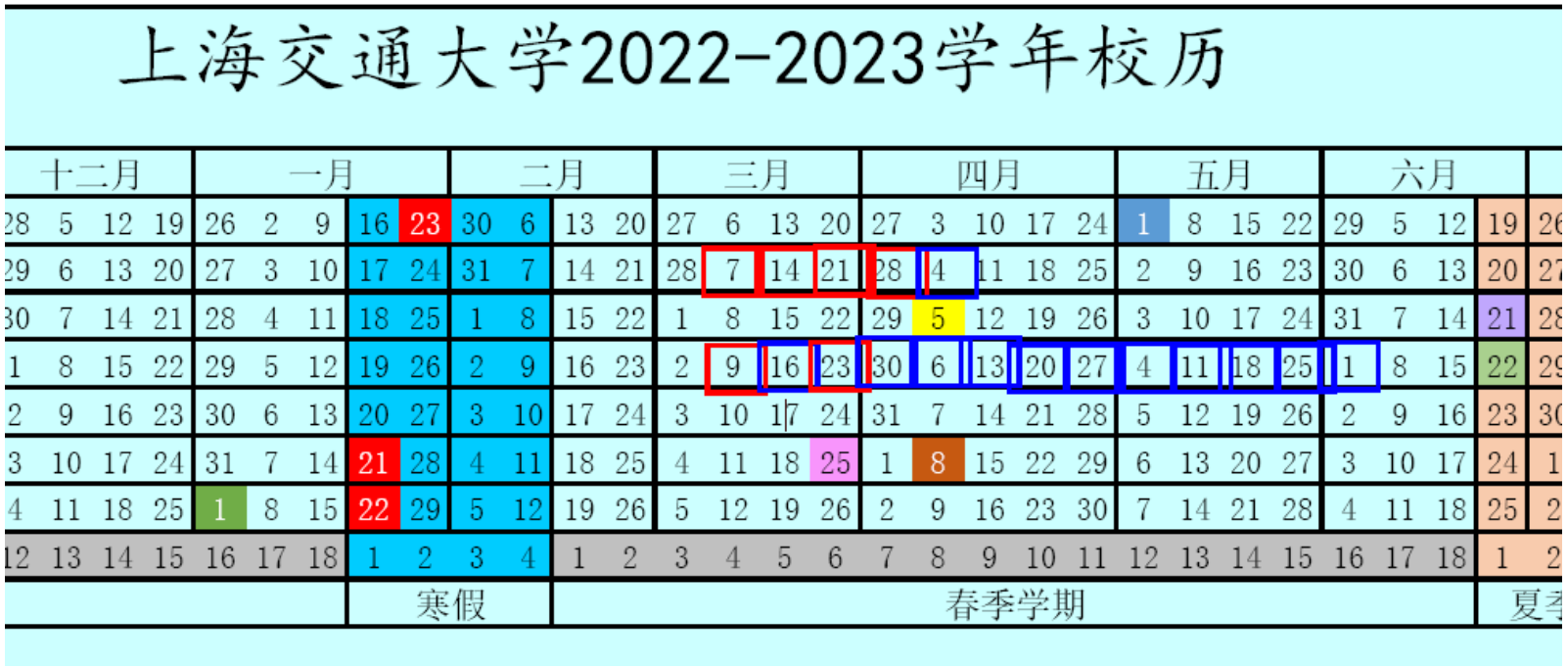
上海交通大学
Shanghai Jiao Tong University

Verilog HDL 硬件描述语言

上海交通大学微电子学院
蒋剑飞

教学安排



12学时上课+20学时实验

课题基本信息

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参考书

1）数字设计与Verilog实现，电子工业出版社，M.Morris Mano，第五 版中文)

2）Verilog HDL数字设计与综合（第二版），（美）Samir Palnitkar 著，电子工业出版社

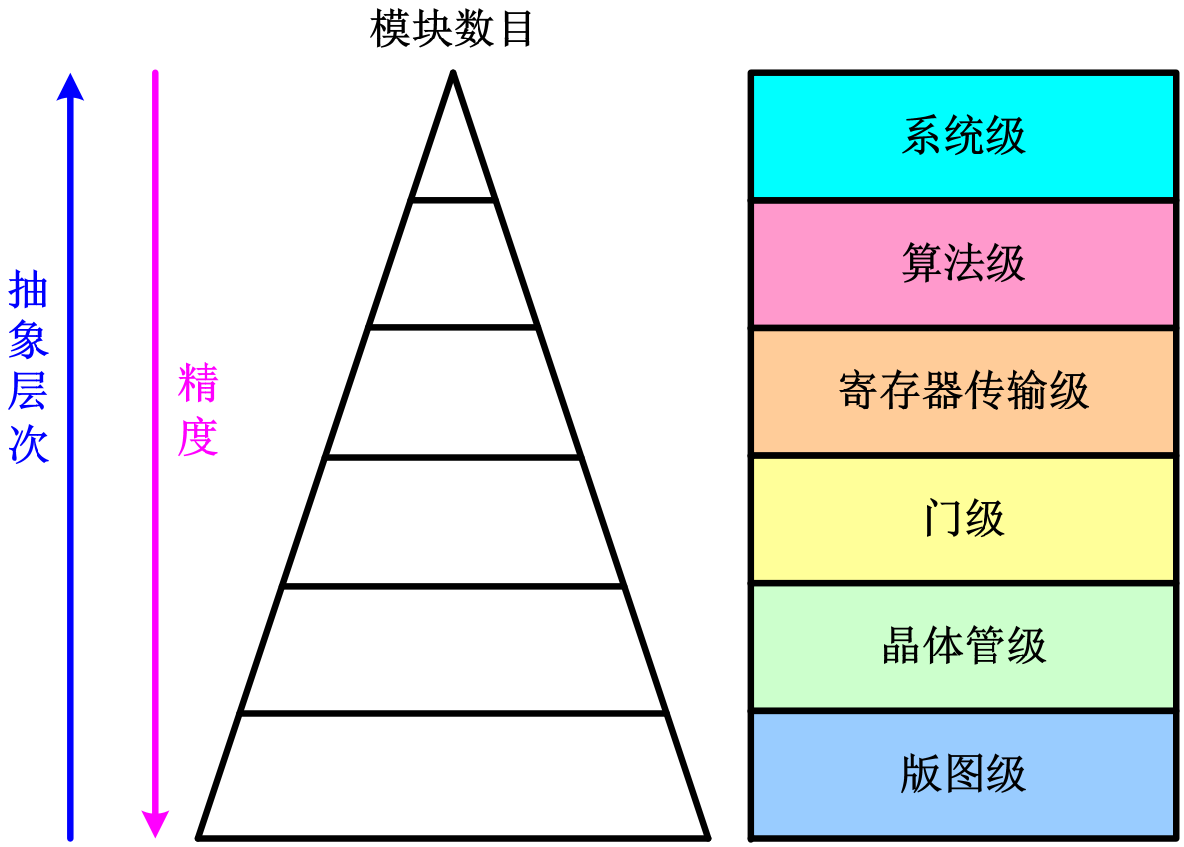
3)《Verilog HDL描述语言 A verilog HDL Primer》，J.Bhasker著/徐振林等译机械工业出版社，2000.7

4)《Verilog HDL高级数字设计 Advanced Digital Design with the Verilog HDL》，Michael D.Ciletti Prentice Hall/Perason翻译：张雅绮、李锵、电子工业出版社

数字集成电路发展

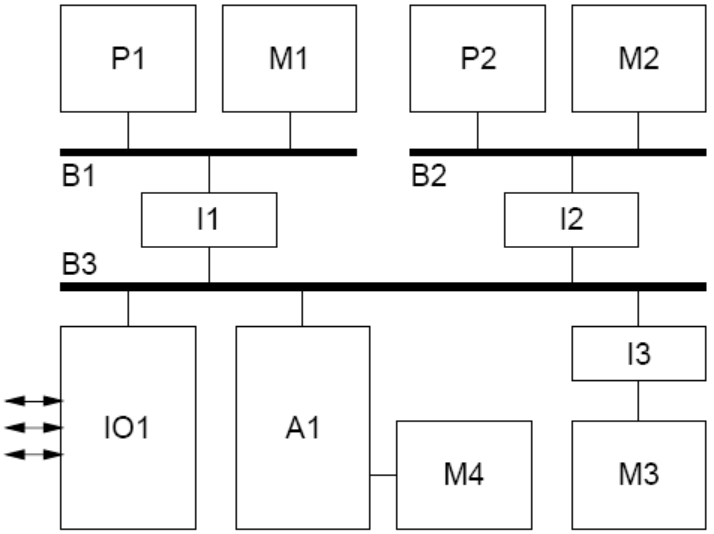
- SSI（Small Scale Integration， about 10^1）
- MSI（Medium scale Integration，about 10^2）
- LSI （Large Scale Integration，about 10^3 ）
- VLSI（Very Large scale Integration），ULSI (Ultra-large scale Integration， SOC (system on chip)，3D-IC $10^4 \sim 10^9$

电路抽象层次



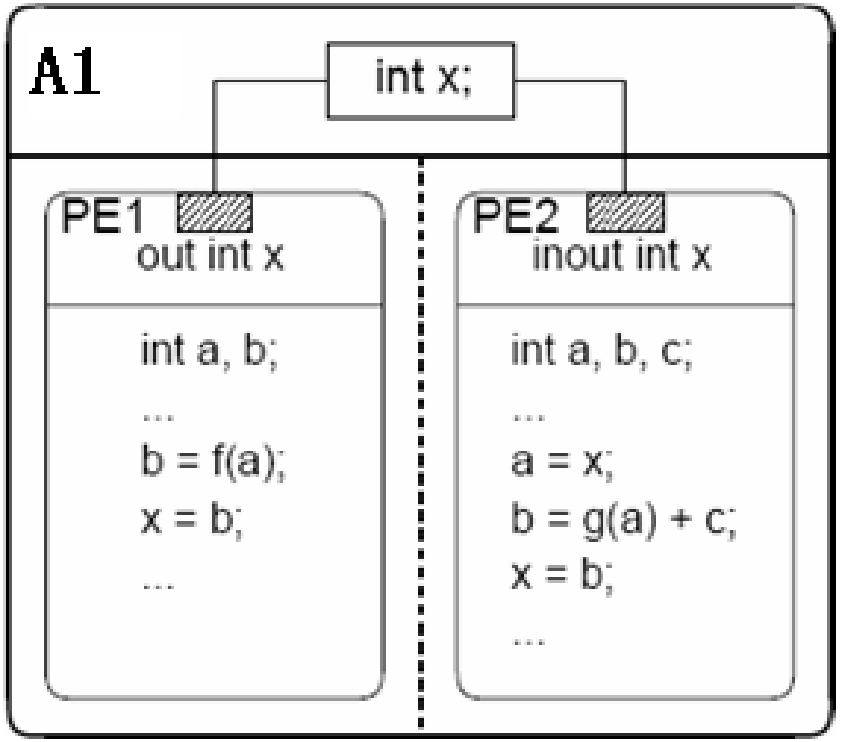
电路抽象层次——系统级

- 在系统级主要定义包括：
  主要实现的功能。
  主要部件、频率、总线带宽等性能指标。
  多采用文字、图、表等形式。
  在嵌入式领域系统级描述语言：
  如UML、SpecC、SystemC



电路抽象层次——算法级

- 实现功能模块的详细算法，多以C/C++或者其他语言实现。



电路抽象层次——寄存器传输级

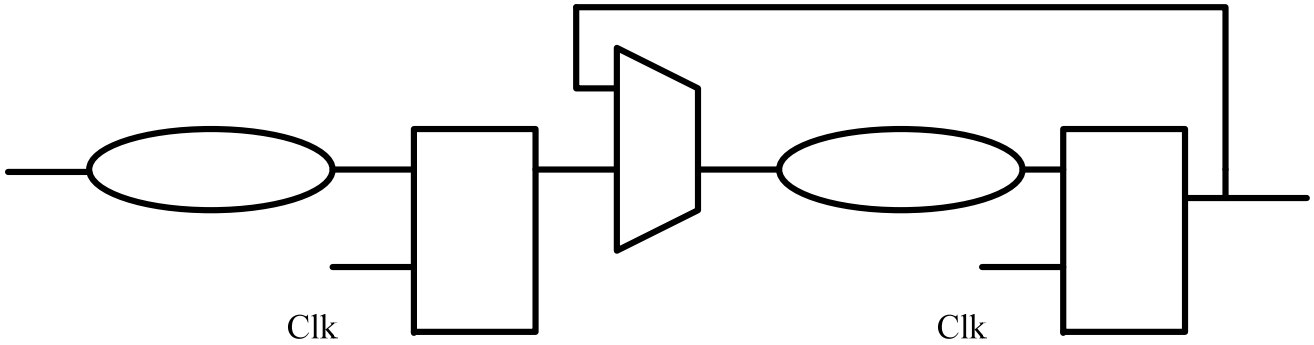
- 寄存器传输级描述这样一个抽象层次：
  在设计中，以时钟实现数据在时序单元（寄存器）之间的传递。

Always @(a or b or c)

c=a&b;

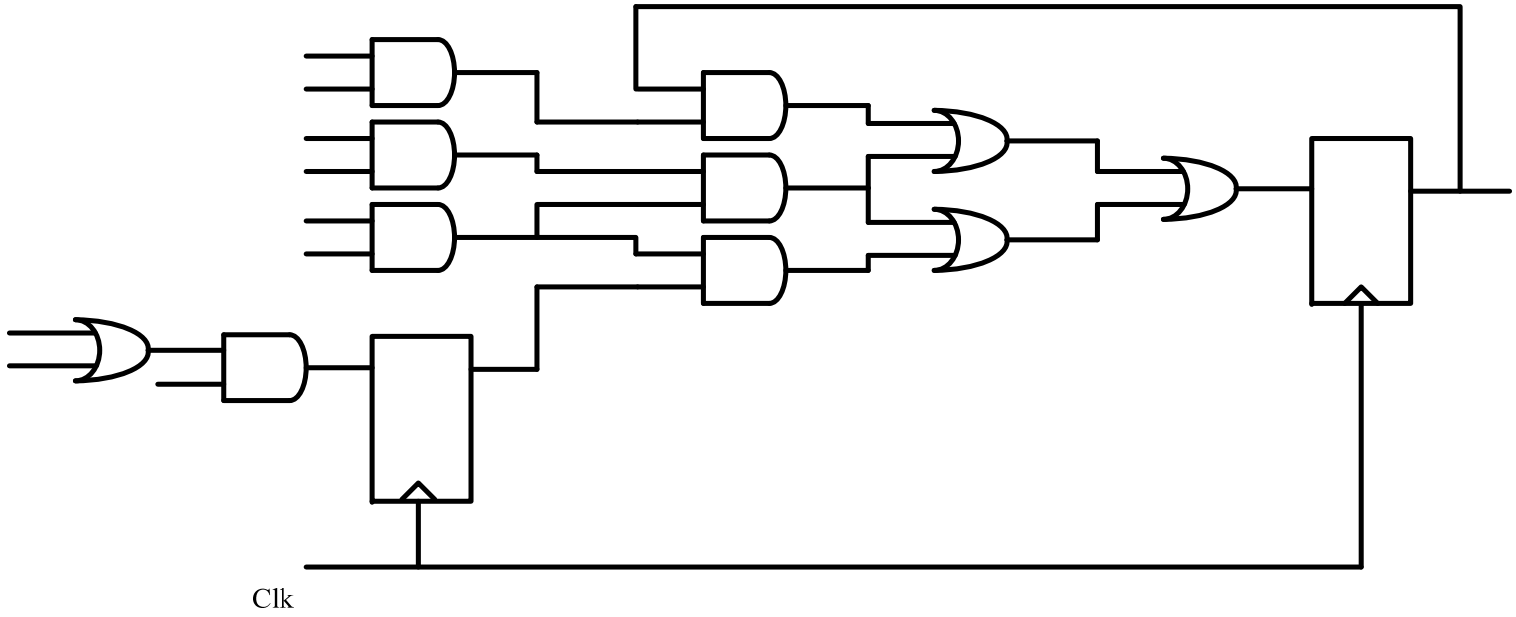
Always @(posedge clk)

q<=d;



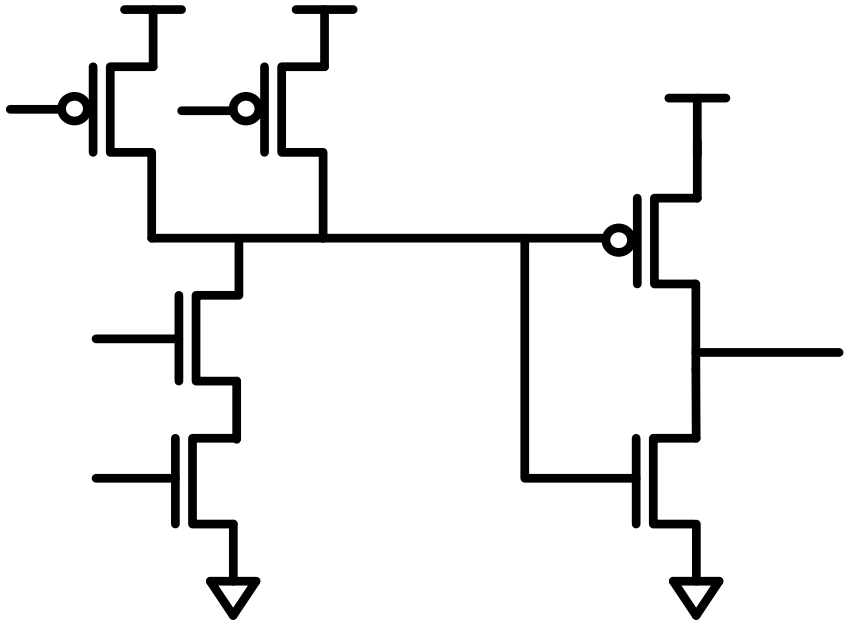
电路抽象层次——门级

- 门级模型：
  电路由基本的门单元来描述



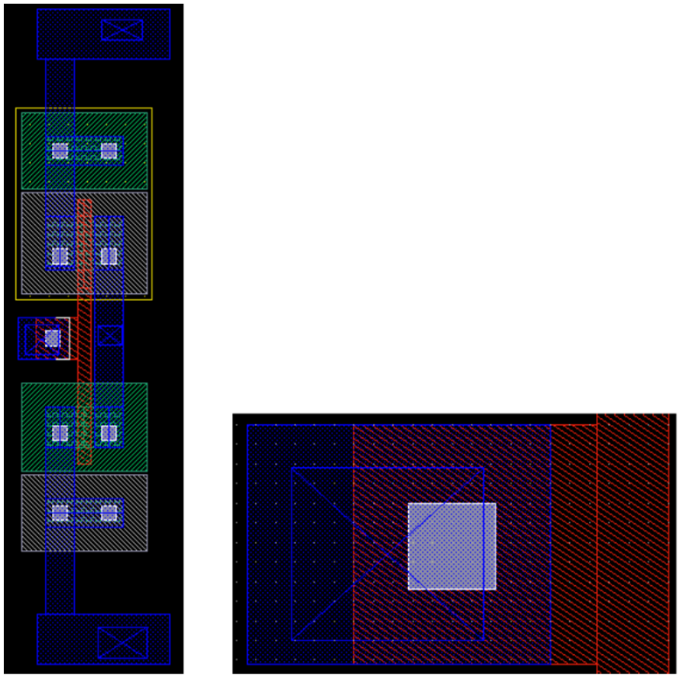
电路抽象层次——晶体管级

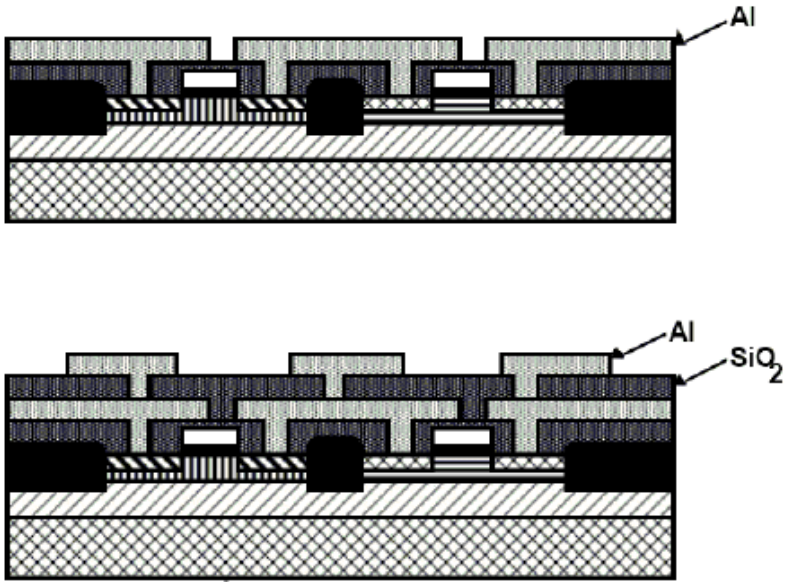
- 晶体管级抽象的精度高，是模拟电路领域的基本抽象层次



电路抽象层次——版图级

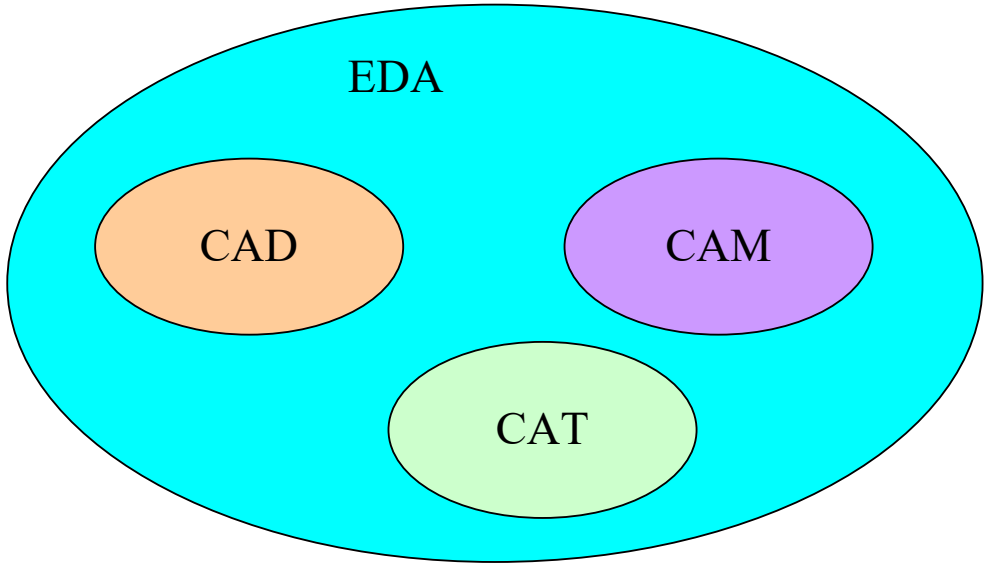
- 版图级：电路在硅片上的模型，以版图级的抽象描述（GDSⅡ），用于生产。





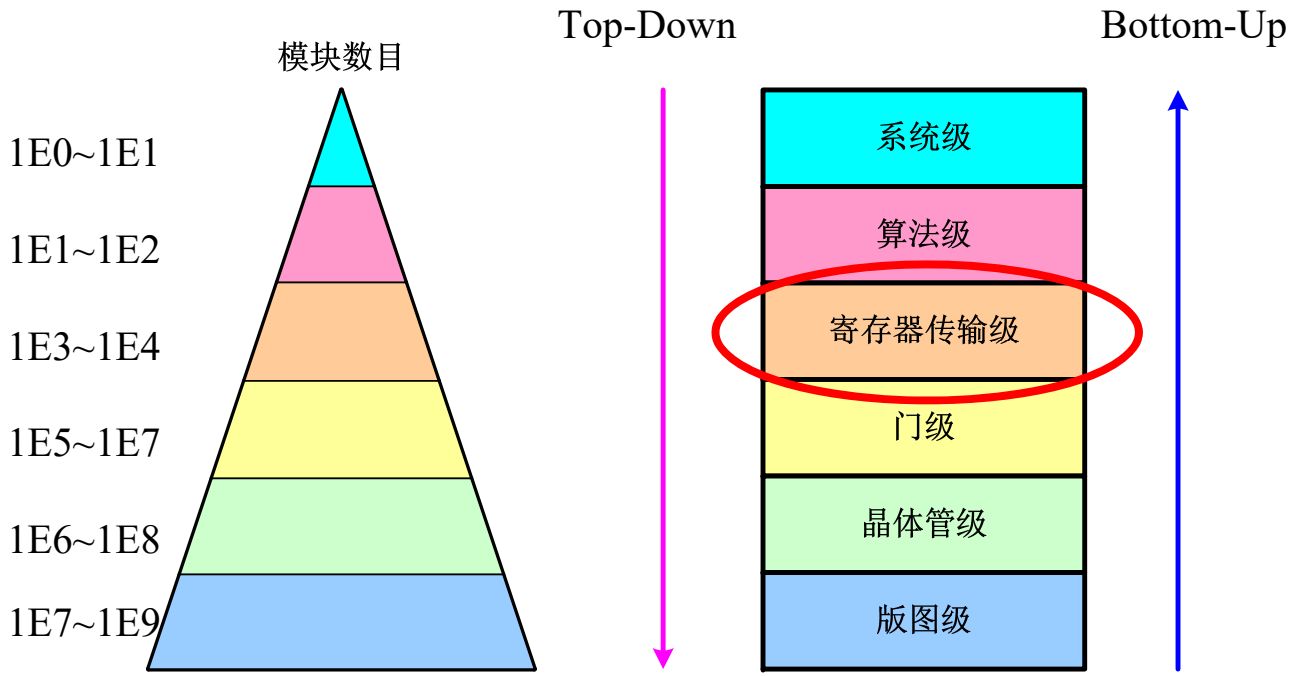
EDA在集成电路领域的应用

- EDA（Electronic Design Automation ）
  - CAD（Computer Aided Design)
  - CAM (Computer Aided Manufacture)
  - CAE（Computer Aided Testing)

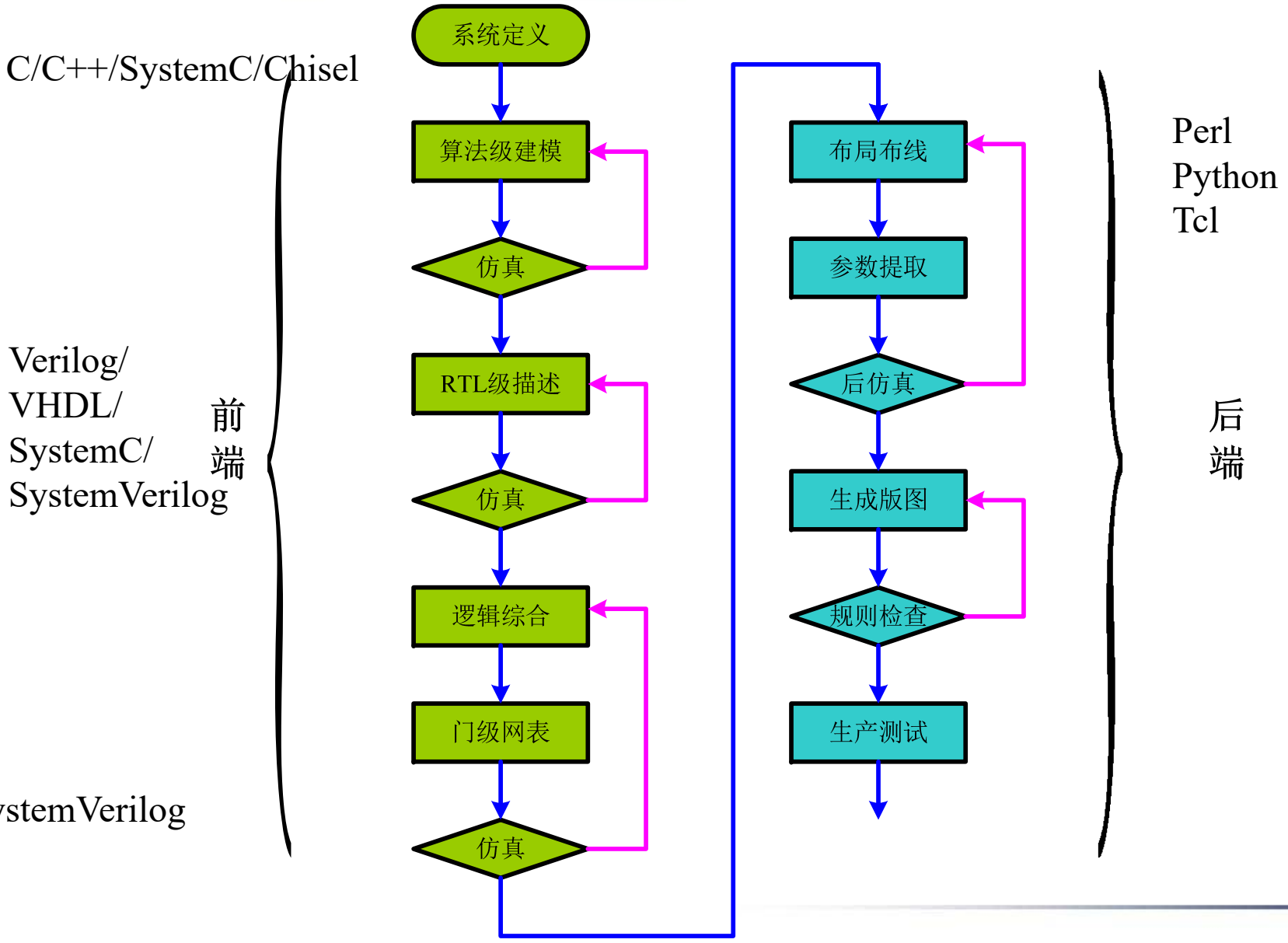


设计方法学

- EDA技术与设计方法学
  - 自顶向下（Top-Down)
  - 自下而上（Bottom-UP)



IC设计中的主要语言


C/C++/SystemC/Chisel
Verilog/
VHDL/
SystemC/
SystemVerilog
前端
SystemVerilog
系统定义
算法级建模
仿真
RTL级描述
仿真
逻辑综合
门级网表
仿真
布局布线
参数提取
后仿真
生成版图
规则检查
生产测试
Perl
Python
Tcl
后端

Languages

- Verilog
- VHDL
- SystemC
- SystemVerilog
- Other languages

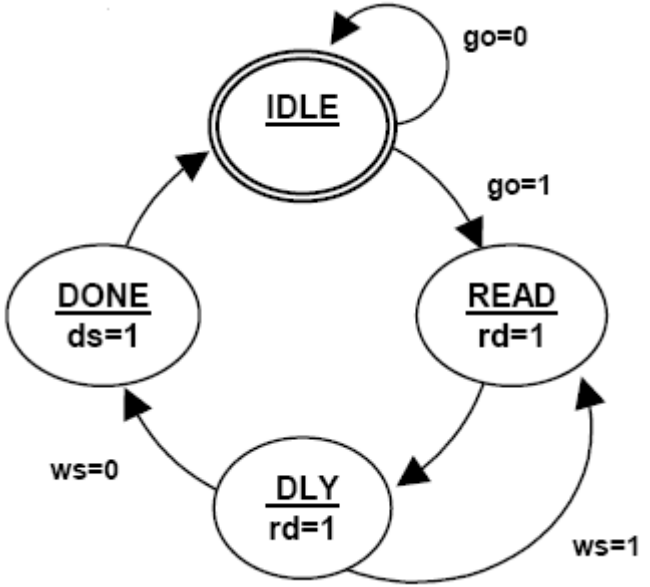
Verilog Hardware Description Language (HDL)

- 1985年在英国由Automated Integrated Design Systems（Gateway Design Automation，1990年被Cadence收购）公司发明，作为仿真语言。
- 1995年成为IEEE（Institute of Electrical and Electronics Engineers，美国电气及电子工程师学会）标准IEEE Standard 1364-1995 （Verilog-95）。
- Verilog-2001（ IEEE Standard 1364-2001）对于Verilog-95的扩展。
- Verilog-2005（ IEEE Standard 1364-2005）最后的Verilog标准。

基本语法

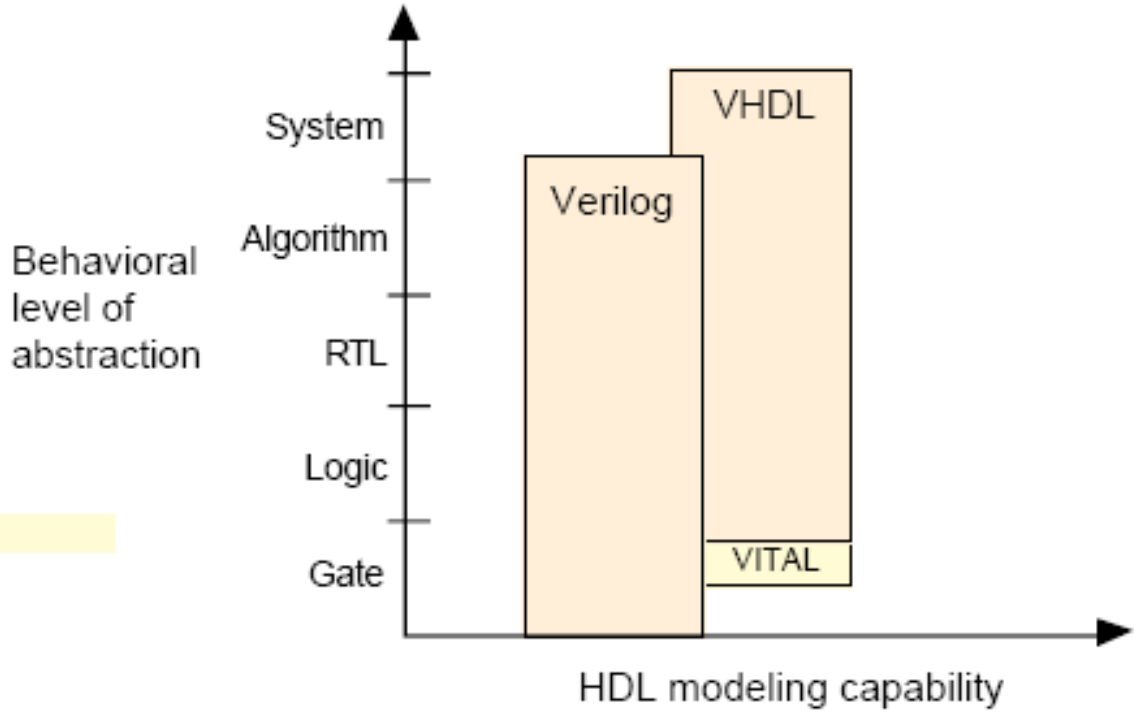
```
module fsm1a (ds, rd, go, ws, clk, rst_n);
output ds, rd;
input go, ws,clk, rst_n;
parameter [1:0]   IDLE = 2'b00,
 READ = 2'b01,DLY = 2'b10,DONE = 2'b11;
reg [1:0] state, next;
wire rd, ds;
always @(posedge clk or negedge rst_n)
if (!rst_n) state <= IDLE;
else        state <= next;
always @(state or go or ws) begin
case (state)
IDLE:     if (go) next = READ;
          else next = IDLE;
READ:   next = DLY;
DLY:      if (ws) next = READ;
          else next = DONE;
DONE: next = IDLE;
endcase    end
```

```
assign rd = (state==READ ||
state==DLY);
assign ds = (state==DONE);
endmodule
```



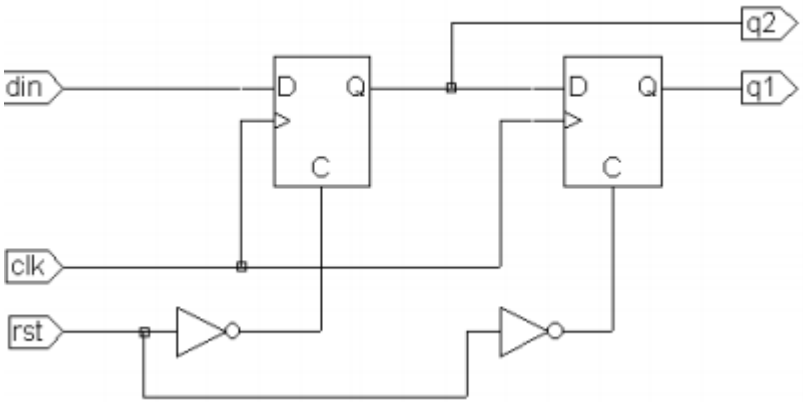
VHDL

- VHDL（VHSIC HDL），美国国防部发起，1987年成为IEEE标准，在欧洲被较多使用。（最新标准： IEEE 1076-2008）



基本语法

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL ;
ENTITY bfexp IS
 PORT(
 clk,rst,din : IN STD_LOGIC ;
 q1 : BUFFER STD_LOGIC ;
 q2 : OUT STD_LOGIC ) ;
END bfexp ;
ARCHITECTURE behav1 OF bfexp IS
 BEGIN
PROCESS(clk, rst)
 BEGIN
 IF rst ='0' THEN
 q1 <= '0' ;
 q2 <= '0' ;
 ELSIF clk'EVENT AND clk = '1' THEN
 q1 <= din ;
 q2 <= q1 ;
 END IF;
 END PROCESS;
 END;
```



HW Design Languages

- **H**ardware **D**escription **L**anguage (HDL) is used to describe digital hardware elements
- Various levels of design abstractions are used:
  - **Behavioral**: flow control, arithmetic operators, complex delays
  - **Register Transfer Level** (RTL): Structural description of the registers and the signal changes between registers
  - **Gate level**: combinatorial logic gates (and, or, not,…)
  - **Switch level**: layout description of the wires, resistors and transistors (CMOS,PMOS, etc)
- Two main subsets:
  - Synthesizable – reflecting HW / Silicon
  - Non-Synthesizable – reflecting *instrumentation* code

SystemC

- 在C++ 基础上增加库面向系统级设计，面向对象设计
- 2005年12月IEEE批准了IEEE 1666™ -2005作为SystemC的国际标准。为了鼓励使用这个标准，OSCI通过和IEEE标准组织协商，目前该标准的文档可以免费下载。
- 最新标准IEEE 1666-2011

SystemC简介

- SystemC是一种基于C++的系统设计语言。在SystemC以前，C和C++是芯片架构设计的主要语言
- 在SoC设计中需要集成各种IP和嵌入式软件，C++具有的面向对象的设计观念因此很适合作为SoC系统的开发语言
- SystemC在C++语言的基础上增加了信号、事件等概念用来描述硬件，而且还可以支持定时、并发等概念
- SystemC可以让系统、硬件和软件工程师使用相同的语言完成整个电子系统的全部建模过程，这样做能够在软硬件划分和缩短产品的上市时间带来帮助。
- SystemC通过定义了新的C++类库和仿真核，用以支持硬件的建模和仿真。

Chisel

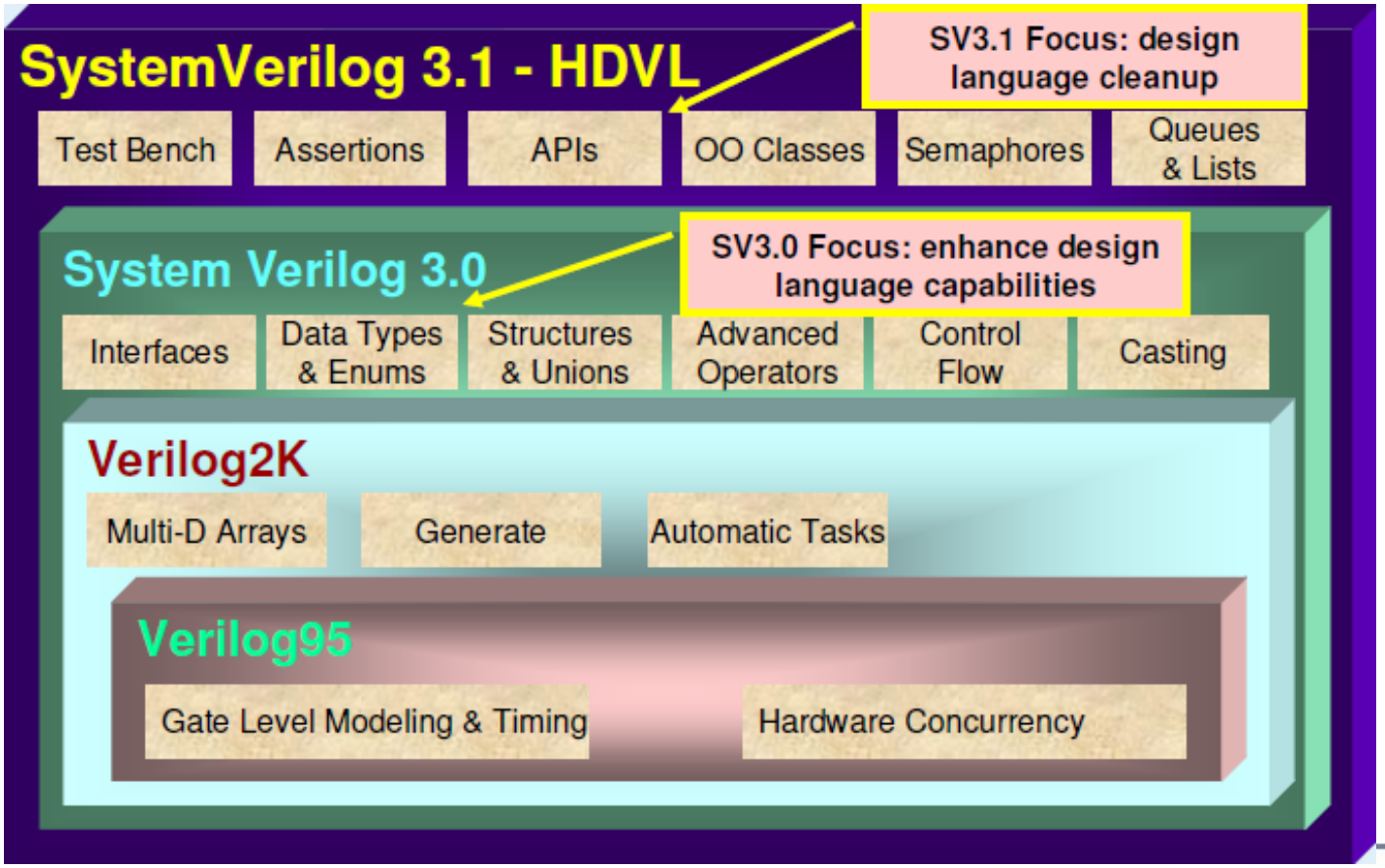
- Constructing Hardware in a Scala Embedded Language(CHISEL)
- Developed at UC Berkeley
- Generates low-level Verilog designed to pass on to standard ASIC or FPGA tools
- With RISC-V

Chisel举例

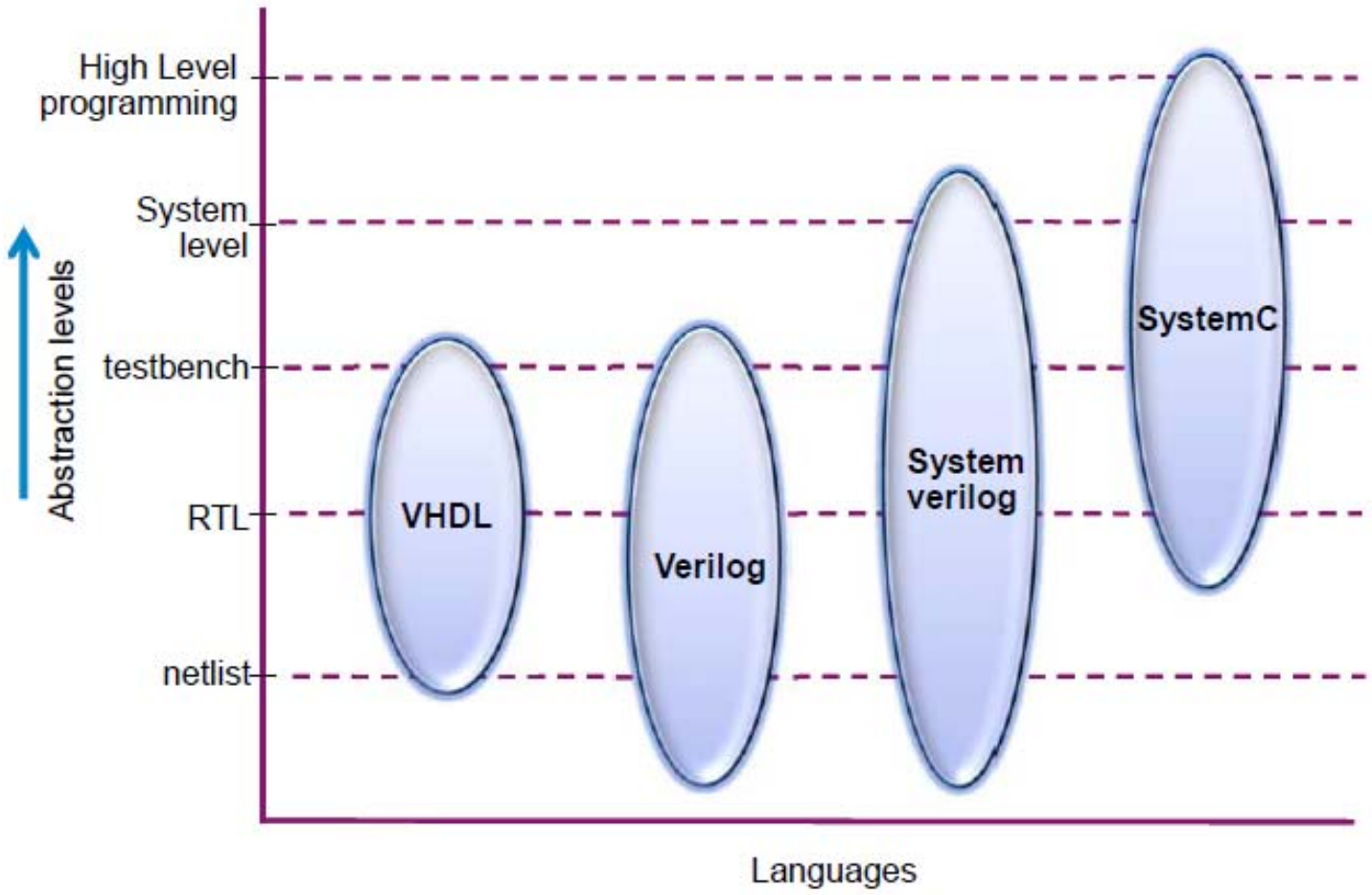
```
class Mux4 extends Component {
  val io = new Bundle {
    val in0 = Bits(1, INPUT)
    val in1 = Bits(1, INPUT)
    val in2 = Bits(1, INPUT)
    val in3 = Bits(1, INPUT)
    val sel = Bits(2, INPUT)
    val out = Bits(1, OUTPUT)
  }
  val m0 = new Mux2()
  m0.io.sel := io.sel(0)
  m0.io.in0 := io.in0; m0.io.in1 := io.in1

  val m1 = new Mux2()
  m1.io.sel := io.sel(0)
  m1.io.in0 := io.in2; m1.io.in1 := io.in3

  val m3 = new Mux2()
  m3.io.sel := io.sel(1)
  m3.io.in0 := m0.io.out; m3.io.in1 := m1.io.out

  io.out := m3.io.out
}
```

SystemVerilog

- SystemVerilog 3.0/3.1 (extension from Verilog 2K)
- SystemVerilog 2005/2009/2012 (IEEE 1800™)



ABSTRACT LEVELS OF HDL / HVL



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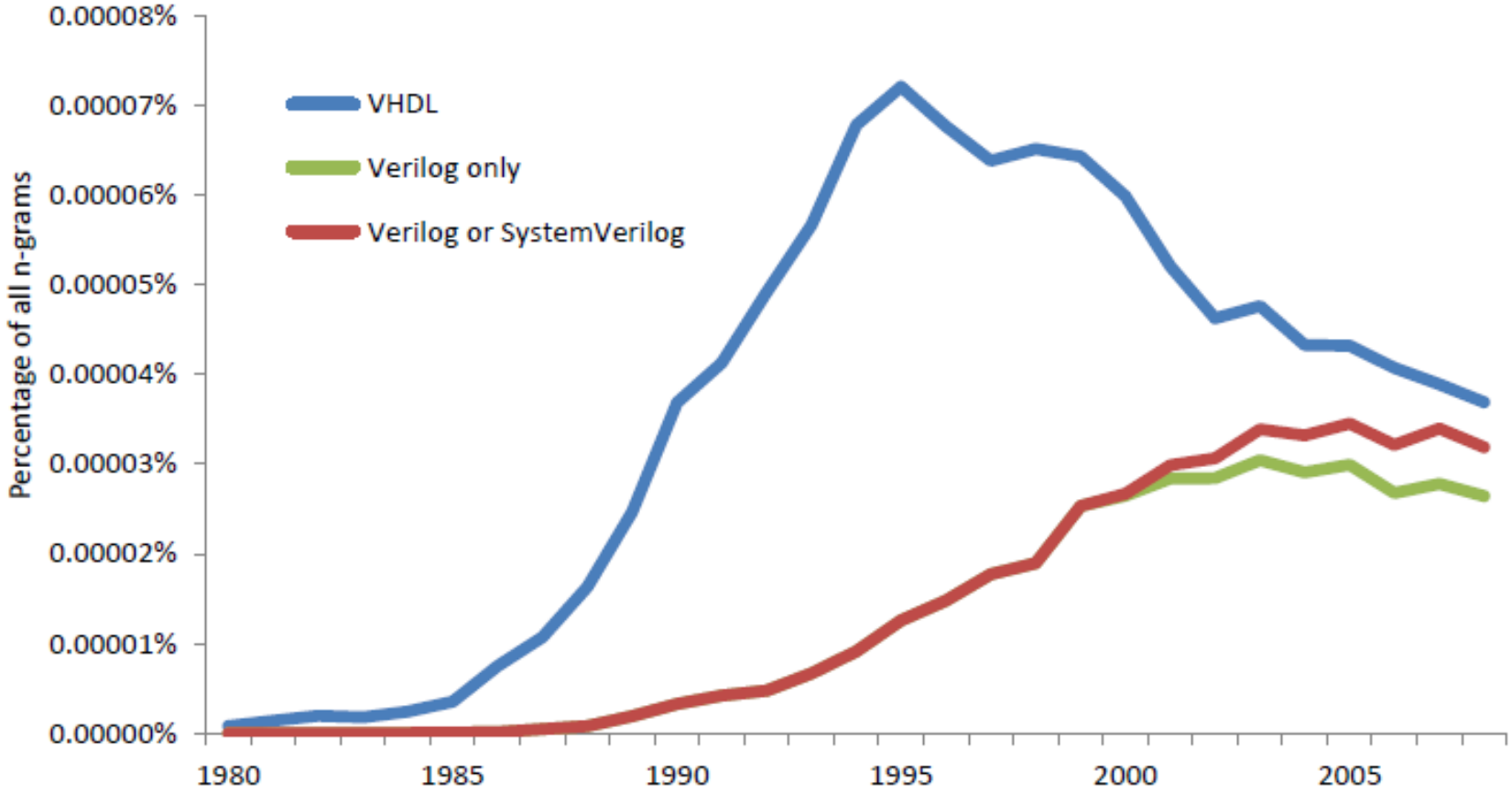
IEEE ranked sales

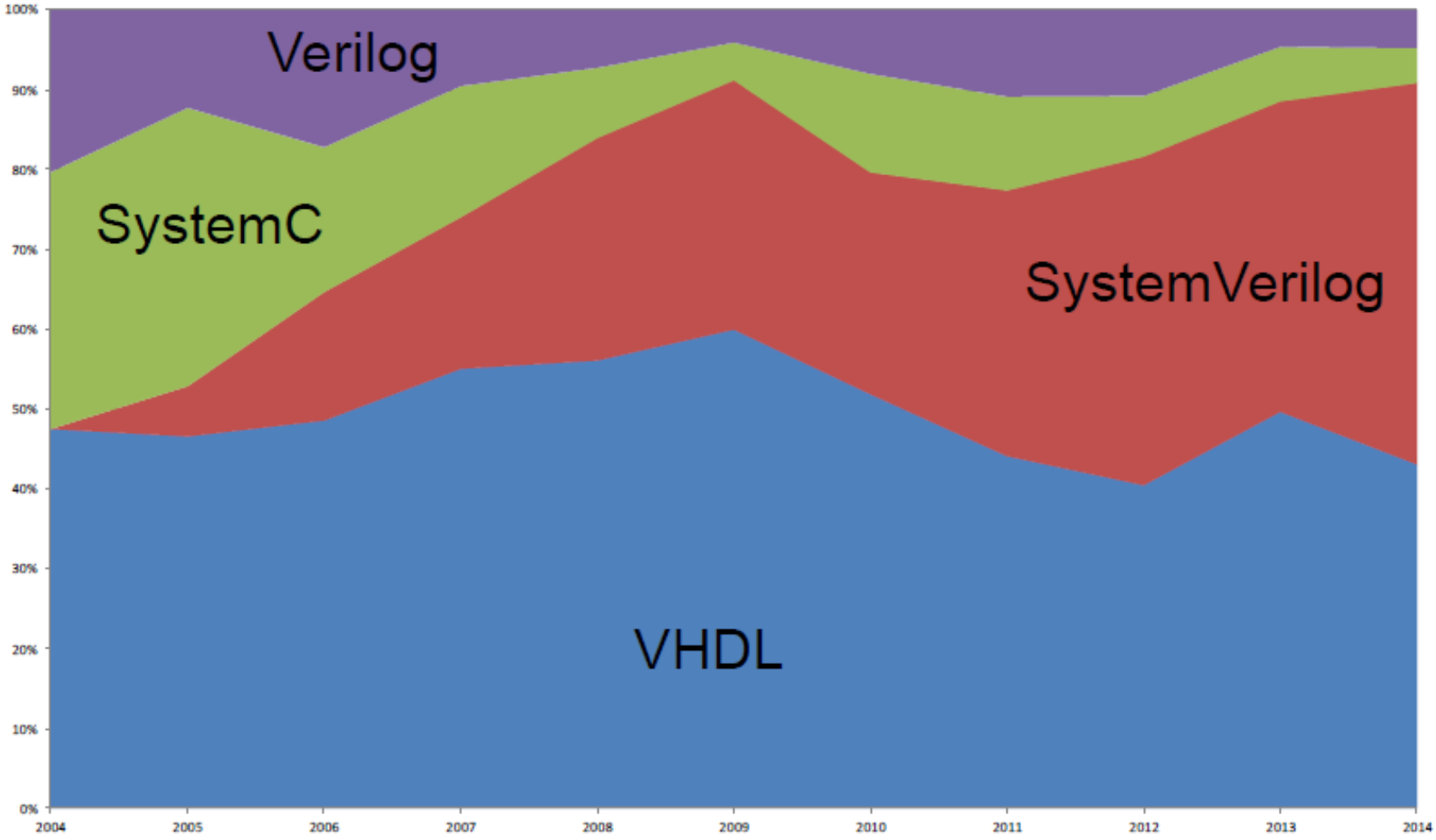
Rank	Standard	Name
1	1364-2001	Verilog Hardware Description Language
2	1800-2009	SystemVerilog–Unified Hardware Design, Specification, and Verification Language
3	1076-2002	VHDL Language Reference Manual
4	1076-1993	VHDL Language Reference Manual
...		
6	1364-1995	Hardware Description Language Based on the Verilog Hardware Description Language
7	1800-2005	SystemVerilog: Unified Hardware Design, Specification and Verification Language
...		
23	1076-1987	VHDL Language Reference Manual
...		
27	1076/INT-1991	Interpretations: IEEE Std 1076-1987, IEEE Standard VHDL Language Reference Manual
...		
32	1666-2005	SystemC Language Reference Manual
...		
34	1364-2005	Verilog Hardware Description Language

Language Wars in the 21st Century



Verilog is like the English of HDLs: everything you like becomes a part of it, and it is spoken around the world. VHDL is more like the Latin of HDLs: we learned many good things from it, but it is old and it is dead, and people do not speak it anymore.

Training Market (Europe)



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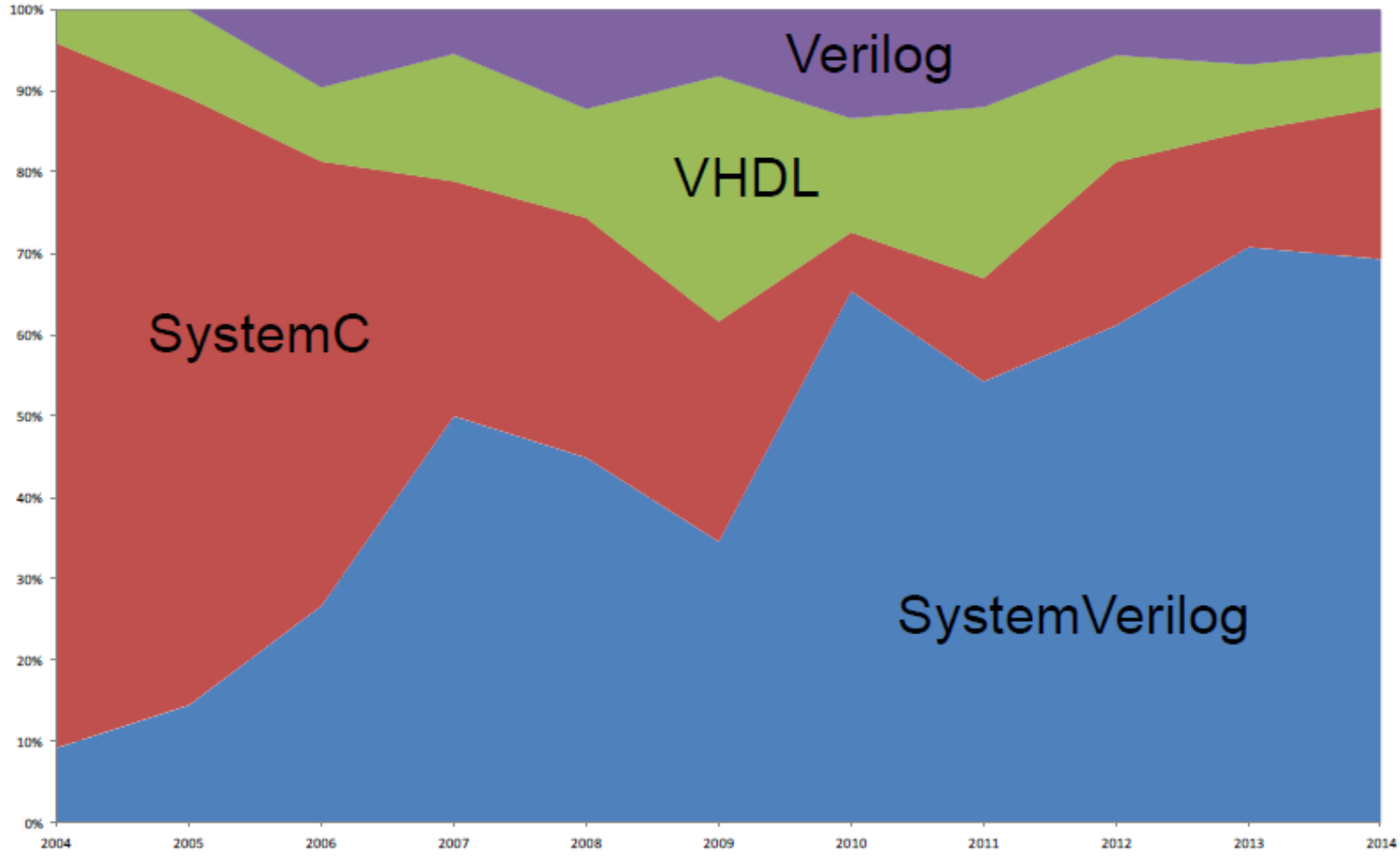
Training(USA & RoW)



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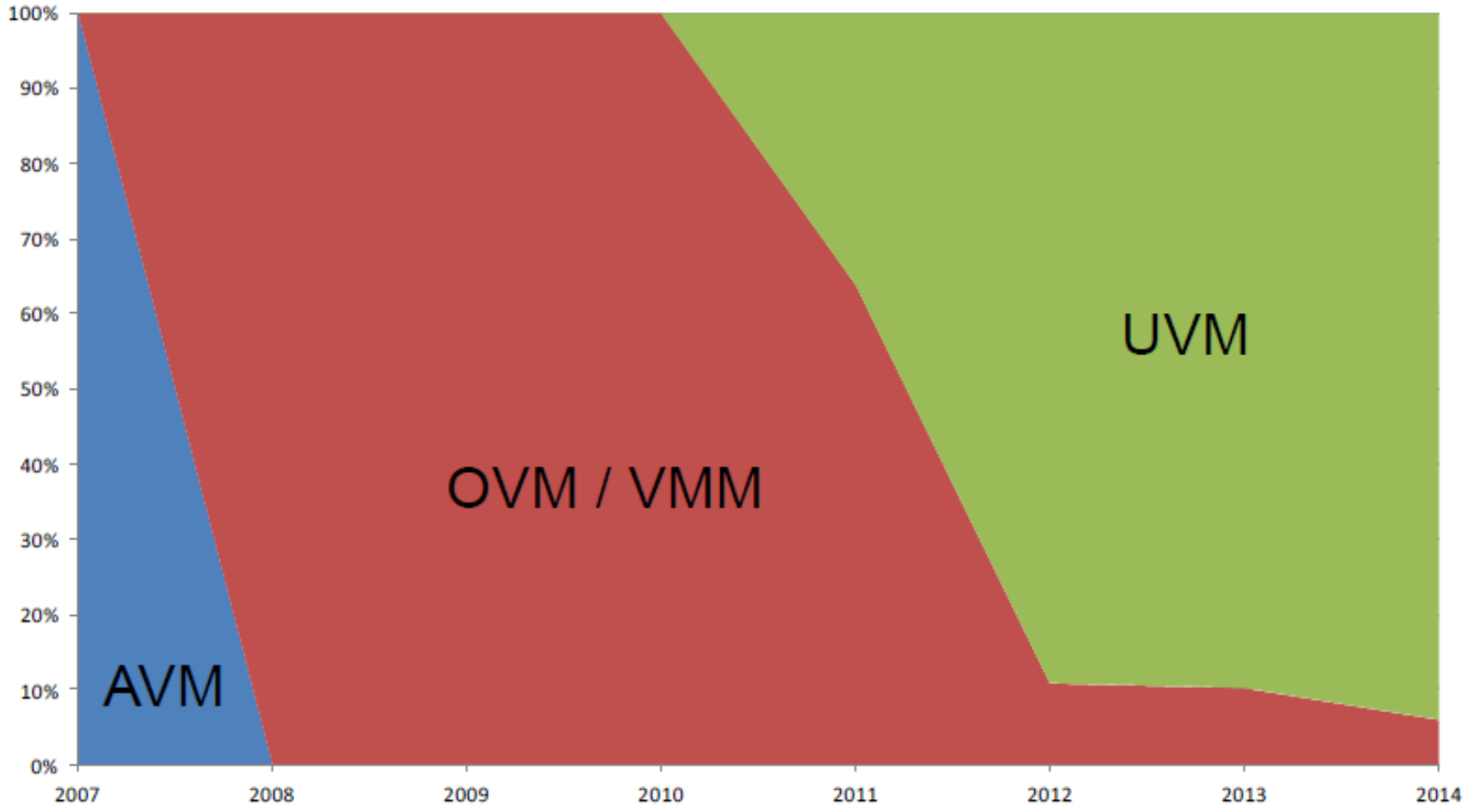
SystemVerilog Methodology



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Survey

"What is your main RTL design language?"

	ASIC	FPGA
SystemC	16	6
SystemVerilog	207	20
Verilog	460	74
VHDL	132	140

"What is your main verification language?"

	ASIC	FPGA
C++ / SystemC	58	11
e / Vera	34	0
SystemVerilog	588	89
Verilog	88	42
VHDL	50	100

Thanks