A. 组合逻辑电路

一、 8-3 编码器

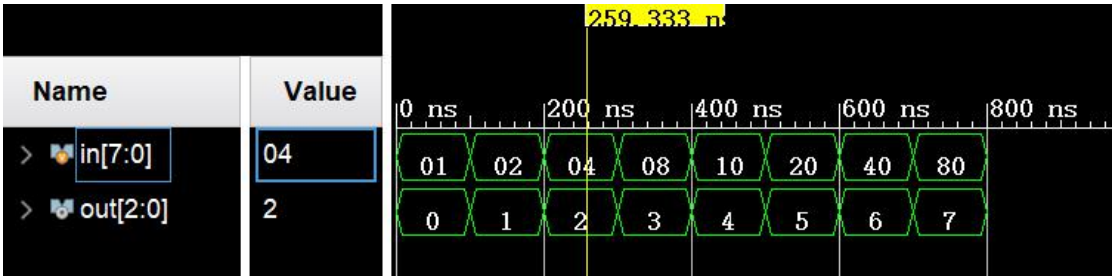
1. 代码实现

```
module biancode(x,y);
    input [7:0] x;
    output reg [2:0] y;
   always@(x)
       begin
           case(x)
           8'b00000001: y = 3'b000;
           8'b00000010: y = 3'b001;
           8'b00000100: y = 3'b010;
           8'b00001000: y = 3'b011;
           8'b00010000: y = 3'b100;
           8'b00100000: y = 3'b101;
           8'b01000000: y = 3'b110;
           8'b10000000: y = 3'b111;
            endcase
       end
endmodule
```

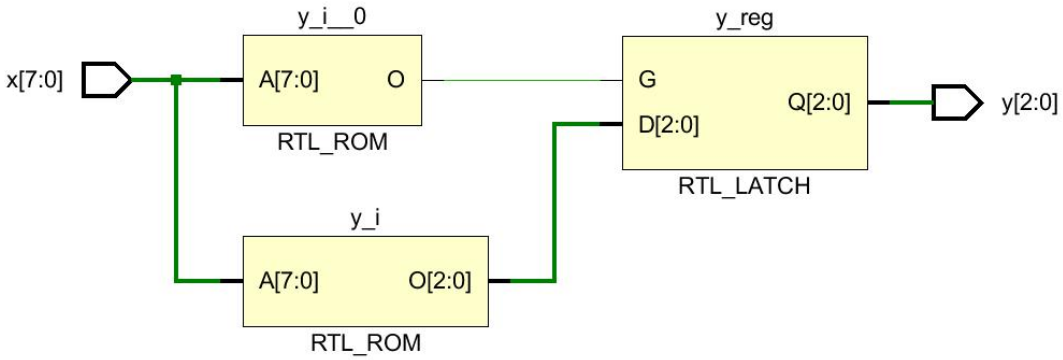
2. 仿真程序及结果

不断改变输入，查看输出是否为预期结果

```
module try();
    reg [7:0] in;
    wire [2:0] out;

   biancode one(in,out);

   initial
   begin
       in = 8'b00000001;
       #100;
       in = 8'b00000010;
       #100
       in = 8'b00000100;
       #100
       in = 8'b00001000;
       #100
       in = 8'b00010000;
       #100;
       in = 8'b00100000;
       #100
       #100
       in = 8'b00010000;
       #100;
       in = 8'b00100000;
       #100
       in = 8'b01000000;
       #100
       in = 8'b10000000;
       #100
       $finish;
       $stop;
    end
endmodule
```

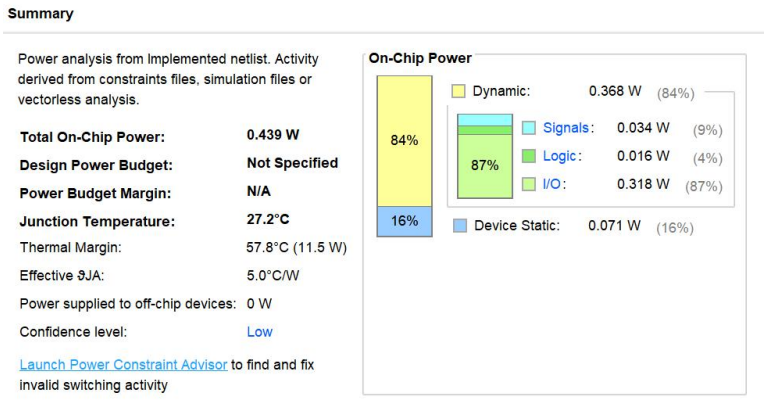


3. 电路分析



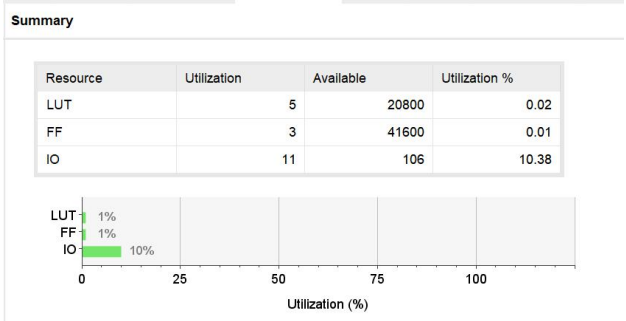
4. 能耗分析

能耗大多消耗在 I/O 上



5. 资源分析

资源利用不多



二、 3-8 译码器

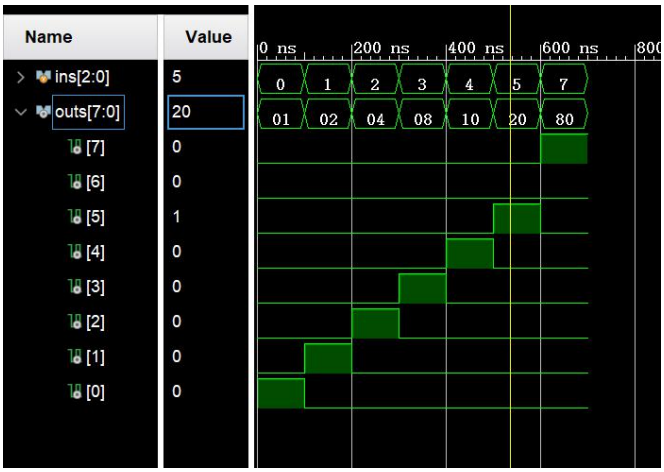
1.代码实现

```
module yicode(in,out);
    input [2:0]in;
    output reg[7:0] out;
    always@(in)
      begin
        case(in)
        3'b000: out = 8'b00000001;
        3'b001: out = 8'b00000010;
        3'b010: out = 8'b00000100;
        3'b011: out = 8'b00001000;
        3'b100: out=  8'b00010000;
        3'b101: out = 8'b00100000;
        3'b110: out = 8'b01000000;
        3'b111: out = 8'b10000000;
        endcase
     end

endmodule
```

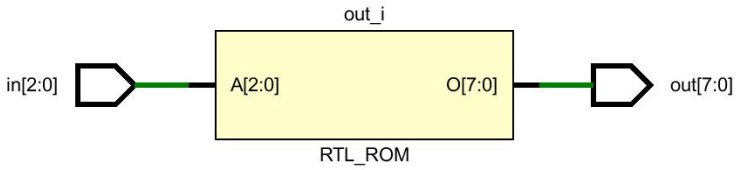
2.仿真代码及结果

不断改变输入，查看输出是否为预期结果

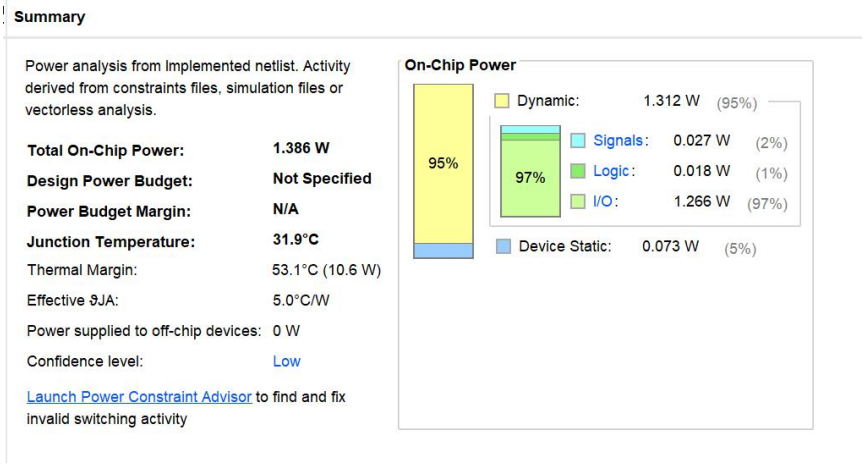
```
module try();
    reg [2:0] ins;
    wire [7:0] outs;

    yicode tyone(ins,outs);
    initial
        begin
        ins = 3'b000;
        #100
        ins = 3'b001;
        #100
        ins = 3'b010;
        #100
        ins = 3'b011;
        #100
        ins = 3'b100;
        #100
        ins = 3'b101;
        #100
        ins = 3'b111;
        #100
```



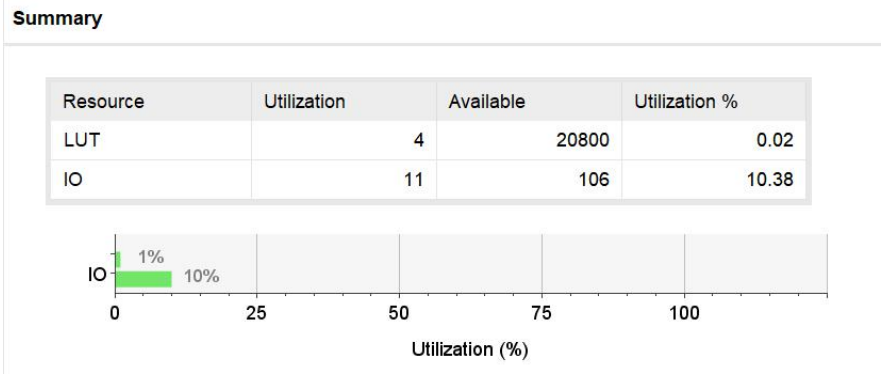
3.电路分析



4.能耗分析 能耗大多消耗在 I/O 上



5.资源分析 LUT 消耗不多



三、 三位四选一数据选择器

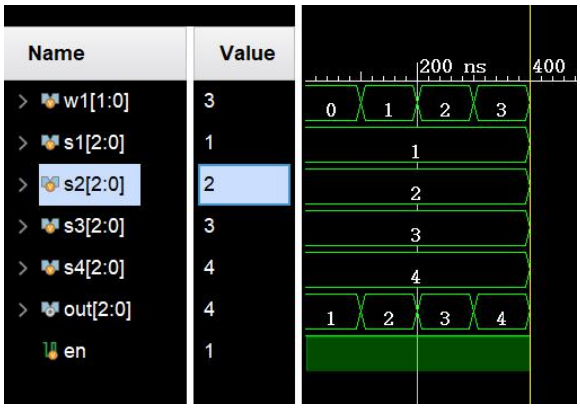
1. 代码实现 （en 为控制开关，en 为 0 时没有输出，w 为选择开关）

```
module FourOne(d1,d2,d3,d4,w,f,en);
    input [2:0]d1;
    input [2:0]d2;
    input [2:0]d3;
    input [2:0]d4;
    input[1:0]w;
    input en;
    output reg[2:0] f;
    always @ (d1 or d2 or d3 or d4 or w or en)
    begin
        if(en==0)
            f=0;
         else
         begin
         case(w)
         2'b00:f=d1;
         2'b01:f=d2;
         2'b10:f=d3;
         2'b11:f=d4;
         endcase
         end
```

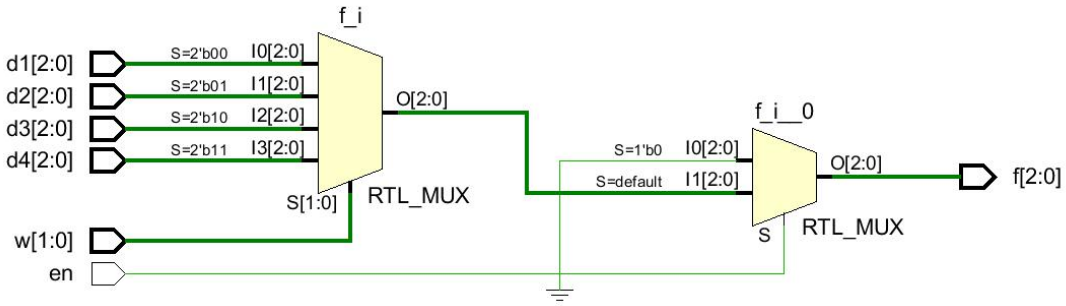
2. 仿真代码及结果

不断改变输入，查看输出是否为预期结果

```
module try();
    reg [1:0]w1;
    reg [2:0] s1;
    reg [2:0] s2;
    reg [2:0] s3;
    reg [2:0] s4;
    wire [2:0] out;
    reg en;
    FourOne tyeone(s1,s2,s3,s4,w1,out,en);

    initial
    begin
        s1 = 001;
        s2 = 010;
        s3 = 011;
        s4 = 100;
        w1 = 2'b00;
        en = 1;
        #100
        w1 = 2'b01;
        #100
        w1 = 2'b10;
        w1 = 2'b10;
        #100
        w1 = 2'b11;
        #100
        $stop;
        $finish;
    end
endmodule
```



3. 电路分析



4. ***能耗分析*** 能耗大多消耗在 I/O 上

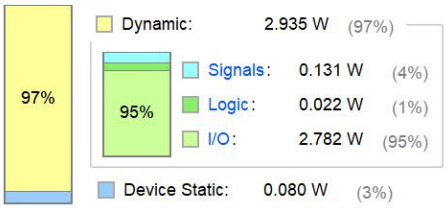
Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**3.015 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**40.1°C**
Thermal Margin:	44.9°C (8.9 W)
Effective ϑJA:	5.0°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

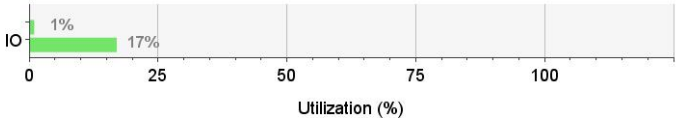
On-Chip Power



5. 资源分析

Summary

Resource	Utilization	Available	Utilization %
LUT	5	20800	0.02
IO	18	106	16.98



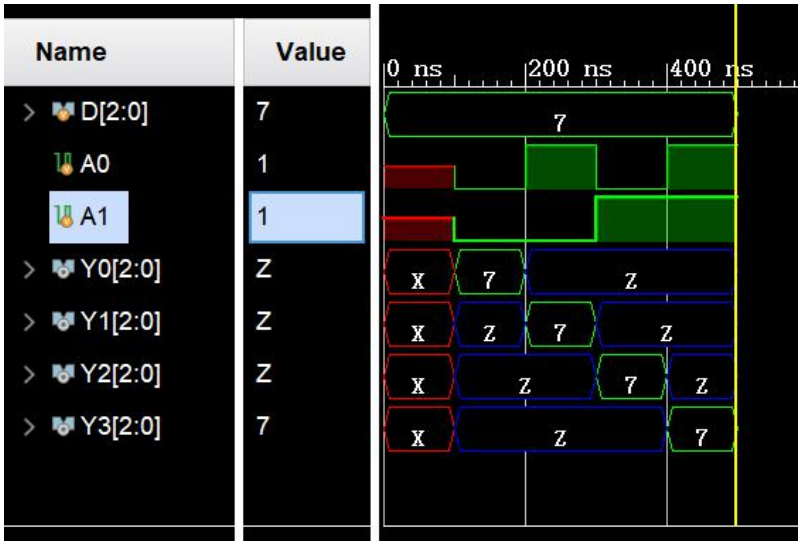
四、 数据分配器（四个输出端口，两位选择输入）

1. 代码实现 （D 为要输出的数据，A0,A1 为选择信号，其余为输出端口）

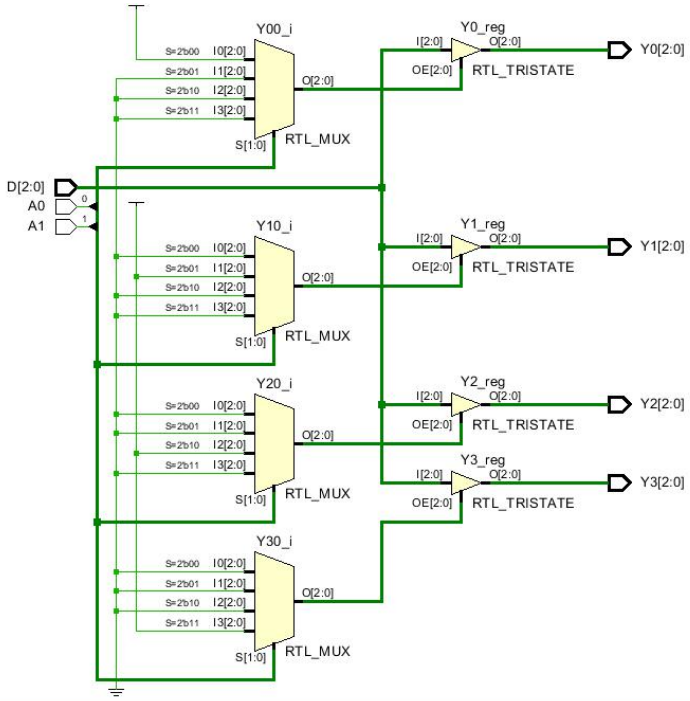
```
module demux(D,A0,A1,Y0,Y1,Y2,Y3);
    input [2:0] D;
    input A0, A1;
    output reg [2:0] Y0;
    output reg [2:0] Y1;
    output reg [2:0] Y2;
    output reg [2:0] Y3;
    always@(D or A0 or A1)
    begin
        case({A1,A0})
            2'b00:
                begin
                    Y0 = D;  Y1 = 3'bzzz; Y2 = 3'bzzz; Y3 = 3'bzzz;
                end
            2'b01:
                begin
                    Y1 = D; Y0 = 3'bzzz; Y2 = 3'bzzz; Y3 = 3'bzzz;
                end

            2'b10:
                begin
                    Y2 = D; Y1 = 3'bzzz; Y0 = 3'bzzz; Y3 = 3'bzzz;
                end

            2'b11:
                begin
                    Y3 = D;Y1 = 3'bzzz; Y2 = 3'bzzz; Y0 = 3'bzzz;
                end
        endcase
    end


endmodule
```

2. 仿真代码及结果

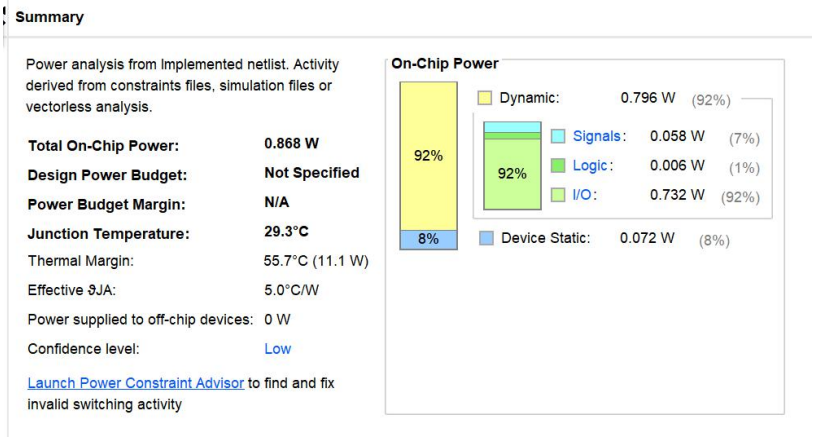
```
module try();
    reg [2:0] D;
    reg A0;
    reg A1;
    wire [2:0] Y0;
    wire [2:0] Y1;
    wire [2:0] Y2;
    wire [2:0] Y3;

    demux tryone(D,A0,A1,Y0,Y1,Y2,Y3);

    initial
        begin
            D = 3'b111;
            #100
            A0 = 1'b0; A1 = 1'b0;
            #100
            A0 = 1'b1; A1 = 1'b0;
            #100
            A0 = 1'b0; A1 = 1'b1;
            #100
            A0 = 1'b1; A1 = 1'b1;
```



3. 电路分析



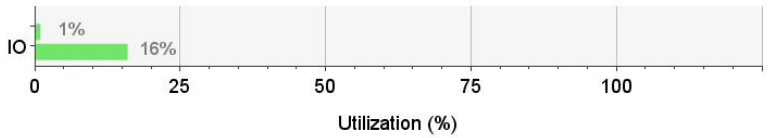
4. 能耗分析　能耗大多消耗在 I/O 上



5. 资源分析

Summary

Resource	Utilization	Available	Utilization %
LUT	2	20800	0.01
IO	17	106	16.04



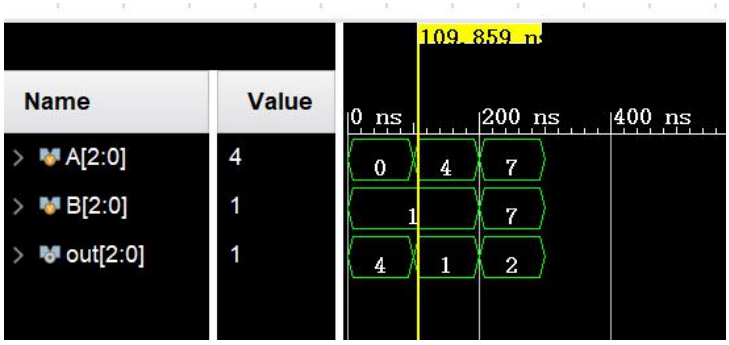
五、 数值比较器（三位）

1. 代码实现（A>B 输出 1，A=B 输出 2，A<B 输出 4）

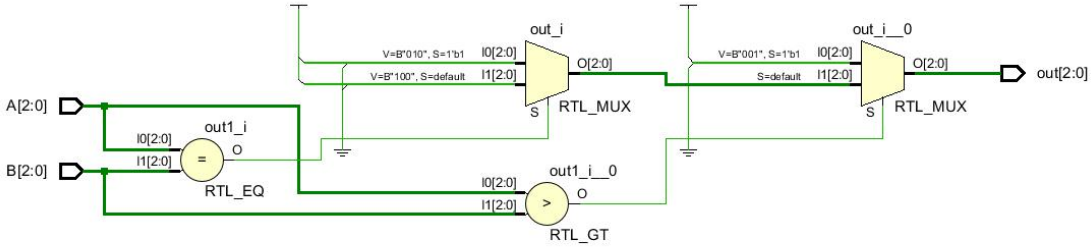
```
module compare(A,B,out);
    input [2:0] A;
    input [2:0] B;
    output reg [2:0] out;

    always@(A,B)
        begin
            if(A > B)
                out <= 3'b001;
            else if(A == B)
                out <= 3'b010;
            else
                out <= 3'b100;
        end
endmodule
```

2. 仿真代码及结果

```
module try();
    reg [2:0] A;
    reg [2:0] B;
    wire [2:0] out;

    compare tyrone(A,B,out);

    initial
        begin
            //#100  //A < B
            A = 3'b000;
            B = 3'b001;
            #100  //A > B
            A = 3'b100;
            B = 3'b001;
            #100  // A = B
            A = 3'b111;
            B = 3'b111;
            #100
            $finish;
            $stop;
        end
```



3. 电路分析



4. 能耗分析

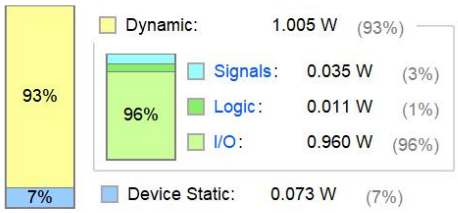
Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**1.078 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**30.4°C**
Thermal Margin:	54.6°C (10.9 W)
Effective ϑJA:	5.0°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

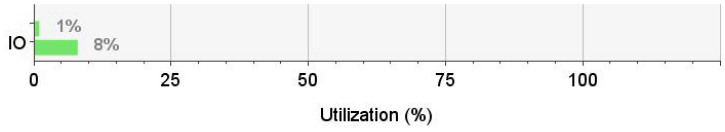
On-Chip Power



5. 资源分析

Summary

Resource	Utilization	Available	Utilization %
LUT	3	20800	0.01
IO	9	106	8.49



B. 时序逻辑电路

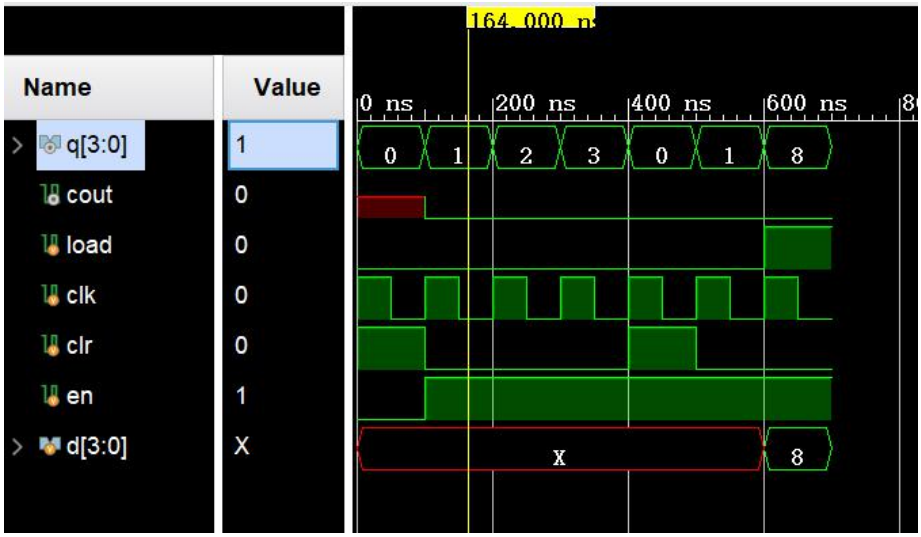
一、同步四位计数器

1. 代码实现

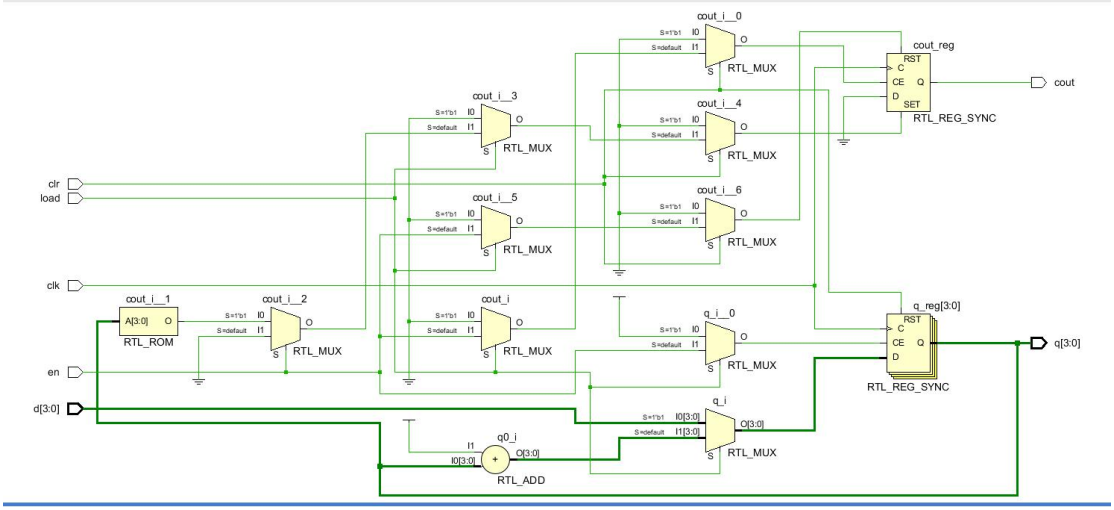
```
module count(cout, q, clk, clr, load, en,d);
    output reg [3:0] q;  //输出
    output reg cout;  //进位信号
    input clk, clr, load, en;  //clr为置0信号, en为计数信号
    input [3:0] d;

    always@(posedge clk)
        begin
            if(clr)
                begin
                    q <=0;
                 end
             else if(load)
                begin
                    q <= d;
                end
             else if(en)
                begin
                    q <= q+1;
                    if(q==4'b1111)
                        begin
                            cout <= 1;
                        end
                    else
                        begin
                            cout <= 0;
                        end
                end
              else
                 begin
                     q <= q;
                 end
          end
endmodule
```

2. 仿真代码及结果

```
module try();
    wire [3:0] q;
    wire cout;
    reg load, clk, clr, en;
    reg [3:0] d;

    count tryone(cout,q,clk,clr,load,en,d);
    initial
    begin
        clk = 1;
        forever #50
            clk = ~clk;
     end

    initial
     begin
        clr = 1;    //一开始要先将输出置0
        en = 0;
        load = 0;
        #100
        clr = 0;
        en = 1;
    clr = 0;
    en = 1;
    load = 0;
    #100
    clr = 0;
    en = 1;
    load = 0;
    #100
    clr = 1;
    en = 1;
    load = 0;
    #100
    clr = 0;
    en = 1;
    load = 0;
    #100
    load = 1;
    d = 4'b1000;
    clr = 0;
    en = 1;
    #100
    $finish;
```



3. 电路分析



4. 能耗分析

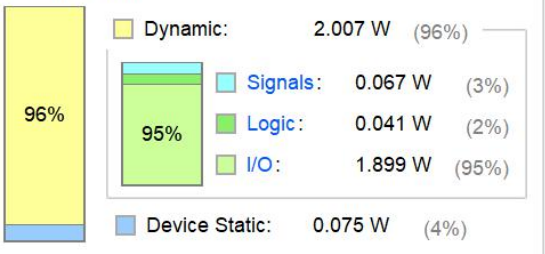
Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**2.083 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**35.4°C**
Thermal Margin:	49.6°C (9.9 W)
Effective ϑJA:	5.0°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

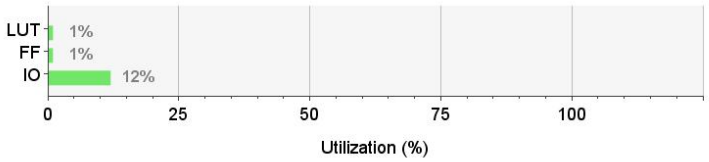
On-Chip Power



5. 资源分析

Summary

Resource	Utilization	Available	Utilization %
LUT	6	20800	0.03
FF	5	41600	0.01
IO	13	106	12.26



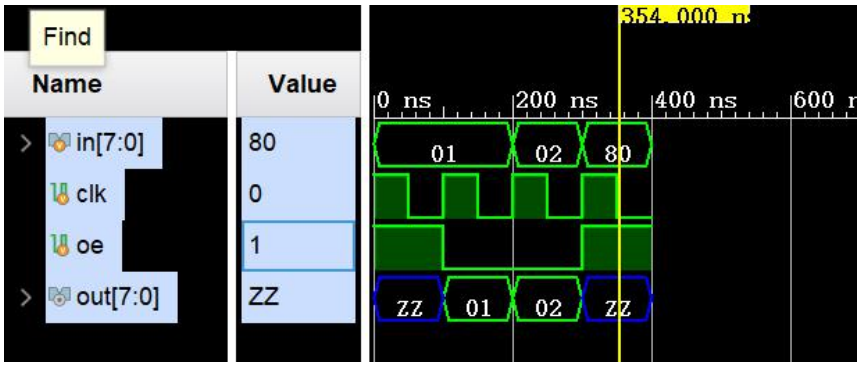
二、 八位二进制寄存器

1. 代码实现

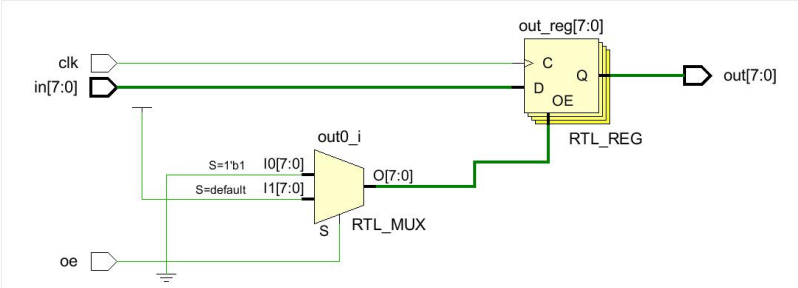
```
module eightreg(out,in,clk,oe);
    input [7:0] in;
    input oe, clk;
    output reg [7:0] out;

    always@(posedge clk)
        begin
            if(oe)
                out <= 8'bz;
             else
                out <= in;
          end
endmodule
```

2. 仿真代码及结果

```
module try( );
    reg [7:0] in;
    reg clk;
    reg oe;
    wire [7:0] out;

    eightreg tryone(out, in, clk, oe);
    initial
        begin
            clk = 1;
                forever #50 clk = ~clk;
          end
    initial
        begin
        oe = 1;
        in = 8'b00000001;
        #100
        oe = 0;
        in = 8'b00000001;
        #100
        oe = 0;
        in = 8'b00000010;
        #100
        oe = 1;
        in = 8'b10000000;
        #100
        $finish;
        $stop;
    end
endmodule
```



3. 电路分析



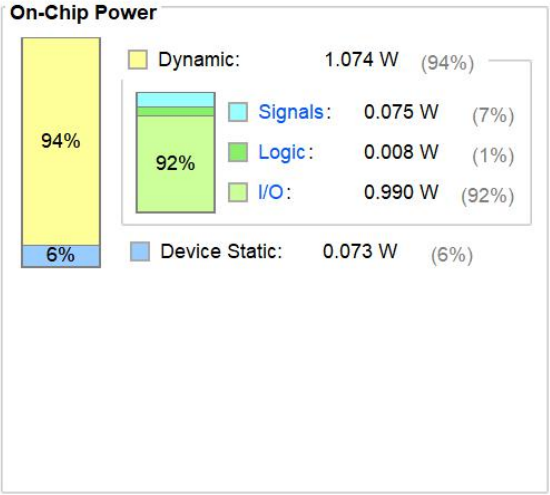
4. 能耗分析

Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**1.146 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**30.7°C**
Thermal Margin:	54.3°C (10.8 W)
Effective ϑJA:	5.0°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

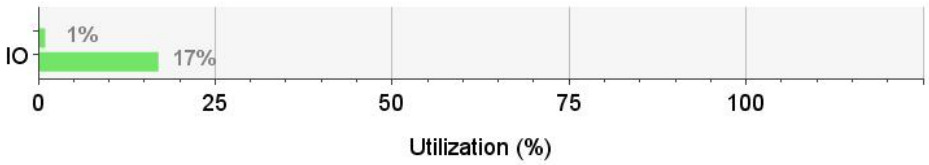
Launch Power Constraint Advisor to find and fix invalid switching activity



5. 资源分析

Summary

Resource	Utilization	Available	Utilization %
FF	9	41600	0.02
IO	18	106	16.98



三、 八位锁存器

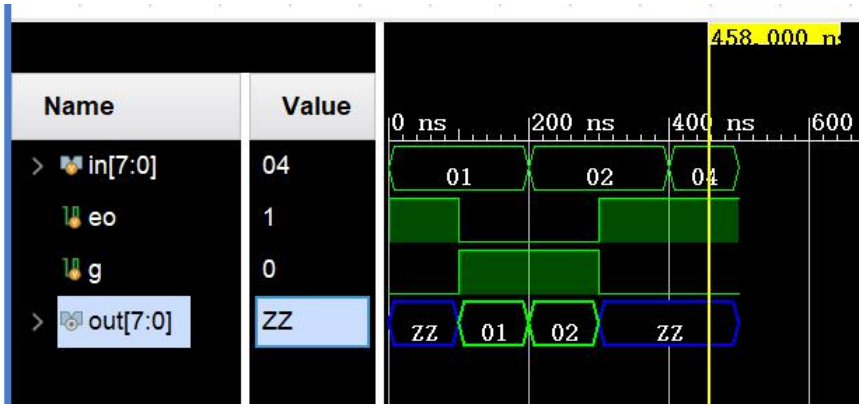
锁存器：锁存器是电平敏感的，只要时钟信号有效，锁存器就会起作用。当 oe 为 1，锁存器工作，输出为高阻值，当 oe 为 0，g 为 1，锁存器不工作，输出等于输入。

1. 代码实现

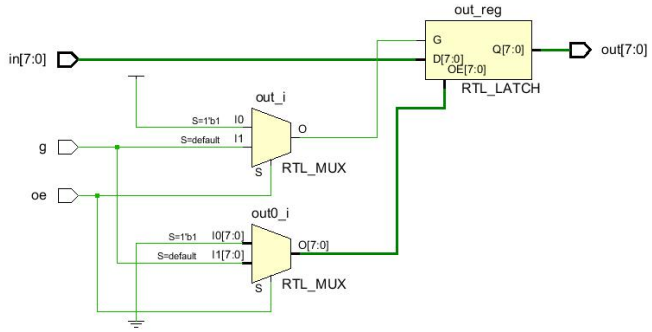
```
module lockreg(in, out, oe, g);
    input [7:0] in;
    output reg [7:0] out;
    input oe, g;  //三态控制端，控制信号

    always@(*)
        begin
            if(oe)
                out <= 8'bz;
             else if(g)
                out <= in;
         end
endmodule
```

2. 仿真代码及结果

```
module try();
    reg [7:0] in;
    reg eo, g;
    wire [7:0] out;

    lockreg tryone(in, out, eo, g);

    initial
        begin
            eo = 1;
            g = 0;
            in = 8'b00000001;
            #100
            eo = 0;
            g = 1;
            in = 8'b00000001;
            #100
            eo = 0;
            g = 1;
            in = 8'b00000010;
            #100
            eo = 1;
            g = 0;
            #100
            in = 8'b00000100;
            #100
            $finish;
            $stop;
        end
endmodule
```



3. 电路分析



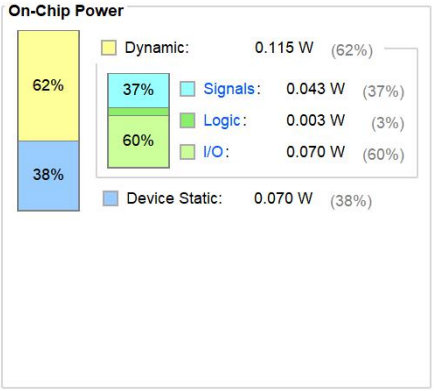
4. 能耗分析　signals 也是消耗了一部分能耗

Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.186 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**25.9°C**
Thermal Margin:	59.1°C (11.7 W)
Effective ϑJA:	5.0°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

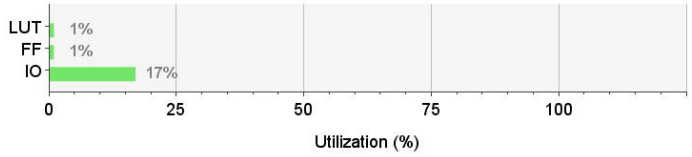
Launch Power Constraint Advisor to find and fix invalid switching activity



5. 资源分析

Summary

Resource	Utilization	Available	Utilization %
LUT	2	20800	0.01
FF	9	41600	0.02
IO	18	106	16.98



四、 存储器

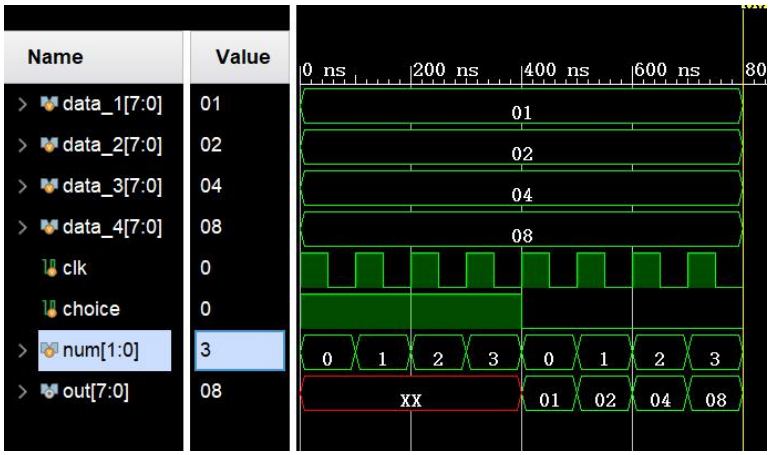
建立一个 4 个 8 位寄存器，choice 代表选择，为 1 时为写入数据状态，为 0 时为读取所存储的数据的状态。num 代表选择写入或读取哪一个数据。

1. .代码实现

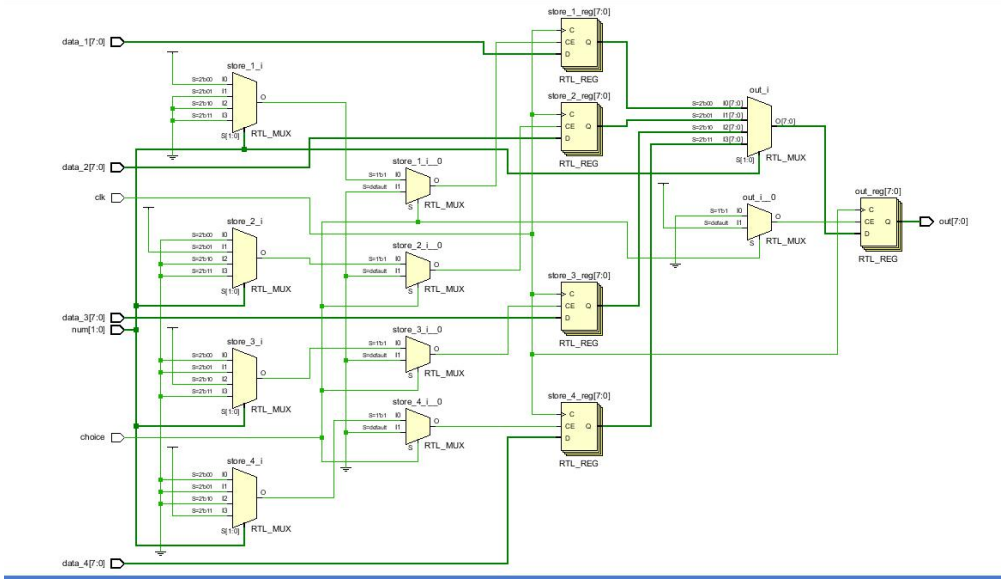
```
module store(data_1, data_2, data_3, data_4,choice,num,out,clk);
    input [7:0] data_1;
    input [7:0] data_2;
    input [7:0] data_3;
    input [7:0] data_4;
    input clk;
    reg [7:0] store_1;
    reg [7:0] store_2;
    reg [7:0] store_3;
    reg [7:0] store_4;
    input choice;
    input [1:0]num;
    output reg [7:0] out;

    always@(posedge clk)
        begin
            if(choice)
                begin
                    case(num)
                        2'b00: store_1 = data_1;
                        2'b01: store_2 = data_2;
                        2'b10: store_3 = data_3;
                        2'b11: store_4 = data_4;
                    endcase
                end
             else
               begin
                    case(num)
                        2'b00: out = store_1;
                        2'b01: out = store_2;
                        2'b10: out = store_3;
                        2'b11: out = store_4;
                      endcase
                 end
           end


endmodule
```

2 仿真文件及结果

```
module try();

    reg [7:0] data_1;
    reg [7:0] data_2;
    reg [7:0] data_3;
    reg [7:0] data_4;
    reg clk;
    reg choice;
    reg [1:0]num;
    wire  [7:0] out;

    store tryone(data_1, data_2, data_3, data_4,choice,num,out,clk);

    initial
    begin
        clk = 1;
        forever #50 clk = ~clk;
     end

     initial
        begin
            data_1 = 8'b00000001;
    data_2 = 8'b00000010;
    data_3 = 8'b00000100;
    data_4 = 8'b00001000;
    choice = 1;
    num = 2'b00;
    #100;
    choice = 1;
    num = 2'b01;
    #100
    num = 2'b10;
    #100
    num = 2'b11;
    #100
    choice = 0;
    num = 2'b00;
    #100
    num = 2'b01;
    #100
    num = 2'b10;
    #100
    num = 2'b11;
    #100
                $finish;
                $stop;
        end
endmodule
```



3 电路分析



4 能耗分析

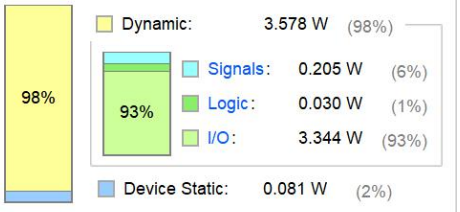
Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**3.66 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**43.3°C**
Thermal Margin:	41.7°C (8.3 W)
Effective ϑJA:	5.0°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power



5 资源分析

Summary

Resource	Utilization	Available	Utilization %
LUT	13	20800	0.06
FF	40	41600	0.10
IO	44	106	41.51