重庆某双一流大学计算机系统结构期末真题

考试时间: 2020 年 12 月 9 日 14:00-16:00
回忆整理: Vayne Duan

写在前面:

1. 试卷总体比较简单, 闭卷, 全英文(单词不认识可以问老师), 可以中文作答,可以带计算器(实际没有什么计算量).
2. 细心一点, 95 分没有问题.
3. 本回忆版真题于 2020 年 12 月 10 日凌晨 1:18 写成, 因为不想复习其他科目了, 好累, 偷个懒.
4. 计院专业课的试卷似乎都不准老师发出来, 希望有学弟学妹们能将我"回忆试卷"的习惯传承下去!
5. 其余专业课的回忆版试卷也许可以在 github.com/VayneDuan 找到, 记得**star & follow, 会持续更新的!**

一、判断题(10 道 * 2 分 = 20 分)

个别题目容易选错, 其余都很简单, 所以不再回忆了(其实是记不住了)
如: LW 指令是 PC-relative 寻址 (F), 这是错的, 应该是基址(base)寻址, 计组学过的, 忘了

二、简答题(5 道* 8 分 = 40 分)

1. Please describe the principle of locality and how it leads to temporal locality and spatial locality

2. Please describe the control hazard and at least 3 technique to deal with it.

3. 比较 tomasulo 和 scroreboard 的异同

4. 描述 写直达 和 写回, 比较异同和优缺点

5. 64bit address, 16KB cache, 32-byte cache line;
   ①两路组相联, block offset 多少 bit? index 多少 bit? tag 多少 bit?
   答案: offset 5 , index 8, tag 51
   ②全相联, block offset 多少 bit? index 多少 bit? tag 多少 bit?
   答案: offset 5 , index 0, tag 59

三、综合题(40 分)

1. 教材附录 C 的 C.7 原题 [Hint: 教材附录 C 的 C1.2.3.4.5.7 都可能作为原题出现在试卷]

C.7 [10/10] <C.3> In this problem, we will explore how deepening the pipeline affects performance in two ways: faster clock cycle and increased stalls due to data and control hazards. Assume that the original machine is a 5-stage pipeline with a 1 ns clock cycle. The second machine is a 12-stage pipeline with a 0.6 ns clock cycle. The 5-stage pipeline experiences a stall due to a data hazard every 5 instructions, whereas the 12-stage pipeline experiences 3 stalls every 8 instructions. In addition, branches constitute 20% of the instructions, and the misprediction rate for both machines is 5%.

a. [10] <C.3> What is the speedup of the 12-stage pipeline over the 5-stage pipeline, taking into account only data hazards?

b. [10] <C.3> If the branch mispredict penalty for the first machine is 2 cycles but the second machine is 5 cycles, what are the CPIs of each, taking into account the stalls due to branch mispredictions?

试卷上改为了 3 个小问:

1. CPI with data hazard (5 分)

答案: 1.2, 1.375

2. speedup of 12-stage to 5-stage (5 分)

答案: 1.45

3. CPI with data hazard and control hazard , speedup of 12-stage to 5-stage (5 分)

答案: 1.22, 1.425, 1.43

2. 给定 1-bit 和 2-bit 的预测器的状态机，给定分支指令是否跳转的序列(e.g. TTTTTTTNNTNNTTNNT 之类的)

让你填表，问上述序列的最后十次跳转，预测正确率是多少

给的表如下

predictor state(X/XX)	predict(T/N)	action(T/N)	correct(T/F)

3. 给定 4 条指令，请画出两种情况下的指令执行的 timing chart.

   a. 有数据前推(6 分)

   b. 无数据前推(7 分)

给定的指令如下:

```
ADD R1, R2, R3
SUB  R4, R1, R5
ADD R6, R1, R7
OR   R8, R1, R9
```