Computer Architecture (Fall 2022)

Quantitative Approach

Dr. Duo Liu (刘铎)
Office: Main Building 0626
Email: liuduo@cqu.edu.cn

Computer Architects and Quantitative Approach

- Design ideas and trade-offs are tested by using tools in order to estimate the impact on performance, power and cost (an iterative process)
  - analytical reasoning and fundamental design principles
  - equations for basic metrics
    - cost, performance, power…
  - simulations at various levels
    - system level, ISA, micro-architecture, memory , RTL, gate, circuit level
  - benchmark programs representing typical workloads

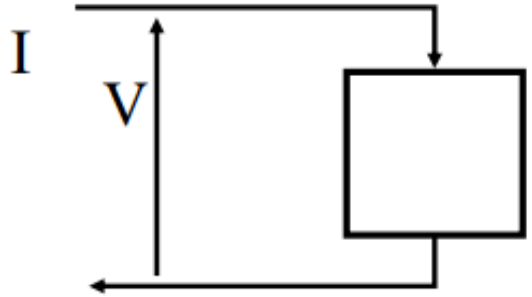
Power and Energy

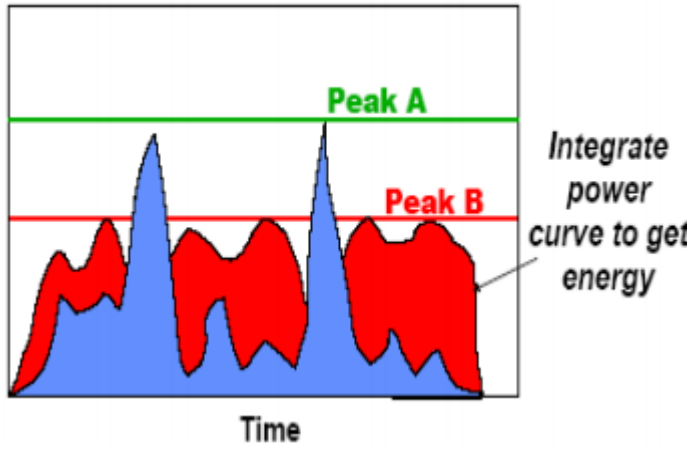
- **Problem: Get power in, get power out**
- **Thermal Design Power (TDP)**
  - Characterizes sustained power consumption
  - Used as target for power supply and cooling system
  - Lower than peak power, higher than average power consumption
- **Clock rate can be reduced dynamically to limit power consumption**
- **Energy per task is often a better measurement**

Power and Energy

- Energy
  - measured in Joules
- Power
  - rate of energy consumption
    - [Watts = Joules/sec]
  - instantaneous power P = V * I
    - voltage drop across a component

    times the current flowing through it
- Example
  - system A
    - higher peak power
    - lower total energy
  - system B
    - lower peak power
    - higher total energy





Power of CMOS Transitor

Dynamic Power

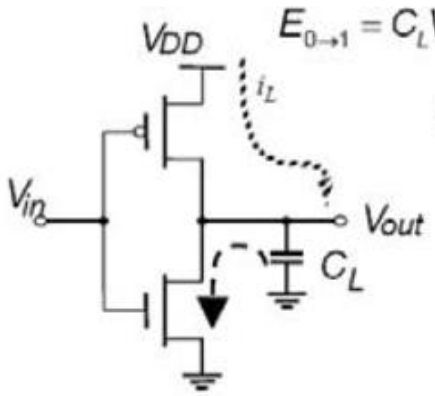
- traditionally dominant component
- dissipated when transitor switches (i.e. data dependent)

Static Power

- becoming more important with transitor scaling
- due to "leakege current" that flows even if there is no switching activity
- proportional to the number of transitors on the chip

Challenges

- power is the key limitation to chip design
  - · distribute power on-chip
  - · remove heat
  - · prevent hot spots
  - · low power design(clock gating,DVFS)



$$E_{0\to1} = C_L V_{DD}^2$$

$$E_R = \frac{1}{2} C_L V_{DD}^2$$

$$E_C = \frac{1}{2} C_L V_{DD}^2$$

- Energy consumed in N cycles, E_N:

$$E_N = C_L \bullet V_{DD}^2 \bullet n_{0\to1}$$

$n_{0\to1}$ – number of 0→1 transitions in N cycles

$$P_{avg} = \lim_{N\to\infty} \frac{E_N}{N} \cdot f = \left(\lim_{N\to\infty} \frac{n_{0\to1}}{N} \right) \cdot C_L \cdot V_{DD}^2 \cdot f$$

$$\alpha_{0\to1} = \lim_{N\to\infty} \frac{n_{0\to1}}{N} \cdot f$$

$$P_{avg} = \alpha_{0\to1} \cdot C_L \cdot V_{DD}^2 \cdot f$$