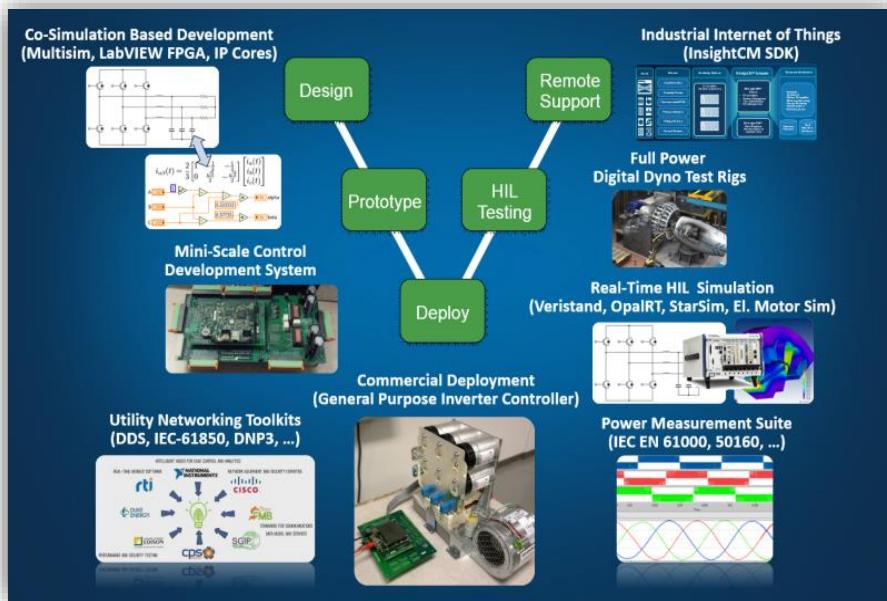


New Open Source Testbed Platform for Smart Grid and Microgrid Research: Go from Paper Design to Prototype Deployment in Days



[Complete Toolchain for Control Design,
HIL Verification and Deployment](#)

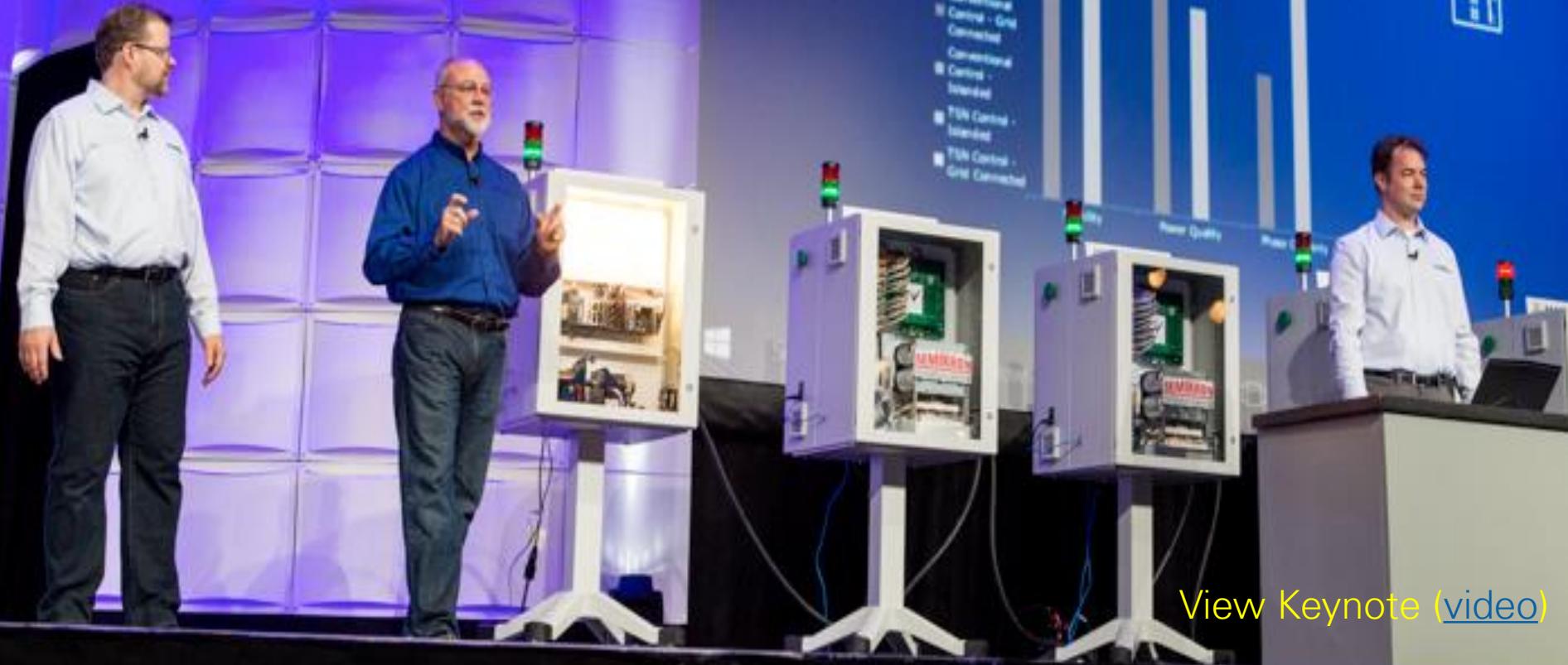


[Teco-Westinghouse 20 MVA Bi-Directional
Medium-Voltage Inverter Production](#)



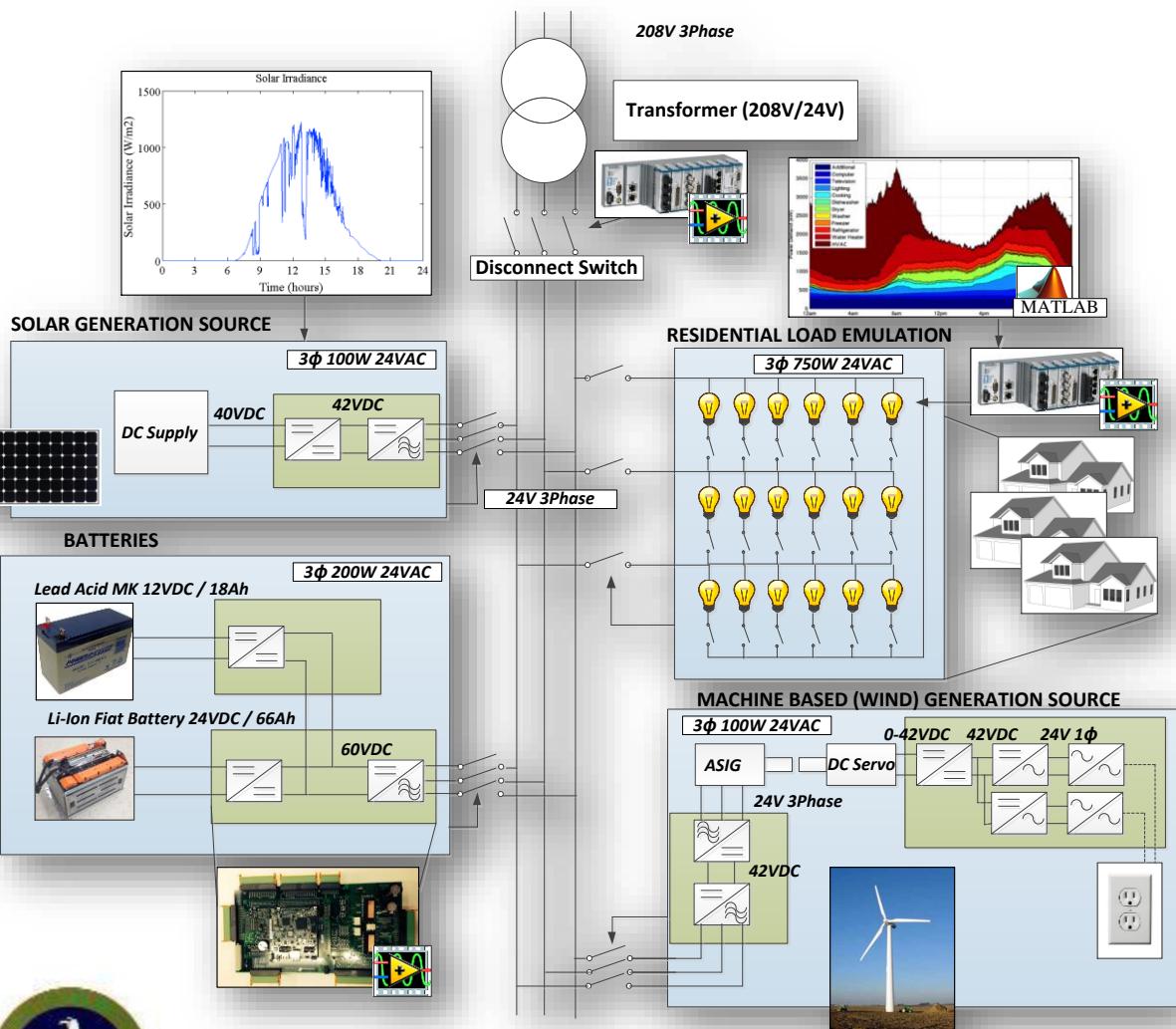
Brian MacCleery – Principal Product Manager for
Clean Energy Technology, National Instruments,
Member IEEE

NIWeek 2016 Keynote

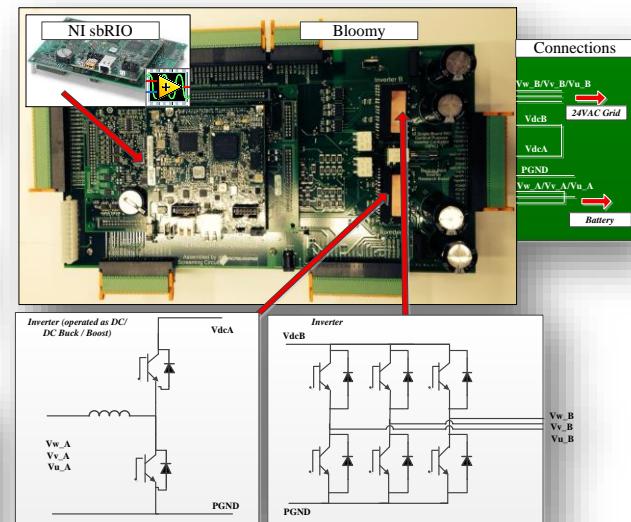


[View Keynote \(video\)](#)

SI-GRID: Software-defined Intelligent Grid Research Integration and Development platform



Real-time co-simulation model
and learning engine runs in the
controller FPGA



DC-DC boost converter and DC/AC inverter implemented
on a NI-GPIC (general purpose inverter control)



[View NIWeek Conference Presentation](#)

CERTS
CONSORTIUM FOR ELECTRIC RELIABILITY TECHNOLOGY SOLUTIONS

New Open Source Testbed Platform for Smart Grid and Microgrid Research



To address the demanding needs of industry and university research groups pursuing critical innovations in Smart Grid and Microgrid technologies, National Instruments has joined forces with other industry leaders to create a new research testbed architecture.

Thank You to Our IIoT Lab Sponsors and Collaborators

Platinum Level



Gold Level



Silver Level



Consortium



Demonstration Collaborators



Cisco
Intel
RTI
Semikron
Viewpoint Systems

New Open Source Testbed Platform for Smart Grid and Microgrid Research



The testbed enables productive, risk free, team based development and testing of advanced intellectual property related to the following priority research areas:

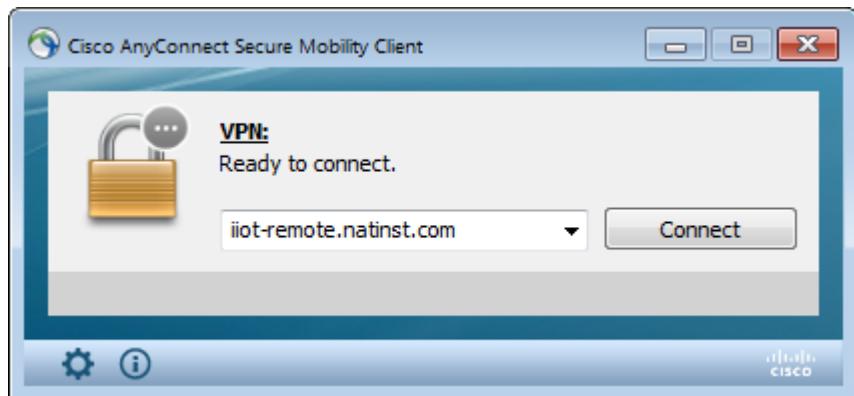
1. Grid stabilizing bidirectional grid tied inverters and DC converter control systems
2. Distributed Energy Resources
3. Demand Response
4. Energy Storage Systems
5. Communication infrastructure and emerging network standards (IEEE 802.1 Time Sensitive Networking)
6. Multiple communication protocols (61850, DNP3, C37.118, Modbus)
7. Distribution Grid Management
8. Cyber Security, Private Communication, and Cyber Attack Resilience
9. Wide Array Situational Awareness
10. Phasor Measurement Units and Intelligent Electric Devices
11. Multi-Agent Distributed Control Schemes
12. Wireless communication and Software Defined Networks
13. Electric Transportation
14. GPS and Network-based Time Synchronization
15. Embedded Real-Time Digital Twins
16. Machine Learning (Deep Reinforcement Learning)
17. Real-Time Hardware-In-the-Loop (HIL) Simulation
18. Grid compliance and interoperability testing such as IEEE 1547 anti-islanding tests
19. Voltage and frequency and control loop stability analysis
20. Islanding, Reconnection and Sectionalizing
21. Resiliency, Fault Recovery, Self Healing
22. A/B comparison testing of new control schemes
23. Automated real-time test execution
24. Remote connection access
25. Data interoperability of equipment (DDS, OpenFMB, 61850, 61870)
26. Interoperability of control code and models

New Open Source Testbed Platform for Smart Grid and Microgrid Research



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HOW TO GO FROM PAPER TO PROTOTYPE IN DAYS

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Example Video:

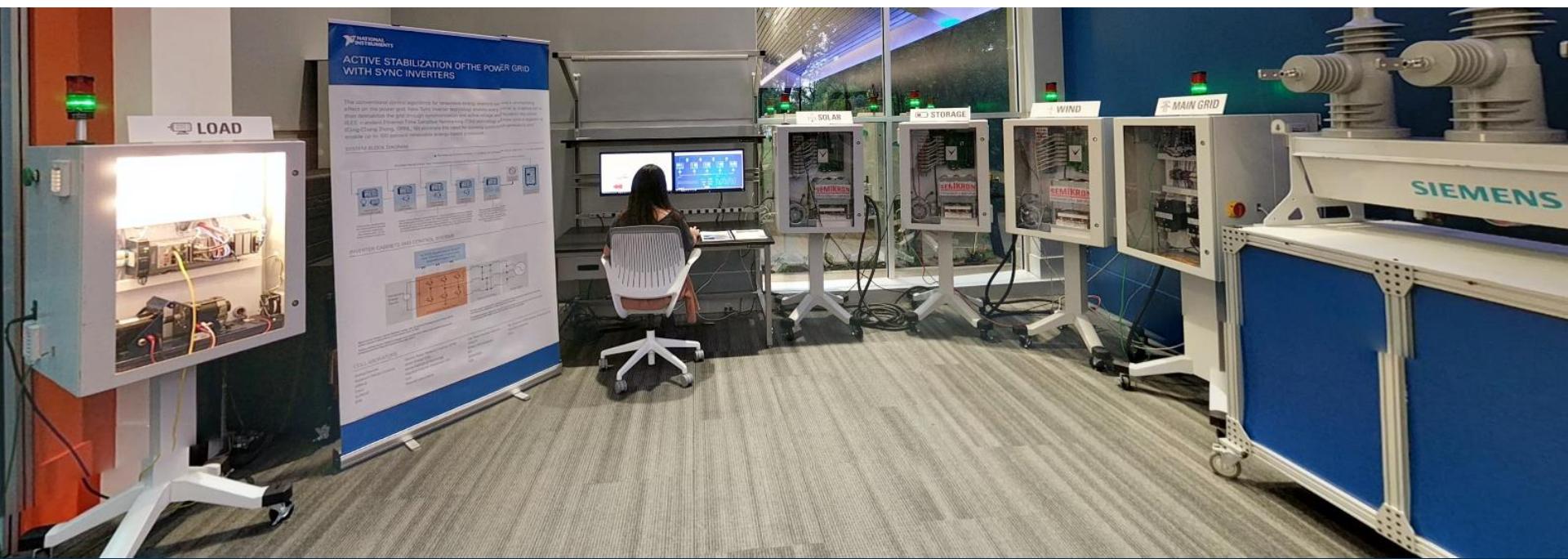
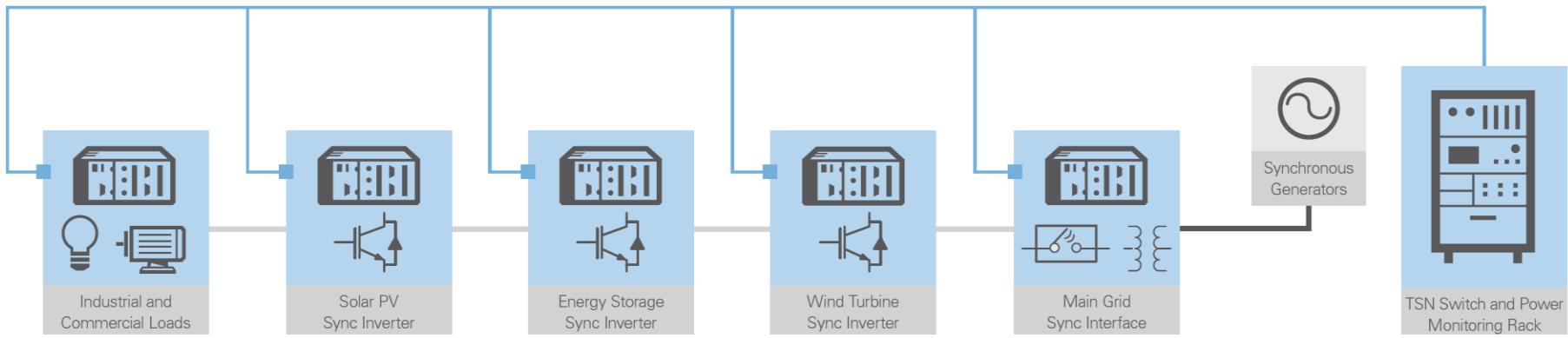
[Self-Synchronized Universal Droop Controller: Paper to Prototype in Three Days](#)



System Block Diagram

■ TSN ENABLED CONTROL SYSTEMS — ETHERNET TSN NETWORK — 3-PHASE MAIN GRID — 3-PHASE MICROGRID

ETHERNET TSN NETWORK: TIME SYNCHRONIZATION, SCHEDULED REAL-TIME COMMUNICATION AND STANDARD ETHERNET TRAFFIC



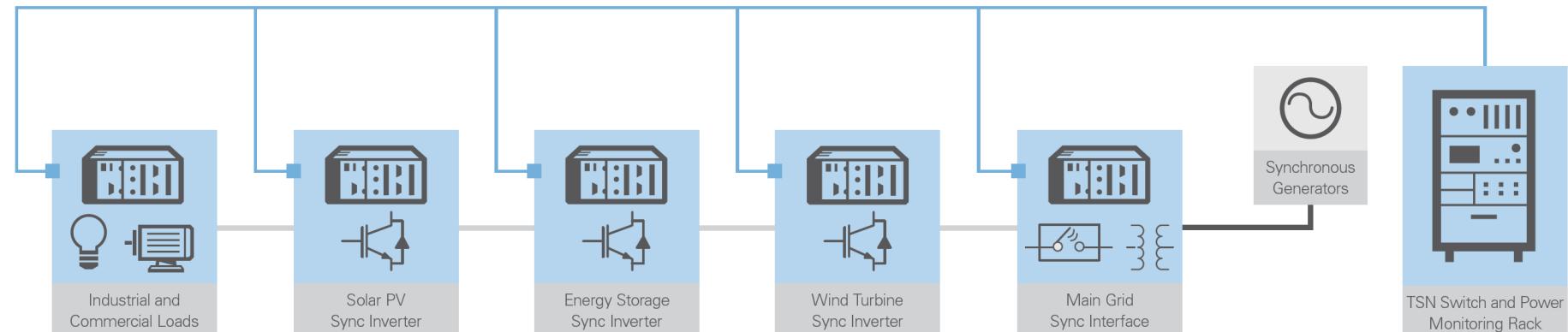
Features/Capabilities



- Ability to operate as an islanded Microgrid or to be tied to your local 240/480 VAC, 3-phase bus
- All voltages less than 60 Volts except for input stage of grid cabinet, which eliminates most electrician safety concerns
- Inverters have fully bi-directional active front end for sourcing and syncing power without time limits (i.e. mimicking hours of energy storage charging/discharging)
- FPGA control system provides dedicated fast protection, allowing the Linux RT programmer to try algorithms/code without risk
- Semikron SKiiP3 Intelligent Power Modules are oversized to eliminate any risk of damaged power electronics
- Connections are fully fuse protected to eliminate risk of melted wires
- Cabinets are on rolling casters to allow them to be easily moved around in the lab

■ TSN ENABLED CONTROL SYSTEMS ■ ETHERNET TSN NETWORK ■ 3-PHASE MAIN GRID ■ 3-PHASE MICROGRID

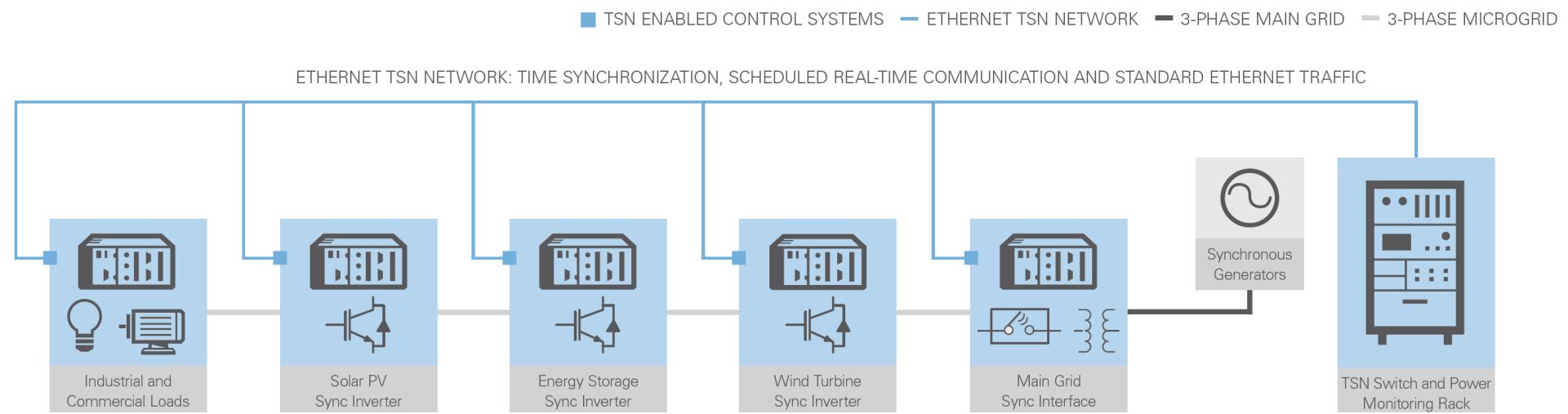
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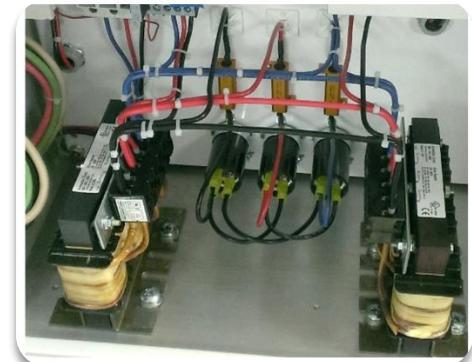
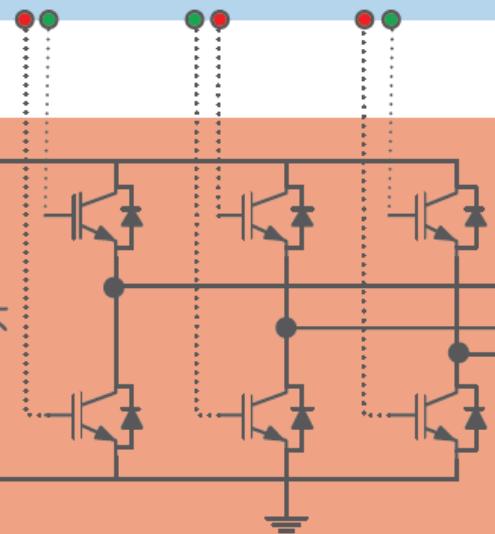
- **Inverter Cabinets** include Semikron SKiiP3 Intelligent Power Modules, ViewPoint voltage/current sense boards, disconnect contactors, 40 Amp DC link supplies with contactor controlled load resistors for bidirectionality, LCL line reactor filters, blower control contactors, control button, Red/Green light stack, dual Ethernet, mechanical disconnect switch
- **Load Cabinet** includes AC Induction motor load with contactor hard start capability and dynamometer brake resistor contactor control, LR reactive load, and lighting loads, DSA quality voltage and current measurements, control button, Red/Green light stack, dual Ethernet, mechanical disconnect switch
- **Grid Interface Cabinet** includes three phase contactor for islanding or connecting the Microgrid, fused step down transformers, DSA quality voltage and current measurements, control button, Red/Green light stack, dual Ethernet, mechanical disconnect switch



Inverter Cabinets

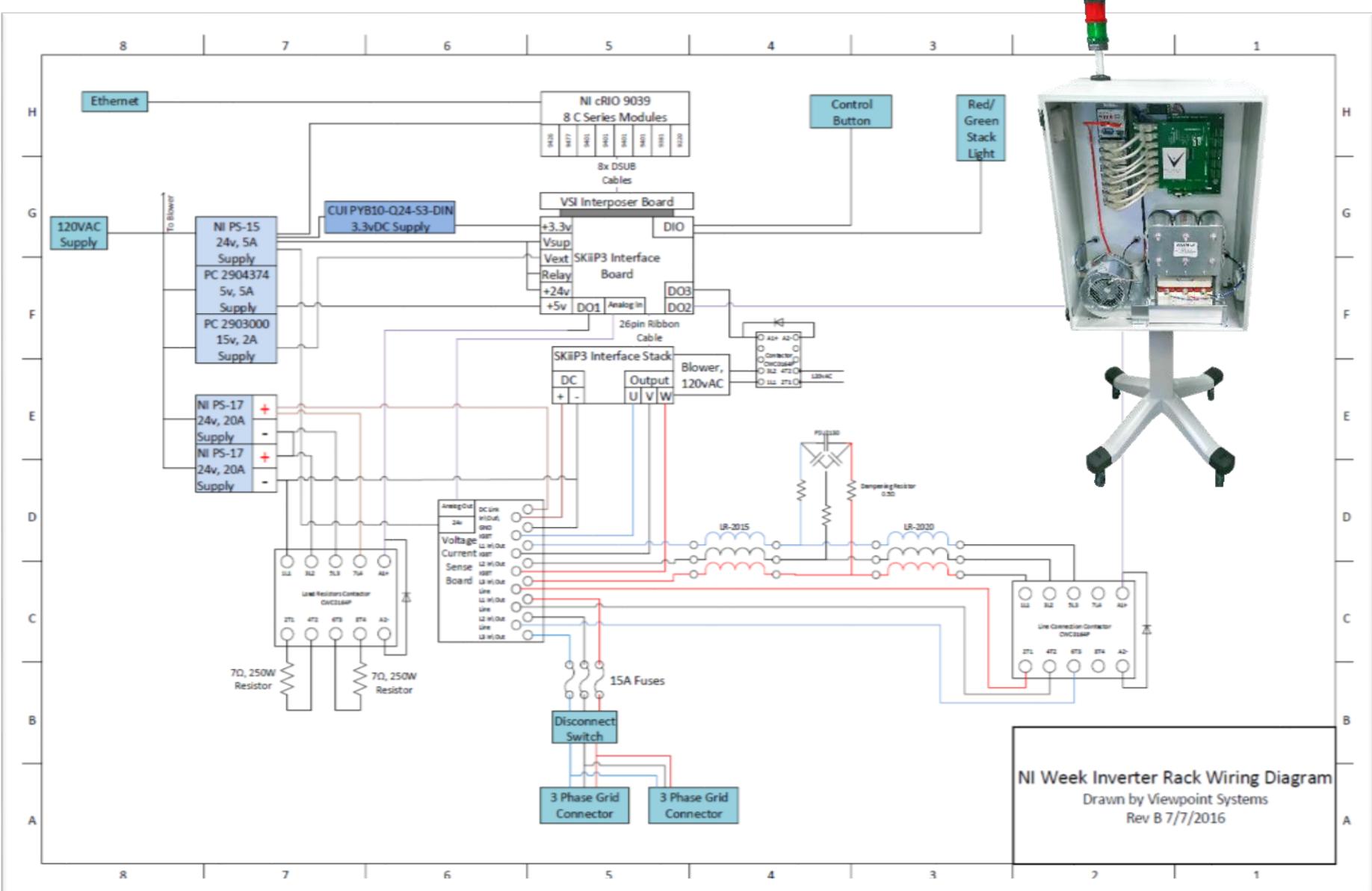


NI FPGA-Based Control System
With TSN Synchronization and
Embedded Digital Twin



LCL Line
Reactor Filter

Open Source Hardware Design



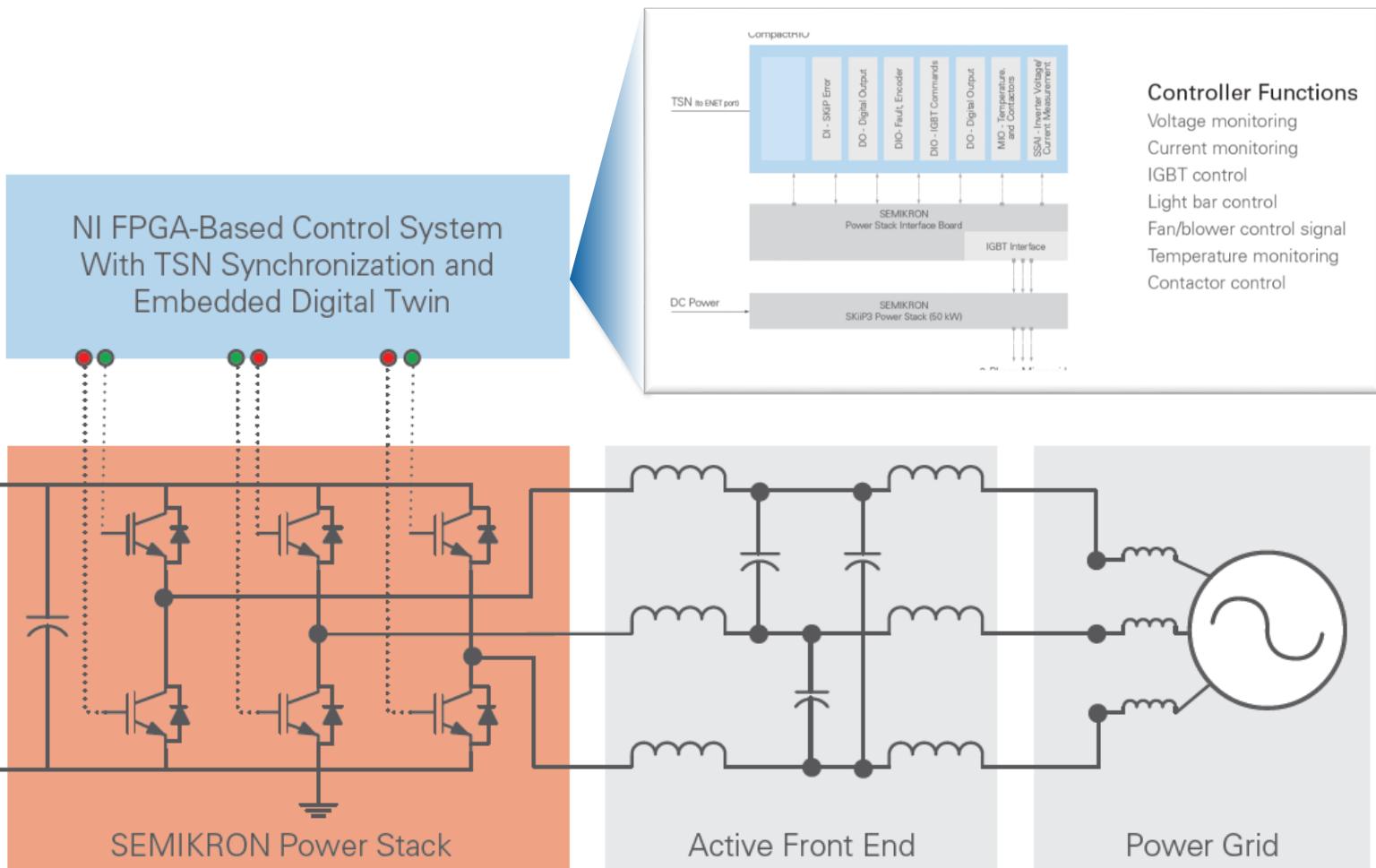


Open Source Hardware Design

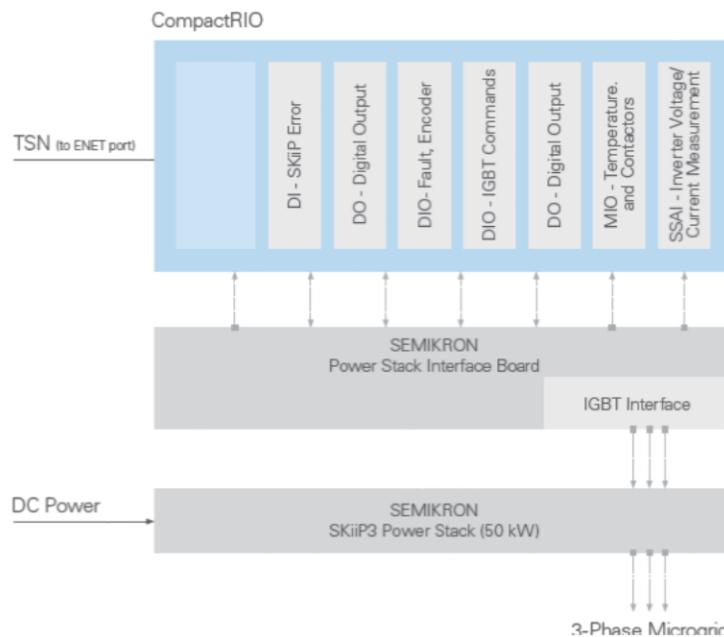
Name	Manufacturer	Part Number	Supplier	Quantity	Order Qty	Order Status	Cost	Extended Cost	URL
Inverter Cabinet									
1 Fan	Hammond	HF0416414	Javlin				2		
2 Grate	Hammond	HG0400404	Javlin				2		
3 Louver	Hammond	AVK34	Javlin				2		
4 Louver Filters	Hammond	AFLT34	Javlin				2		
5 Ethernet Panel Mount	LCOM	ECF504-SC6A	LCOM	1	4		\$15.95	\$63.80	http://www.l-com.com
6 120v input / switch	Schurter-Inc	486-2200-ND	Digikey	1	4		\$33.68	\$134.72	http://www.digikey.com
7 Power Cable	Tensility	839-1185-ND	Digikey	1	4		\$3.54	\$14.16	http://www.digikey.com
8 cRIO Power Supply	NI	PS-15	NI	1	4		\$0.00	\$0.00	
9 DC Bus Power Supply	NI	PS-17	NI	2	8		\$0.00	\$0.00	
10 Gate Driver Power Supply	Phoenix Contact	2903000	Digikey	1	10		\$48.76	\$487.60	http://www.digikey.com
11 Accessory Power Supply	Phoenix Contact	2904374	Digikey	1	4		\$59.00	\$236.00	http://www.digikey.com
12 Gate Driver Driver Supply	CUI	PYB10-Q24-S3-DIN	Mouser	1	5		\$44.11	\$220.55	http://www.mouser.com
13 Regen Resistor Contactor	WEG	CWC016-00-40L03	Automation Direct	1	4		\$22.50	\$90.00	http://www.automationdirect.com
14 Regen Resistor Diode	WEG	DICO-1C33	Automation Direct	1	4		\$1.50	\$6.00	
15 Regen Resistors	Vishay	FVE300-5.0-ND	Digikey	2	8		\$15.29	\$122.32	http://www.digikey.com
16 Regen Resistor Mounts	Vishay	HEIKIT1030300E293-ND	Digikey	2	8		\$9.10	\$72.80	http://www.digikey.com
17 Voltage Current Sense Board	VSI		VSI	1	0			\$0.00	
18 VI Board Power Connector	VSI		VSI	8	0			\$0.00	
19 VI Board Signal Connector	VSI		VSI	2	0			\$0.00	
20 VI Board Control Connector	VSI		VSI	3	0			\$0.00	
21 3phase LV Panel Connector	Anderson Power	SK2-076C04	Mouser	2	8		\$24.37	\$194.96	http://www.mouser.com
22 Inveter Fuses	Edison	MCL15	Automation Direct	3	2		\$69.00	\$138.00	http://www.automationdirect.com
23 Fuse Holder			Javlin	1					
24 3 Phase Contactor	WEG	CWC016-00-40L03	Automation Direct	1	2		\$22.50	\$45.00	http://www.automationdirect.com
25 3 Phase Contactor Diode	WEG	DICO-1C33	Automation Direct	1	2		\$1.50	\$3.00	
26 Grid Side Reactor	Automation Direct	LR-2020	Automation Direct	1	4		\$157.00	\$628.00	http://www.automationdirect.com
27 Dampening Resistor	TE Connectivity	A102448-ND	Digikey	3	12		\$3.84	\$46.08	http://www.digikey.com
28 Filter Capacitors	Cornell Dubilier	PSU2130	Digikey	3	12		\$17.12	\$205.43	http://www.digikey.com
29 Filter Cap Mounts	Cornell Dubilier	125565-06	Mouser	3	12		\$3.05	\$36.60	http://www.mouser.com
30 Inverter Side Reactor	Automation Direct	LR-2015	Automation Direct	1	4		\$147.00	\$588.00	http://www.automationdirect.com
31 SKiiP3 Inverter	Semikron	SKiiP3 613 GD123-3DUL	Semikron	1	3		\$0.00	\$0.00	
32 Blower Contactor	WEG	CWC016-00-40L03	Automation Direct	1	4		\$22.50	\$90.00	http://www.automationdirect.com
33 Blower Contactor Diode	WEG	DICO-1C33	Automation Direct	1	4		\$1.50	\$6.00	
34 SKiiP3 Interface Board	NI		NI	1	4		\$0.00	\$0.00	
35 SKiiP3 Ribbon Cable	NI		NI	1	4		\$0.00	\$0.00	
36 VSI Interposer Board	VSI		VSI	1	4		\$0.00	\$0.00	
37 37pin DSUB Cables	LCOM	CRMN37MF-1	LCOM	4	16		\$33.95	\$543.20	http://www.l-com.com
38 25pin DSUB Cables	LCOM	CRMN25MF-1	LCOM	4	16		\$20.65	\$330.40	http://www.l-com.com



Inverter Cabinets: Control System



NI FPGA-Based Control System With Ethernet TSN Synchronization



Controller Functions

- Voltage monitoring
- Current monitoring
- IGBT control
- Light bar control
- Fan/blower control signal
- Temperature monitoring
- Contactor control



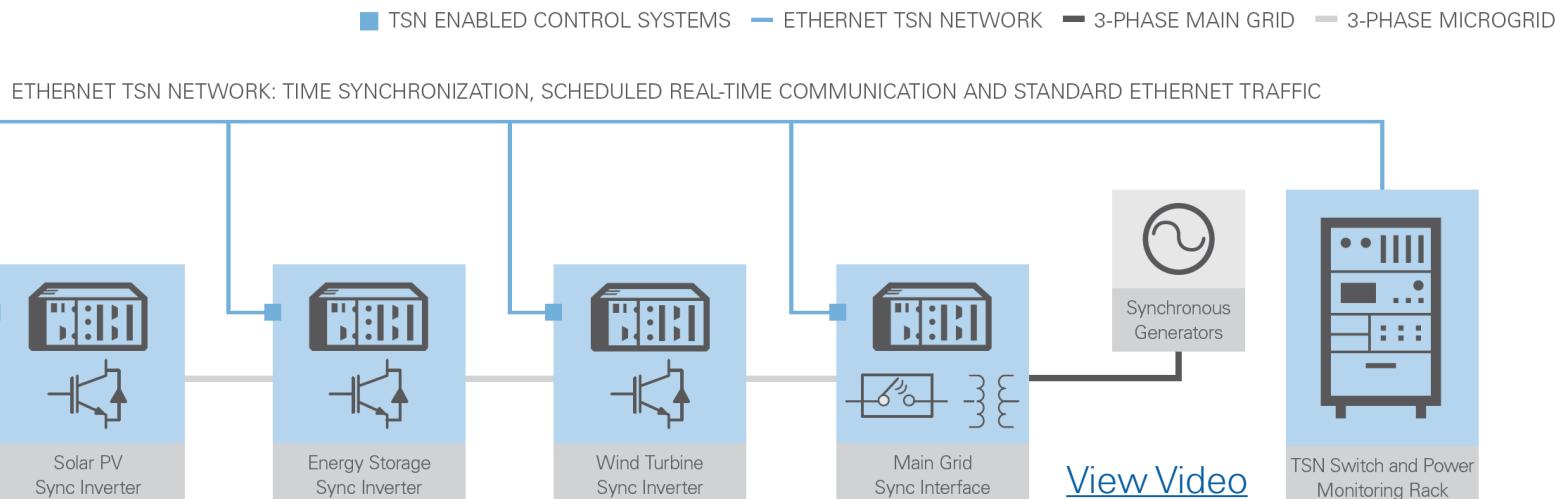
[784775-01](#) cRIO-9039 Sync CompactRIO Controller, 1.91 GHz Quad-Core CPU, Kintex-7 325T FPGA, TSN Synchronization

- New IEEE 802 standards that enable time synchronization and deterministic communication over standard Ethernet while maintaining interoperability with traditional “best effort” traffic.
- Major implications for smart grid and microgrid control.

Standard	Area	Title
IEEE 802.1ASrev, IEEE 1588	Timing & Synchronization	Enhancements and Performance Improvements
IEEE 802.1Qbu & IEEE 802.3br	Forwarding and Queuing	Frame Preemption
IEEE 802.1Qbv	Forwarding and Queuing	Enhancements for Scheduled Traffic
IEEE 802.1Qca	Path Control and Reservation	Path Control and Reservation
IEEE 802.1Qcc	Central Configuration Method	Enhancements and Performance Improvements
IEEE 802.1Qci	Time Based Ingress Policing	Per-Stream Filtering and Policing
IEEE 802.1CB	Seamless Redundancy	Frame Replication & Elimination for Reliability

DEMO: ACTIVE STABILIZATION OF THE POWER GRID WITH NEW SYNC INVERTER TECHNOLOGY

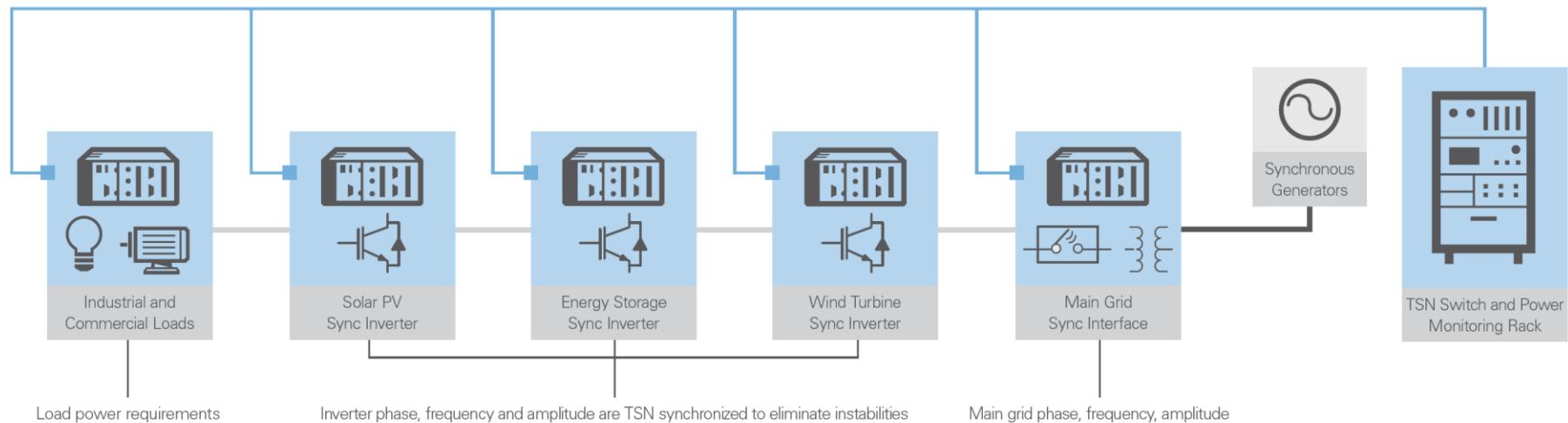
- The conventional control algorithms for renewable energy inverters can have a destabilizing effect on the power grid.
- New Sync Inverter technology enables every inverter to stabilize rather than destabilize the grid through synchronization and active voltage and frequency regulation.
- IEEE standard Ethernet Time Sensitive Networking (TSN) technology and new control algorithms (Qing-Chang Zhong, ORNL, NI) eliminate the need for spinning synchronous generators and enable up to 100 percent renewable energy based production.



ACTIVE STABILIZATION OF THE POWER GRID WITH NEW SYNC INVERTER TECHNOLOGY

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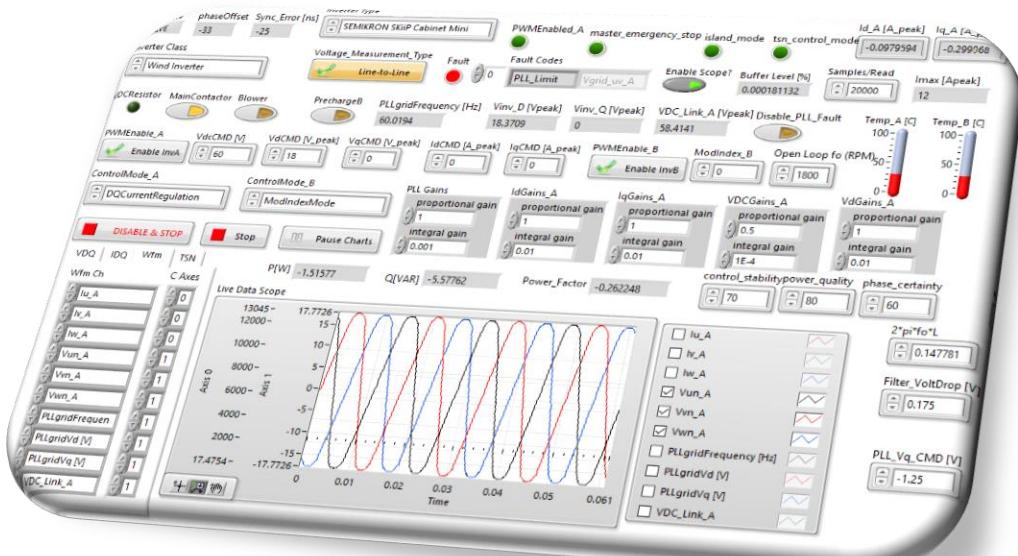
ACTIVE STABILIZATION OF THE POWER GRID WITH NEW SYNC INVERTER TECHNOLOGY

1. All grid tied inverters actively stabilize (rather than de-stabilize) the power grid by actively regulating voltage and frequency (rather than injecting current without regard to grid stability),
2. After a disconnection, islanded microgrid sections are reconnected reliably and without risk or delays by automatically aligning phase and amplitude,
3. The supply from renewable energy sources is automatically matched to demand, even over long distances (using fiber optic Ethernet links), faster than sags/swells and frequency disturbances propagate through power lines,
4. Islanded Microgrids are reliably operated with 100 percent renewable energy power electronics sources (rather than the majority of the power being required to come from diesel/natural gas synchronous generators)- instead at least X percent of power generation must come from Sync Inverters since they actively stabilize like synchronous generators,
5. The unintended circulating currents between inverters in high penetration applications is eliminated (compared to about 5 percent of rated power circulating using conventional field oriented control in the allowed case of 8 percent voltage THD) resulting in higher energy efficiency and improved control stability gain/phase margins,
6. Forced manual curtailment of renewable energy production by operators due to the risk of over/under-supply issues is reduced, allowing a higher percentage of power generation to come from renewable energy sources,
7. The amount of spinning reserve generation required to offset the destabilizing effect of current source inverters is reduced (which today has the unfortunate effect of mitigating the environmental benefits of renewable energy production),
8. The cost of installing synchronous condensers and other “band aid” mitigations to counteract the power quality and stability issues created by conventional renewable energy inverter control systems is eliminated (by requiring all inverters to actively stabilize the power grid like synchronous generators do),
9. The lifetime of power electronics transistors is actively managed by the control application to give investors a better assurance of Return On Investment, and OEM equipment manufacturers a reduced risk of pre-mature failures resulting in unexpected warranty recalls (which in the past resulted in bankruptcy for small OEMs).

Open Source Reference Design Software



- State of the art, conventional open-source vector field oriented control code for synchronous reference frame bidirectional three-phase inverter active front end (AFE) with control loops for real and reactive power (power factor). Features include:
- The ability to operate as standard current source inverters, or as grid forming voltage source inverters with voltage and frequency regulation
 - Cascaded DQ axis current and voltage regulation with optional DC link voltage regulation
 - Voltage/Frequency (V/F) regulation mode supports seamless transition from grid tied to islanded mode with pre-arm capability and configurable voltage engagement threshold
 - Voltage/Frequency (V/F) regulation mode supports cascaded D and Q axis current regulation
- Online configurable control settings including control mode, PWM carrier frequency, control loop tuning, filtering, limits, etc.



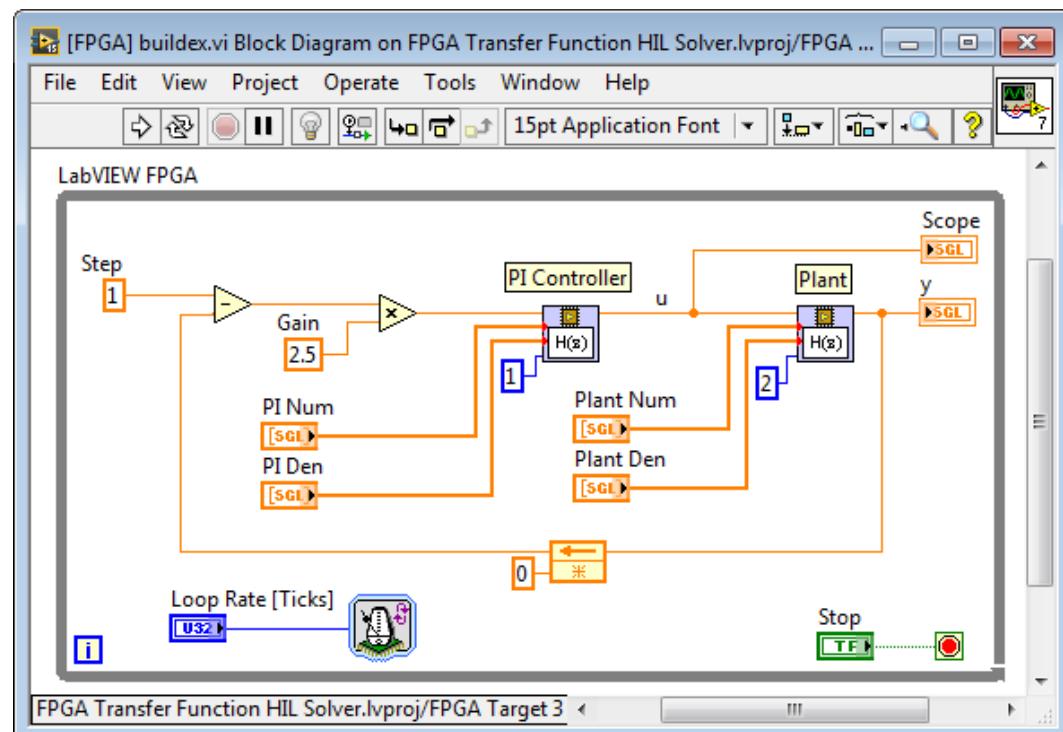
Open Source Reference Design Software



- Synchronous Reference Frame (SRF) bi-directional active front end control features include grid voltage feedforward, line reactor cross decoupling terms, DC link voltage scaling, advanced current limiting, rate limiting, enable delay timers, setpoint tracking limits
- Built in “logic analyzer type” simultaneous data capture, web streaming and triggered TDMS format data logging for over 80 channels of physical measurements, calculated values, control registers, etc.
- Automatic fault waveform recording to non-volatile storage with pre, during and post event capture along with configurable event capture
- All measurement and control signals are in SI units of Volts and Amps for intuitive interpretation/understanding of results
- FPGA based high speed fault handling with 50 nanosecond response time
- 1547 anti-islanding with enable/disable capability
- Instantaneous power analysis for P, Q, S, and power factor
- Built in control stability analyzer for measuring open/closed loop bode plots with gain and phase margin analysis- supports professional control tuning and apples to apples A/B test comparison between control algorithms
- Advanced current limiting and thermal modeling capability
- Option for embedded real-time simulation digital twin for advanced IOT prognostics, auto-tuning, parameter identification, lifetime extension, etc.
- Option for AC induction motor variable frequency drive (VFD) control mode
- Option for Ethernet TSN control mode with +/- 100 nanosecond time synchronization between the control systems and kHz speed real-time communication for control coordination

Pop Quiz!

What does this code do?



Pop Quiz!

THIS IS LABVIEW FPGA!

Implementation:

Single Precision Floating Point

Performance:

2.95 microseconds (339 kHz)

339 times faster than real-time

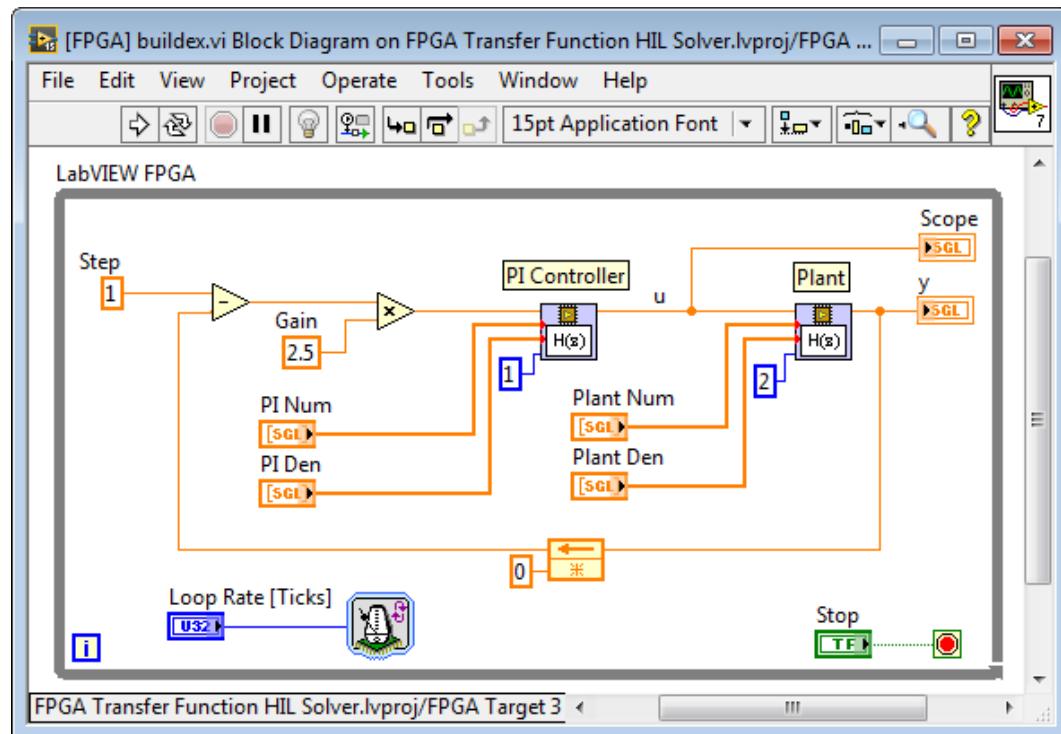
FPGA Resources (Spartan-6 LX45):

Slice Registers: 3.6% (1953 out of 54576)

Slice LUTs: 11.1% (3018 out of 27288)

DSP48s: 34.5% (20 out of 58)

Block RAMs: 0.0% (0 out of 116)



[Download the LabVIEW FPGA Floating Point Toolkit](#)

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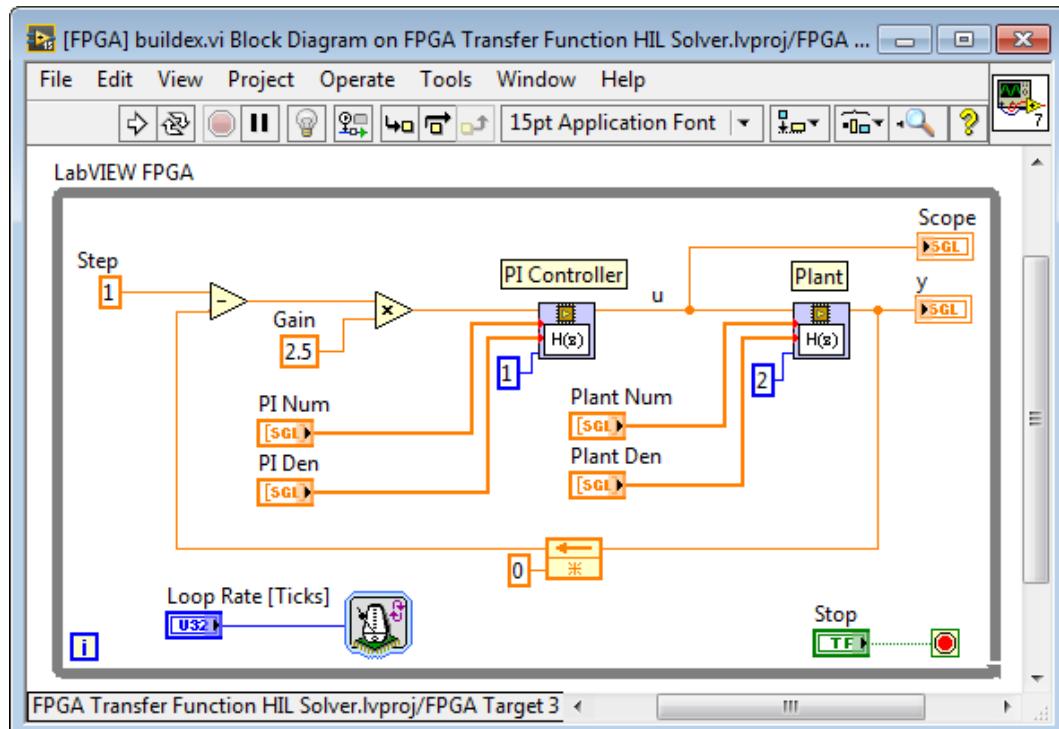
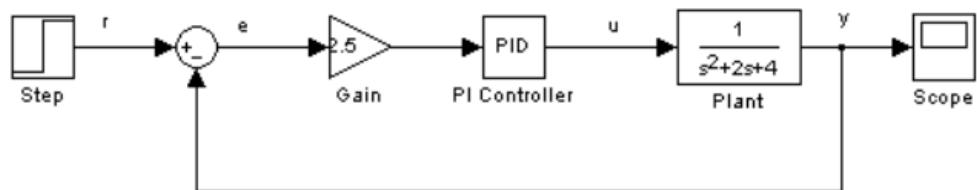
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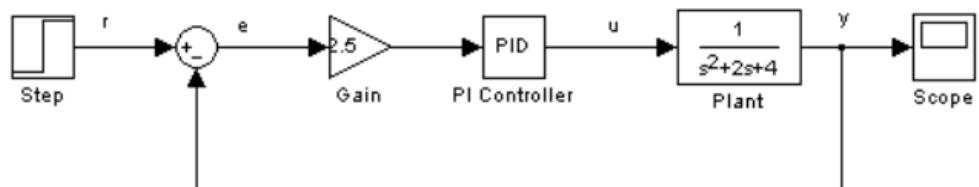


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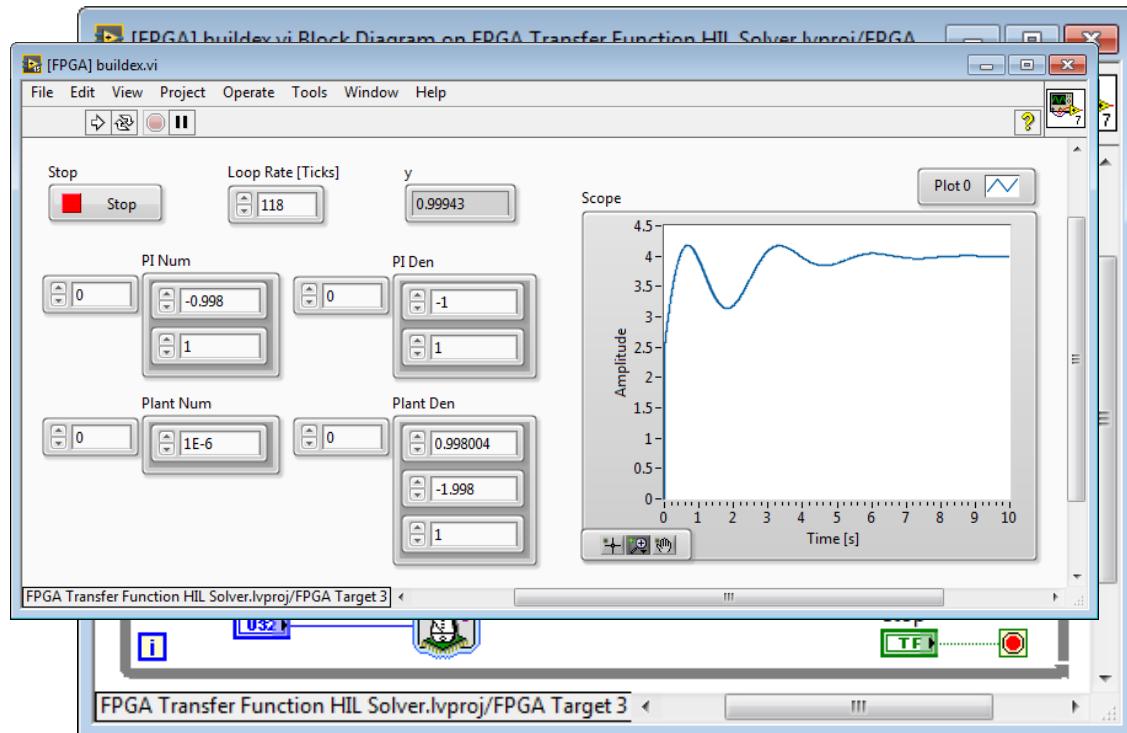
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Demo: Open Source Reference Design Software

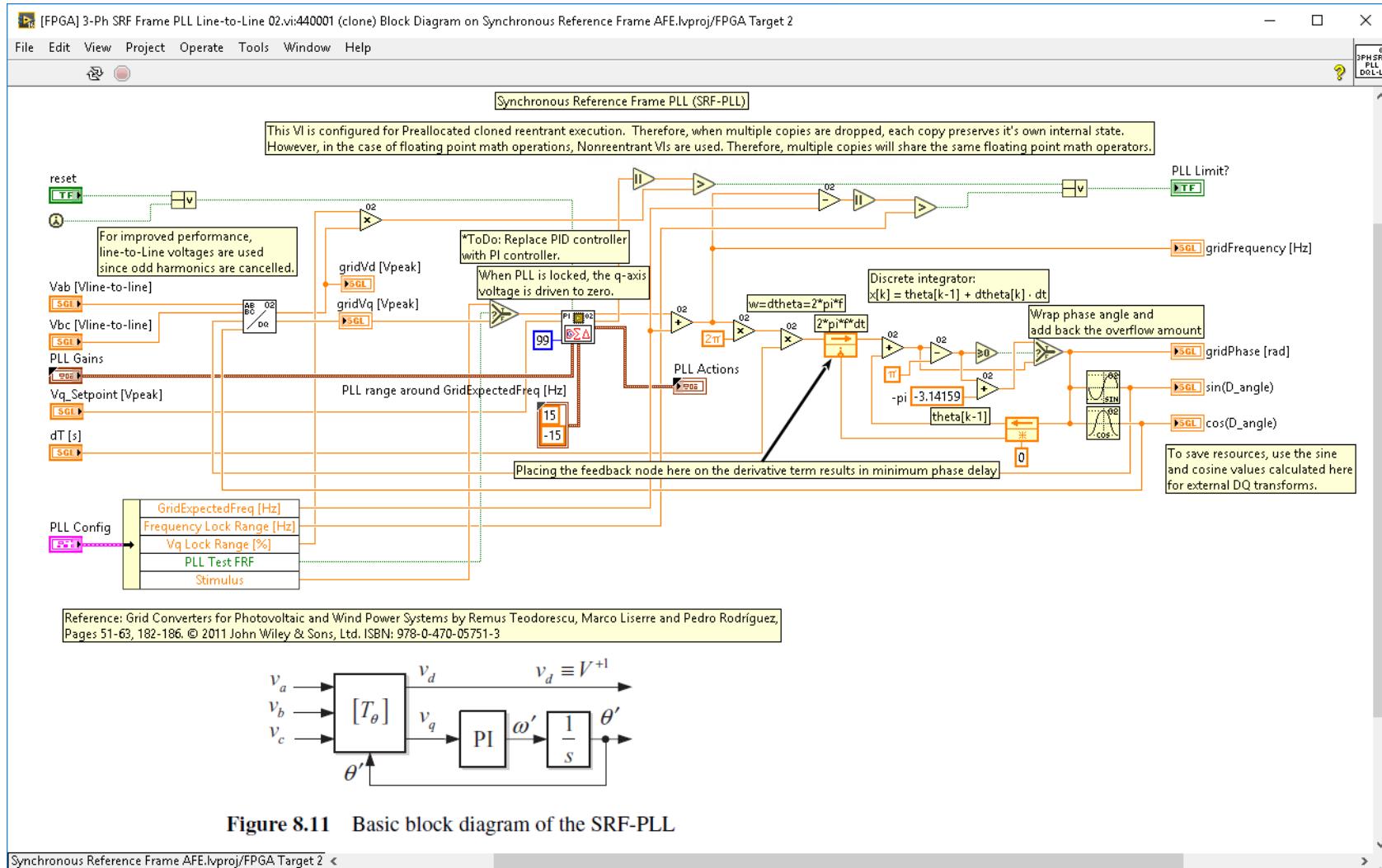


Figure 8.11 Basic block diagram of the SRF-PLL

HOW TO GO FROM PAPER TO ~~PROTOTYPE~~ IN DAYS

1. “3D print” your own custom control chip using reconfigurable FPGA hardware with high level graphical floating point tools
2. Be 95 percent confident before you compile by developing your control algorithms in a variable timestep co-simulation environment
3. Start with open source IP core libraries and reference design frameworks (rather than reinventing the wheel)
4. Deploy to industry proven, commercially deployable embedded control and I/O systems
5. Don’t create a “prototype” - create a “minimum viable product”

Demo Video:

[Self-Synchronized Universal Droop Controller: Paper to Prototype in Three Days](#)



HOW TO GO FROM PAPER TO MINIMUM VIABLE PRODUCT IN DAYS

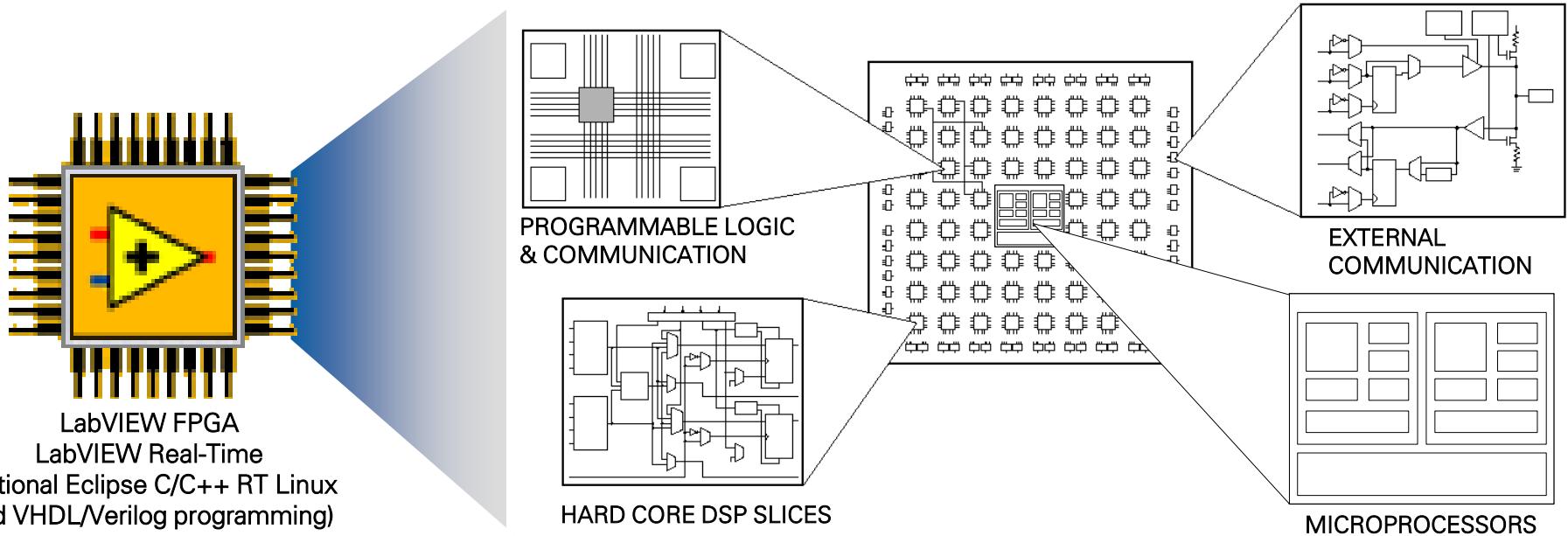
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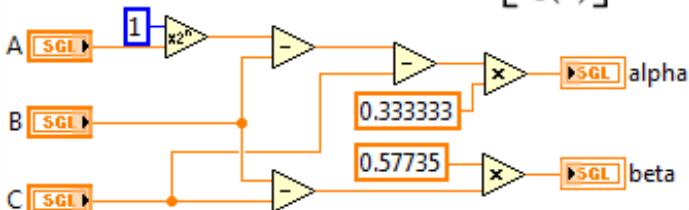
[Self-Synchronized Universal Droop Controller: Paper to Prototype in Three Days](#)



SOC FPGA: Embedded System 3D Printer

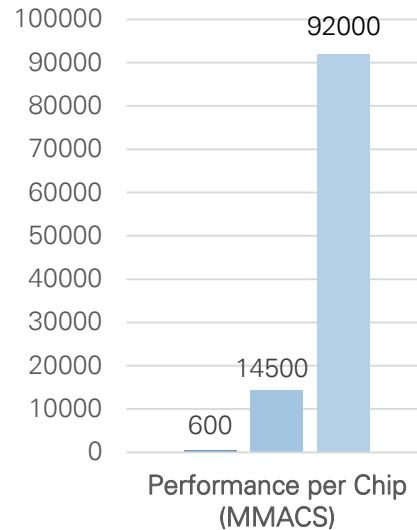
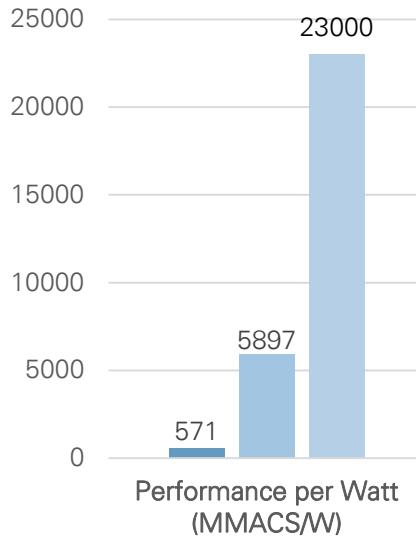
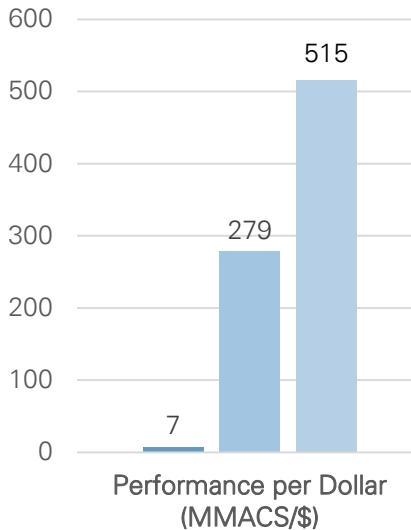


$$i_{\alpha\beta}(t) = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix}$$



"In the past it took us several times longer for a full custom design for a DSP-based circuit board prototype, which then had to be redesigned for volume commercialization after the field trials. We could not have loop frequencies above about 40 kHz, even with a highly skilled DSP programmer. With FPGA, everything is truly running in parallel so I don't have timing problems. I'm able to program the FPGA using LabVIEW and run loops in nanoseconds on the NI General Purpose Inverter Controller. We can now have commercial hardware out for field testing in 3 months." – [Eaton Corporation](#)

Traditional DSP vs. System-on-Chip (SOC) FPGA



- 2 Core DSP
- 58 DSP Core SOC FPGA
- 220 DSP Core SOC FPGA

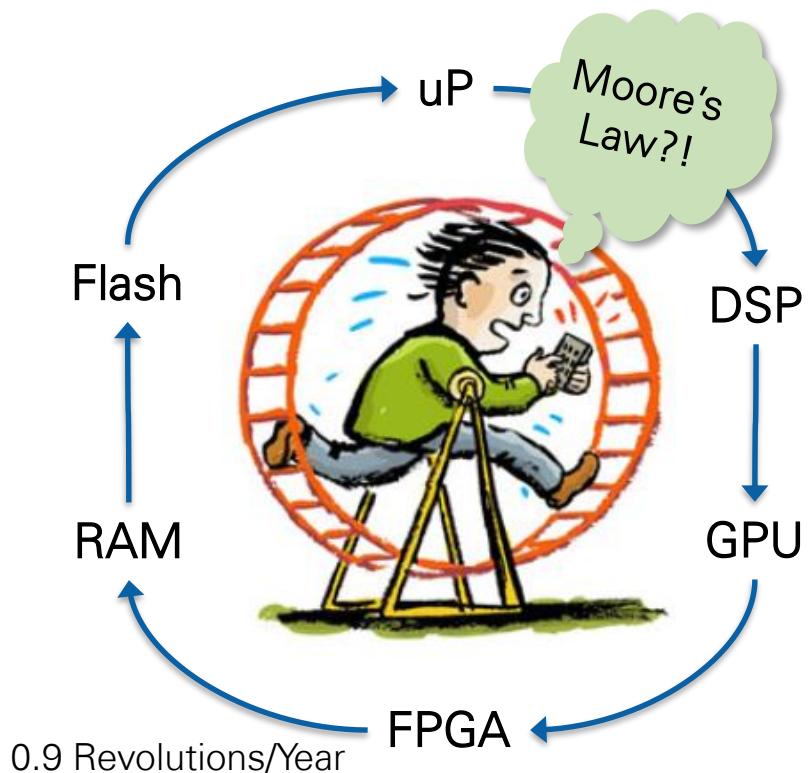


NI General Purpose
Inverter Controller (GPIC)

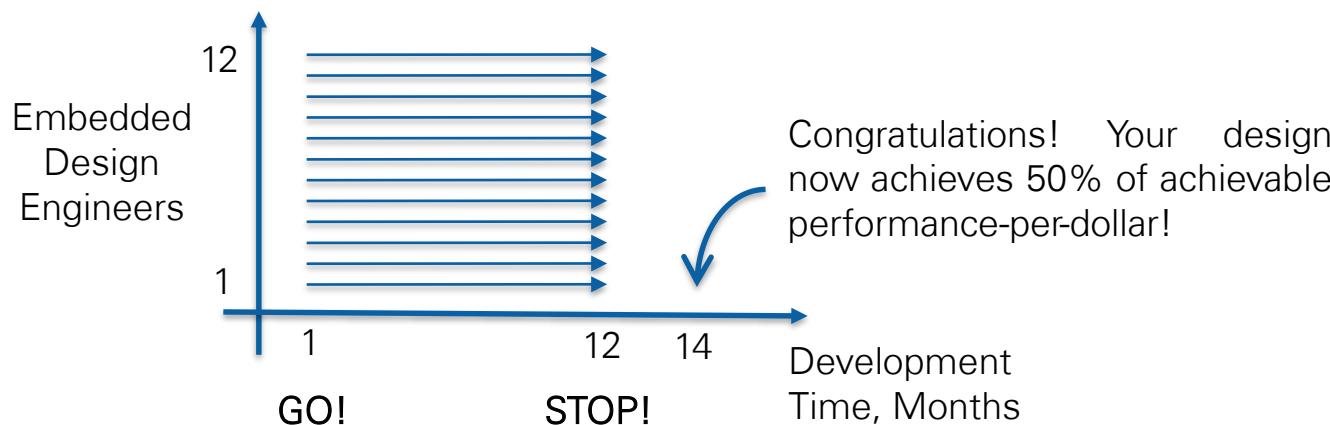
	Performance Ratio (Spartan-6/DSP)	Performance Ratio (Zynq-7020/DSP)
MMACS per Chip	24	94
MMACS per Watt	10	31
MMACS per Dollar	40	69

MMACS = Multiply-accumulate operations per second
(measure of DSP computing performance)

The Problem with Moore's Law

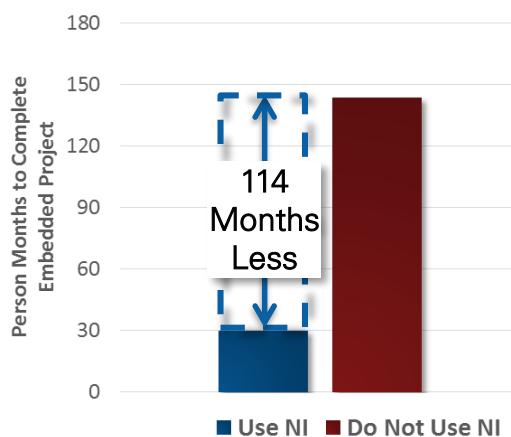


- The hamster wheel of embedded hardware technology makes a complete rotation every 14 months
 - Performance-per-dollar doubles
- Traditional embedded design takes about 12 engineers working for 12 months:
 - 144 person-months
 - 12 person-years
 - \$1.44M at \$100,000/person/year

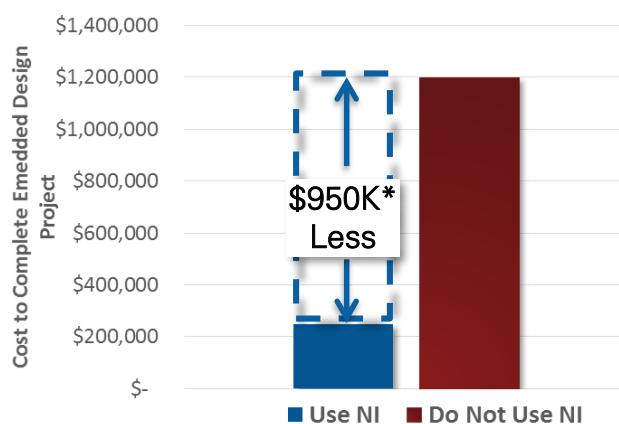


The results are in: Improved approach to embedded design delivers a 4X advantage

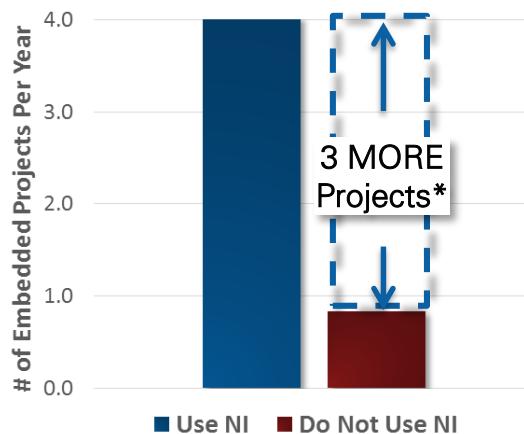
What More Could Your Business do with an Additional 114 Months?



What Could You Change in Your Products to Win More Business?



What More Could You do with 3 Additional Embedded Projects /Year with the Same Development Budget?



Based on data from Wilson Research Group, 2012 National Instruments/UBM Survey of Embedded Markets, January – April 2012

* Assumes \$100K per engineer fully burdened cost/year.

Does not include additional cost such as high-end EDA tools required for custom design – if included your advantage using NI increases.

[View Survey Results](#)

The UBM/EETimes study included 1,648 responses from embedded engineers from Americas, Europe and Asia (margin of error +/- 2.0%). The Wilson Research study included 443 responses NI embedded design customers from Americas, Europe and Asia (margin of error +/- 3.9%).



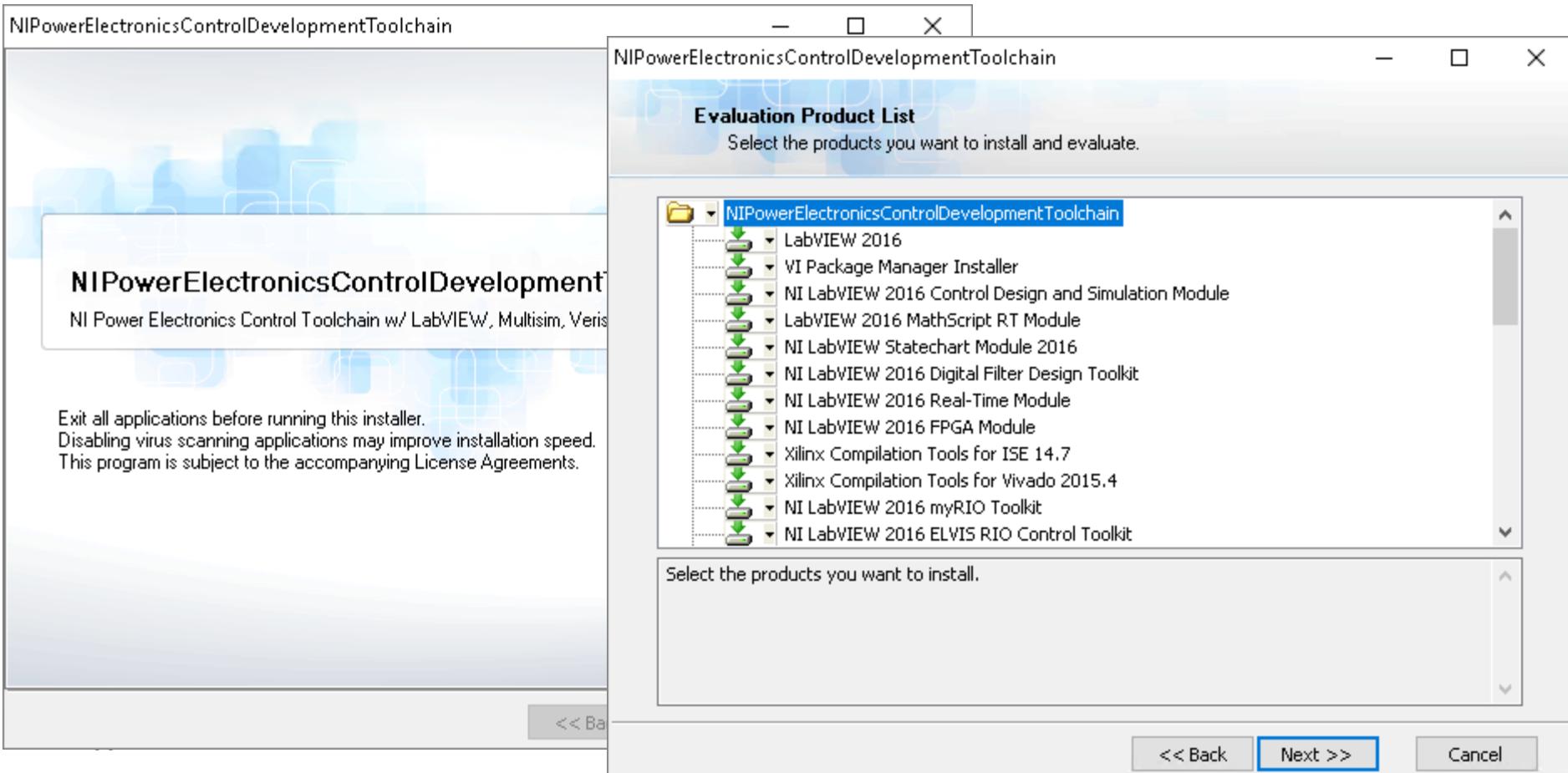
Step 1! Download and Install the Development Tools

Download ZIP file:

<ftp://ftp.ni.com/evaluation/powerdev/NIPowerElectronicsControlDevelopmentToolchain.zip>

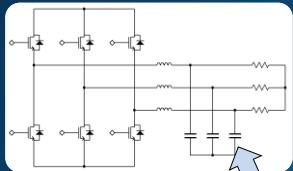
Download individual files:

<ftp://ftp.ni.com/evaluation/powerdev/devtools/>



Comprehensive Power Electronics Control Design Toolchain

Co-Simulation Based Development
(Multisim, LabVIEW FPGA, IP Cores)



Design

$$i_{\alpha\beta}(t) = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix}$$

Mini-Scale Control Development System



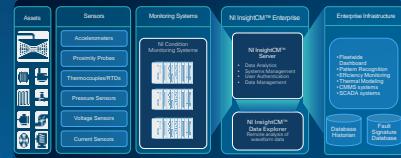
Prototype

Remote Support

HIL Testing

Deploy

Industrial Internet of Things
(InsightCM SDK)



Full Power Digital Dyno Test Rigs



Real-Time HIL Simulation
(Veristand, OpalRT, StarSim, El. Motor Sim)



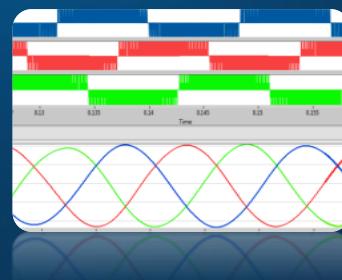
Commercial Deployment
(General Purpose Inverter Controller)



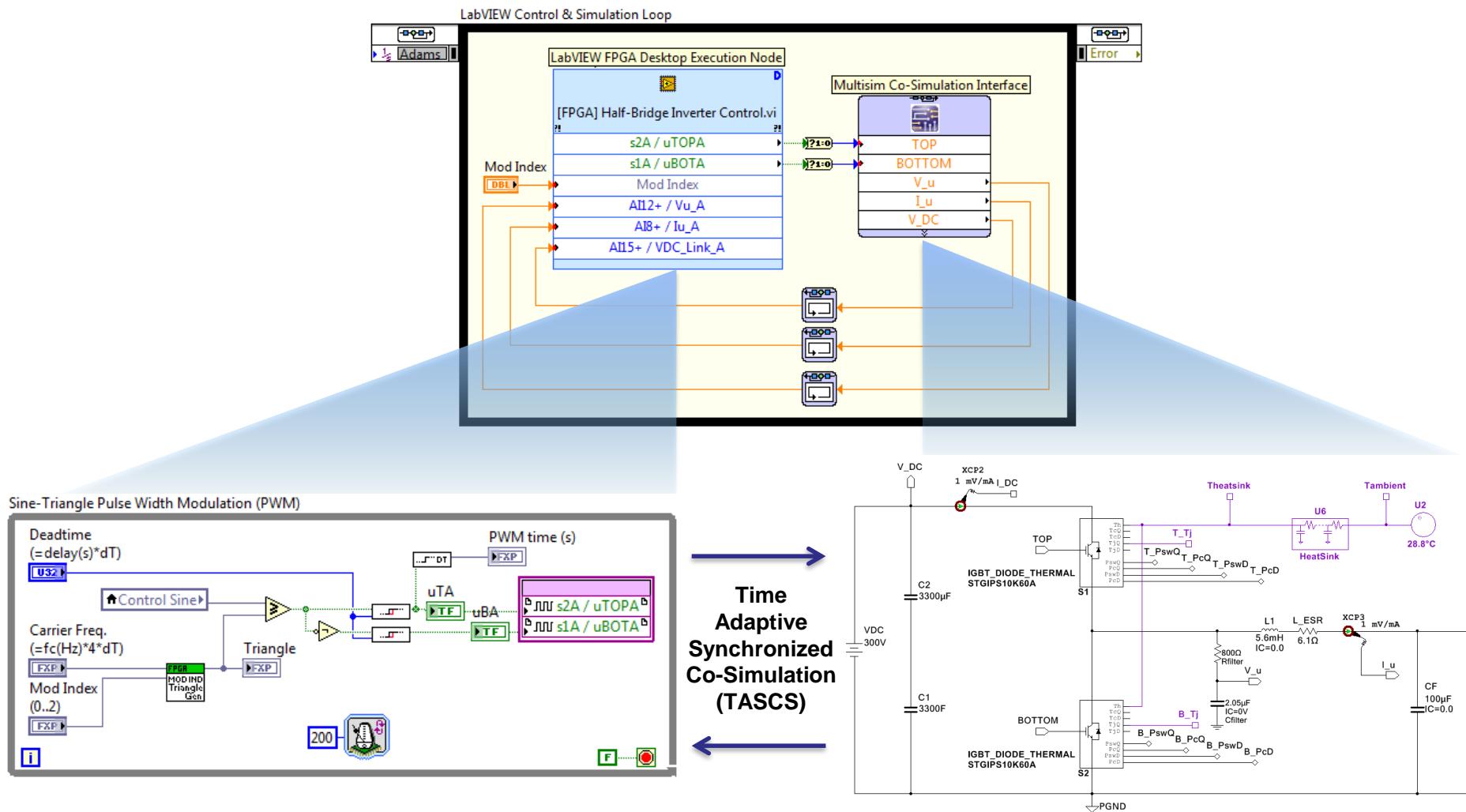
Utility Networking Toolkits
(DDS, IEC-61850, DNP3, ...)



Power Measurement Suite
(IEC EN 61000, 50160, ...)



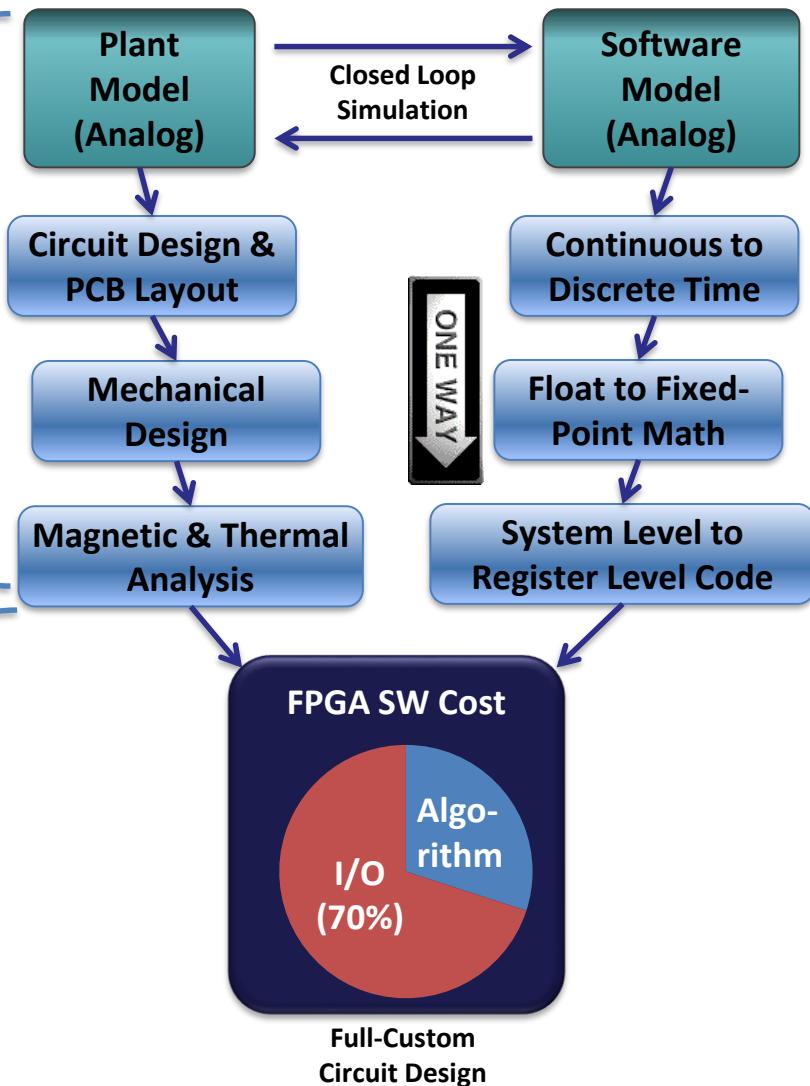
Co-Simulation Based FPGA Control Design



Reducing the Simulation to Deployment Cycle from Weeks to Hours

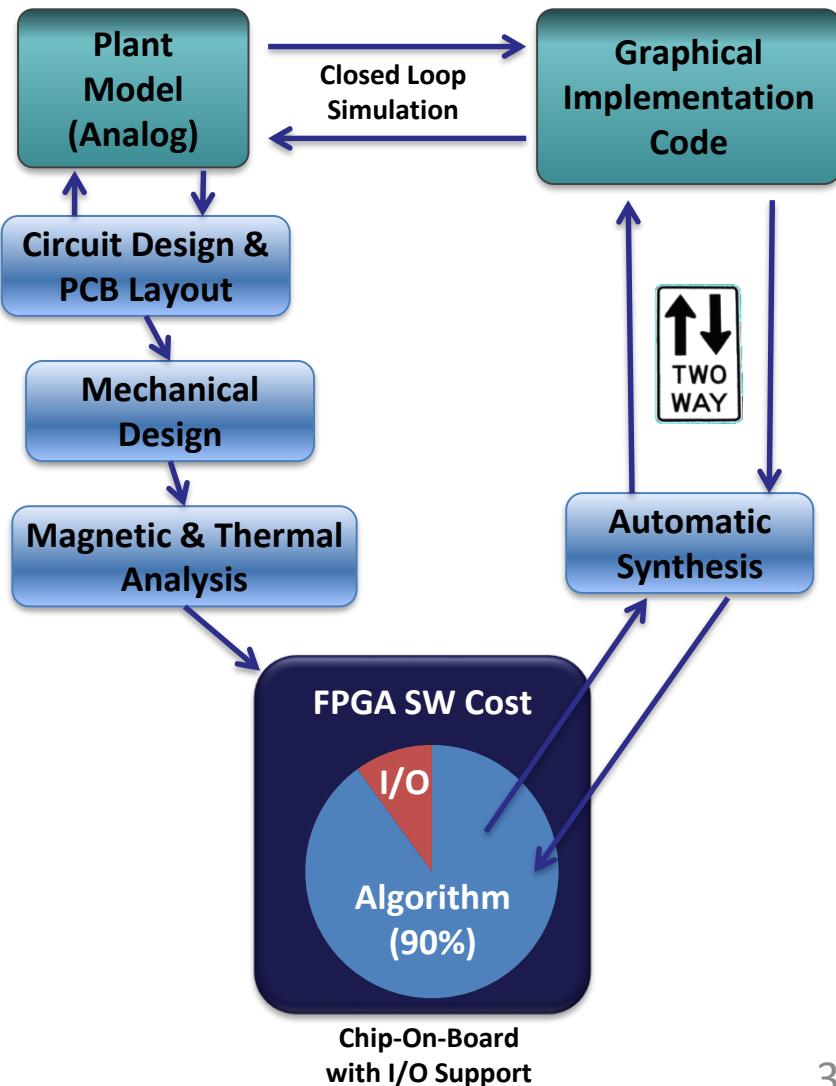
Traditional Methodology

Simulation Context



NI LabVIEW RIO Toolchain

Simulation Context



[Download conference papers](#)

LabVIEW FPGA Open Source IP and Examples Library

Guide to Power Electronics Control Application Examples and IP Cores for NI GPIC

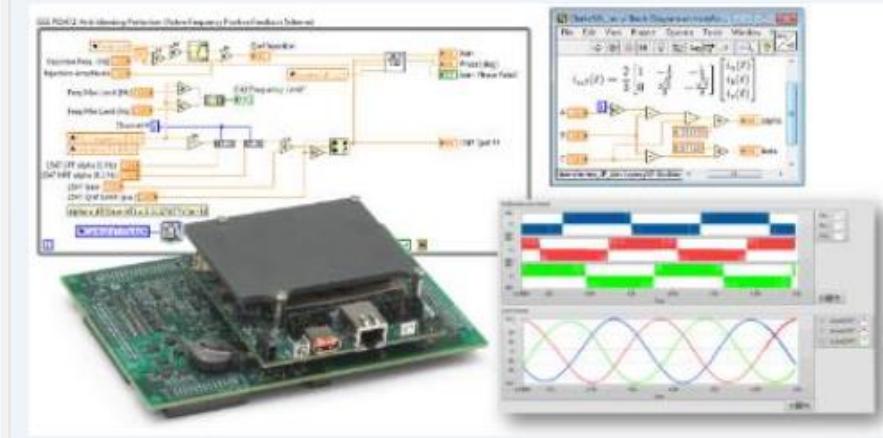
Updated March 16, 2016. Please download the latest library using the link below. See the bottom of this post for details.

This document is a guide to LabVIEW FPGA power electronics control examples and IP.

Dozens of open source example apps. Examples: 3-phase bidirectional active front end (AFE), induction motor VFD (V/Hz, FOC), buck-boost energy storage converter, isolated bidirectional DC (IBDC), ...

Hundreds of open source IP cores. Examples: Field oriented control transforms (i.e. ABC to DQ), sine-triangle PWM, space-vector PWM, PID control, 1547 anti-islanding, FRF control stability analyzer, ...

[Click here to download the library.](#) Unzip to a short path (not desktop). LabVIEW 2015 development toolchain is **required** (see announcement above titled "What tools do I need to get started developing power conversion equipment?"). Examples and IP are provided for both sbRIO-9607 GPIC and sbRIO-9606 GPIC targets when available. The path locations below assume you have unzipped the library in a directory named "C:\LabVIEW 2015".



Open Source Reference Design Software Architecture

Remote System Management Utilities for Design Team & Operators

Live Data Stream, Logging

Configuration Management

Control Tuner, Stability Analyzer

Data Analytics

Remote Update

SCADA Systems

Operator HMI, PLC

External Controllers

Linux Real-Time: Eclipse C/C++, Simulink®, LabVIEW RT

ENET: TCP/IP, UDP, HTTPS, FTP

DDS, DNP IEC-61850

RS-232 Modbus

ENET, CAN, 1588

Supervisory State Machines

Live Data Scope (10-20 kHz)

Automatic Fault Logging

Single-Point and Streaming Network Comm.

Software Updater (RAD)

Matlab® Simulink®

Global Optimizer, Machine Learning

Reconfigurable DSP/FPGA Fabric (LabVIEW FPGA, HDL)

AXI/PCI: Host Memory Buffer, Single Point I/F, DMA Streaming I/F

PID, PLL, State-Space, Transfer FN

Transforms (ABC to DQ), Power Analysis, Harmonic Comp.

SVPWM, SPWM, Custom PWM

Control State Machines

Fault Handler, Protection Interlocks

Acquisition, Scaling, Limits, Filtering

I Limiting, Active Junc Temp Reg.

Digital Twin Observer / Predictor

Input / Output Board (GPIB)

RIO Mezzanine Connector (RMC)

Gate Command HBDO (14)

Simultaneous AI (16)

Scanned AI, AO (8,8)

Relay Control DO (4)

Sinking DO (24)

Sourcing DI (28)

FPGA IOB LVTTL (32)

Custom Interface PCB

Stack Gate Drivers, Fiber TX

Grid I/V, Stack I/V, Stator/Rotor I/V, Battery I/V, DC Link

Case Temperature, DC Link, Monitoring

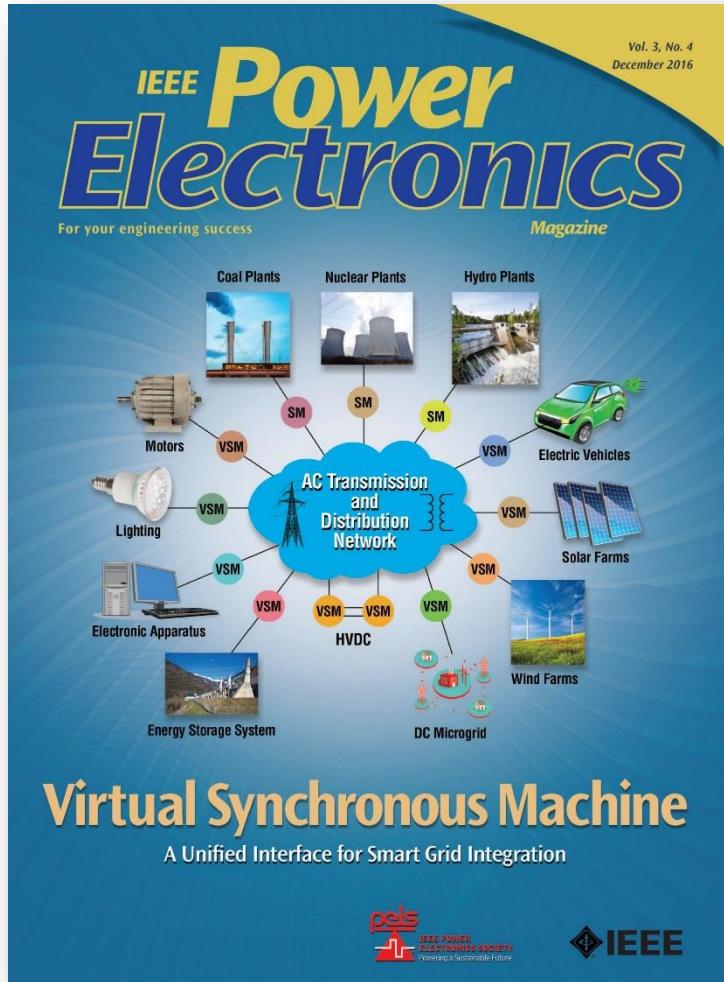
Pre-Charge, Line, DC Contactors

Pilot Relays, Fans/Pumps, Faults, Resets, Indicator Lights

Over-Current Comparators, Desat., Over-Temp, Auxiliary, E-Stop, Door open

Fiber RX/TX, Redundancy, Time Sync, Mux, Custom Protocols, HBDO, ADCs

DEMO: GO FROM PAPER TO MINIMUM VIABLE PRODUCT IN 3 DAYS



Demo Video:
[Self-Synchronized Universal Droop Controller: Paper to Prototype in Three Days](#)

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Digital Object Identifier: <https://doi.org/10.1109/ACCESS.2016.2616875>

Self-Synchronized Universal Droop Controller

QING-CHANG ZHONG^{1,2}, (Senior Member, IEEE), WEN-LONG MING², AND YU ZENG²

¹Department of Electrical and Computer Engineering, Illinois Institute of Technology, Chicago, IL 60616, USA
²Department of Automatic Control and Systems Engineering, The University of Sheffield, Sheffield, S1 3JD, U.K.
Corresponding author: Q.-C. Zhong (zhongqc@iit.edu)
This work was supported by EPSRC, U.K., under Grant EP/J01558X/1.

ABSTRACT In this paper, a self-synchronization mechanism is embedded into the universal droop controller (UDC), which is applicable to inverters having an impedance angle between $-\pi/2$ rad and $\pi/2$ rad, to form a self-synchronized UDC (SUDC). Both the voltage loop and the frequency loop of the UDC are modified to facilitate the standalone and grid-connected operation of inverters. Importantly, the dedicated phase-locked-loop that is often needed for grid-connected or parallel-operated converters is removed. The inverter is able to achieve synchronization before and after connection without the need of a dedicated synchronization unit. Since the original structure of the UDC is kept in the SUDC, the properties of the UDC, such as accurate power sharing and tight output voltage regulation, are well maintained. Extensive experimental results are presented to demonstrate the performance of the proposed SUDC for a grid-connected single-phase inverter.

INDEX TERMS Grid-connected inverters, universal droop controller (UDC), phase-locked-loop, self-synchronization, smart grid integration, parallel operation.

I. INTRODUCTION

Due to global warming and environmental crisis, renewable energy systems in smart grids, e.g., wind, solar and tidal power, have been extensively studied during the last few decades [1]–[3]. When the amount of such renewable energy exceeds a certain level, it is inevitable that they will be required to take part in the regulation of system frequency and voltage in smart grids. This means numerous power inverters will be connected to the power grid, which are practically operated in parallel. For such applications, droop control is widely considered as a key technique to regulate the power flow between renewable energy sources and power grid [1], [2], [4]–[10], due to its simple structure and the independence from external communication.

Grid-connected inverters can be operated in the islanded and grid-connected mode. In the islanded mode, the main control objective is to achieve accurate load sharing among inverters and voltage regulation. Sharing linear and non-linear loads equally has been extensively investigated [11]–[16] and high accuracy of equal sharing can be achieved. In order to achieve accurate proportional sharing, it was required that the inverters in parallel operation should have the same per-unit output impedance, which is difficult to be satisfied in practice. This problem is solved in [17] with a robust droop controller to achieve accurate proportional sharing without the need of having the same per-unit output impedances for all the inverters. In addition, the load voltage drop due to the load effect and the droop effect is significantly reduced. However, inverters can have different types of output impedance, which requires changing the form of the droop controller. Recently, the requirement on the same type of output impedance for droop control is removed in [18], where it is mathematically proven and experimentally validated that the robust droop controller proposed in [17] originally for R-inverters can actually be applied to all practical inverters having an impedance angle between $-\frac{\pi}{2}$ rad and $\frac{\pi}{2}$ rad, without the need of knowing the type or value of the impedance. In other words, it is a universal droop controller (UDC) [18].

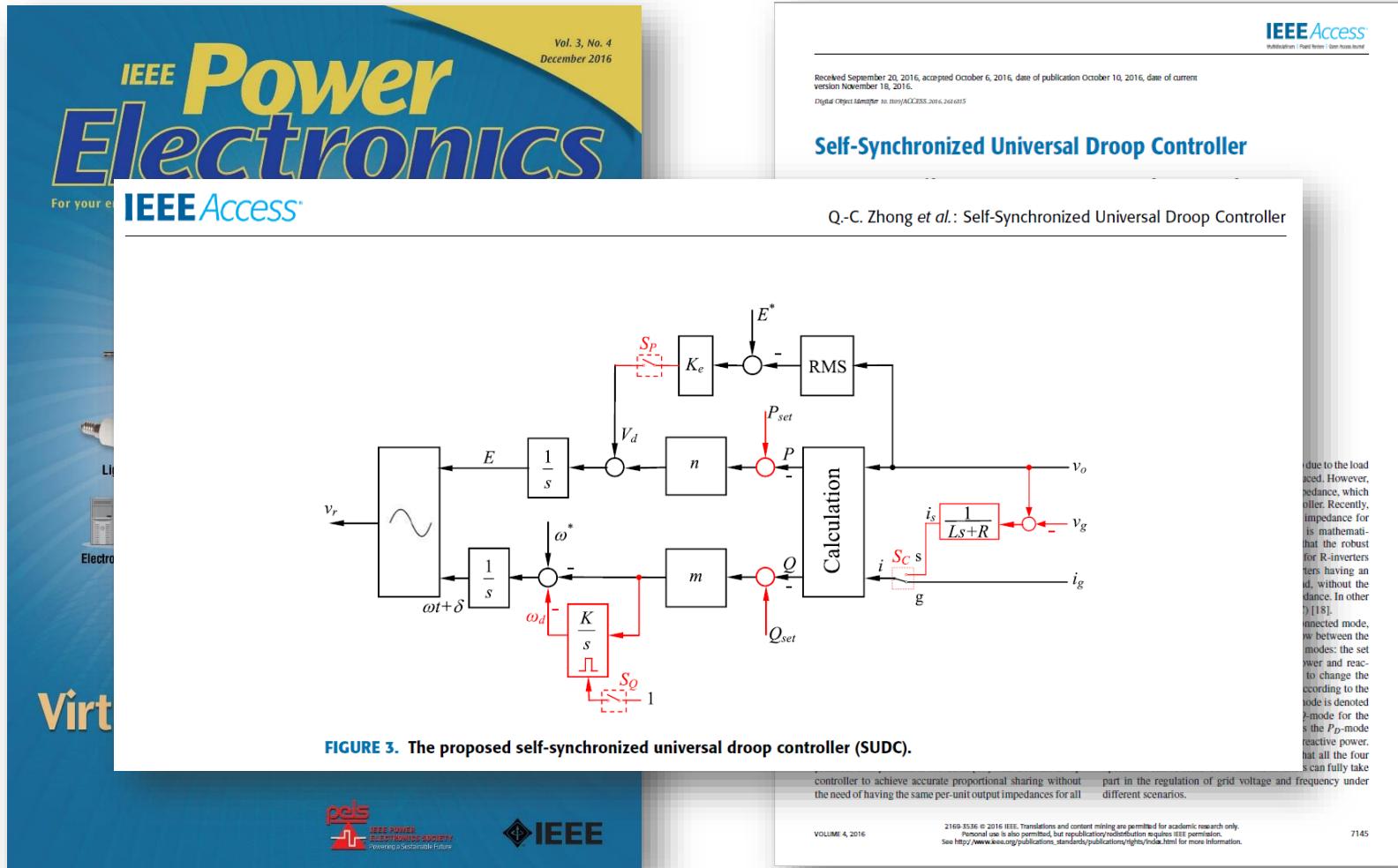
When an inverter is operated in the grid-connected mode, the main objective is to regulate the power flow between the inverter and the grid. There are two different modes: the set mode to send the desired amount of real power and reactive power to the grid and the droop mode to change the real/reactive power exchanged with the grid according to the grid frequency/voltage. In this paper, the set mode is denoted as the *P*-mode for the real power and the *Q*-mode for the reactive power; the droop mode is denoted as the *P_D*-mode for the real power and the *Q_D*-mode for the reactive power. For grid-connected inverters, it is expected that all the four operations can be achieved so that the inverters can fully take part in the regulation of grid voltage and frequency under different scenarios.

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Self-Synchronized Universal Droop Controller: Paper to Prototype in Three Days

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References:

Qing-Chang Zhong, "Robust Droop Controller for Accurate Proportional Load Sharing Among Inverters Operated in Parallel"
<http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=5754573>

Qing-Chang Zhong, Wen-Long Ming, Yu Zeng, "Self-Synchronized Universal Droop Controller"
<http://ieeexplore.ieee.org/document/7587397/citations>

Static synchronous generators, US Patent 8880236 B2
<https://www.google.com/patents/US8880236>

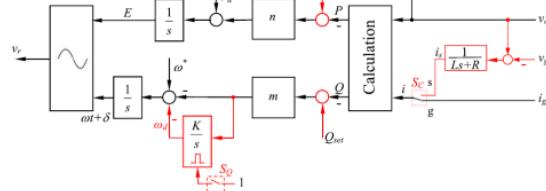
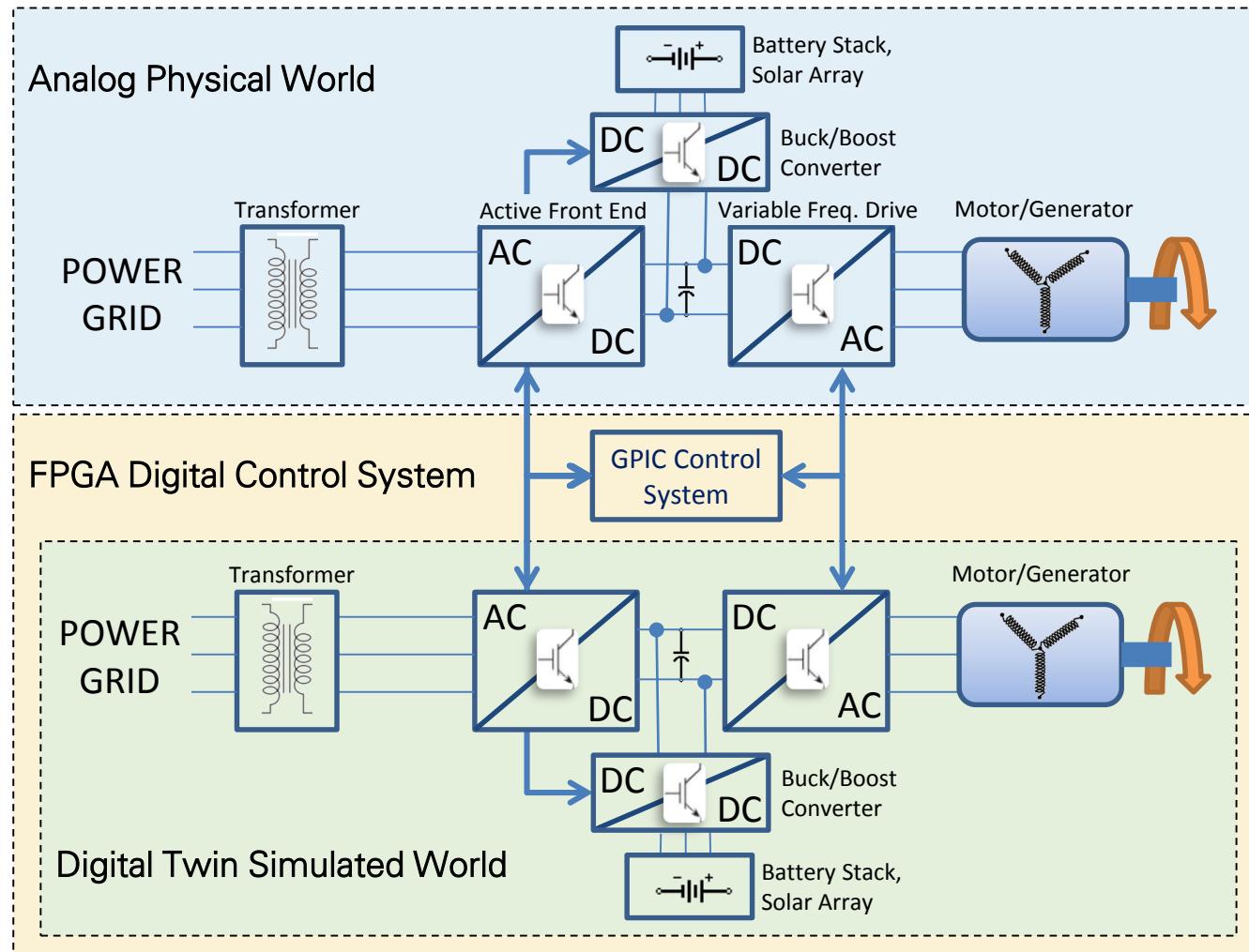


FIGURE 3. The proposed self-synchronized universal droop controller (SUDC).



Demo Video:
[Self-Synchronized Universal Droop Controller: Paper to Prototype in Three Days](#)

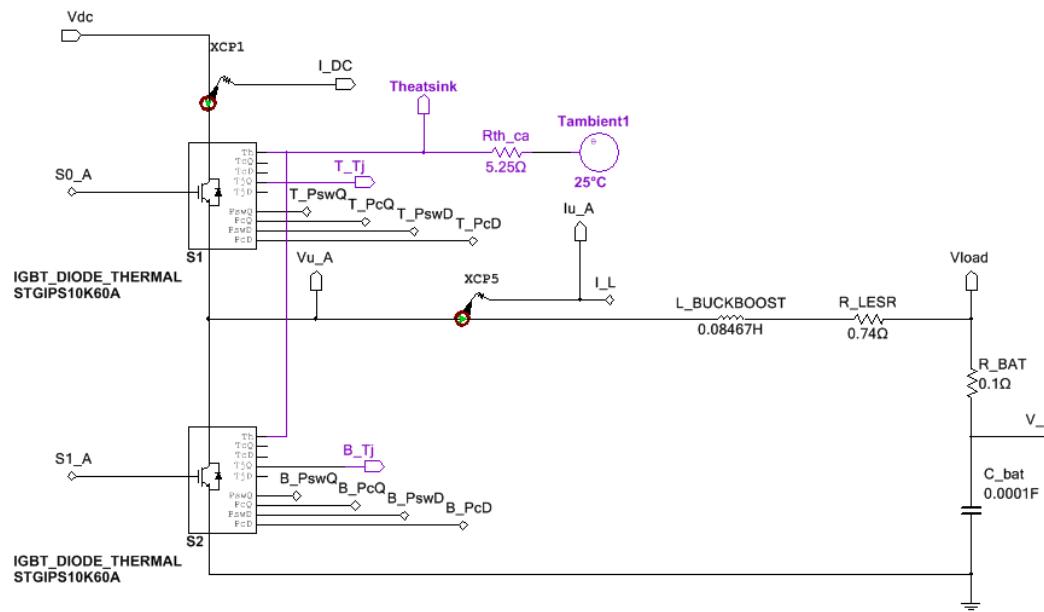
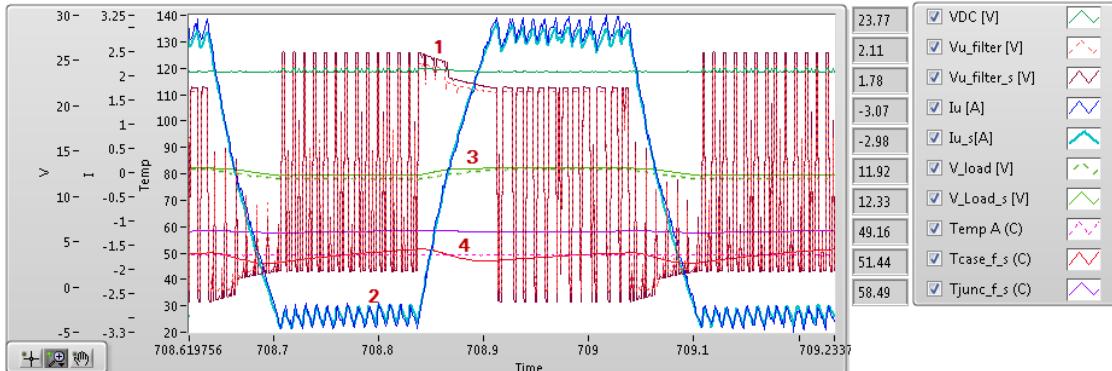
FPGA BASED CONTROL SYSTEM WITH LOCAL REAL-TIME DIGITAL TWIN



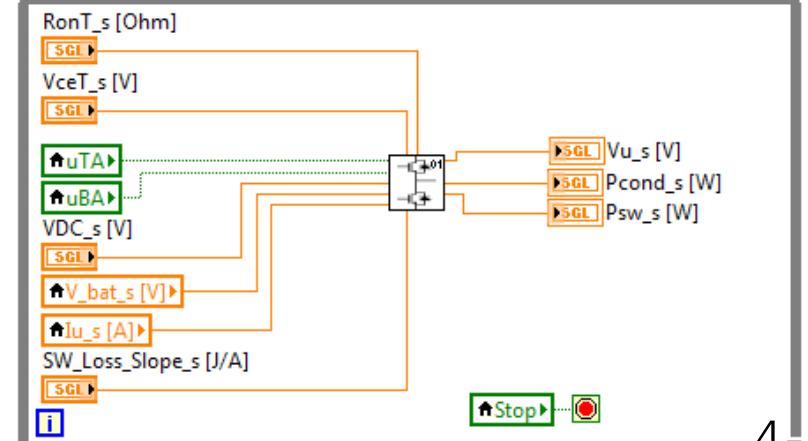
Buck-Boost Energy Storage Converter with Embedded Real-Time Digital Twin for Active Junction Temperature Regulation

1. IGBT half-bridge output voltage (red)
2. Battery Charge/Discharge Current (blue)
3. Battery Terminal Voltage (green)
4. Case Temperature (red)

SINGLE IGBT HALF-BRIDGE DATA
(PHYSICAL MEASUREMENT vs. DIGITAL TWIN)



LabVIEW FPGA Half-Bridge Converter Digital Twin w/ Conduction and Switching Losses



EMBEDDED DIGITAL TWIN APPLICATIONS BY STAKEHOLDER

- **SYSTEM DESIGN TEAM**

- **Model Validation:** Continuous online validation of the model during field deployments closes the loop with the design team and confirms or rejects the assumptions on which their design decisions are based.
- **Design Optimization:** Digital twin models combined with advanced machine learning algorithms facilitates design optimization that spans the boundaries between the physical system design and the control algorithms to satisfy multiple design objectives. Example: Optimize the design for energy efficiency, cost reduction, and uptime

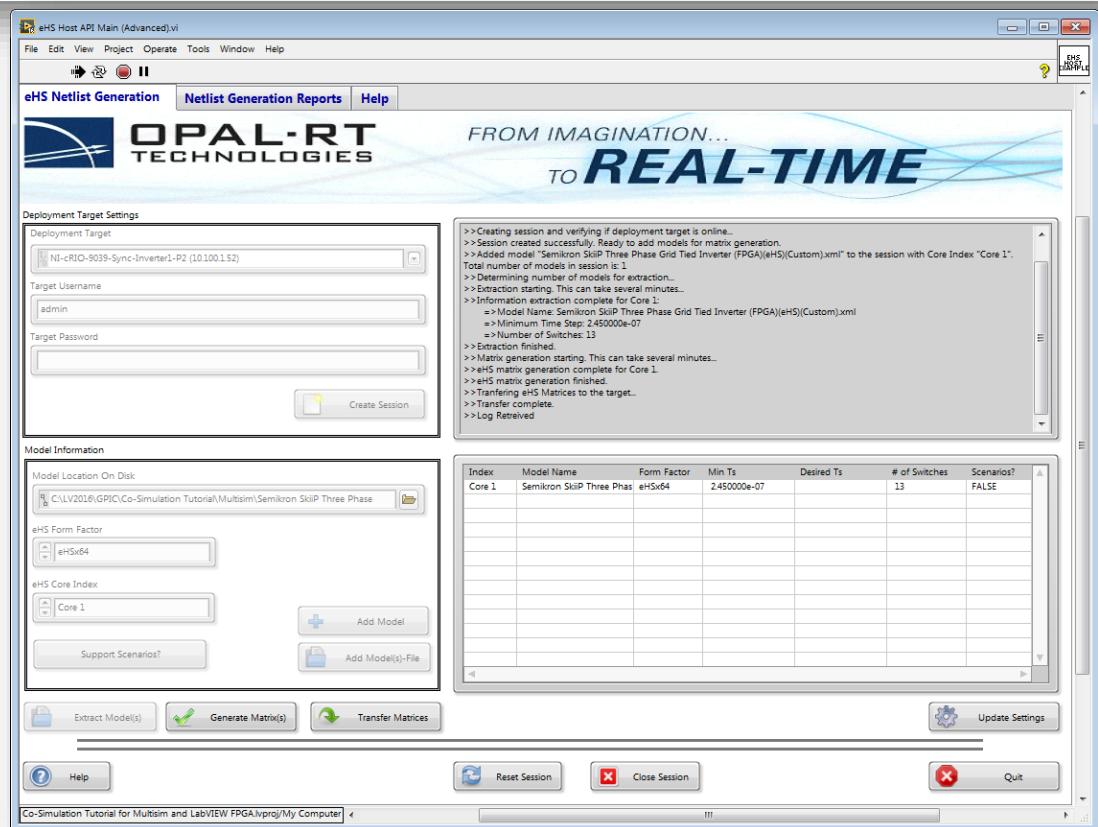
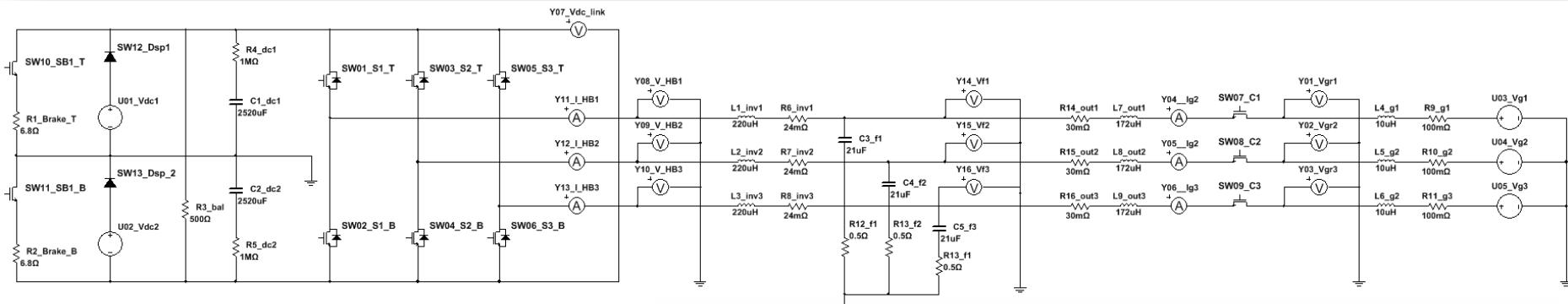
- **CONTROL DESIGN TEAM**

- **Observer-based Control:** Many internal states in cyber-physical systems cannot be physically measured but are modeled in the digital twin and can be used as feedback signals for control. Example: IGBT junction temperature active regulation
- **Delay Removal:** Time delays are very problematic for control systems and can be removed in the digital twin model. “Zero delay” digital twin signals can be used as feedback signals for control. Example: Zero delay temperature control
- **Automatic Online Re-Tuning:** The digital twin model combined with advanced machine learning algorithms can be used to find the optimal tuning gains that satisfy multiple linear and non-linear control objectives. Example: Simultaneous tuning of cascaded control loops for setpoint tracking, stability, and IEEE 1547 compliance objectives.
- **Predictive Control:** Faster than real-time digital twin models can be used to explore multiple control strategies before committing to one.

- **OPERATIONS & MAINTENANCE TEAM**

- **Prognostics:** A mismatch between the physical system response and the digital twin may indicate a problem. The digital twin endows the control system with an expectation for the system response, enabling problems to be detected long before a failure occurs.
- **Lifetime Extension:** Digital twins can include models for component lifetime, which can be incorporated in the control strategy to extend lifetime and increase reliability.

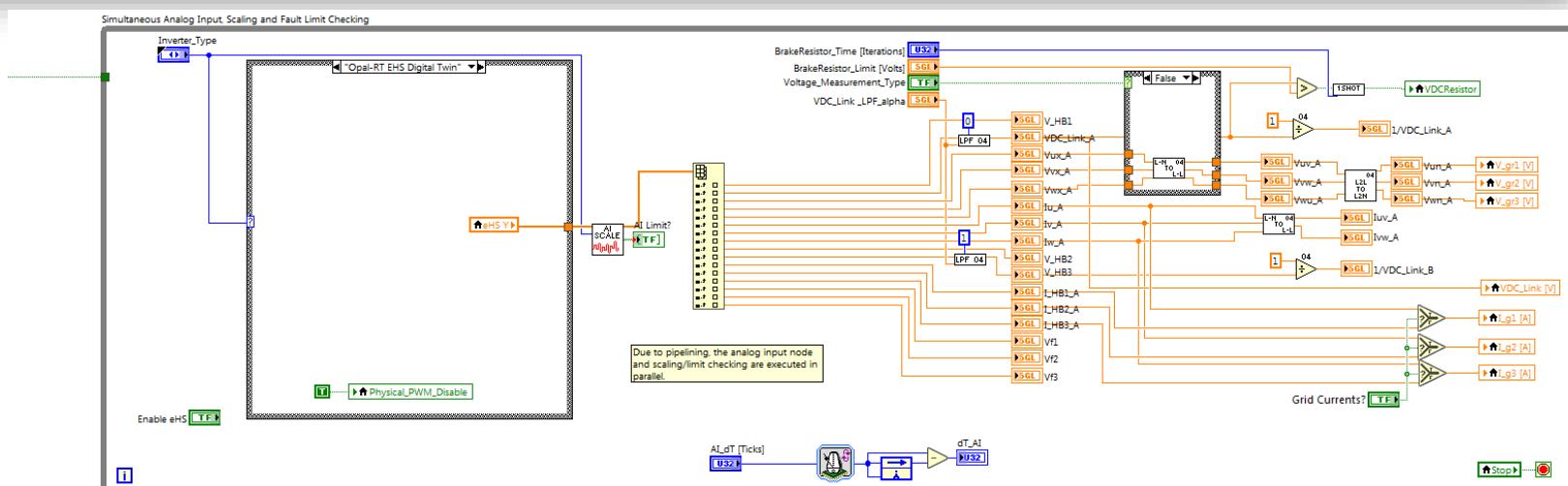
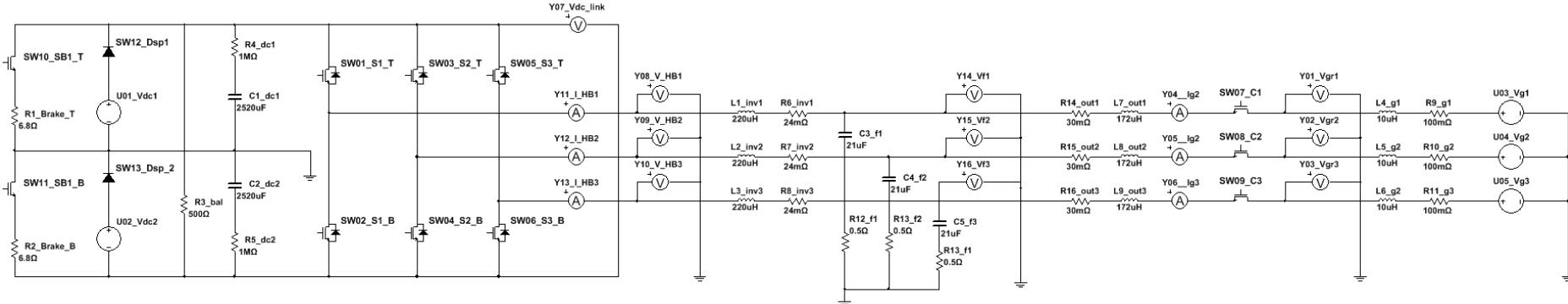
DEMO: OPAL-RT EMBEDDED DIGITAL TWIN – AUTOMATIC MULTISIM MODEL DOWNLOAD FOR FPGA SOLVER



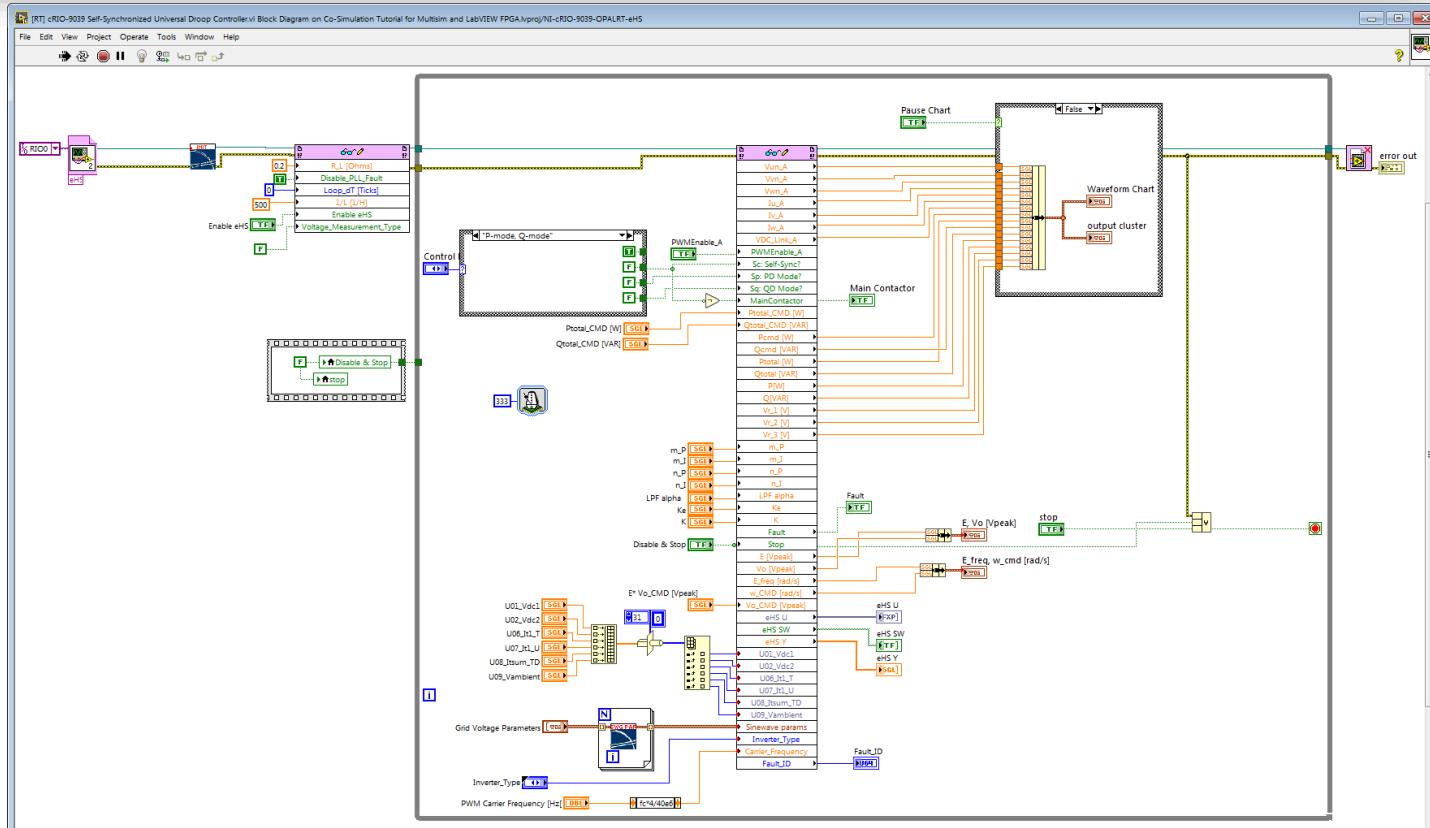
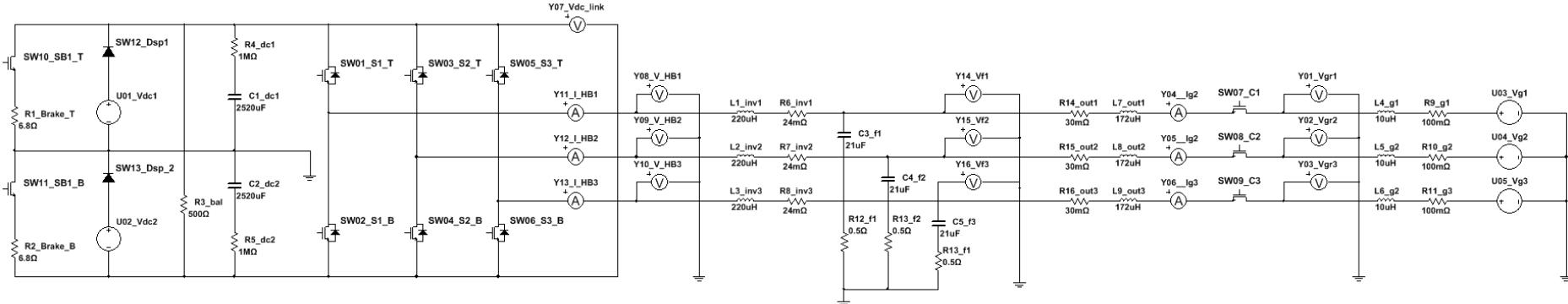
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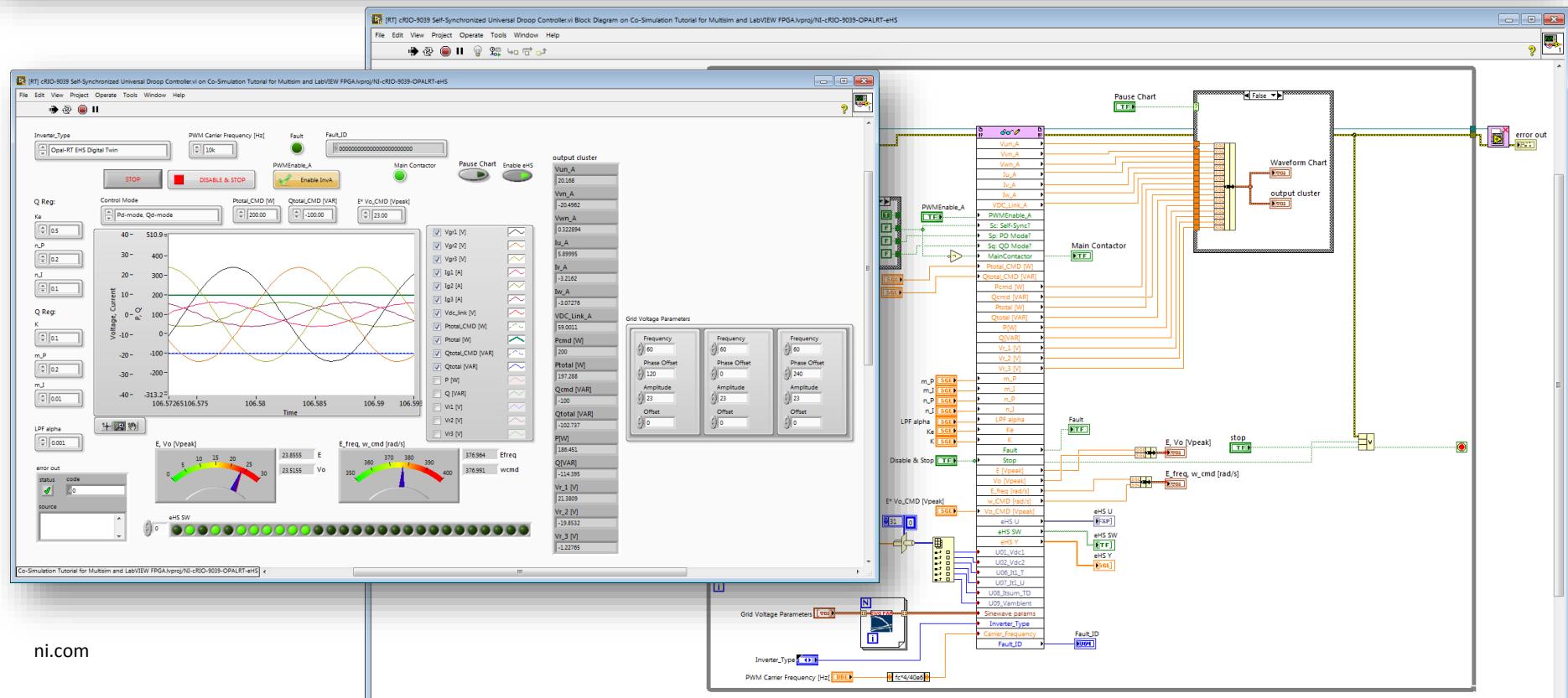
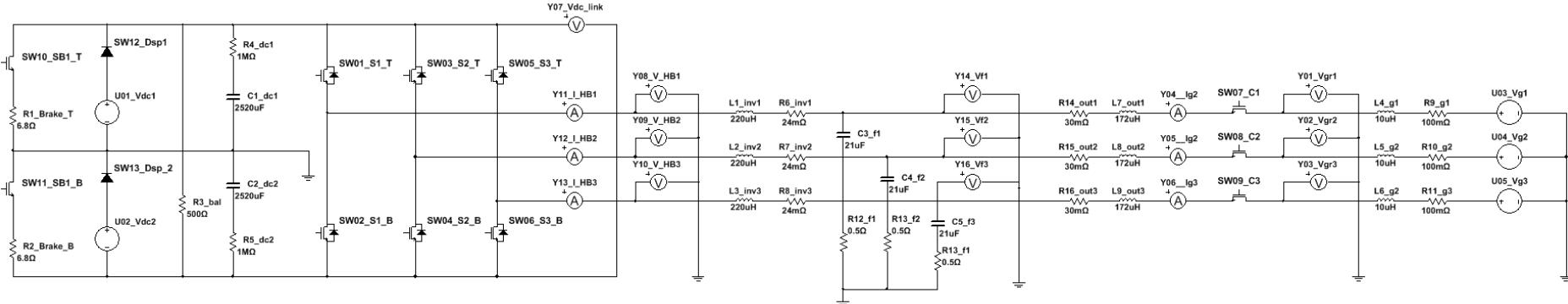
DEMO: OPAL-RT EMBEDDED DIGITAL TWIN – FPGA APPLICATION



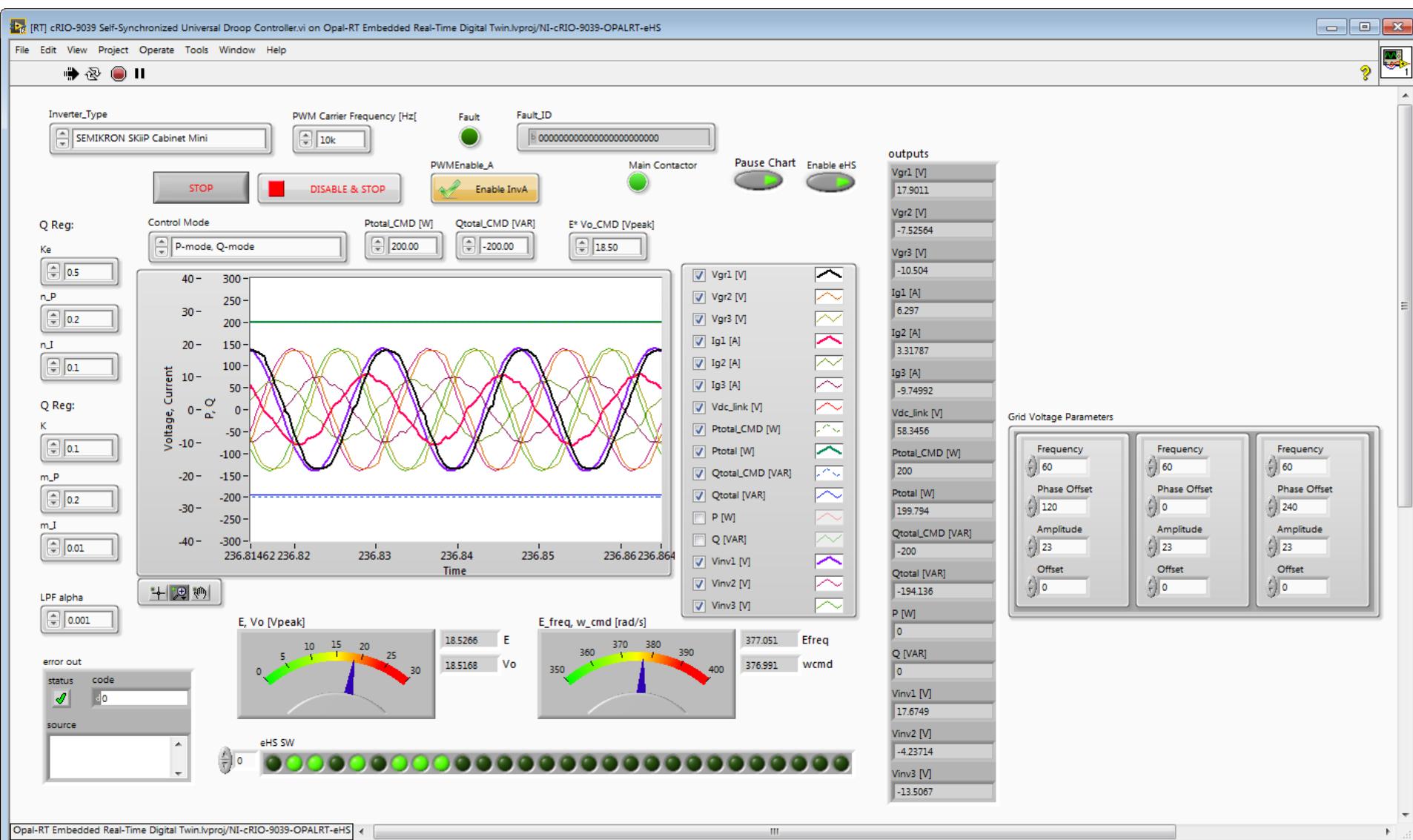
DEMO: OPAL-RT EMBEDDED DIGITAL TWIN – RT APPLICATION



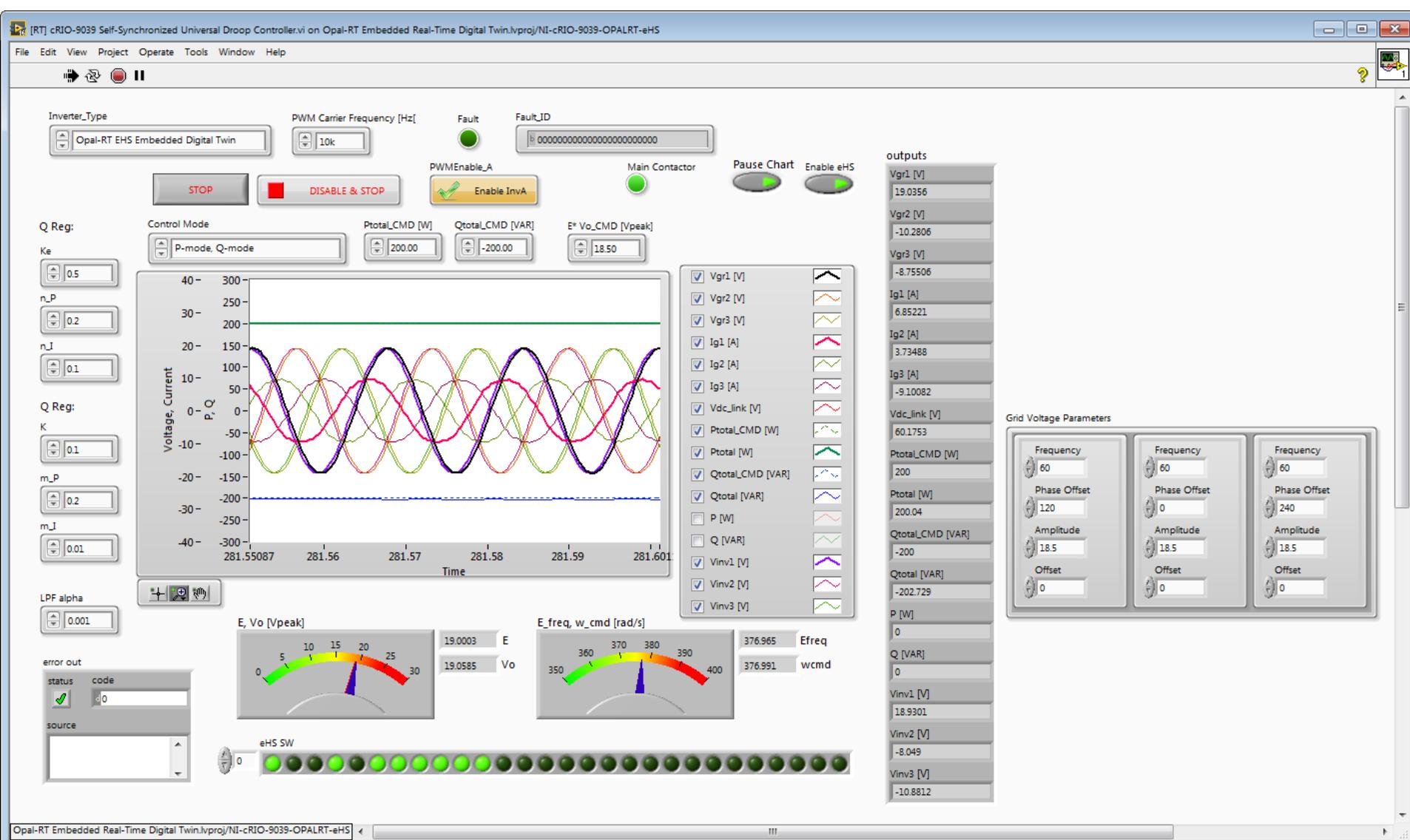
DEMO: OPAL-RT EMBEDDED DIGITAL TWIN – RT APPLICATION



COMPARISON: PHYSICAL INVERTER RESULTS



COMPARISON: EMBEDDED DIGITAL TWIN SIMULATION RESULTS

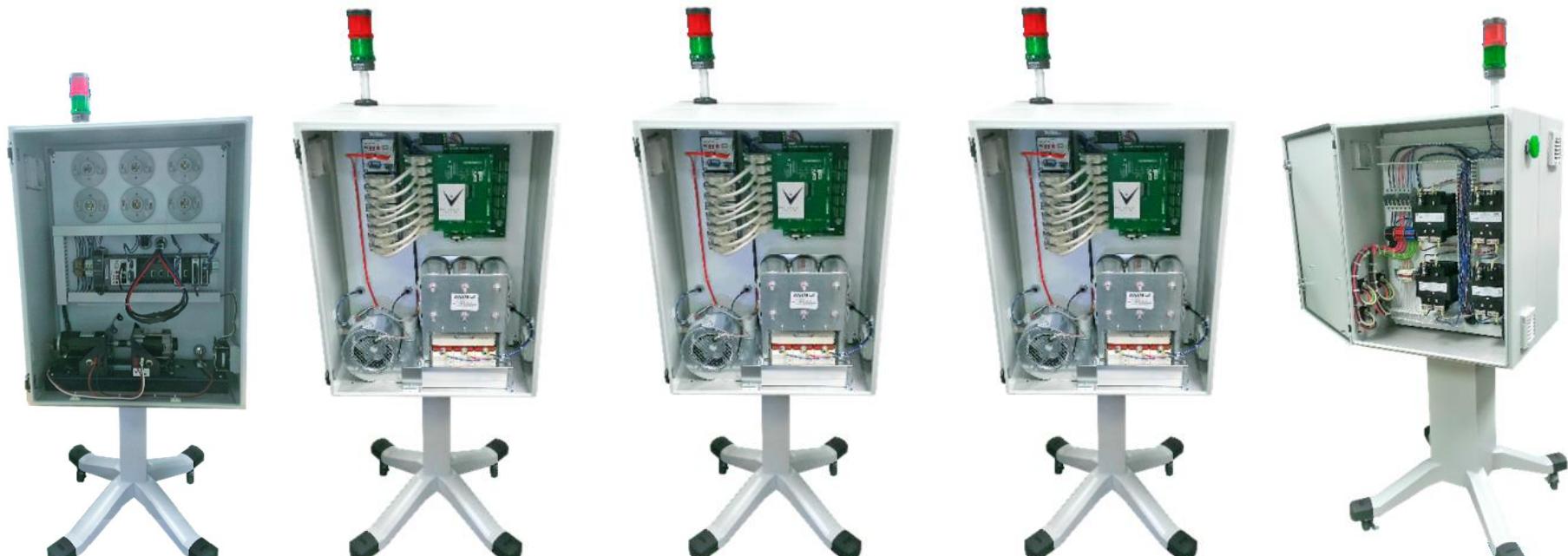


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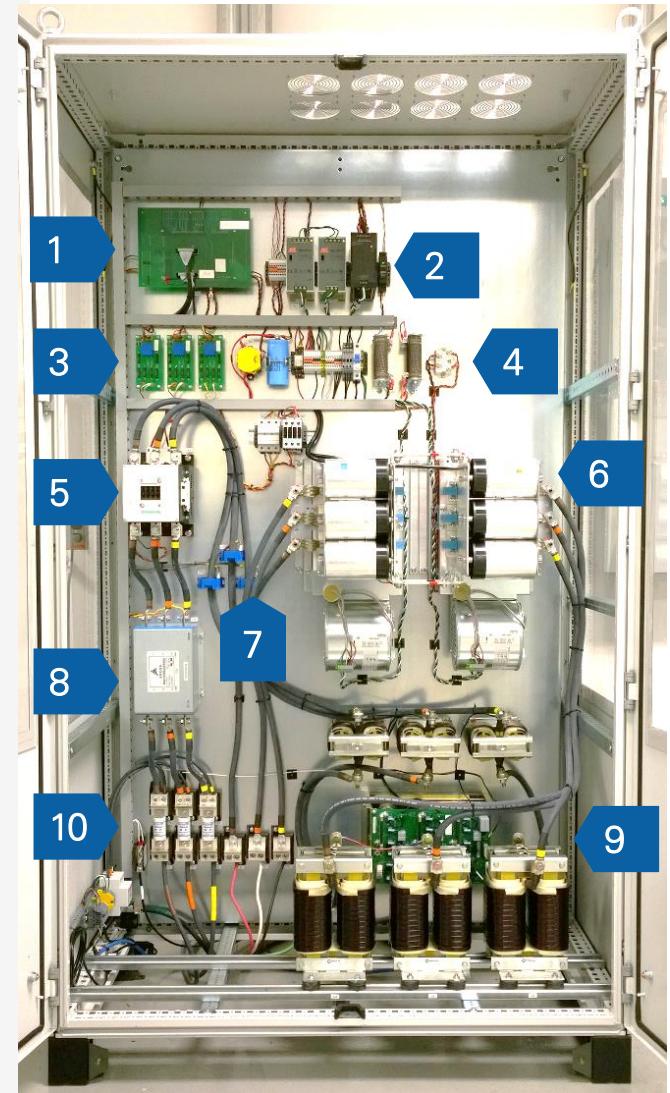
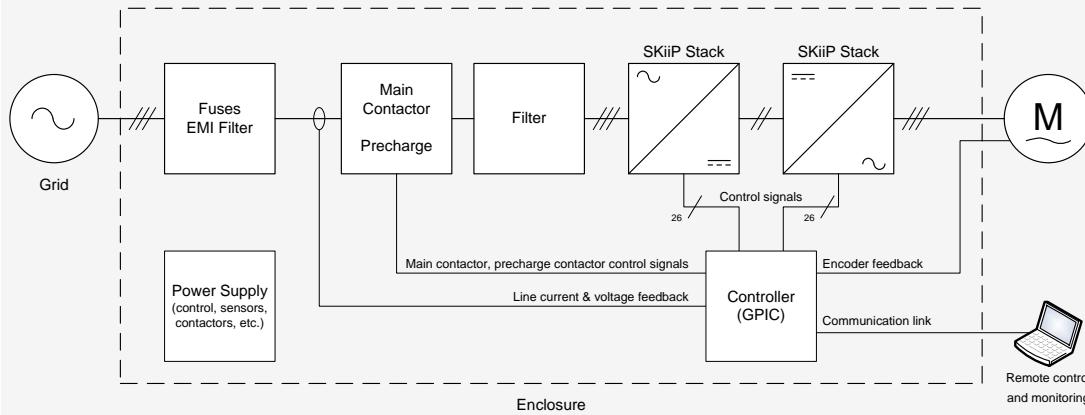
INVERTER
CABINET

GRID
CABINET

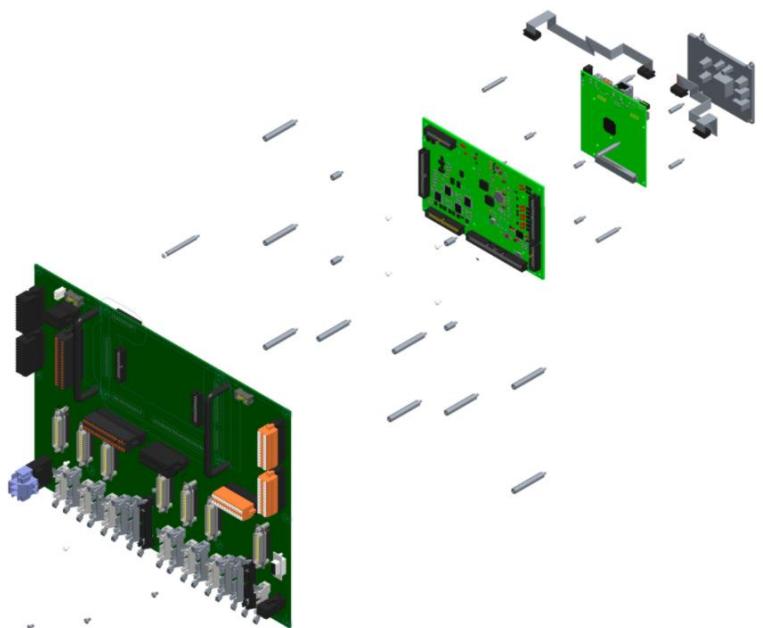
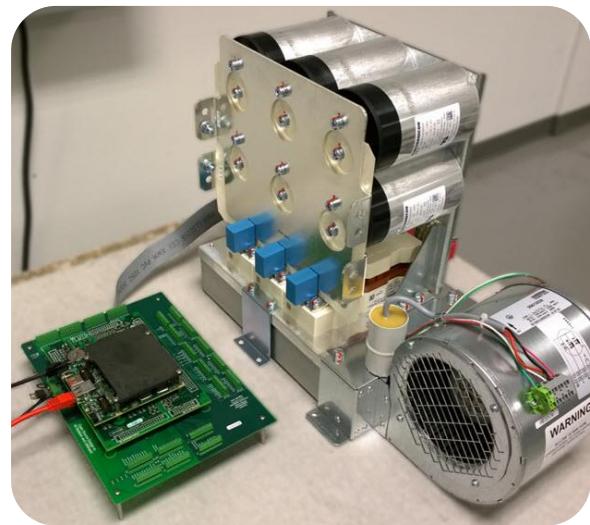
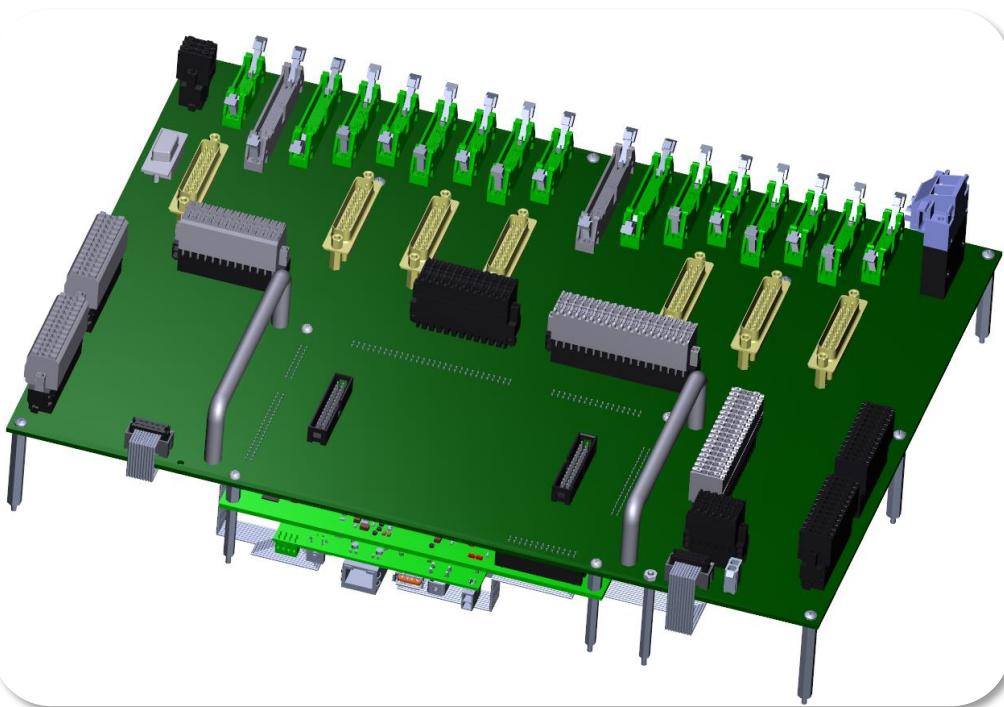
Semikron SKiiP3 100 kVA Back-to-Back Converter Cabinets

(Order from [Semikron USA](#))

1. NI sbRIO-9607 Zynq-7020, NI-9684 GPIC, I/F board
2. Power supplies
3. LEM isolated voltage sensors
4. DC Link capacitor pre-charge contactor circuit
5. Main grid connection contactor
6. SEMIKRON SKiiP power electronics stacks
7. LEM isolated current sensors
8. EMI Filter
9. LCL line reactor filter
10. Fuses and terminal blocks



NI GPIC Semikron Universal Interface Board



*In Development: Seeking beta customers
who will test in full power conditions.*

[Download 3D PDF](#)

NI GPIC Semikron Universal Interface Board



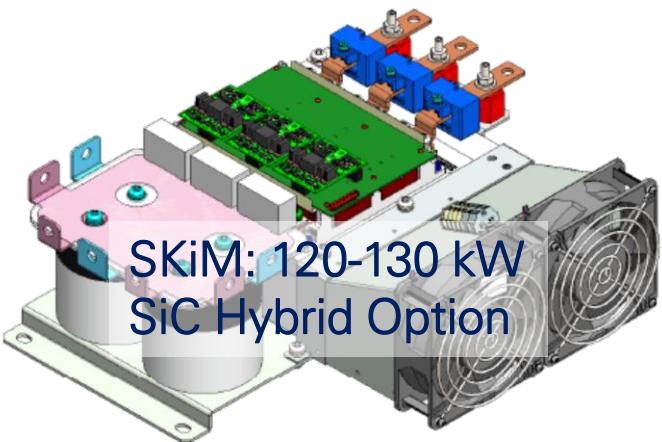
SEMIX: 15-28 kW



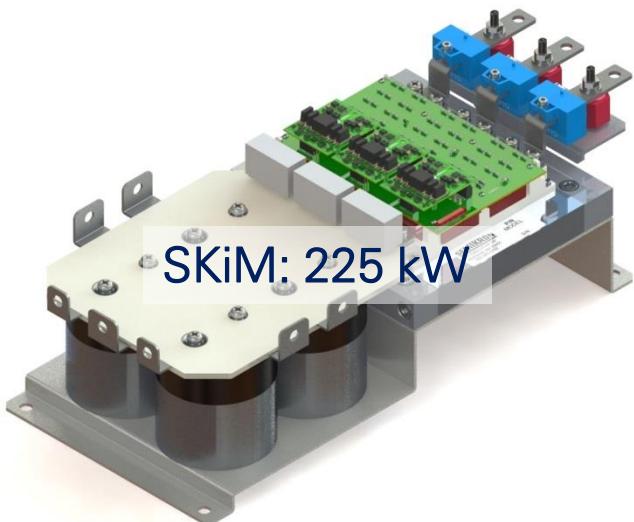
SKiiP3: 78 kW



SKM: 120 kW
Full SiC Stack



SKiM: 120-130 kW
SiC Hybrid Option



SKiM: 225 kW

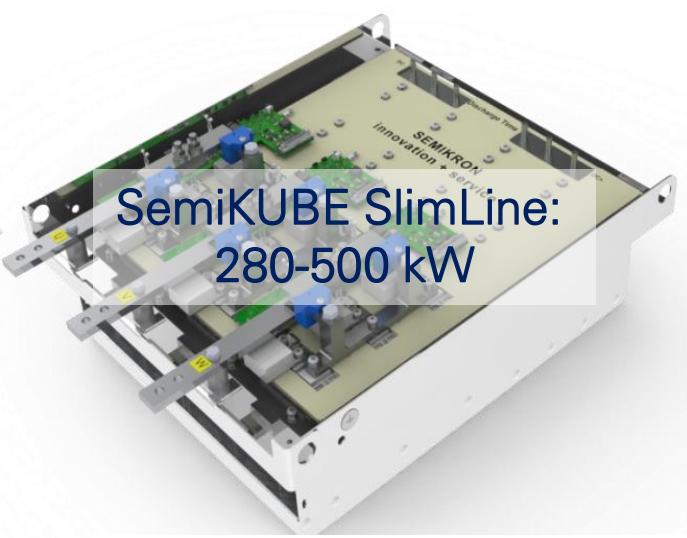


SemiKUBE: 150 kW

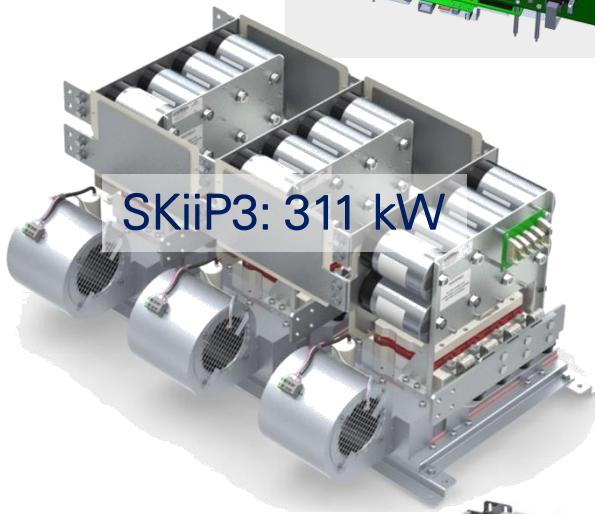
NI GPIC Semikron Universal Interface Board



SKiiP3: 175-212 kW



SemiKUBE SlimLine:
280-500 kW



SKiiP3: 311 kW



SemiKUBE SlimLine:
1 MW



SKiiP4: 565 kW



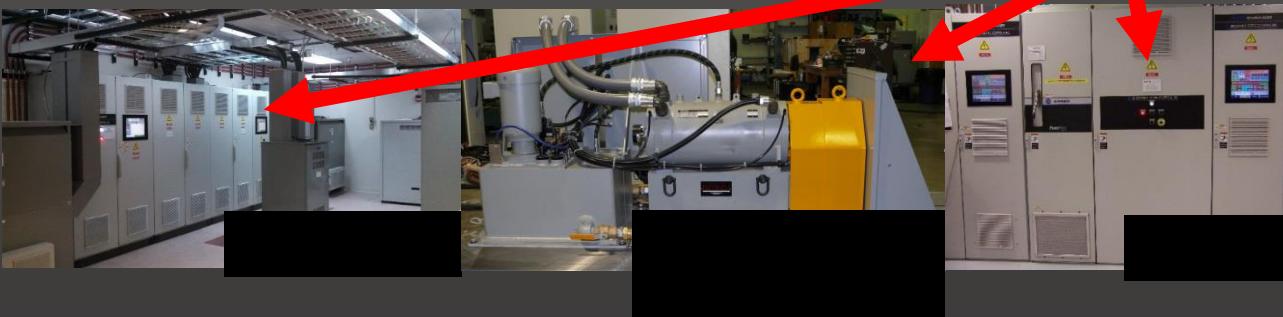
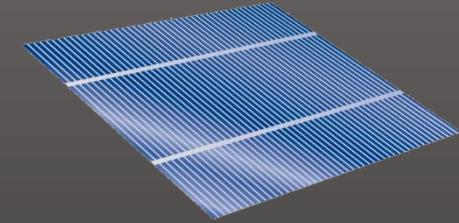
SEMISTACK RE:
1.6 MW



SEMISTACK RE:
3.2 MW

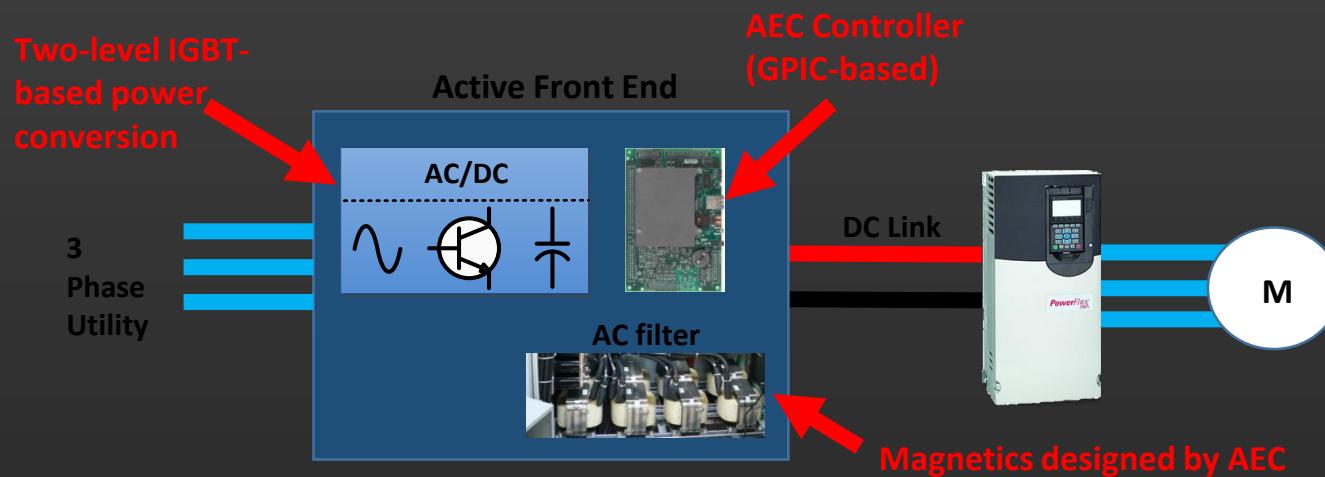
AE Controls – Application Portfolio

- Microgrid Inverters
- Regenerative multi-unit applications (DC/AC)
- PV applications (DC/DC, DC/AC)
- Energy storage applications (PV, battery, wind)
- Electric Vehicle Dynes
- Turn-key Systems up to
2000VDC / 690VAC



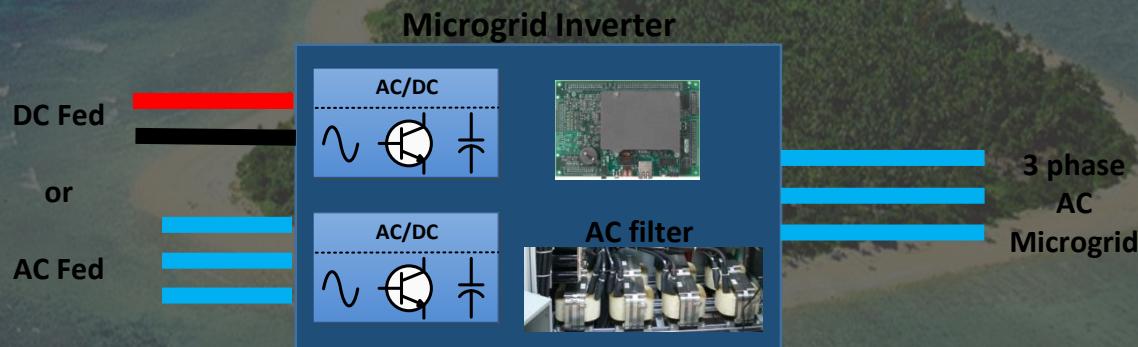
AE Controls – Active Front End

- AC to DC converter, fully regenerative to grid (sink/source)
- Power Levels: 36kW up to 2MW (240 VAC to 690 VAC)
- AFE Features:
 - IEEE-519 compliant
 - Turn-key packaging available
 - Standard two-Level IGBT topology



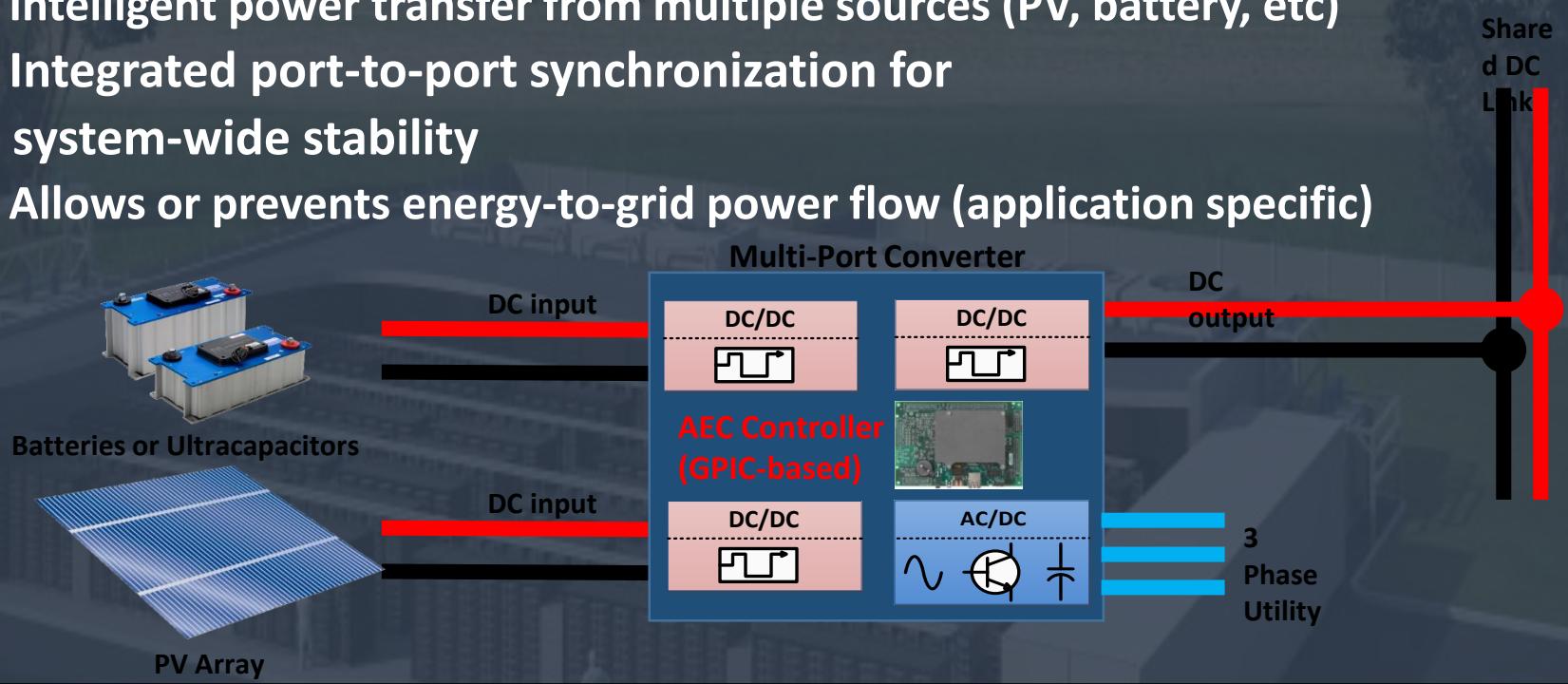
AE Controls – AC Microgrid

- Power Levels: 20kW to 5MW available (120 VAC to 690 VAC)
- Frequency Rating: 50 / 60 Hz, 400 Hz available
- AC Microgrid Features:
 - Auto-sync to utility for bumpless transfer
 - Anti-islanding detection (UL-1741, IEEE-1547)
 - Integrated fiber-optic sync for multi-unit stability

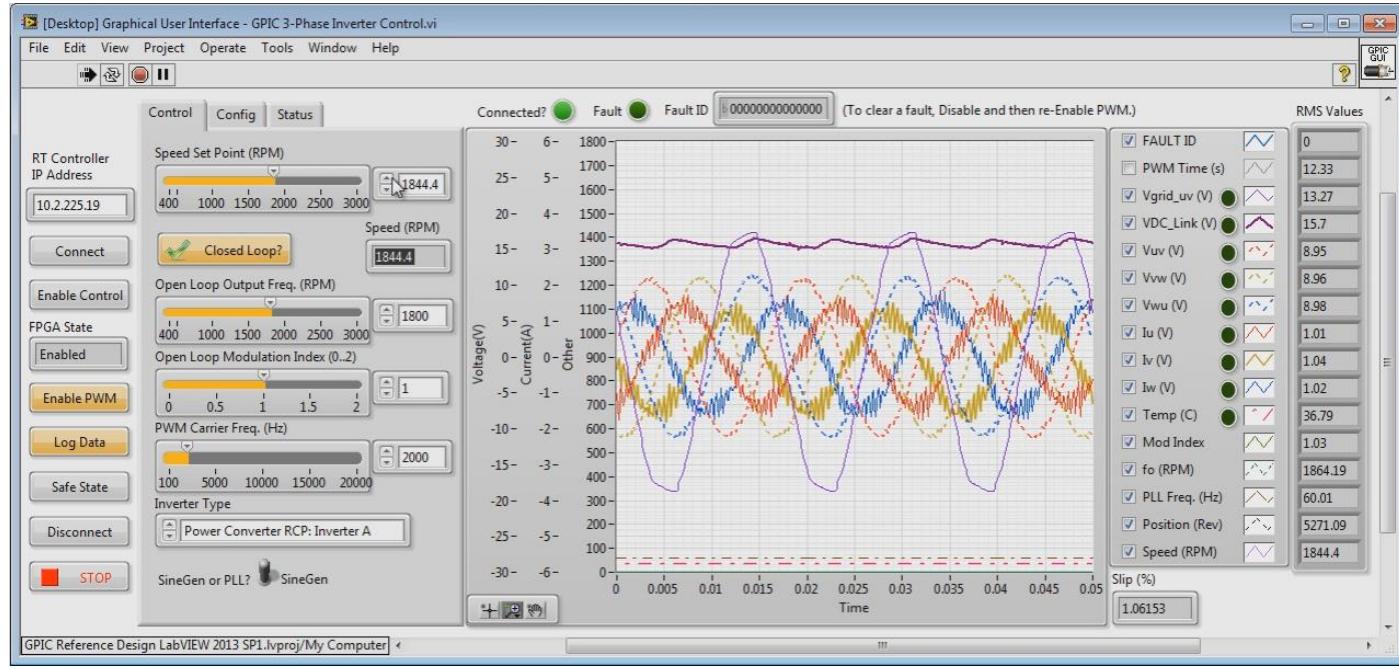
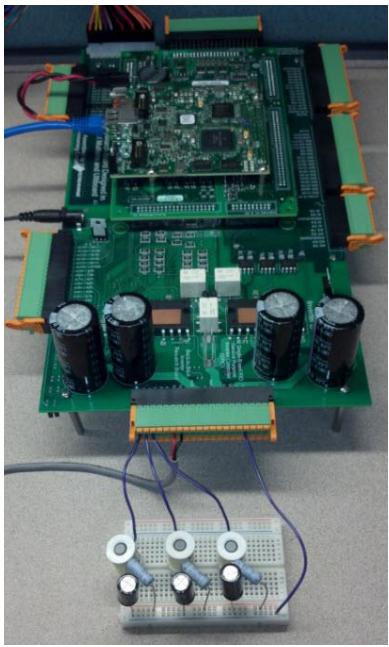


AE Controls – Energy Storage

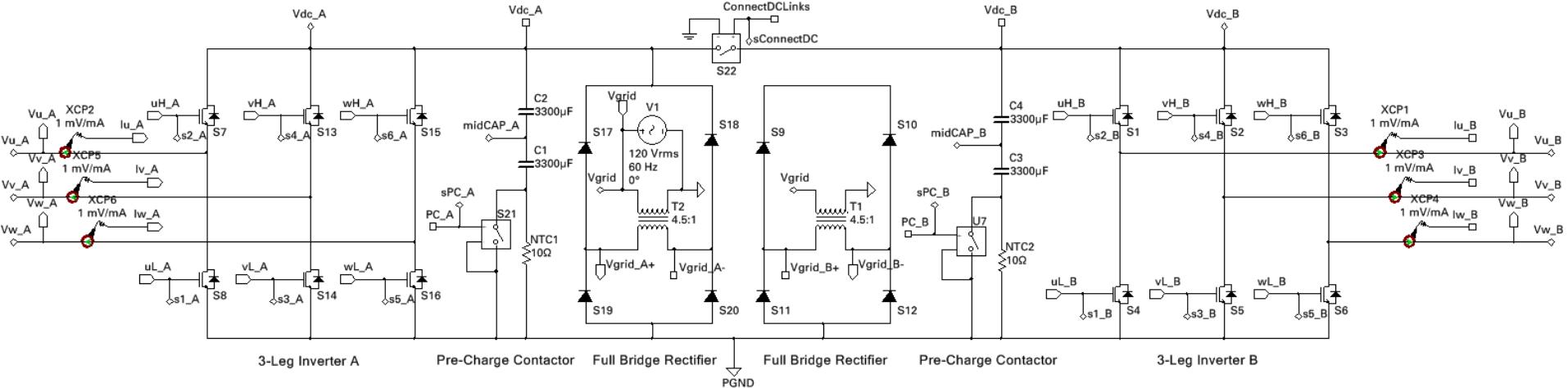
- Multi-port Power Conversion (AC/DC, DC/AC, and DC/DC)
- Power Levels: 20kW up to 5MW available (up to 2000 VDC, 5000 ADC)
- Multi-Port Features:
 - Intelligent power transfer from multiple sources (PV, battery, etc)
 - Integrated port-to-port synchronization for system-wide stability
 - Allows or prevents energy-to-grid power flow (application specific)



SKiiP Replica Control Development System with NI sbRIO GPIC



NI Single-Board RIO General Purpose Inverter Controller 3-Phase Back-to-Back Inverter Research Board



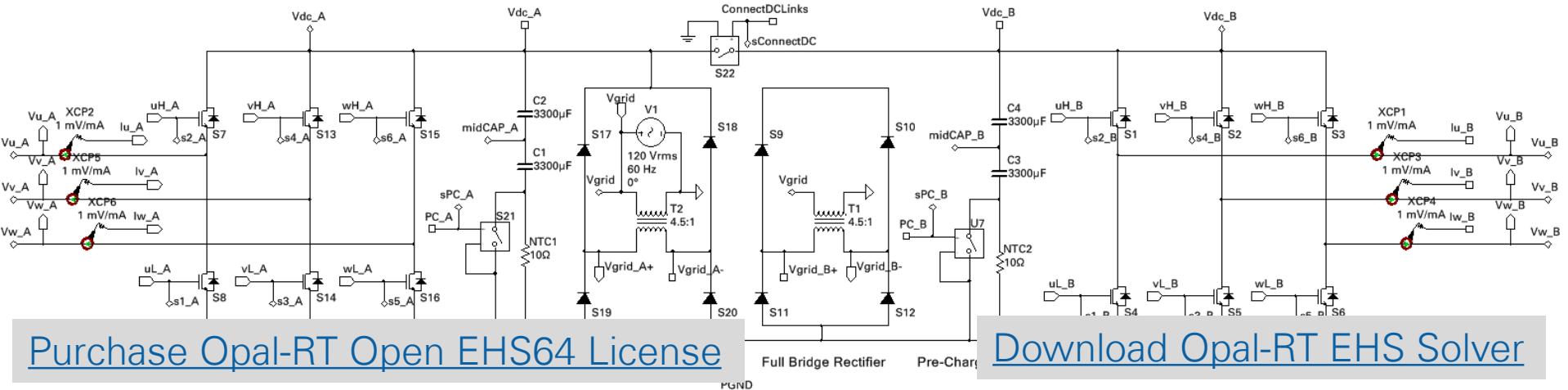
SKiiP Replica Control Development System with cRIO-9039 Sync and Opal-RT EHS Support



OPAL-RT
TECHNOLOGIES



NI Single-Board RIO General Purpose Inverter Controller 3-Phase Back-to-Back Inverter Research Board



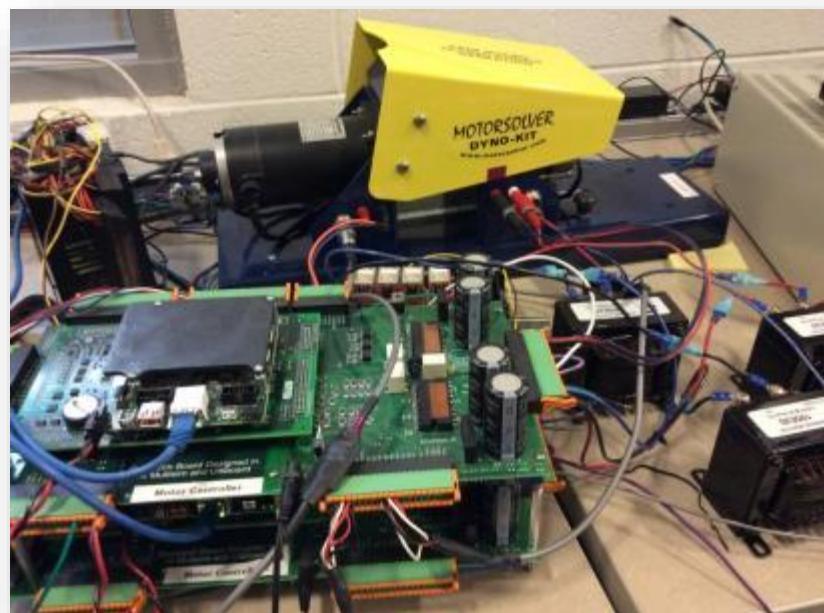
[Purchase Opal-RT Open EHS64 License](#)

[Download Opal-RT EHS Solver](#)

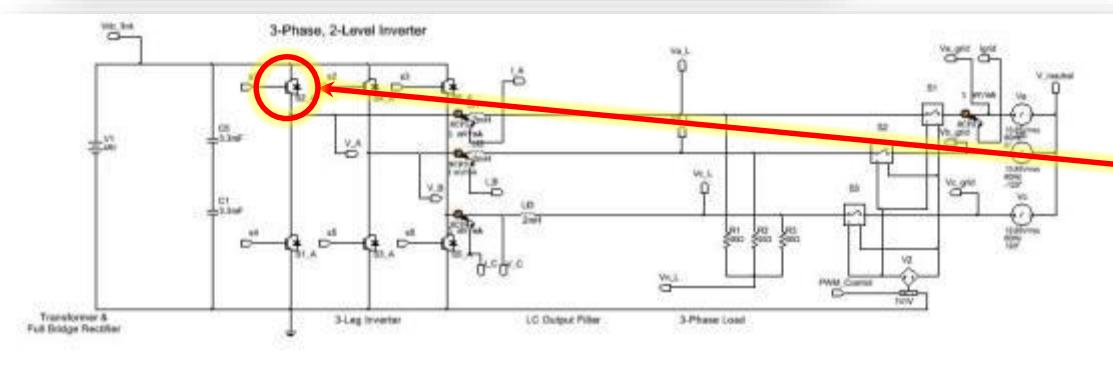
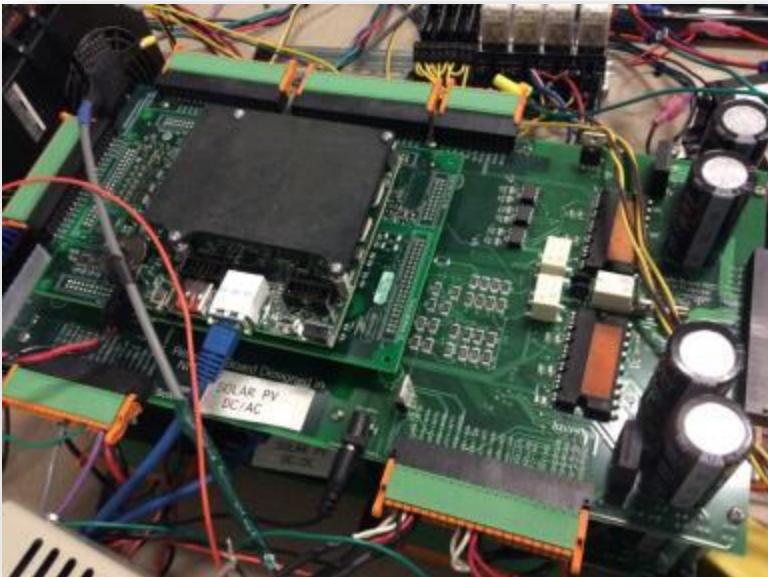
The Power of Mini-Scale: ORNL Motor Drive Setup



FPGA Front Panel During Run-Time - Physical IO and HIL Model
Running in GPIC FPGA



The Power of Mini-Scale: PV Inverter (MPPT)



Label	Display	Value	Pack	Pins	Transient	User Fields
Transistor on voltage:		600m	V			
Transistor on resistance:		500m	O			
Transistor off resistance:		1M	O			
Transistor forward voltage drop:		600m	V			
Diode on resistance:		360m	O			
Diode off resistance:		1M	O			
Diode forward drop voltage:		600m	V			

Parameters of IGBT of NI Multisim 3-Phase Back-to-Back Inverter Model

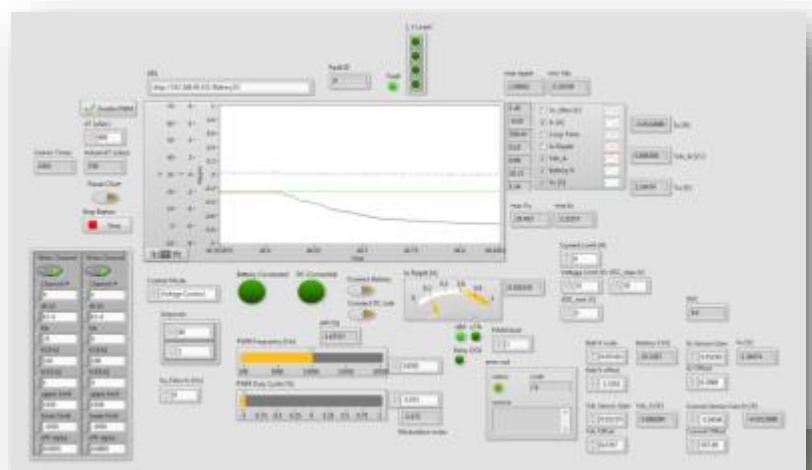
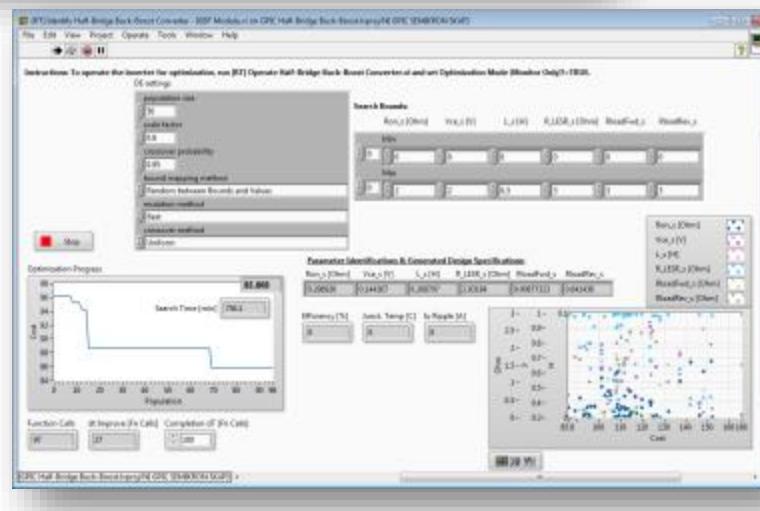
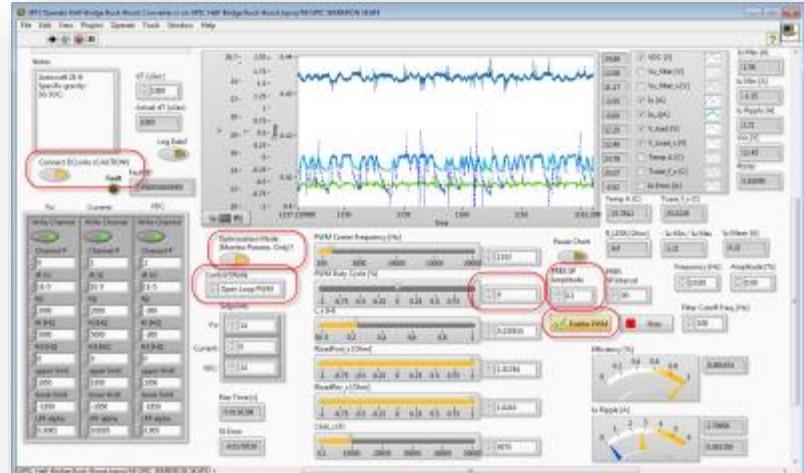


CERTS
CONSORTIUM FOR ELECTRIC RELIABILITY TECHNOLOGY SOLUTIONS

The Power of Mini-Scale: Energy Storage Setup



Physical and FPGA-simulated waveforms – use DE optimizer on
(Vce, Ron, L, R_ESR, RloadFwd, RloadRev)



CERTS
CONSORTIUM FOR ELECTRIC RELIABILITY TECHNOLOGY SOLUTIONS

The Power of Mini-Scale: Machine Learning for Embedded Digital Twin Parameter ID & Model Validation



Hand tuned parameters before global optimization



Validation of parameter ID



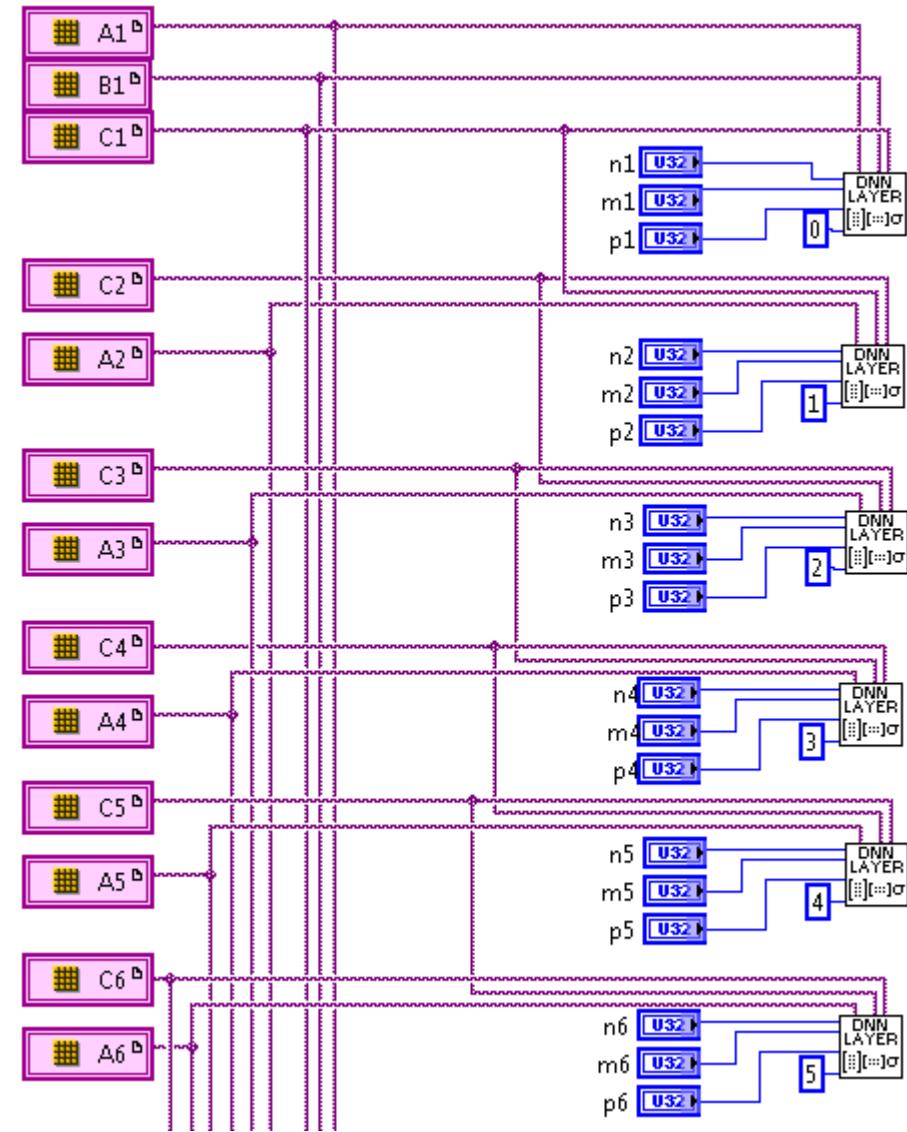
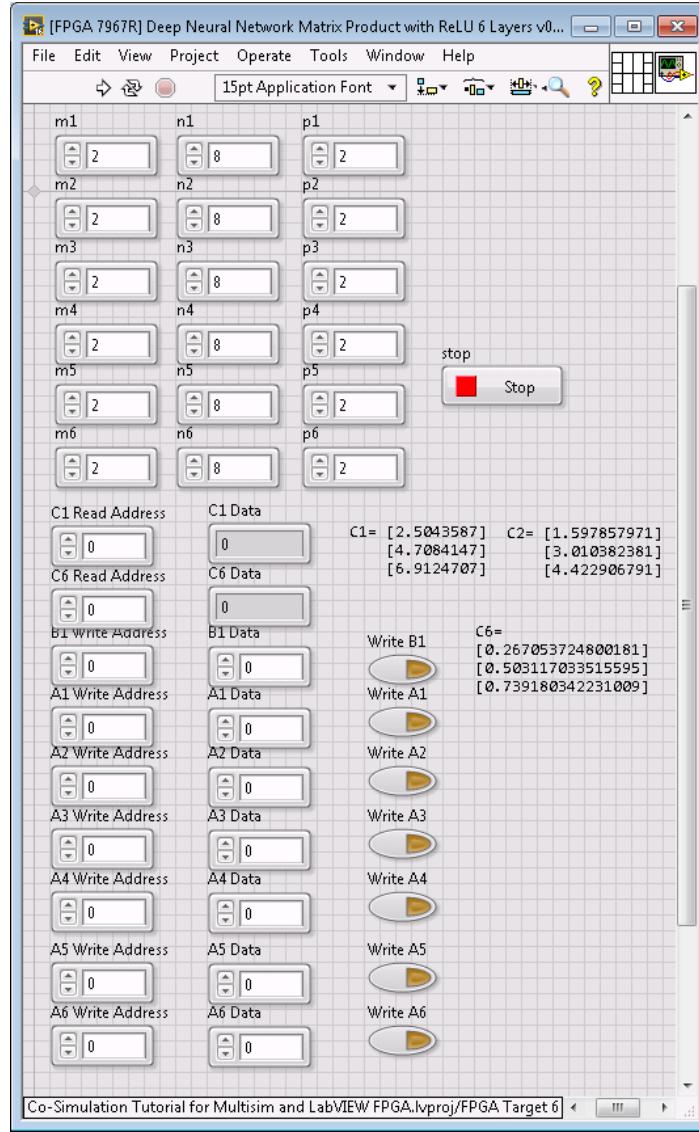
Physical and FPGA-simulated waveforms after global optimization of (Vce, Ron, L, R_LESR, R_BATCharge, R_BATDischarge)



Test	Description	mean(X1 error)	mean(X1 error * evaluations)
1	No local optimization	0.568	238.5408
2	Optimize only the best	0.5631	483.66
3	Sequentially Optimize the N Best (N=5)	0.3358	248.2386
4	Optimize one random population member	0.5612	475.4459
5	Locally optimize every population member	0.007	52.7633
6	Sequentially Optimize the N Best (N=10)	0.2383	176.3019
7	Sequentially Optimize the N Best (N=15)	0.1935	143.4965
8	Sequentially Optimize the N Best (N=20)	0.1995	147.9021
9	Locally optimize best 5 population members	0.2908	649.2309
10	Locally optimize worst 5 population members	0.568	471.6775
11	Locally optimize random 5 population members	0.5351	1386.9866

LabVIEW FPGA Deep Neural Network Solver

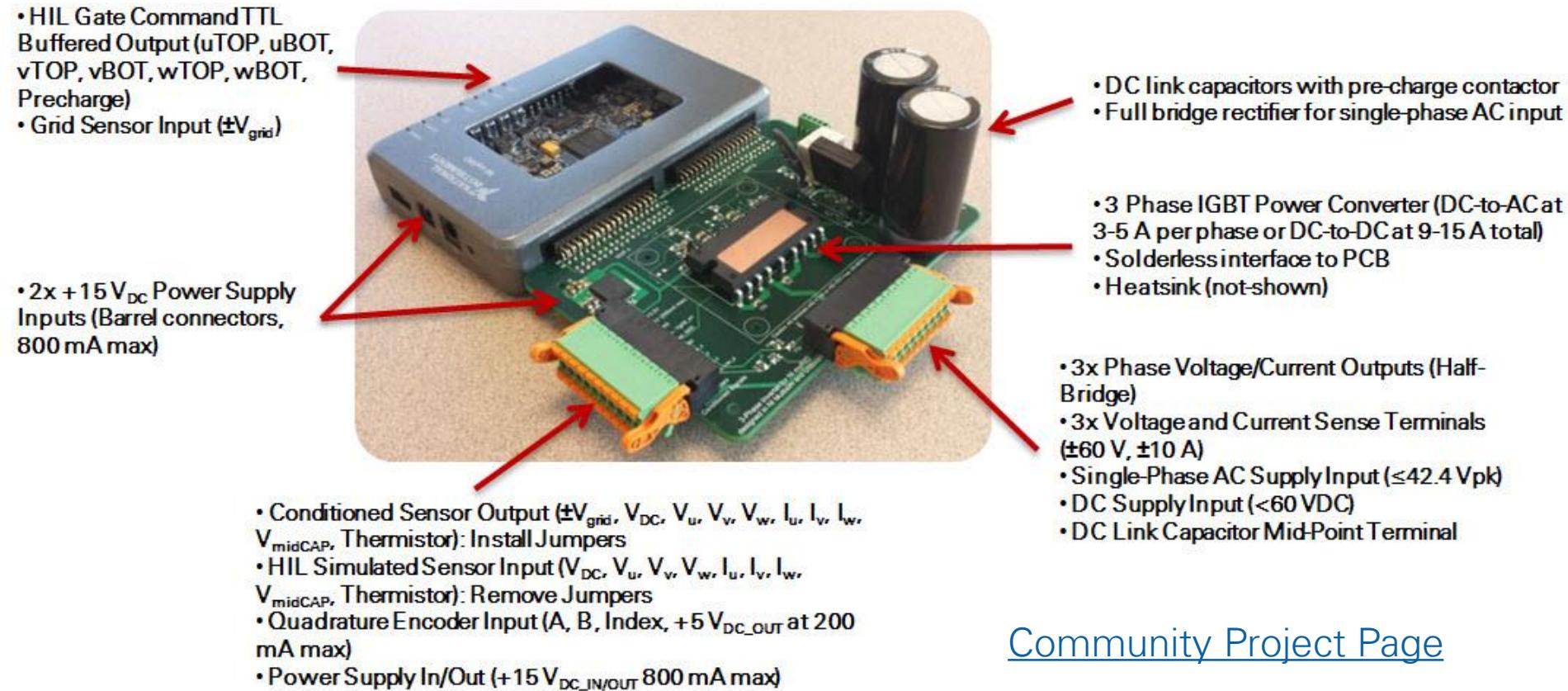
6-Layer Fully Connected DNN with ReLU Activation



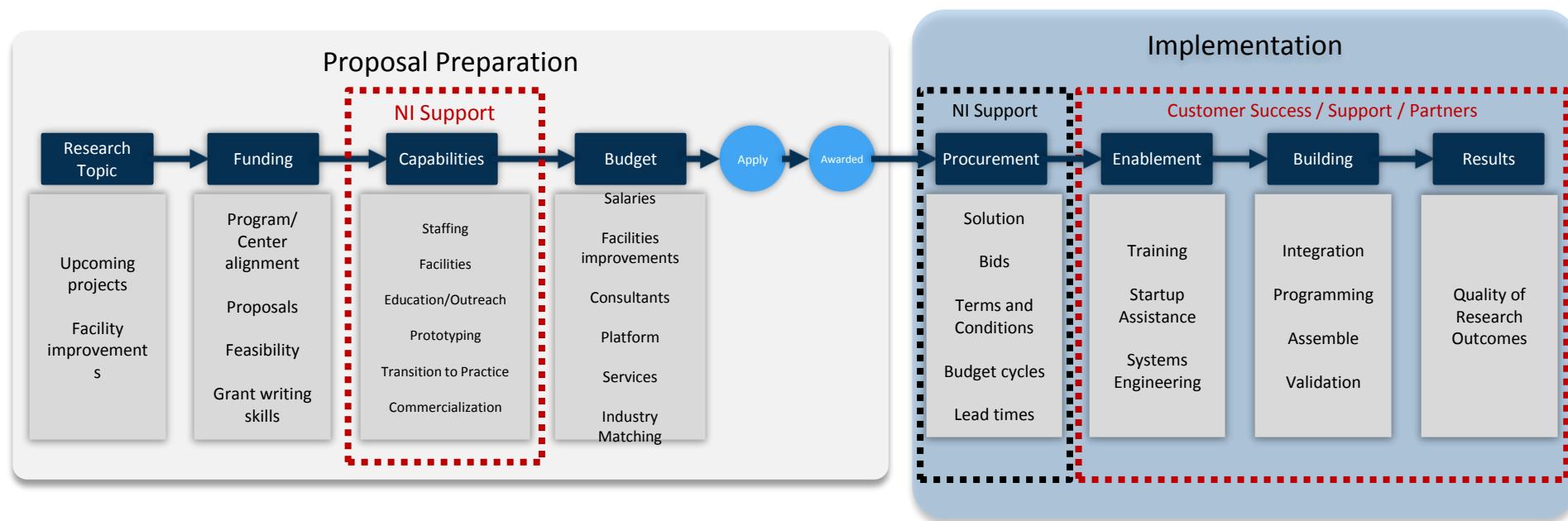
MyRIO Mycrogrid Inverter Board

This open source design is currently being updated to add a line-reactor filter and DC link brake contactor, enabling students to build their own bi-directional microgrid with just DC power supplies and jumper wires for the three-phase power bus.

NI thanks the [UT Center for Electromechanics](#) for their contributions.



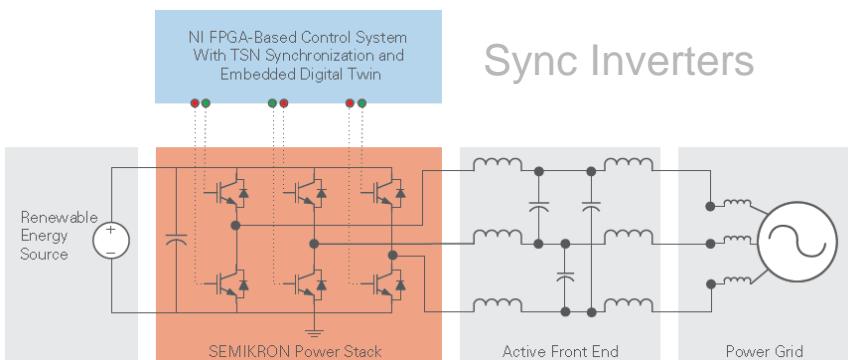
Working with NI: Government and Academic Research Support

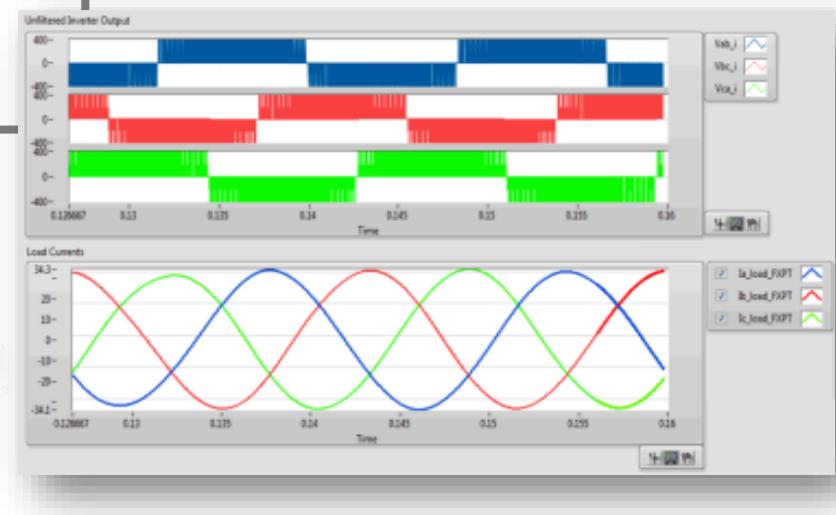
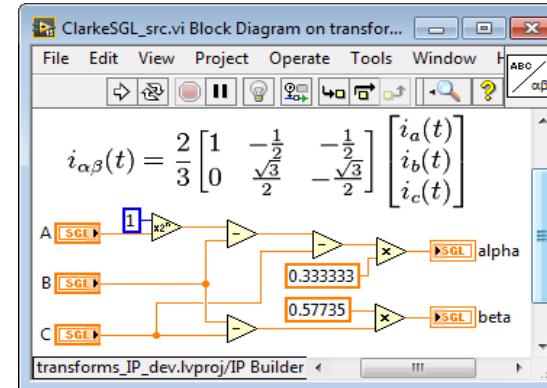
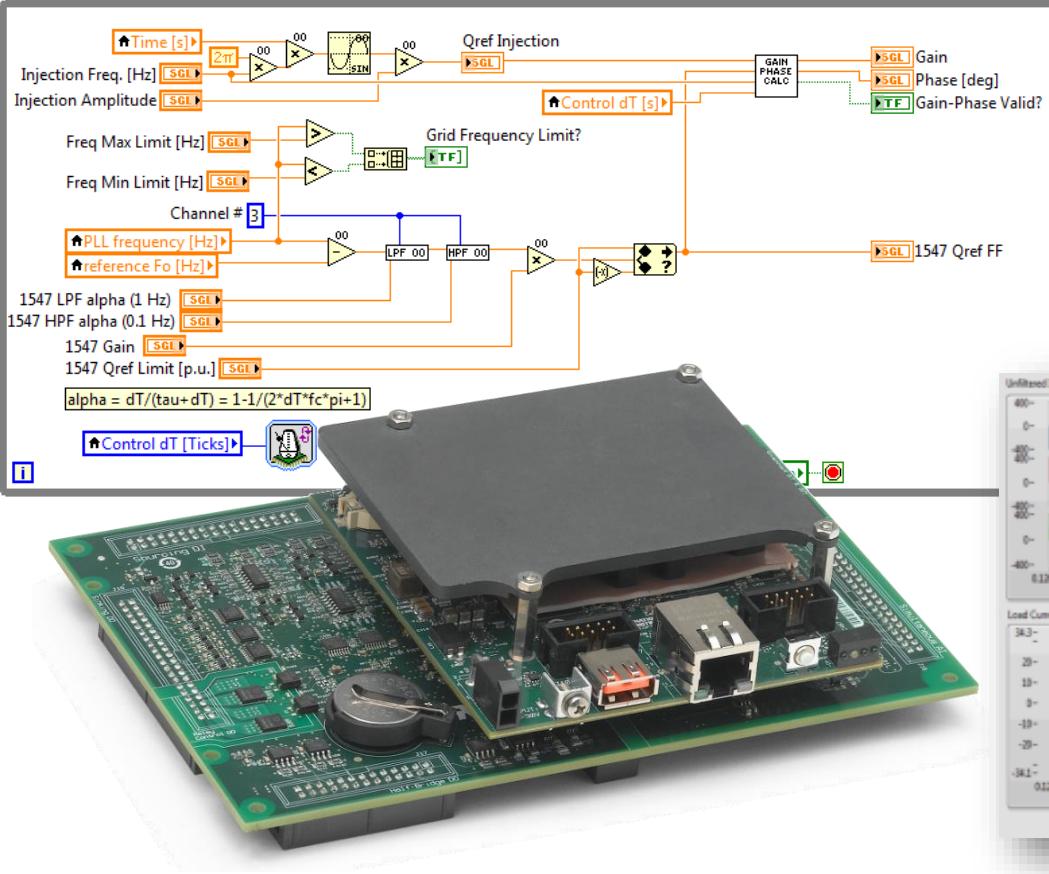


New Open Source Testbed Platform for Smart Grid and Microgrid Research: Go from Paper Design to Prototype Deployment in Days

What to Do Next

- Find out more about the capabilities and solutions presented
 - Academic and Applied Researchers – please contact Eric Dean (eric.dean@ni.com)
 - Commercial - please contact Eric Bradley (eric.bradley@ni.com)
- Come to NIWeek in Austin, TX for the Digital Energy Summit – 23-24 May 2017
 - Co-sponsored and presentations by Semikron and OPAL-RT
 - Keynote by Dr. Qing-Chang Zhong, IEEE Fellow and Max McGraw Endowed Chair Professor of Energy and Power Engineering and Management at the Illinois Institute of Technology, presentations by Oak Ridge National Labs, Dr. Alessandro Lidozzi from the Center for Power Electronics and Drives & Roma Tre University, NextEra, Siemens, Viewpoint Systems and others
 - Learn about some of the latest developments in power electronics design, simulation, test and deployment
 - See the IIoT Lab equipment/demos and network with peers, NI personnel
 - www.ni.com/niweek
- Join the NI Power Electronics Community
 - www.ni.com/powerdev
- Read more and watch the IEEE Webcast series
 - www.ni.com/power/electronics/
- Webpage for the NI IIoT Lab
 - www.ni.com/iiot-lab





NEXT STEP

JOIN THE DEVELOPER COMMUNITY AT
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