bool
EnumType
uint32_t
sl_start_symbol_r16_opts
sl_len_symbols_r16_opts
subcarrier_spacing_opts
sl_ptrs_re_offset_r16_opts
dl_ul_tx_periodicity_v1530_opts
dl_ul_tx_periodicity_opts
sl_alpha_pssch_pscch_r16_opts
dl_alpha_pssch_pscch_r16_opts
dl_alpha_psfch_r16_opts
sl_time_win_size_cbr_r16_opts
asn1::enumerated< EnumType, E, M >
sl_time_win_size_cr_r16_opts
sl_subch_size_r16_opts
sl_add_mcs_table_r16_opts
filt_coef_opts
sl_rs_for_sensing_r16_opts
sl_max_num_per_reserve_r16_opts
sl_sensing_win_r16_opts
sl_preemption_enable_r16_opts
sl_x_overhead_r16_opts
asn1::bitstring< LB, UB, ext, aligned >
asn1::bitstring< 10, 160 >
< 10, 160 >
asn1::enumerated< sl_start_symbol_r16_opts >
asn1::enumerated< sl_len_symbols_r16_opts >
asn1::enumerated< subcarrier_spacing_opts >
asn1::enumerated< sl_ptrs_re_offset_r16_opts >
asn1::setup_release_c< T >
asn1::enumerated< dl_ul_tx_periodicity_v1530_opts >
asn1::enumerated< dl_ul_tx_periodicity_opts >
asn1::enumerated< sl_alpha_pssch_pscch_r16_opts >
asn1::enumerated< dl_alpha_pssch_pscch_r16_opts >
asn1::enumerated< dl_alpha_psfch_r16_opts >
asn1::enumerated< sl_time_win_size_cbr_r16_opts >
asn1::enumerated< sl_time_win_size_cr_r16_opts >
asn1::enumerated< sl_subch_size_r16_opts >
asn1::enumerated< sl_add_mcs_table_r16_opts >
asn1::enumerated< filt_coef_opts, true >
asn1::enumerated< sl_rs_for_sensing_r16_opts >
asn1::enumerated< sl_max_num_per_reserve_r16_opts >
asn1::enumerated< sl_sensing_win_r16_opts >
asn1::enumerated< sl_preemption_enable_r16_opts >
asn1::enumerated< sl_x_overhead_r16_opts >
asn1::rrc_nr::sl_sync_allowed_r16_s
uint16_t
array< uint8_t, 3 >
array< uint16_t, 2 >
int16_t
int8_t
uint8_t
asn1::rrc_nr::bwp_s
asn1::setup_release_c< asn1::rrc_nr::sl_ps_bch_cfg_r16_s >
asn1::bounded_array< T, MAX_N >
asn1::rrc_nr::sl_ptrs_cfg_r16_s
asn1::rrc_nr::tdd_ul_dl_pattern_s
asn1::rrc_nr::sl_pwr_ctrl_r16_s
asn1::setup_release_c< asn1::rrc_nr::sl_psfch_cfg_r16_s >
asn1::setup_release_c< asn1::rrc_nr::sl_pscch_cfg_r16_s >
asn1::setup_release_c< asn1::rrc_nr::sl_pssch_cfg_r16_s >
asn1::rrc_nr::tdd_ul_dl_cfg_common_s
asn1::rrc_nr::sl_res_pool_r16_s::sl_rx_params_ncell_r16_s_
asn1::bounded_array< uint8_t, 8 >
< uint8_t, 8 >
asn1::rrc_nr::sl_bwp_generic_r16_s
asn1::rrc_nr::sl_tx_pool_ded_r16_s
asn1::dyn_array< T >
asn1::copy_ptr< T >
asn1::dyn_array< sl_res_pool_cfg_r16_s >
asn1::dyn_array< sl_res_reserve_period_r16_c >
asn1::dyn_array< sl_prio_tx_cfg_idx_r16_s >
asn1::copy_ptr< asn1::dyn_array >
asn1::dyn_array< sl_min_max_mcs_cfg_r16_s >
asn1::copy_ptr< asn1::setup_release_c< asn1::rrc_nr::sl_inter_ue_coordination_cfg_r17_s > >
asn1::copy_ptr< asn1::setup_release_c< asn1::rrc_nr::sl_pbps_cp_s_cfg_r17_s > >
array< uint8_t, 64 >
array< sl_sel_win_cfg_r16_s, 8 >
array< sl_tx_percentage_cfg_r16_s, 8 >
asn1::rrc_nr::sl_ue_sel_cfg_rp_r16_s
asn1::dyn_array< sl_res_pool_r16_s >
array< sl_zone_cfg_mcr_r16_s, 16 >
asn1::rrc_nr::sl_res_pool_r16_s
+ sl_pssch_cfg_r16_present
+ sl_sync_allowed_r16_present
+ sl_subch_size_r16_present
+ sl_start_rb_subch_r16_present
+ sl_thresh_s_rssi_cbr_r16_present
+ sl_time_win_size_cbr_r16_present
+ sl_time_win_size_cr_r16_present
+ sl_ptrs_cfg_r16_present
+ sl_ue_sel_cfg_rp_r16_present
+ sl_rx_params_ncell_r16_present
and 6 more...
+ pack()
+ unpack()
+ to_json()
asn1::rrc_nr::sl_res_pool_cfg_r16_s
asn1::rrc_nr::sl_bwp_pool_cfg_r16_s
asn1::copy_ptr< asn1::setup_release_c< asn1::rrc_nr::sl_bwp_pool_cfg_r16_s > >
asn1::copy_ptr< asn1::setup_release_c< asn1::rrc_nr::sl_bwp_disc_pool_cfg_r17_s > >
< asn1::setup_release_c< asn1::rrc_nr::sl_bwp_disc_pool_cfg_r17_s > >
asn1::rrc_nr::sl_bwp_cfg_r16_s
+ pack()
+ unpack()
+ to_json()
+has_ext
+nof_exts
+nof_types
+has_ext
+is_aligned
+lb
+ub
+ext
+sl_bwp_r16_present
+sl_len_symbols_r16_present
+sl_ps_bch_cfg_r16_present
+sl_start_symbol_r16_present
+sl_tx_direct_current_location_r16_present
+cp_present
+ext
+sl_ptrs_freq_density_r16_present
+sl_ptrs_re_offset_r16_present
+sl_ptrs_time_density_r16_present
+dl_ul_tx_periodicity_v1530_present
+ext
+ext
+pattern2_present
+dl_alpha_psfch_r16_present
+dl_alpha_pssch_pscch_r16_present
+dl_p0_psfch_r16_present
+dl_p0_psfch_r17_present
+dl_p0_pssch_pscch_r16_present
+dl_p0_pssch_pscch_r17_present
+ext
+sl_alpha_pssch_pscch_r16_present
+sl_p0_pssch_pscch_r16_present
+sl_p0_pssch_pscch_r17_present
...
+gnb_enb_sync_r16_present
+gnss_sync_r16_present
+ue_sync_r16_present
+ext
+sl_max_num_per_reserve_r16_present
+sl_multi_reserve_res_r16_present
+sl_sel_win_list_r16_present
+sl_sensing_win_r16_present
+sl_thres_rsrp_list_r16_present
+dummy_present
+ext
+sl_add_mcs_table_r16_present
+sl_filt_coef_r16_present
+sl_num_subch_r16_present
+sl_preemption_enable_r16_present
+sl_prio_thres_r16_present
+sl_prio_thres_ul_urllc_r16_present
+sl_pscch_cfg_r16_present
+sl_psfch_cfg_r16_present
...
+sl_tx_pool_exceptional_r16_present
+sl_tx_pool_sched_r16_present
+sl_tx_pool_sel_normal_r16_present
+sl_res_pool_r16_present
+sl_tdd_cfg_r16_present
< sl_start_symbol_r16_opts >
< sl_len_symbols_r16_opts >
< subcarrier_spacing_opts >
< sl_ptrs_re_offset_r16_opts >
< dl_ul_tx_periodicity_v1530_opts >
< dl_ul_tx_periodicity_opts >
< sl_alpha_pssch_pscch_r16_opts >
< dl_alpha_pssch_pscch_r16_opts >
< dl_alpha_psfch_r16_opts >
< sl_time_win_size_cbr_r16_opts >
< sl_time_win_size_cr_r16_opts >
< sl_subch_size_r16_opts >
< sl_add_mcs_table_r16_opts >
< filt_coef_opts, true >
< sl_rs_for_sensing_r16_opts >
< sl_max_num_per_reserve_r16_opts >
< sl_sensing_win_r16_opts >
< sl_preemption_enable_r16_opts >
< sl_x_overhead_r16_opts >
< asn1::rrc_nr::sl_ps_bch_cfg_r16_s >
< asn1::rrc_nr::sl_psfch_cfg_r16_s >
< asn1::rrc_nr::sl_pscch_cfg_r16_s >
< asn1::rrc_nr::sl_pssch_cfg_r16_s >
< sl_res_pool_cfg_r16_s >
< sl_min_max_mcs_cfg_r16_s >
< sl_res_reserve_period_r16_c >
< sl_prio_tx_cfg_idx_r16_s >
< asn1::setup_release_c< asn1::rrc_nr::sl_inter_ue_coordination_cfg_r17_s > >
< asn1::setup_release_c< asn1::rrc_nr::sl_pbps_cp_s_cfg_r17_s > >
< asn1::dyn_array >
+location_and_bw
+sl_ptrs_time_density_r16
+subcarrier_spacing
+sl_ptrs_freq_density_r16
+sl_ptrs_re_offset_r16
+nrof_dl_slots
+nrof_ul_slots
+nrof_dl_symbols
+nrof_ul_symbols
+ref_subcarrier_spacing
+dl_ul_tx_periodicity_v1530
+dl_ul_tx_periodicity
+dl_p0_psfch_r17
+dl_p0_pssch_pscch_r17
+sl_p0_pssch_pscch_r17
+dl_p0_psfch_r16
+dl_p0_pssch_pscch_r16
+sl_max_trans_pwr_r16
+sl_p0_pssch_pscch_r16
+sl_alpha_pssch_pscch_r16
+dl_alpha_pssch_pscch_r16
+dl_alpha_psfch_r16
+pattern1
+pattern2
+sl_start_symbol_r16
+sl_len_symbols_r16
+sl_tx_direct_current_location_r16
+sl_bwp_r16
+sl_ps_bch_cfg_r16
+sl_pool_to_release_list_r16
+sl_rb_num_r16
+sl_start_rb_subch_r16
+sl_ptrs_cfg_r16
+sl_psfch_cfg_r16
+sl_pscch_cfg_r16
+sl_pssch_cfg_r16
+sl_tdd_cfg_r16
+sl_rx_params_ncell_r16
+sl_add_mcs_table_r16
+sl_filt_coef_r16
+sl_pool_to_add_mod_list_r16
+sl_res_reserve_period_list_r16
+sl_min_max_mcs_list_r16
+sl_inter_ue_coordination_cfg_r17
+sl_tx_percentage_list_r16
+sl_cbr_prio_tx_cfg_list_r16
+sl_thres_rsrp_list_r16
+sl_cbr_prio_tx_cfg_list_v1650
+sl_sel_win_list_r16
+sl_pbps_cp_s_cfg_r17
+sl_rs_for_sensing_r16
+sl_max_num_per_reserve_r16
+sl_ue_sel_cfg_rp_r16
+sl_zone_cfg_mcr_list_r16
+sl_res_pool_r16
+sl_tx_pool_exceptional_r16
+sl_rx_pool_r16
+sl_bwp_id
+sl_bwp_pool_cfg_ps_r17
+sl_bwp_disc_pool_cfg_r17