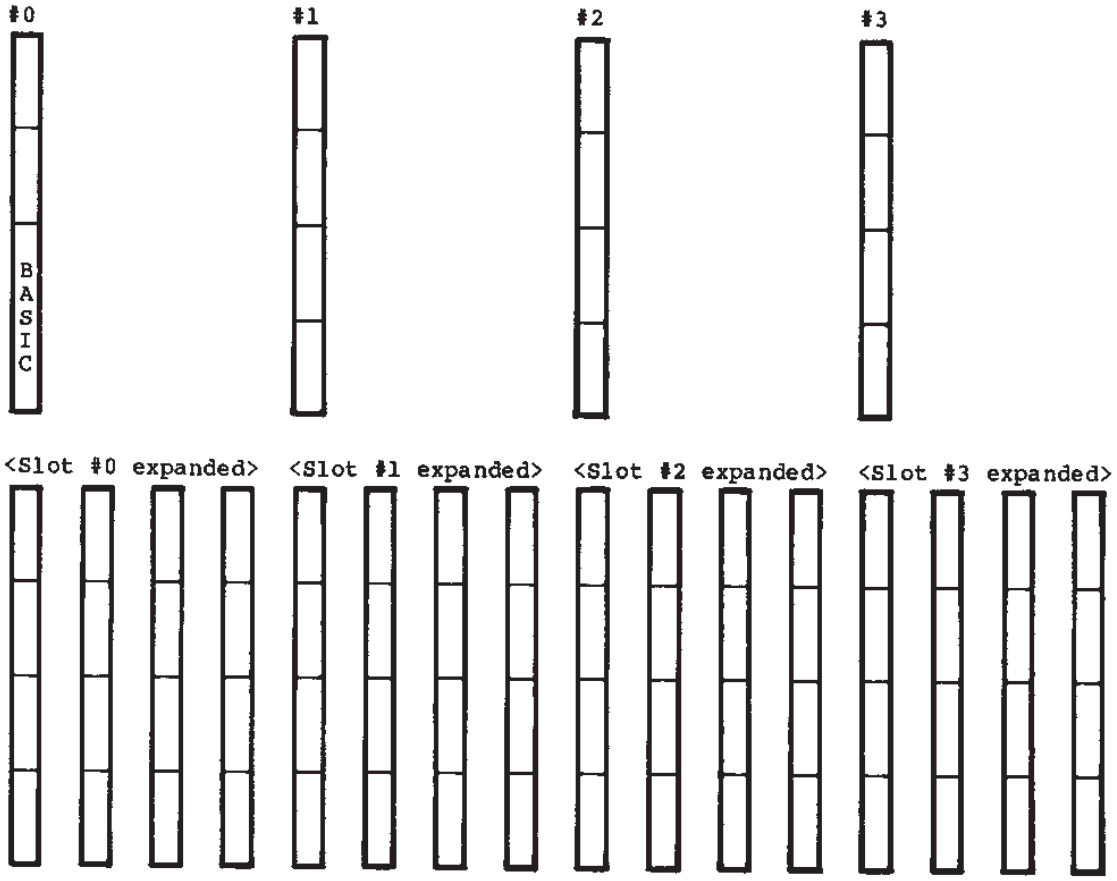
2.2.3 Slot Control

[Memory structure of MSX]



Total: 1024K bytes (16*64K bytes)

Terminology:

Primary slot:	Slot enabled by the slot select register in the 8255 PPI.
Secondary slot:	Slot enabled by the expansion slot register at 0FFFFH.
Page:	Memory block (maximum 16K) in each slot. The slots are divided into four pages (0000H to 3FFFH, 4000H to 7FFFH, 8000H to 0BFFFH, and 0C000H to 0FFFFH).

o Minimum configuration

a) Microsoft MSX-BASIC interpreter at slot #0 from 0000H to 7FFFH.
b) Minimum of 8K RAM from 0E000H to 0FFFFH in any slot (including the secondary slot)

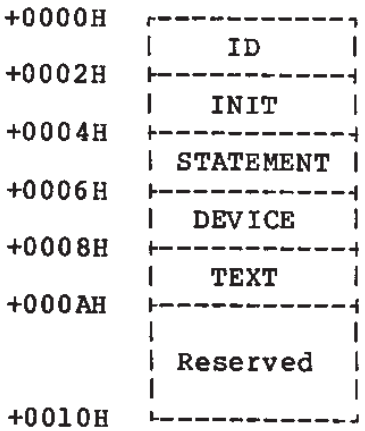
o RAM search procedure

MSX-BASIC first searches for available RAM from 0BFFFH down to 08000H (including the secondary slots), then enables the page with the largest available RAM. If there are more than one such pages, MSX-BASIC selects the leftmost page in the figure above. MSX-BASIC next searches for RAM from 0FFFFH down to 0C000H, and does the same procedure. Finally, MSX-BASIC searches for a continuous RAM block from 0FFFFH to 8000H and sets the system variable 'BOTTOM'.

o PROGRAM CARTRIGE search procedure

MSX-BASIC scans all slots (including secondary slots) from 4000H to 0BFFFH for a valid ID at the beginning of each page, collects information, and passes control to each page. The scan order is from left to right in the figure above. The format of the ID and other information are as follows.

Offset from top



- The ID is a two-byte code used to distinguish the ROM cartridges from the empty pages by using 'AB' (41H,42H).

- INIT holds the address of the initialization procedure specific to this cartridge. The default is 0 when no such procedure is necessary. Programs that need to interact with the BASIC interpreter should return control to it with a Z-80 'RET' instruction (all registers except [SP] may be destroyed). Note, however, that other programs (such as games) do not need to do this.

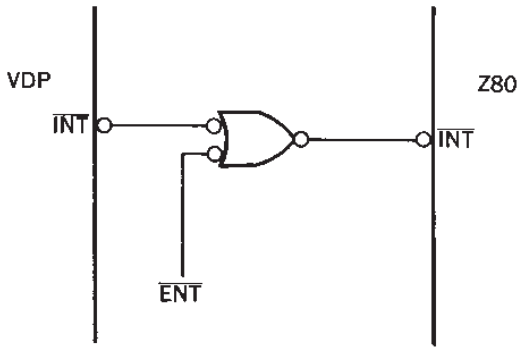
1.3.3 Interrupts

o NMI

Not used. MSX ROM only provides a RAM hook.

o INT

Interrupts are accepted from the VDP and the cartridges. The interrupt mode is 1. (Branch to 38H) The MSX system software uses an interrupt from the VDP. The interrupt intervals are 60 Hz in the NTSC version and 50 Hz in the PAL/SECAM version.



NOTE

It is not possible to support NMI under MSX-DOS because the address 66H (an entry vector for the NMI) is used by the MSX-DOS FCB data.

1.3.5 Keyboard

o Layout

Alphanumerics	: ASCII standard
Japanese syllables	: JIS standard syllable layout
European	: International versions
Graphic Characters	: Depending on international version (Selected by jumper connection)

o Scanning

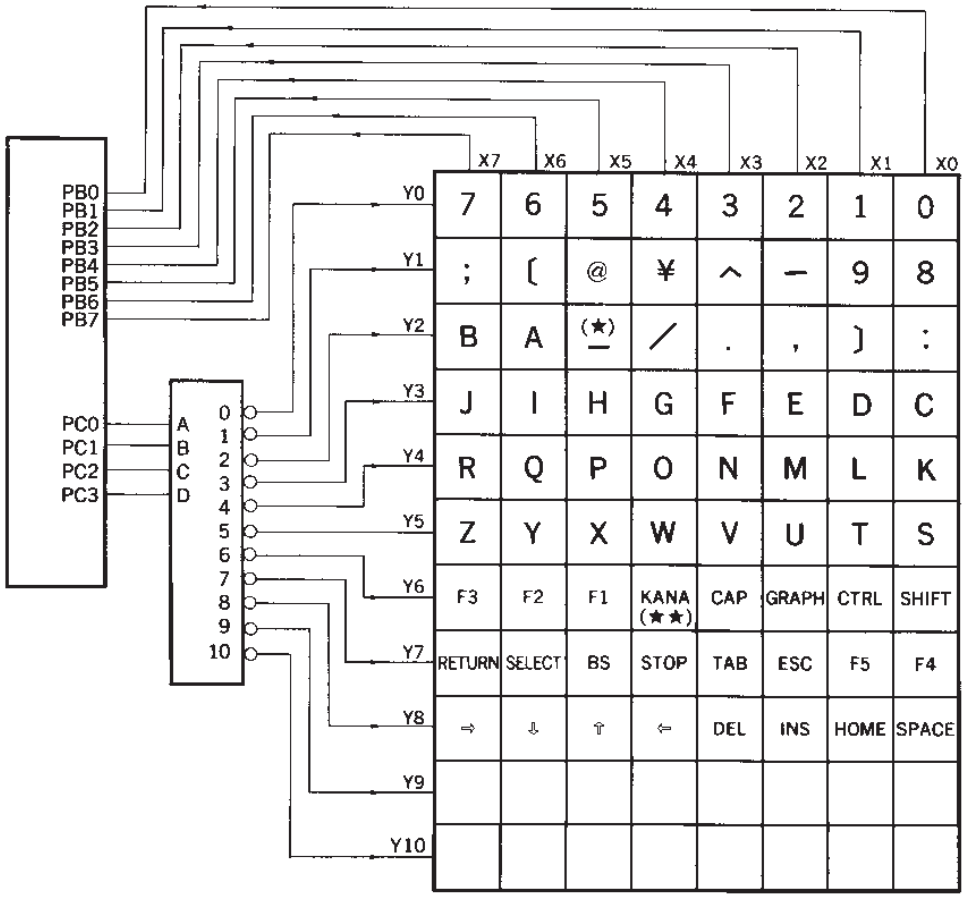
Software scanning driven by VDP interrupt

o Number of keys

72

See section 5.2.2/5.2.3 for details.

o Matrix diagram



★ Underscore character.
★★ Code Lock key in international versions.

1.3.6 Sound

- LSI
  GI AY-3-8910 Compatible.Clock 1.7897725 MHz (1/2 CPU clock)

- OCTAVES
  8 Octaves (3 Voices)

- SOUND EFFECTS
  Available

- SOFTWARE SOUND OUTPUT
  1 bit from output port

- OUTPUT LEVEL
  -5dbm (Providing the system has an output connector)

- CONNECTOR
  RCA 2 pins (Providing the system has an output connector)

1.4 Interfaces

1.4.1 Cassette Interface

o INPUT
From the earphone terminal of the tape recorder

o OUTPUT
To the microphone terminal of the tape recorder

o SYNCHRONIZATION
Asynchronous, software-controlled

o BAUD RATES
1200 baud (1200Hz - 1 wave "0", 2400Hz - 2 waves "1") (Default)

2400 baud (2400Hz - 1 wave "0", 4800Hz - 2 waves "1"), software-selected
(The tape recorder to be used may have to be specified by the manufacturer when using 2400 baud)

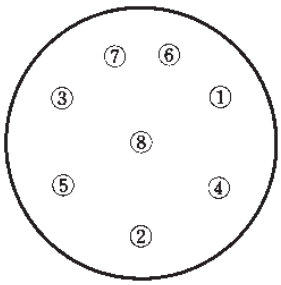
o MODULATION
FSK (Frequency Shift Keying), software-controlled

o DEMODULATION
Software-controlled. The system software automatically detects the baud rate upon receiving the data.

o MOTOR CONTROL
Available

o CONNECTOR
DIN 45326 (8 pins)

o TABLE OF SIGNAL PINS

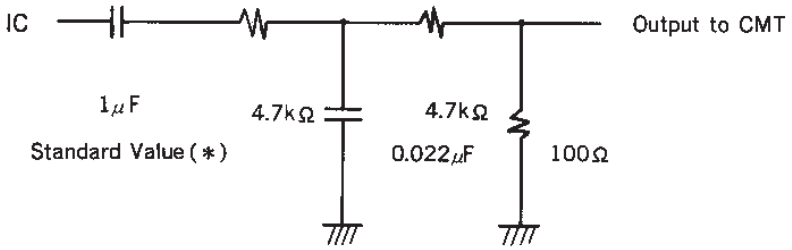
PIN NO.	SIGNAL NAME	DIRECTION	PIN CONNECTION
1	GND	---	
2	GND	---	
3	GND	---	
4	CMTOUT	OUTPUT	
5	CMTIN	INPUT	
6	REMOTE +	OUTPUT	
7	REMOTE -	OUTPUT	
8	GND	---	

o SAVE Level
The constants in the SAVE circuit should be adjusted so as to perform the output level as follows:

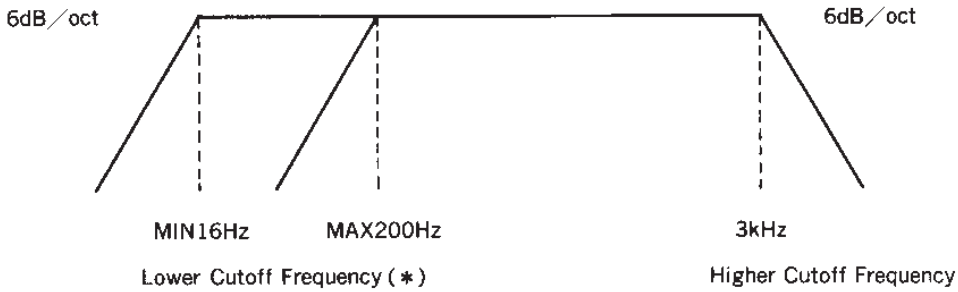
Output level -45 dBm ± 5 dBm (0 dBm = 0.775 V)

The output should be 22 mVp-p ~ 7 mVp-p at 1200 Hz input signal.

o Sample Circuit for SAVE



o Frequency Characteristics



* Note that the lower cutoff capacitor is to protect the IC of MSX. Cassette tape recorders themselves will not be harmed even if it is not there. The capacitance may be in the range 0.1 ~ 2.2μF. Adjust the capacitor to limit the lower cutoff frequency in the range 16 ~ 200Hz, if the output inpedance of the IC is too high.

1.4.9 Slots

o CONCEPT OF SLOTS

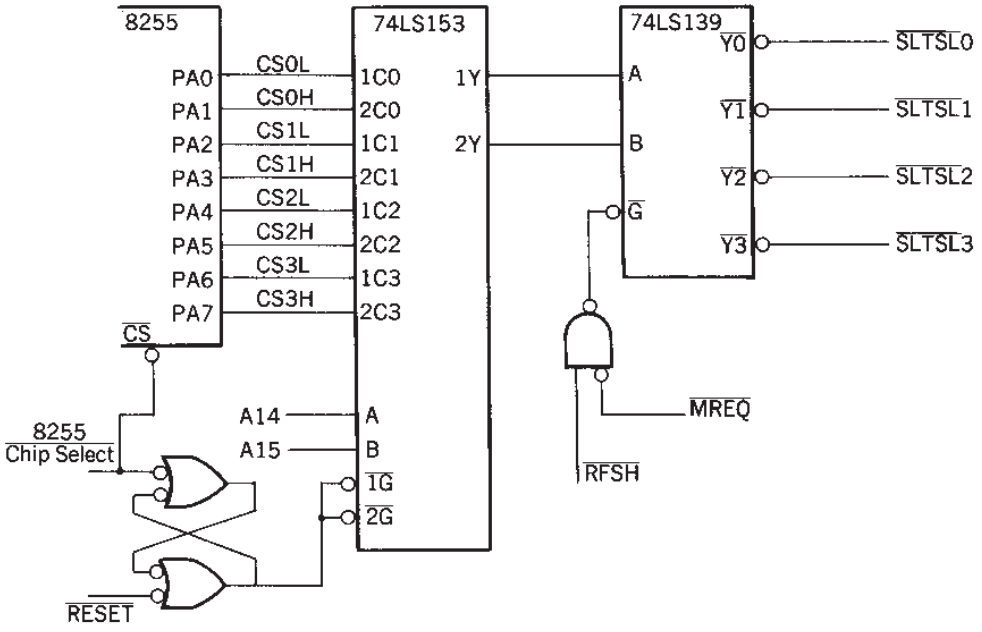
For computers having 64K bytes of memory, the concepts of slots and memory banking are nearly identical. The CPU can directly choose the cartridge by its slot number.

The slot concept originated from a desire to support the maximum amount of software. Using the slots, the software can be run, regardless of the number of physical slots available to the computer.

o ADVANTAGES OF SLOT STRUCTURE

In a common bus structure, when there is an even number of memory banks, the device select signal connected to the bus cannot distinguish between the different devices by using the same memory area. If this were to occur, the system would not only be unusable, but the hardware would quickly deteriorate. By using the slot select signal to choose the memory devices, the above problem is avoided, and programs that handle two or more devices having the same memory area are made possible. This is a favorable point, considering the system's flexibility and expandability.

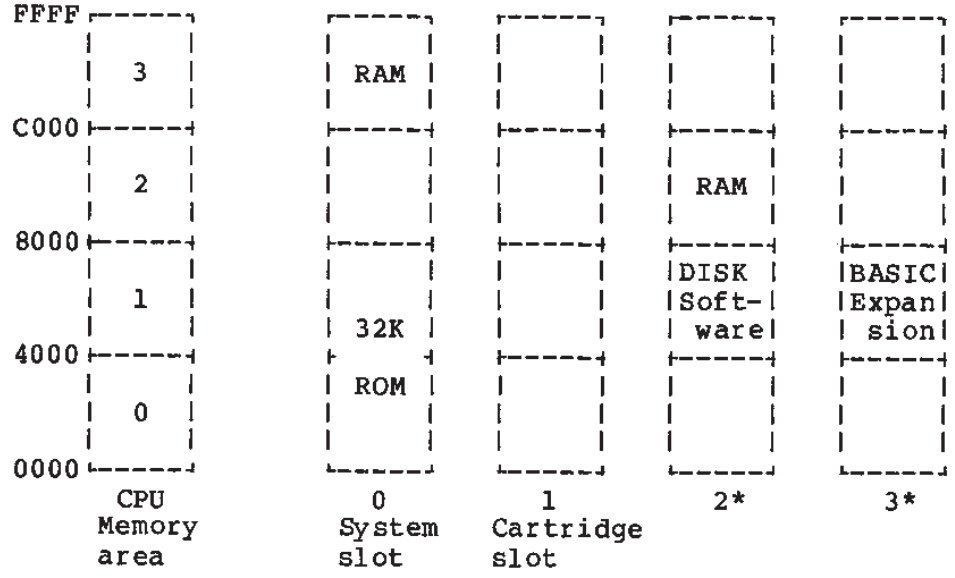
o Circuit diagram



1.7 Address Maps

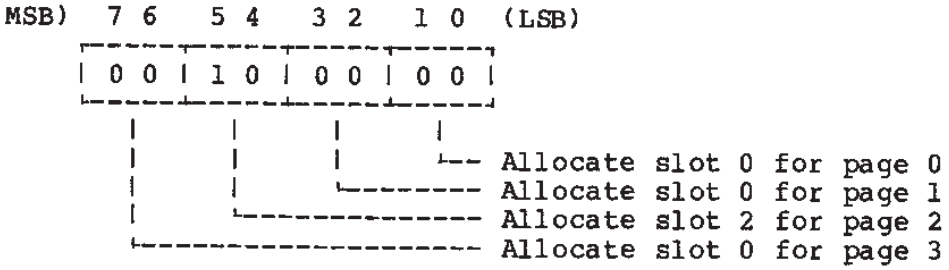
1.7.1 Memory Map

o The following is an example memory map.



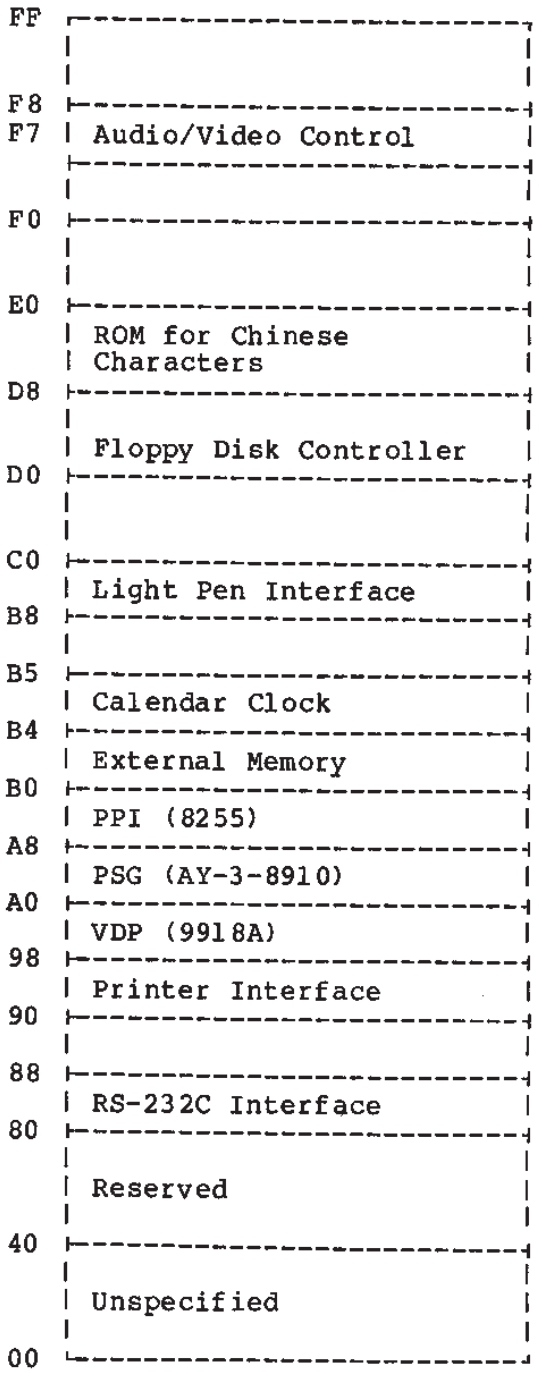
o MSX BASIC uses the largest contiguous available RAM area installed from 8000 to FFFF for its system working RAM area. This RAM may be placed in any slot, including the expansion slots.

o The slot select register, port A of the 8255, maps the physical memory space to the logical CPU memory space in 16K-byte units (pages). For example, the following value in the slot select register allocates pages 0 and 1 from slot 0, page 2 from slot 2, and page 3 from slot 0.



The physical memory is always allocated to the same memory page in the CPU memory space. It is not possible to allocate it to a different page, as in allocating page 3 of slot 3 to page 0 of the CPU memory space.

1.7.2 I/O Address Map



1.7.3 Printer Port

90H	R	Busy state: Bit 1
90H	W	Strobe output: Bit 0
91H	W	Print data

1.7.4 VDP Port

98H	R/W	Video RAM data
99H	R/W	Command and status register

1.7.5 PSG Port

A0H	W	Address latch
A1H	W	Data write
A2H	R	Data read

1.7.6 PPI Port

A8H	R/W	Port A
A9H	R/W	Port B
AAH	R/W	Port C
ABH	R/W	Mode register

1.7.7 External Memory (Sony)

B0H thruogh B3H

1.7.8 Light Pen (Sanyo)

B8H through BBH

1.7.9 Audio/Video Control

F7H	W	BIT4 - AV Control	L - TV
	W	BIT5 - Ym Control	L - TV
	W	BIT6 - Ys Control	L - Super
	W	BIT7 - Video select	L - TV

1.7.10 Notes on I/O Address Assignments

o I/O addresses 40-FF are assigned for system use. The unused empty area is also reserved for system use.

  Although I/O addresses are defined above, the software must not access those devices directly using the above ports. All I/O accesses must be done using BIOS calls, in order to make the software independent of hardware differences. MSX manufacturers may change some of the hardware from the standard MSX system and maintain software compatibility by rewriting BIOS. The hardware differences would thus be transparent to the software.

  The only exception to the above is the access to the VDP. Locations 6 and 7 of the MSX system ROM contains the Read and Write addresses of the VDP register. Software that must access the VDP quickly may access the VDP directly by using the addresses stored in ROM.

o Addresses 00 to 3F are free. Different devices using the same address must not be accessed simultaneously. In general, the I/O devices that are not defined here should be placed in the memory space as memory-mapped I/O. See section 1.6.3 for further details.

% The FDC may be placed in the I/O area; however, it must have a mechanism to disable it, and it must be enabled only if the system does accesses to the FDC. This makes it possible for the system to have more than one FDC interface for handling different media types.

1.7.11 8255 (PPI) Bit Assignments

PORT	BIT	I/O	SIGNAL NAME	DESCRIPTION
A	0		CS0L	0000-3FFF Address slot select signal
	1	O	CS0H	
	2	U	CS1L	4000-7FFF Address slot select signal
	3	T	CS1H	
	4	P	CS2L	8000-BFFF Address slot select signal
	5	U	CS2H	
	6	T	CS3L	C000-FFFF Address slot select signal
	7		CS3H	
B	0	I		Keyboard return signal
	|	N		
	|	P		
	|	U		
	7	T		
C	0		KB0	Keyboard scan signal
	1		KB1	
	2	O	KB2	
	3		KB3	
		U		
	4	T	CASON	Cassette control signal (L=ON)
		P		
	5		CASW	Cassette write signal
		U		
	6	T	CAPS	CAPS lamp signal (L=ON)
	7		SOUND	Software-controlled sound output

1.7.12 PSG Bit Assignments

PORT	BIT	I/O	CONNECTOR PIN NO.	NOTES
A	0		J3-PIN 1 #1	FWD1
			J4-PIN 1 * #2	FWD2
	1	I	J3-PIN 2 #1	BACK1
			J4-PIN 2 * #2	BACK2
	2	N	J3-PIN 3 #1	LEFT1
			J4-PIN 3 * #2	LEFT2
	3	P	J3-PIN 4 #1	RIGHT1
			J4-PIN 4 * #2	RIGHT2
	4	U	J3-PIN 6 #1	TRGA1
			J4-PIN 6 * #2	TRGA2
	5	T	J3-PIN 7 #1	TRGB1
			J4-PIN 7 * #2	TRGB2
	6		KEY LAYOUT Select #4	Japanese version only
	7		CSAR (Cassette tape READ)	
B	0		J3-PIN 6 #3	--
	1	O	J3-PIN 7 #3	| "H" Level
	2	U	J4-PIN 6 * #3	|
	3	T	J4-PIN 7 * #3	--
	4	P	J3-PIN 8	
	5	U	J4-PIN 8 *	
	6	T	PORT A INPUT SELECT	Selects J3 or J4
	7		KLAMP (KANA LAMP L=ON)	Japanese version only

#1 Available if bit 6 of port B is LOW and is used by JOYSTICK1
#2 Available if bit 6 of port B is HIGH and is used by JOYSTICK2
#3 Set these pins to "H" when using them as an input port.
Connect an open collector buffer to the output.
#4 JIS layout - "H", syllable layout - "L"

<Remark> PIN 5: +5V
PIN 9: GND

o On the minimum MSX system, there is no J4 connector.