

一种硅锗双极技术中的60GHz超外差下变频混频器

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Abstract—A single-balanced Gilbert mixer intended for use in

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mixer core current consumption of 3.2 A at 2.7 V. Total test-site current consumption, including an output buffer, is 19.2 mA.

索引词-毫米波频率, 混频器, MMIC, re-接收器, SiGe.

I. INTRODUCTION

THE steadily increasing frequency ranges of SiGe bipolar and CMOS process technologies have made millimeter-wave radio circuits possible in silicon [1]–[4]. This has created the possibility of low-cost, highly integrated millimeter-wave radios for a variety of applications, such as wireless data transmission over directed links [5], wireless personal-area networks (WPANs) [6], and automotive radar [7]. For wireless data transmission, there is particular interest in the unlicensed 57–64-GHz Industrial, Scientific, and Medical (ISM) band because the large amount of bandwidth available there allows high data rates.

This paper describes the design and measurement results of a single-balanced Gilbert mixer intended for use in a superheterodyne receiver with an RF input of 57–64 GHz and a variable IF in the range of 8.3–9.1 GHz, as shown in the simplified schematic of Fig. 1. This is one of the first reports of silicon-based active mixers at this frequency. Earlier, we reported a direct-conversion quadrature downconverter in the same SiGe process technology [8], and others have reported a double-balanced mixer at 77 GHz [9]. SiGe bipolar technology has been used to fabricate low-noise amplifiers, voltage-controlled oscillators, and power amplifiers in the 60- and 77-GHz bands as well [10], [11]. The present superheterodyne mixer achieves approximately 10 dB wider dynamic range than the previously reported direct downconverter, as judged by the relative noise figures and input-referred 1-dB compression points.

The present single-balanced mixer is envisioned as the first mixer in a future double-conversion superheterodyne receiver. The second frequency conversion would be a quadrature mixer converting the 8.3–9.1-GHz IF signal to baseband. The variable IF is chosen because it allows the use of a single frequency synthesizer to generate both the first and second LO signals. This overall receiver architecture minimizes the amount of signal processing done at 60 GHz, in contrast to the earlier reported direct-conversion architecture [8].

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In some applications, double-balanced mixers are preferred over single-balanced designs because they provide reduced leakage of the local oscillator (LO) signal to the IF output. Double-balanced mixers may also provide reduced second-order intermodulation distortion products due to the cancellation of even-order distortion terms. Third-order intermodulation distortion is primarily determined by the transconductor portion of the mixer and both topologies can perform well in this respect. In the present architecture, the single-balanced mixer is chosen over a double-balanced design because it simplifies the 60-GHz circuitry, having only two switching transistors (Q3 and Q4 in Fig. 1) and requiring only a single (unbalanced) RF input. The LO signal and any second-order distortion products present at the mixer output are removed by filtering in the subsequent IF amplifier.

In a 60-GHz WPAN application, the lack of stronger adjacent-channel interferers means that linearity requirements are not stringent. Our system design assumes a maximum received signal of approximately -30 dBm at the antenna, and both the present single-balanced mixer and the earlier double-balanced design have adequate linearity and dynamic range for such an application, especially when preceded by a variable-gain low-noise amplifier (LNA).

II. DESIGN

The mixer is fabricated in a $0.12\text{-}\mu\text{m}$ emitter-stripe width SiGe bipolar process that achieves $f_T \geq 200$ GHz and $f_{\text{MAX}} \geq 250$ GHz [1]. Other technology features include thin-film metal resistors and four layers of metal with two thick final Al layers that facilitate high- Q inductors, transmission lines, and metal-insulator-metal (MIM) capacitors. In the technology version used, there were not yet any MOSFETs or related devices.

Referring to Fig. 1, the RF input signal is applied through an input-matching network to a common-base input stage (Q1) which is biased with a constant-current source (Q2) at 3.2 mA. The supply voltage V_{CC} is 2.7 V. In simulation, the stability of the common-base input stage was less sensitive to parasitic ground inductance than a common-emitter stage. Although inductive degeneration often stabilizes a common-emitter stage, the overall effect of simulated test fixture ground inductance (including inductance added to the input network and power supply network) was to de-stabilize the common-emitter stage. However, in laboratory measurements, neither common-emitter nor common-base stages exhibited instability. The choice of the common-base stage also simplifies the input matching network and allows for high linearity. The input matching inductor (L1) is a $100\text{-}\mu\text{m}$ long section of top-level metal over the substrate, with the silicon under L1 cross-hatched with oxide-filled trenches.

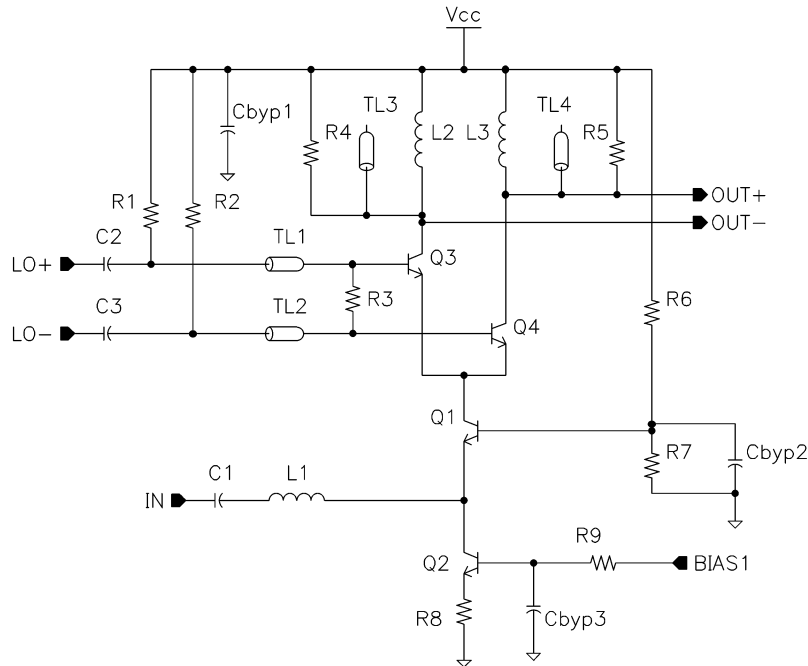


Fig. 1. Simplified schematic of the mixer. The output buffer, biasing circuits, and power supply decoupling components are omitted.

The mixer switches are driven from off-chip with an LO signal in the 48–56 GHz range, depending on the RF input frequency. The LO signals are routed on the chip using microstrip transmission lines which are resistively terminated near the mixer switches.

The mixer's tuned *RLC* load ($L2$ - $R4$ - $TL3$ and $L3$ - $R5$ - $TL4$) is designed to resonate at approximately 8.8 GHz. The load resistors $R4$ and $R5$ are 300 Ω , so a unity voltage-gain output buffer is used to drive off-chip test equipment which has a 100- Ω differential input impedance. The output buffer consists of a resistively degenerated differential pair with an inductive load, biased at 16 mA total. The buffer has high output impedance and is designed for operation into the external 100- Ω load. The output buffer is for test only, since in a more highly integrated receiver circuit the mixer output would drive the following IF amplifier without going off the chip. The input capacitance of the output buffer is absorbed into the mixer load capacitance. Since the additional explicit load capacitance required by the mixer is small, the capacitors are realized by short lengths of open-circuited microstrip transmission line ($TL3$ and $TL4$). Explicit load capacitance was added instead of making $L2$ and $L3$ larger because it makes the resonant frequency less sensitive to the amount of parasitic capacitance on these nodes.

III. MEASUREMENTS AND DISCUSSION

The mixers were tested by wafer probing using coplanar waveguide probes in a ground-signal-ground configuration for the RF, LO, and IF signals. For test purposes, the 100- Ω balanced output of the buffer drives a hybrid coupler which converts the signal into a 50- Ω unbalanced signal to drive our test equipment. In order to create an accurate 100- Ω differential load for the output buffer, 6-dB resistive attenuators were used between each of the buffer's outputs and the hybrid coupler's inputs. The total loss in the output IF path is about 7 dB,

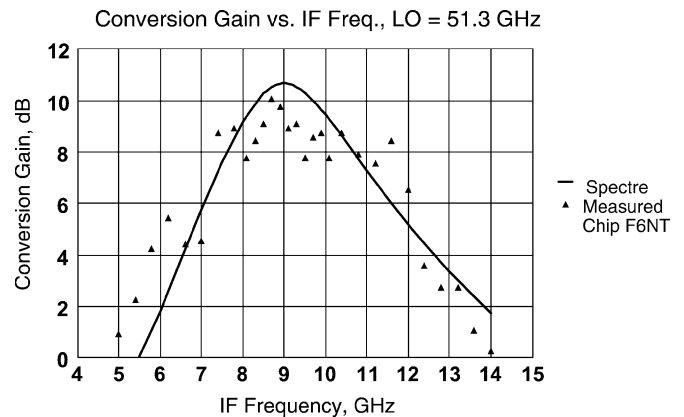


Fig. 2. Measured and simulated voltage conversion gain of the mixer versus IF, with LO frequency held constant at 51.3 GHz.

including the 1-dB insertion loss of the coupler. Measurements are also adjusted to account for the frequency-dependent loss of the probes (approximately 0.9 dB at 60 GHz) and coaxial cables. Total loss in the RF input path is about 3.9 dB. No on-chip losses were de-embedded.

Fig. 2 shows the measured and simulated voltage conversion gain of the mixer as a function of the IF frequency, with the LO frequency held constant at 51.3 GHz. Insertion power gain was measured from the RF input of the mixer to the unbalanced output of the coupler. By adding 3 dB to account for the 100–50 Ω impedance transformation, this power gain was converted to a voltage conversion gain, which can be thought of as the ratio of the differential IF-signal voltage at the mixer output to the RF-signal voltage at the mixer input. It is the output voltage of the mixer which is relevant in our system, since the mixer output is not impedance matched to the following stage. The power conversion gain of the cascaded mixer and output buffer can be obtained by subtracting 3 dB from the data in

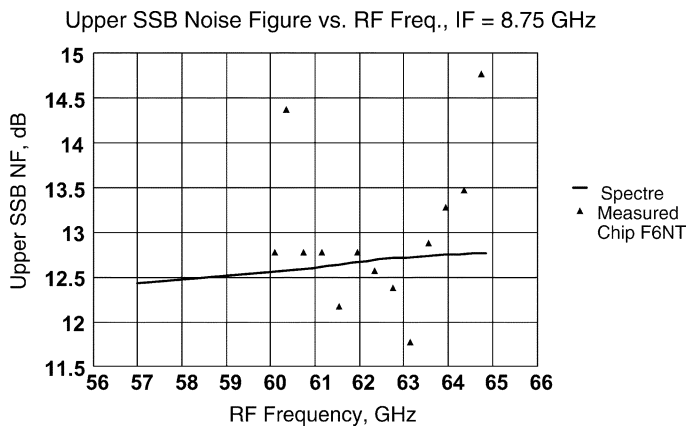


Fig. 3. Measured and simulated upper SSB NF of the mixer versus RF input frequency, with IF held constant at 8.75 GHz.

Fig. 2. The measured input-referred 1-dB compression point (ICP1dB) of the cascaded mixer and output buffer is -7 dBm. Note that much higher power gains could have been obtained by designing the output buffer to have greater than unity voltage gain, although of course this would affect ICP1dB, IIP3, and power consumption.

Input return loss (S_{11}) for the mixer input is -10 to -11 dB over the 57–64 GHz band. This compares with simulated values of -15 to -19 dB; the poorer measured input match (and lower Q) is believed to be due to inadequately modeled losses in the input pad. The measurements shown in Fig. 2 were not corrected for the imperfect S_{11} of the mixer; such a correction would be 0.5 dB or less and is within the measurement tolerance.

The conversion gain data in Fig. 2 were taken manually, using as an RF source a frequency synthesizer driving a frequency multiplier (Anritsu 54000-4WR15) and measuring IF output power using a spectrum analyzer. The equipment was calibrated over the frequency range of the measurements, but variations in the synthesizer output, frequency multiplier gain, spectrum analyzer sensitivity, and test setup losses contribute to an estimated tolerance of about ± 1 dB in the conversion gain data.

Fig. 3 shows the measured and simulated upper single-sideband (SSB) noise figure (NF) of the mixer. To make SSB measurements, the output of our noise source was passed through a waveguide filter with a very sharp cutoff below 59.5 GHz, to remove the noise power from the lower sideband. Upper SSB NF measurements below 60 GHz were thus not possible, but an NF of 13 dB or below was achieved over most of the band, and close agreement with the simulated NF data was observed. NF measurements at these frequencies are difficult due to variations in wafer probe resistance, variations in noise source effective noise ratio (ENR) over frequency, and the need to accurately account for frequency-dependent losses between the noise source and the circuit. Thus, the NF data shows more scatter than might be expected at lower frequencies.

Fig. 4 shows the variation in NF and conversion gain with LO power, using an LO frequency of 52 GHz and an IF frequency of 8.75 GHz. The NF and gain are quite sensitive to reduction of LO power below approximately -4 dBm (560-mV peak-to-

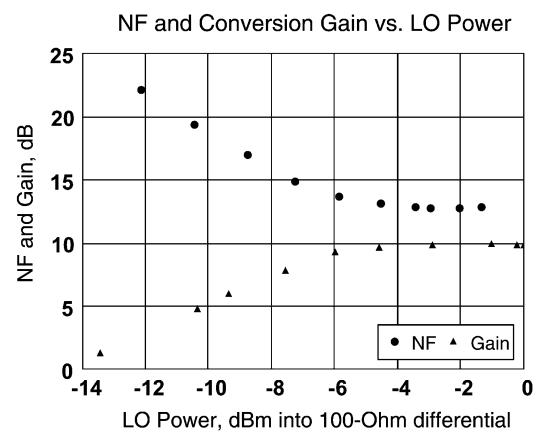


Fig. 4. Measured upper SSB NF and voltage conversion gain of mixer versus LO input power, with RF, LO, and IF frequencies held constant at 60.75 GHz, 52 GHz, and 8.75.

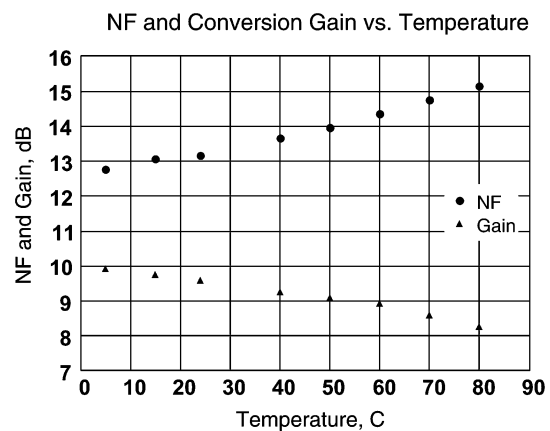


Fig. 5. Measured upper SSB NF and voltage conversion gain of the mixer versus temperature, with RF, LO, and IF frequencies held constant at 60.15, 51.4, and 8.75 GHz, respectively.

peak differential at the mixer switches), and an LO power level of -3 dBm was used for all other measurements in this paper.

Isolation between the LO port and the RF and IF ports is a concern with any mixer. Measured LO-to-RF isolation is in the 26–30-dB range. Direct measurement of LO-to-IF isolation was not possible because the on-chip output buffer and off-chip test fixture do not pass the LO frequency. Circuit simulations indicate that the LO signal is passed to the mixer output with approximately 20 dB of attenuation.

Fig. 5 summarizes temperature measurements on the mixer. At constant bias current, the conversion gain decreases by 1.8 dB from 5°C to 80°C , while the NF rises from 12.8 to 15.2 dB. Measurements at temperatures above 80°C were erratic due to oxidation of the Al pads; the Be–Cu probes could not achieve a low-resistance contact above these temperatures. Tungsten or Ni probes more suitable for probing Al pads will be used in future testing.

A die photograph of the mixer and output buffer is shown in Fig. 6. The RF input is on the right, the differential LO inputs are on the left, and the IF outputs are taken from the top and bottom of the pad frame. Spiral inductors L2 and L3 which form part of the mixer load can be seen on the right, and the spiral load

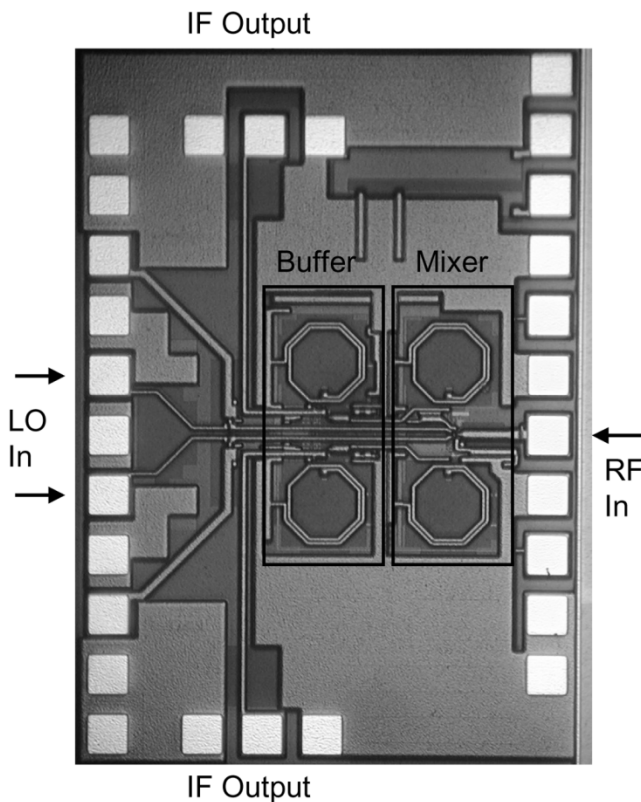


Fig. 6. Die photograph of mixer test site. Die size to outside of pad frame is 1.24 mm by 1.8 mm. See text for other component locations.

inductors for the output buffer are in the center. Input-matching inductor L1 can be seen extending from the RF-input pad to input-transistor Q1, located between L2 and L3. The test site is 1.24 mm by 1.8 mm to the outside of the pad frame.

The present superheterodyne mixer's 13-dB NF is comparable to the NF of the previously reported direct downconverter [8], but the superheterodyne mixer's ICP1dB of -7 dBm is 10 dB better than the -17 -dBm ICP1dB of the direct downconverter. Cascaded in a single IC with the previously reported LNA [8], which has 17 dB of gain and an NF of 4.4 dB or better, both the superheterodyne and direct-conversion mixers would give an RFIC NF in the range of 5–6 dB, and both would appear to be practical choices for a highly integrated 60-GHz transceiver chip.

IV. CONCLUSION

A single-balanced Gilbert mixer, for use in the 60-GHz ISM band, and fabricated in a SiGe bipolar technology, has been reported. It is among the first reported active mixers in silicon

at these frequencies. The mixer uses low-side LO injection at 48–56 GHz and an 8.3–9.1-GHz variable IF. It achieves a 13-dB NF and has greater than 9 dB of voltage conversion gain, with a mixer current consumption of 3.2 mA. Including an IF output buffer for test purposes, it has greater than 6 dB of power conversion gain and 19.2-mA total current. The design and testing of this mixer is one of the first steps toward the fabrication of a highly integrated 60-GHz transceiver system in silicon.

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