CoreSight™ ETM™-A7

Revision: r0p0

Technical Reference Manual

ARM®

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CoreSight ETM-A7
Technical Reference Manual

Release Information

The following changes have been made to this book.

Change history

Date	Issue	Confidentiality	Change
12 September 2011	A	Non-Confidential	First release for r0p0

Proprietary Notice

Confidentiality Status

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Product Status

The information in this document is final, that is for a developed product.

Web Address

`http://www.arm.com`

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CoreSight ETM-A7 Technical Reference Manual

Preface

This preface introduces the *CoreSight ETM-A7 Technical Reference Manual*. It contains the following sections:

About this book

This book is for the CoreSight *Embedded Trace Macrocell* (ETM) for the Cortex-A7 MPCore™ processor, the ETM-A7 macrocell. Implementation-specific behavior is described in this document. You can find complementary information in the *Embedded Trace Macrocell Architecture Specification*.

Product revision status

The r*n*p*n* identifier indicates the revision status of the product described in this book, where:

r*n* Identifies the major revision of the product.

p*n* Identifies the minor revision or modification status of the product.

Intended audience

This book is written for designers of development tools, who are providing support for ETM functionality.

Using this book

This book is organized into the following chapters:

Chapter 1 *Introduction*

Read this for an introduction to the functionality of the macrocell.

Chapter 2 *Functional Description*

Read this for a description of the interfaces, operation, clocking and resets of the macrocell.

Chapter 3 *Programmers Model*

Read this for a description of the programmers model for the macrocell.

Appendix A *Signal Descriptions*

Read this for a description of all signals.

Appendix B *Revisions*

Read this for a description of technical changes between released issues of this book.

Glossary

The ARM glossary is a list of terms used in ARM documentation, together with definitions for those terms. The ARM glossary does not contain terms that are industry standard unless the ARM meaning differs from the generally accepted meaning.

See *ARM Glossary*, http://infocenter.arm.com/help/topic/com.arm.doc.aeg0014-/index.html.

Conventions

Conventions that this book can use are described in:

- *Typographical* on page vii
- *Timing diagrams* on page vii
- *Signals* on page vii.

Typographical

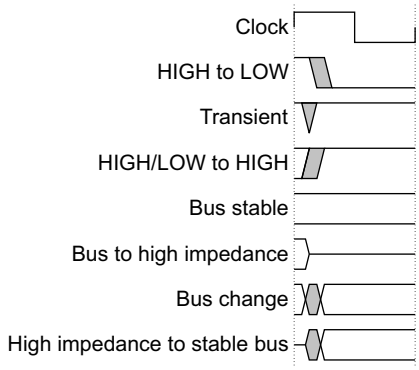
The typographical conventions are:

italic	Highlights important notes, introduces special terminology, denotes internal cross-references, and citations.
bold	Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.
`monospace`	Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.
`mono`space	Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.
`monospace italic`	Denotes arguments to monospace text where the argument is to be replaced by a specific value.
`monospace bold`	Denotes language keywords when used outside example code.
< and >	Enclose replaceable terms for assembler syntax where they appear in code or code fragments. For example: `MRC p15, 0 <Rd>, <CRn>, <CRm>, <Opcode_2>`

Timing diagrams

The figure named *Key to timing diagram conventions* explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams.

Shaded bus and signal areas are undefined, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.



Key to timing diagram conventions

Signals

The signal conventions are:

Signal level The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW. Asserted means:

- HIGH for active-HIGH signals
- LOW for active-LOW signals.

Lower-case n At the start or end of a signal name denotes an active-LOW signal.

Additional reading

This section lists publications by ARM and by third parties.

See Infocenter, http://infocenter.arm.com, for access to ARM documentation.

ARM publications

This book contains information that is specific to this product. See the following documents for other relevant information:

- *AMBA® APB Protocol Specification* (ARM IHI 0024)
- *AMBA 3 ATB Protocol Specification* (ARM IHI 0032)
- *CoreSight Architecture Specification* (ARM IHI 0029)
- *CoreSight ETM-A7 Configuration and Sign-off Guide (*ARM DII 0261)
- *CoreSight ETM-A7 Release Note* (TM956-DC-06003)
- *Embedded Trace Macrocell Architecture Specification* (ARM IHI 0014)
- *Cortex-A7 MPCore Technical Reference Manual* (ARM DDI 0434)
- *CoreSight SoC User Guide* (ARM DUI 0563).

Feedback

ARM welcomes feedback on this product and its documentation.

Feedback on this product

If you have any comments or suggestions about this product, contact your supplier and give:

- The product name.
- The product revision or version.
- An explanation with as much information as you can provide. Include symptoms and diagnostic procedures if appropriate.

Feedback on content

If you have comments on content then send an e-mail to `errata@arm.com`. Give:

- the title
- the number, ARM DDI 0468A
- the page numbers to which your comments apply
- a concise explanation of your comments.

ARM also welcomes general suggestions for additions and improvements.

Chapter 1
Introduction

This chapter introduces the CoreSight ETM-A7 macrocell. It contains the following sections:

1.1 About the CoreSight ETM-A7 macrocell

The CoreSight ETM-A7 macrocell provides instruction trace and data trace for the Cortex-A7 MPCore processor. The macrocell is designed for you to use in a CoreSight system.

Figure 1-1 shows the main functional blocks of a Cortex-A7 integration layer, that includes a CoreSight ETM-A7 macrocell, in a typical CoreSight *System-on-Chip* (SoC).

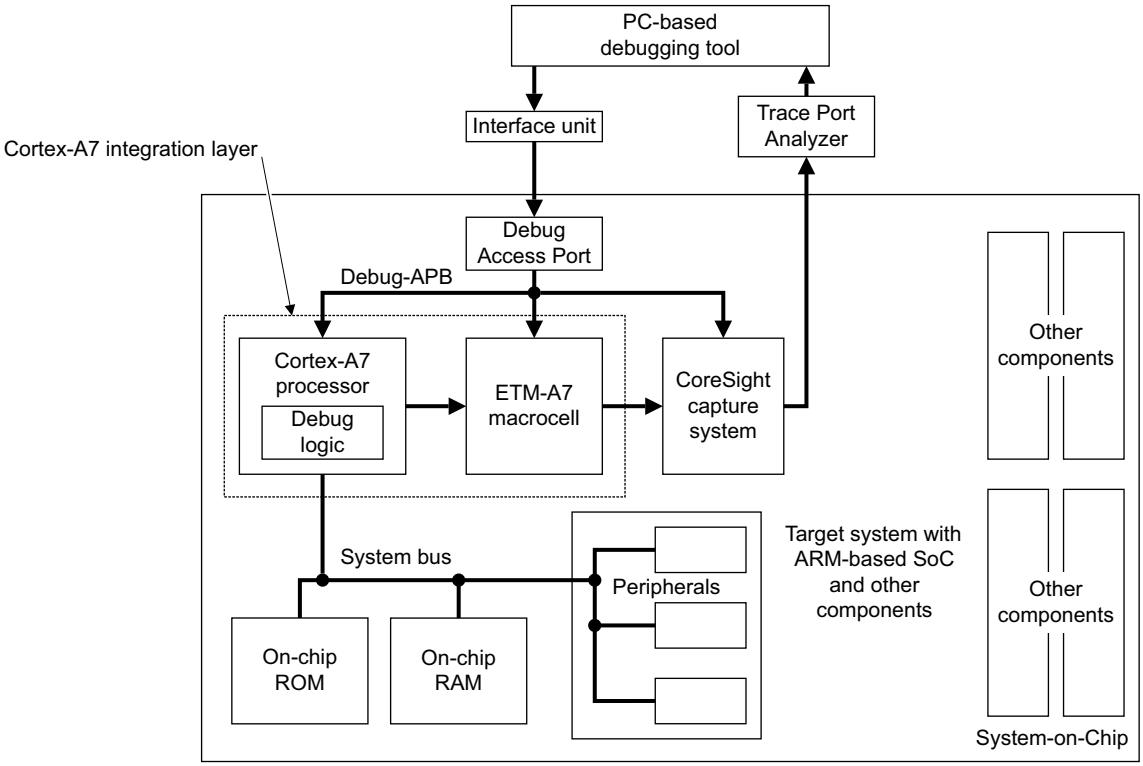


Figure 1-1 Cortex-A7 integration layer with ETM-A7 block diagram

1.2 Compliance

The ETM-A7 complies with, or implements, the specifications described in:

- *Embedded Trace Macrocell architecture*
- *CoreSight Architecture*
- *Advanced Microcontroller Bus Architecture*.

This TRM complements architecture reference manuals, architecture specifications, protocol specifications, and relevant external standards. It does not duplicate information from these sources.

1.2.1 Embedded Trace Macrocell architecture

The ETM-A7 macrocell implements ETM architecture version 3.5. See the *Embedded Trace Macrocell Architecture Specification*.

1.2.2 CoreSight Architecture

The ETM-A7 macrocell complies with CoreSight architecture version 1.0. See the *CoreSight Architecture Specification*.

1.2.3 Advanced Microcontroller Bus Architecture

The ETM-A7 macrocell complies with the:

- AMBA 3 *Advanced Peripheral Bus* (APB) protocol. See the *AMBA APB Protocol Specification.*
- AMBA 3 *Advanced Trace Bus* (ATB) protocol. See the *AMBA 3 ATB Protocol Specification*.

1.3 Features

The ETM-A7 macrocell supports tracing of ARM and Thumb instructions.

The *Embedded Trace Macrocell Architecture Specification* describes the features of ETM v3.5.

Table 1-1 lists the configured features of the ETM-A7 macrocell that are implementation-defined, in terms of either:

- the number of times the feature is implemented
- the size of the feature.

Table 1-1 Configured features of the ETM-A7 macrocell

Feature	Configuration	Notes
Address comparators	4 pairs	See bits[3:0] of the ETMCCR[a]
Data value comparators	2	See bits[7:4] of the ETMCCR[a]
EmbeddedICE watchpoint comparators	0	See bits[19:16] of the ETMCCER[b]
Context ID comparators	1	See bits[25:24] of the ETMCCR[a]
Counters	2	See bits[15:13] of the ETMCCR[a]
Sequencer	1	See bit[16] of the ETMCCR[a]
Memory Map decoder inputs	0	See bits[12:8] of the ETMCCR[a]
External inputs	0-4	See bits[19:17] of the ETMCCR[a]
External outputs	0-2	See bits[22:20] of the ETMCCR[a]
Extended external input bus width	30	See bits[10:3] of the ETMCCER[b]
Extended external input selectors	2	See bits[2:0] of the ETMCCER[b]
Instrumentation resources	0	See bits[15:13] of the ETMCCER[b]
Trace port size	64-bit	See bits[21,6:4] of the ETMCR[c]
VMID comparator	1	See bit[26] of the ETMCCER[b]
FIFO size	144 bytes	-
ASICCTL general-purpose bus interface	8-bit	See *ASIC Control Register* on page 3-19

a. See *Configuration Code Register* on page 3-18.
b. See *Configuration Code Extension Register* on page 3-21.
c. See *Main Control Register* on page 3-14.

Table 1-2 shows the optional ETM architecture features the ETM-A7 macrocell implements.

Table 1-2 ETM-A7 macrocell implementation of optional features

Feature	Implemented	Notes
FIFOFULL control	No	See bit[23] of the ETMCCR[a]
Trace Start/Stop block	Yes	See bit[26] of the ETMCCR[a]
Trace all branches	Yes	See bit[8] of the ETMCR[b]

Table 1-2 ETM-A7 macrocell implementation of optional features (continued)

Feature	Implemented	Notes
Cycle-accurate trace	Yes	See bit[12] of the ETMCR[b]
Data trace options		
Data address tracing	Yes	See bits[3:2] of the ETMCR[b]
Data value tracing	Yes	See bits[3:2] of the ETMCR[b]
Data-only tracing	Yes	See bit[20] of the ETMCR[b]
CPRT tracing	Yes	See bits[19, 1] of the ETMCR[b]
Timestamping	Yes	See bit[28] of the ETMCCER[c]
Data address comparison	Yes	bit[12] of the ETMCCER[c]
EmbeddedICE behavior control	No	See bit[21] of the ETMCCER[c]
EmbeddedICE inputs to Trace Start/Stop block	No	See bit[20] of the ETMCCER[c]
Alternative address compression	No	See bit[20] of the ETMIDR
OS Lock mechanism	Yes	See bits[3, 0] of the ETMOSLSR
Secure non-invasive debug	Yes	See the *Embedded Trace Macrocell Architecture Specification*
Context ID tracing	Yes	See bits[15:14] of the ETMCR[b]
VMID tracing	Yes	See bit[26] of the ETMCCER[c]
Reduced function counter	No	See bit[27] of the ETMCCER[c]

a. See *Configuration Code Register* on page 3-18.
b. See *Main Control Register* on page 3-14.
c. See *Configuration Code Extension Register* on page 3-21.

See the *Embedded Trace Macrocell Architecture Specification* for information about:
- the trace protocol
- controlling tracing using triggering and filtering resources
- ETM sharing.

See Appendix A *Signal Descriptions* for information about the macrocell signals.

1.4 Interfaces

A debugger:

- programs the macrocell through its *Advanced Peripheral Bus* (APB) interface. In a CoreSight system, the APB interface connects to the Debug APB bus.
- collects trace data through the *Advanced Trace Bus* (ATB).

The other external connections to the ETM-A7 macrocell are:

- 0-4 external inputs
- 0-2 external outputs
- a 30-bit extended external input bus.

See *Configurable options* on page 1-7 for more information about the external inputs and external outputs.

In a Cortex-A7 integration layer, each ETM-A7 macrocell connects to the corresponding processor in the multiprocessor device:

- ETM interface.
- *Performance Monitoring Unit* (PMU). The PMU **PMUEVENT[29:0]** signals connect directly to the ETM-A7 macrocell extended external interface bus signals.

Interfaces on page 2-3 describes the ETM-A7 macrocell interfaces in more detail.

1.5 Configurable options

The ETM-A7 macrocell includes the following configuration inputs:

- **MAXEXTOUT[1:0]** determines the maximum number of external outputs
- **MAXEXTIN[2:0]** determines the maximum number of external inputs.

On an ETM-A7 implementation, these configuration inputs might be tied off to fixed values, or they might be available as configuration pins on the SoC.

The MAXETIN and MAXEXTOUT values are determined by bits[21:17] of the ETMCCR. See *Configuration Code Register* on page 3-18 for more information.

1.6 Test features

The ETM-A7 macrocell provides the **DFTSE** and **DFTRSTDISABLE** inputs for testing the implemented device. See *Signal descriptions* on page A-2 for more information.

See also *Integration test registers* on page 3-29 for information about the integration test registers provided for testing the ETM-A7 macrocell implementation in the SoC.

1.7 Product documentation and design flow

This section describes the ETM-A7 macrocell books and how they relate to the design flow:

- *Documentation*
- *Design flow*.

See *Additional reading* on page viii for more information about the books described in this section.

1.7.1 Documentation

The ETM-A7 documentation is as follows:

Technical Reference Manual

The *Technical Reference Manual* (TRM) describes the functionality and the effects of functional options on the behavior of the ETM-A7 macrocell. It is required at all stages of the design flow. Some behavior described in the TRM might not be relevant because of the way that the ETM-A7 macrocell is implemented and integrated. If you are programming the ETM-A7 macrocell then contact the integrator to determine the pin configuration of the SoC that you are using.

Configuration and Sign-Off Guide

The *Configuration and Sign-Off Guide* (CSG) describes:

- the available build configuration options and related issues in selecting them
- how to configure the *Register Transfer Level* (RTL) description with the build configuration options
- the processes to sign off the configured design.

The ARM product deliverables include reference scripts and information about using them to implement your design. Reference methodology flows supplied by ARM are example reference implementations. For EDA tool support, contact your EDA vendor.

The CSG is a confidential book that is only available to licensees.

1.7.2 Design flow

The ETM-A7 macrocell is delivered as synthesizable RTL. Before it can be used in a product, it must go through the following processes:

Implementation

The implementer configures and synthesizes the RTL to produce a macrocell..

Integration The integrator connects the implemented design into a SoC. This includes connecting it to a CoreSight System.

Programming

The system programmer develops the software required to configure and initialize the ETM-A7 macrocell, and tests the required application software.

Each process:

- can be performed by a different party

- can include implementation and integration choices that affect the behavior and features of the ETM-A7 macrocell.

  Build configuration

  The ETM-A7 macrocell has no implementer defined options.

  Configuration inputs

  The integrator configures some features of the ETM-A7 macrocell by tying inputs to specific values. These configurations affect the start-up behavior before any software configuration is made. They can also limit the options available to the software.

  Software configuration

  The programmer configures the ETM-A7 macrocell by programming particular values into software-visible registers. This affects the behavior of the ETM-A7 macrocell.

  See *Register summary* on page 3-5 and *Register descriptions* on page 3-14 for information on the ETM-A7 macrocell registers.

Note

This manual refers to implementation-defined features that are applicable to build configuration options. References to a feature that is included mean that the appropriate build and pin configuration options have been selected. Reference to an enabled feature means that the feature has also been configured by software.

1.8 Product revisions

This section describes the differences in functionality between product revisions:

r0p0 First release.

Chapter 2
Functional Description

This chapter describes the interfaces, operation, and clocking and resets of the ETM-A7 macrocell. It contains the following sections:

2.1 About the ETM-A7 macrocell functions

Figure 2-1 shows the main functional blocks. The ETM-A7 macrocell operates in a single clock domain, **CLK**, which is identical to the processor clock. The ATB and APB interfaces can operate at slower clock rates, but still synchronously to **CLK**, using the **ATCLKEN** and **PCLKENDBG** clock enables respectively. If the system requires the ETM-A7 macrocell to operate asynchronously to the system ATB clock or APB clock then the ETM-A7 macrocell interfaces must include the appropriate bridge components as shown in Figure 2-1.

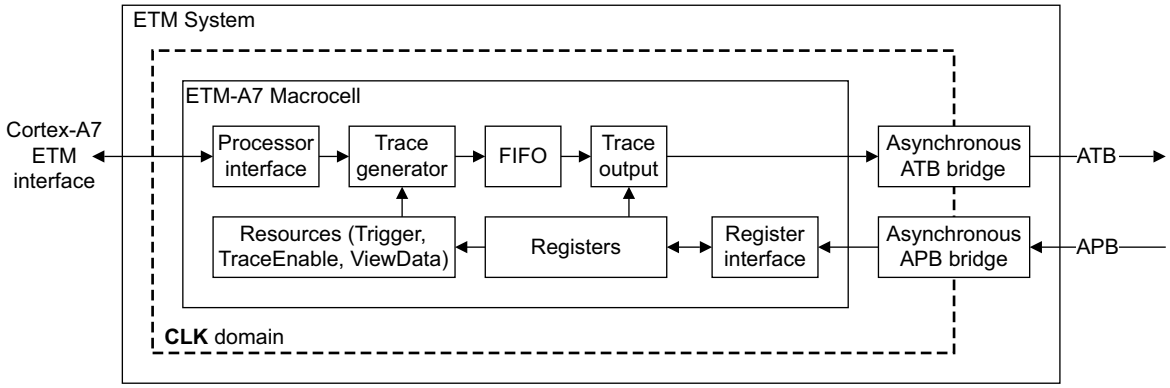


Figure 2-1 ETM-A7 Macrocell functional blocks and clock domains

2.2 Interfaces

The ETM-A7 macrocell has the following external interfaces:

ATB A 64-bit ATB, used for trace output from the macrocell. See the *AMBA 3 ATB Protocol Specification* for more information about this interface.

APB An APB provides the control interface for the macrocell. See the *AMBA APB Protocol Specification* for more information about this interface.

Cortex-A7 MPCore ETM interface

The Cortex-A7 MPCore processor passes its execution information to the ETM-A7 macrocell over this bus. This includes instruction address, branch, exception, data address, data value and PMU information.

2.3 Clocking and resets

The following sections describe the ETM-A7 clock, clock enable, and reset signals:

- *Clock signals*
- *Clock enable signals*
- *Resets*.

2.3.1 Clock signals

The ETM-A7 macrocell uses a single clock, **CLK**. This must be the same clock as that wired to the **CLKIN** input of the Cortex-A7 MPCore processor.

2.3.2 Clock enable signals

The ETM-A7 macrocell has the following clock enable signals:

ATCLKEN This is the ATB clock enable. It can be used to operate the trace port at any integer multiple that is equal to, or slower, than **CLK**.

PCLKENDBG This is the Debug APB interface clock enable. It can be used to operate the debug logic at any integer multiple that is equal to, or slower, than **CLK**.

2.3.3 Resets

The ETM-A7 macrocell has the following reset:

nSYSPORESET This signal is the main power-on reset. It is active-LOW.

2.4 Operation

This section describes the implementation-defined features. It contains the following sections:

- *Implementation-defined registers*
- *Precise TraceEnable events*
- *Parallel instruction execution* on page 2-6
- *Context ID tracing* on page 2-6
- *Trace and Comparator features* on page 2-6
- *Interaction with the Performance Monitoring Unit (PMU)* on page 2-6
- *Other implementation-defined features of the macrocell* on page 2-7.

See the *Embedded Trace Macrocell Architecture Specification* for more information about the operation of the ETM-A7 macrocell.

2.4.1 Implementation-defined registers

In terms of how they are defined, there are two groups of ETM registers:

- registers that are completely defined by the *Embedded Trace Macrocell Architecture Specification*
- registers that are at least partly implementation-defined.

Chapter 3 *Programmers Model* gives more information about the ETM registers in the following sections:

- *Register summary* on page 3-5
- *Register descriptions* on page 3-14.

In Chapter 3, the following sections describe each of the implementation-defined registers:

- *Main Control Register* on page 3-14
- *Configuration Code Register* on page 3-18
- *ASIC Control Register* on page 3-19
- *ID Register* on page 3-20
- *Configuration Code Extension Register* on page 3-21
- *Extended External Input Selection Register* on page 3-23
- *Power-Down Status Register* on page 3-24
- *Auxiliary Control Register* on page 3-25
- *ETM ID Register 2* on page 3-25
- *Peripheral identification registers* on page 3-26
- *Component identification registers* on page 3-28
- *Integration test registers* on page 3-29.

2.4.2 Precise TraceEnable events

The *Embedded Trace Macrocell Architecture Specification* states that **TraceEnable** is imprecise under certain conditions, with some implementation-defined exceptions. When the enabling event selects the following resources, it does not cause **TraceEnable** to be imprecise, provided that the resources are themselves precise:

- single address comparators
- address range comparators.

2.4.3 Parallel instruction execution

The Cortex-A7 MPCore processor supports parallel instruction execution. This means the ETM is capable of tracing two instructions per cycle.

Although the trace start/stop block is evaluated for each instruction as required, the ETM-A7 macrocell cannot trace one instruction without the other. In other words, if one instruction is traced, the instruction it is paired with is also traced. If **ViewData** is active, any data associated with the paired instruction is also traced.

2.4.4 Context ID tracing

The ETM-A7 macrocell detects the `MCR` instruction that changes the context ID, and traces the appropriate number of bytes as a context ID packet instead of a normal data packet. This means that if context ID tracing is enabled, an `MCR` instruction that changes the context ID does not have its data traced separately.

2.4.5 VMID tracing

The ETM-A7 macrocell detects the `MCR` instruction that changes the VMID, and traces the appropriate number of bytes as a VMID packet along with the normal data packet.

2.4.6 Trace and Comparator features

In ETM Architecture v3.5, it is implementation-defined whether an ETM supports a number of Trace and Comparator features. This section specifies the implementation of these features on the CoreSight ETM-A7 macrocell:

- *Trace features*
- *Comparator features*.

Trace features

The ETM-A7 macrocell implements all of the ETMv3.5 trace features. This means it supports:

- data value and data address tracing
- data suppression
- cycle-accurate tracing.

For descriptions of these features, see the *Embedded Trace Macrocell Architecture Specification*.

Comparator features

The ETM-A7 macrocell implements data address comparison. For a description of data address comparison see the *Embedded Trace Macrocell Architecture Specification*.

2.4.7 Interaction with the *Performance Monitoring Unit* (PMU)

The Cortex-A7 MPCore processor includes a PMU that enables events, such as cache misses and instructions executed, to be counted over a period of time. The macrocell can still use these events by means of the extended external input facility. Each bit in the **PMUEVENT[29:0]** input is mapped to the corresponding extended external input. See the *Cortex-A7 MPCore Technical Reference Manual* for information about the mapping of events to bits within this bus.

The Cortex-A7 MPCore PMU can count the two external outputs as additional events. These events are not provided back to the macrocell as extended external inputs.

These facilities enable additional filtering of the system events using ETM resources, such as instruction address ranges or the start/stop resource, before they are passed back to the PMU for counting. To do this:

- Configure the ETM extended external input selectors to the system events you want to count.
- Configure the required ETM filtering resource as appropriate.
- Configure the ETM external outputs to extended external input selector and the required ETM filtering resource.
- Select the ETM external outputs as the events to be counted in the Cortex-A7 MPCore PMU.

2.4.8 Other implementation-defined features of the macrocell

The following implementation-defined features of the macrocell do not affect the descriptions of the features given in the *Embedded Trace Macrocell Architecture Specification*:

- Value Not Traced packets are not output in data-only mode. When data address tracing is enabled in data-only mode, an address packet is output for each traced data transfer for which the data address is not sequential to the previously traced data transfer.
- When a branch packet is traced because of entry to a prohibited region, the packet always indicates an ISA of ARM state.
- The cycle counter continues to count while Non-invasive debug is disabled.
- The **ETMDBGRQ** signal is deasserted when the programming bit is set.

2.5 Constraints and limitations of use

This section describes the constraints and limitations of use that apply to the ETM-A7 macrocell.

2.5.1 Port mode and port size

The ETM-A7 macrocell only supports a 64-bit port size, and only supports the dynamic port mode.

In the ETMCR, at offset `0x0`, from reset:

- the Port size bits, bits[21, 6:4], take the value `0b0110`, indicating a 64-bit port
- the Port mode bits, bits[17:16, 13], take the value `0b000`, indicating dynamic port mode.

For more information see *Main Control Register* on page 3-14.

Chapter 3
Programmers Model

This chapter describes the programmers model of the CoreSight ETM-A7 macrocell. It contains the following sections:

3.1 About the programmers model

This chapter describes the mechanisms for programming the registers used to set up the trace and triggering facilities of the macrocell. The programmers model enables you to use the ETM registers to control the macrocell.

3.2 Mode of operation

The following sections describe how you control ETM programming.

- *Controlling ETM programming*
- *Programming and reading ETM registers*.

3.2.1 Controlling ETM programming

When programming the ETM registers you must enable all the changes at the same time. For example, if the counter is reprogrammed, it might start to count based on incorrect events, before the trigger condition has been correctly set up.

You can use the ETM programming bit in the ETMCR to disable all trace operations during programming. See *Main Control Register* on page 3-14.

The processor does not have to be in debug state while you program the ETM registers.

3.2.2 Programming and reading ETM registers

You program and read the ETM registers using the debug APB interface. This provides a direct method of programming:

- a stand-alone macrocell
- a macrocell in a CoreSight system.

Note

Access to the ETM registers using coprocessor instructions, or the Direct JTAG access method, is not supported.

3.3 Data structures

See the *Embedded Trace Macrocell Architecture Specification* for descriptions of the trace packet formats generated by the ETM-A7 macrocell.

3.4 Register summary

This section gives a summary of the ETM registers. See the *Embedded Trace Macrocell Architecture Specification*, for more information a using the ETM registers.

Table 3-1 shows all of the ETM registers listed in register number order and indicates where each register is described.

The macrocell registers are listed by functional group in *Functional grouping of registers* on page 3-9. The functional group register tables include additional information about each register, they provide:

- the register number.
- additional information about the implementation of the register, where appropriate.
- access type of each ETM register as follows:

  RW Read and write.

  RO Read only.

  WO Write only.

Note

Registers not listed here are not implemented. Reading a non-implemented register address returns 0. Writing to a non-implemented register address has no effect.

All ETM registers are 32 bits wide.

Table 3-1 ETM-A7 register summary

Register number	Name	Type	Reset	Description
0x000	ETMCR	RW	0x00000461	*Main Control Register* on page 3-14
0x001	ETMCCR	RO	0x8D014024[a]	*Configuration Code Register* on page 3-18
0x002	ETMTRIGGER	RW	-[b]	Trigger Event Register, see the*Embedded Trace Macrocell Architecture Specification*
0x003	ETMASICCTLR	RW	-[b]	*ASIC Control Register* on page 3-19
0x004	ETMSR	RW	-[b]	ETM Status Register, see the *Embedded Trace Macrocell Architecture Specification*
0x005	ETMSCR	RO	0x00020C0C[c]	System Configuration Register, see the *Embedded Trace Macrocell Architecture Specification*
0x006	ETMTSSCR	RW	-[b]	TraceEnable Start/Stop Control Register, see the *Embedded Trace Macrocell Architecture Specification*
0x007	ETMTECR2	RW	-[b]	TraceEnable Control 2 Register, see the *Embedded Trace Macrocell Architecture Specification*
0x008	ETMTEEVR	RW	-[b]	TraceEnable Event Register, see the *Embedded Trace Macrocell Architecture Specification*
0x009	ETMTECR1	RW	-[b]	TraceEnable Control 1 Register, see the *Embedded Trace Macrocell Architecture Specification*
0x00B	ETMFFLR[d]	RW	-[b]	FIFOFULL Level Register, see the *Embedded Trace Macrocell Architecture Specification*

Table 3-1 ETM-A7 register summary (continued)

Register number	Name	Type	Reset	Description
0x00C	ETMVDEVR	RW	-[b]	ViewData Event Register, see the *Embedded Trace Macrocell Architecture Specification*
0x00D	ETMVDCR1	RW	-[b]	ViewData Control 1 Register, see the *Embedded Trace Macrocell Architecture Specification*
0x00F	ETMVDCR3	RW	-[b]	ViewData Control 3 Register, see the *Embedded Trace Macrocell Architecture Specification*
0x010-0x017	ETMACVR1-8	RW	-[b]	Address Comparator Value Registers 1-8, see the *Embedded Trace Macrocell Architecture Specification*
0x020-0x027	ETMACTR1-8	RW	-[b]	Address Comparator Access Type Registers 1-8, see the *Embedded Trace Macrocell Architecture Specification*
0x030[e]	ETMDCVR1[e]	RW	-[b]	Data Comparator Value Register 1, see the *Embedded Trace Macrocell Architecture Specification*
0x032[e]	ETMDCVR3[e]	RW	-[b]	Data Comparator Value Register 3, see the *Embedded Trace Macrocell Architecture Specification*
0x040[e]	ETMDCMR1[e]	RW	-[b]	Data Comparator Mask Register 1, see the *Embedded Trace Macrocell Architecture Specification*
0x042[e]	ETMDCMR3[e]	RW	-[b]	Data Comparator Mask Register 3, see the *Embedded Trace Macrocell Architecture Specification*
0x050, 0x051	ETMCNTRLDVR1-2	RW	-[b]	Counter Reload Value Registers 1-2, see the *Embedded Trace Macrocell Architecture Specification*
0x054, 0x055	ETMCNTENR1-2	RW	-[b]	Counter Enable Registers 1-2, see the *Embedded Trace Macrocell Architecture Specification*
0x058, 0x059	ETMCNTRLDEVR1-2	RW	-[b]	Counter Reload Event Registers 1-2, see the *Embedded Trace Macrocell Architecture Specification*
0x05C, 0x05D	ETMCNTVR1-2	RW	-[b]	Counter Value Registers 1-2, see the *Embedded Trace Macrocell Architecture Specification*
0x060 0x065	ETMSQ*ab*EVR	RW	-[b]	Sequencer State Transition Event Registers, see the *Embedded Trace Macrocell Architecture Specification*
0x067	ETMSQR	RW	-[b]	Current Sequencer State Register, see the *Embedded Trace Macrocell Architecture Specification*
0x068, 0x069	ETMEXTOUTEVR1-2	RW	-[b]	External Output Event Registers 1-2, see the *Embedded Trace Macrocell Architecture Specification*
0x06C	ETMCIDCVR1	RW	-[b]	Context ID Comparator Value 1 Register, see the *Embedded Trace Macrocell Architecture Specification*
0x06F	ETMCIDCMR	RW	-[b]	Context ID Comparator Mask Register, see the *Embedded Trace Macrocell Architecture Specification*
0x078	ETMSYNCFR	RW	0x00000400	Synchronization Frequency Register, see the *Embedded Trace Macrocell Architecture Specification*
0x079	ETMIDR	RO	0x410CF25x[f]	*ID Register* on page 3-20
0x07A	ETMCCER	RO	0x344008F2	*Configuration Code Extension Register* on page 3-21

Table 3-1 ETM-A7 register summary (continued)

Register number	Name	Type	Reset	Description
0x07B	ETMEXTINSELR	RW	-[b]	*Extended External Input Selection Register* on page 3-23
0x07E	ETMTSEVR	RW	-[b]	Timestamp Event Register, see the *Embedded Trace Macrocell Architecture Specification*
0x07F	ETMAUXCR	RW	-	*Auxiliary Control Register* on page 3-25
0x080	ETMTRACEIDR	RW	0x00000000	CoreSight Trace ID Register, see the *Embedded Trace Macrocell Architecture Specification*
0x082	ETMIDR2	RO	-	*ETM ID Register 2* on page 3-25
0x090	ETMVMIDCVR	WO	-[b]	VMID Comparator Value Register, see the *Embedded Trace Macrocell Architecture Specification*
0x0C0	ETMOSLAR	WO	-	OS Lock Access Register, see the *Embedded Trace Macrocell Architecture Specification*
0x0C1	ETMOSLSR	RO	-	OS Lock Status Register, see the *Embedded Trace Macrocell Architecture Specification*
0x0C2	ETMOSSRR	RW	-	OS Save and Restore Register, see the *Embedded Trace Macrocell Architecture Specification*
0x0C4	ETMPDCR	RW	-	*Power-Down Control Register* on page 3-23
0x0C5	ETMPDSR	RO	-[b]	*Power-Down Status Register* on page 3-24
0x3B7	ITMISCOUT	WO	n/a[i]	*Integration Test Miscellaneous Outputs register* on page 3-31
0x3B8	ITMISCIN	RO[g]	-[h]	*Integration Test Miscellaneous Input Register* on page 3-32
0x3BA	ITTRIGGERREQ	WO	n/a[i]	*Integration Test Trigger Request Register* on page 3-33
0x3BB	ITATBDATA0	WO	n/a[i]	*Integration Test ATB Data 0 Register* on page 3-34
0x3BC	ITATBCTR2	RO[g]	-[h]	*Integration Test ATB Control Register 2* on page 3-35
0x3BD	ITATBCTR1	WO	n/a[i]	*Integration Test ATB Control Register 1* on page 3-36
0x3BE	ITATBCTR0	WO	n/a[i]	*Integration Test ATB Control Register 0* on page 3-37
0x3C0	ETMITCTRL	RW	0x00000000	Integration Mode Control Register, see the *Embedded Trace Macrocell Architecture Specification*
0x3E8	ETMCLAIMSET	RW	0x000000FF	Claim Tag Set Register, see the *Embedded Trace Macrocell Architecture Specification*
0x3E9	ETMCLAIMCLR	RW	0x00000000	Claim Tag Clear Register, see the *Embedded Trace Macrocell Architecture Specification*
0x3EC	ETMLAR	WO	n/a[i]	Lock Access Register, see the *Embedded Trace Macrocell Architecture Specification*
0x3ED	ETMLSR	RO	-	Lock Status Register, see the *Embedded Trace Macrocell Architecture Specification*
0x3EE	ETMAUTHSTATUS	RO	-	Authentication Status Register, see the *Embedded Trace Macrocell Architecture Specification*

Table 3-1 ETM-A7 register summary (continued)

Register number	Name	Type	Reset	Description
0x3F2	ETMDEVID	RO	0x00000000	CoreSight Device Configuration Register, see the *Embedded Trace Macrocell Architecture Specification*
0x3F3	ETMDEVTYPE	RO	0x00000013	CoreSight Device Type Register, see the *Embedded Trace Macrocell Architecture Specification*
0x3F4-0x3F7	ETMPIDR4-7	RO	-	*Peripheral identification registers* on page 3-26
0x3F8-0x3FB	ETMPIDR0-3	RO	-	
0x3FC-0x3FF	ETMCIDR0-3	RO	-	*Component identification registers* on page 3-28

a. Default value when **MAXEXTOUT[1:0]** and **MAXEXTIN[2:0]** are all tied LOW, see the register description for more information.

b. The register is not reset by a reset of the macrocell. Therefore, it does not have a specific default value, and its reset value is UNKNOWN.

c. Bits[14:12] of the System Configuration Register are tied to the **MAXCORES[2:0]** signals. If a **MAXCORES** bit is HIGH then the corresponding bit in the System Configuration Register is set to 1, for example if **MAXCORES[0]** is tied HIGH then bit[12] is set to 1. The default value given is for all **MAXCORES** signals tied LOW, bits[14:12] = 0b000.

For more information about the **MAXCORES[2:0]** signals, see *Signal descriptions* on page A-2.

d. Although the macrocell does not include FIFOFULL logic, the FIFOFULL Level Register controls the FIFO level at which data suppression occurs. For more information, see the *Embedded Trace Macrocell Architecture Specification*.

e. In the Data Comparator register area, even number registers are reserved. For the CoreSight ETM-A7 macrocell, reserved areas are:

Register 0x031, Data Comparator Value 2, at offset 0x0C4.

Register 0x033, Data Comparator Value 4, at offset 0x0CC.

Register 0x041, Data Comparator Mask 2, at offset 0x104.

Register 0x043, Data Comparator Mask 4, at offset 0x10C.

You must not write to these reserved register addresses. Reads from these addresses are UNPREDICTABLE.

f. The value of bits[3:0] of the ETMIDR depend on the macrocell revision, see *ID Register* on page 3-20 for more information.

g. The values of the read-only Integration Test registers are valid only when the macrocell is in Integration Test mode. If you read one of these registers when the macrocell is in normal operating mode, the result returned is UNKNOWN.

h. See the register description for information.

i. Not applicable.

3.4.1 Functional grouping of registers

This section lists the ETM-A7 macrocell registers by functional group as follows:

- *General control and ID registers*
- *TraceEnable and ViewData registers* on page 3-10
- *Comparator registers* on page 3-10
- *Counter, sequencer and other resource registers* on page 3-11
- *CoreSight management registers* on page 3-13
- *Integration test registers* on page 3-13.

These functional groups include all of the registers.

Note

All registers are in the **CLK** clock domain.

General control and ID registers

Table 3-2 shows the general control and ID registers in register number order.

Table 3-2 General control and ID registers

Register number	Name	Base offset	Description
0x000	ETMCR	0x000	*Main Control Register* on page 3-14
0x001	ETMCCR	0x004	*Configuration Code Register* on page 3-18
0x003	ETMASICCR	0x00C	*ASIC Control Register* on page 3-19
0x004	ETMSR	0x010	ETM Status Register, see the *Embedded Trace Macrocell Architecture Specification*
0x005	ETMSCR	0x014	System Configuration Register, see the *Embedded Trace Macrocell Architecture Specification*
0x00B	ETMFFLR[a]	0x02C	FIFOFULL Level Register, see the *Embedded Trace Macrocell Architecture Specification*
0x078	ETMSYNCFR	0x1E0	Synchronization Frequency Register, see the *Embedded Trace Macrocell Architecture Specification*
0x079	ETMIDR	0x1E4	*ID Register* on page 3-20
0x07A	ETMCCER	0x1E8	*Configuration Code Extension Register* on page 3-21
0x07F	ETMAUXCR	0x1FC	*Auxiliary Control Register* on page 3-25
0x080	ETMTRACEIDR	0x200	CoreSight Trace ID Register, see the *Embedded Trace Macrocell Architecture Specification*
0x082	ETMIDR2	0x208	*ETM ID Register 2* on page 3-25
0x0C0	ETMOSLAR	0x300	OS Lock Access Register, see the *Embedded Trace Macrocell Architecture Specification*
0x0C1	ETMOSLSR	0x304	OS Lock Status Register, see the *Embedded Trace Macrocell Architecture Specification*
0x0C2	ETMOSSRR	0x308	OS Save and Restore Register, see the *Embedded Trace Macrocell Architecture Specification*
0x0C4	ETMPDCR	0x310	*Power-Down Control Register* on page 3-23
0x0C5	ETMPDSR	0x314	*Power-Down Status Register* on page 3-24

a. Although the ETM-A7 macrocell does not include FIFOFULL logic, the FIFOFULL Level Register controls the FIFO level at which data suppression occurs. See the *Embedded Trace Macrocell Architecture Specification* for more information.

TraceEnable and ViewData registers

Table 3-3 shows the TraceEnable and ViewData registers in register number order.

Table 3-3 TraceEnable and ViewData registers

Register number	Name	Base offset	Description
0x006	ETMTSSCR	0x018	TraceEnable Start/Stop Control Register, see the *Embedded Trace Macrocell Architecture Specification*
0x007	ETMTECR2	0x01C	TraceEnable Control 2 Register, see the *Embedded Trace Macrocell Architecture Specification*
0x008	ETMTEEVR	0x020	TraceEnable Event Register, see the *Embedded Trace Macrocell Architecture Specification*
0x009	ETMTECR1	0x024	TraceEnable Control 1 Register, see the *Embedded Trace Macrocell Architecture Specification*
0x00C	ETMVDEVR	0x030	ViewData Event Register, see the *Embedded Trace Macrocell Architecture Specification*
0x00D	ETMVDCR1	0x034	ViewData Control 1 Register, see the *Embedded Trace Macrocell Architecture Specification*
0x00F	ETMVDCR3	0x03C	ViewData Control 3 Register, see the *Embedded Trace Macrocell Architecture Specification*

Comparator registers

Table 3-4 shows the comparator registers in register number order. These control the address, data, and context ID comparators.

Table 3-4 Comparator registers

Register number	Name	Base offset	Description
0x010-0x017	ETMACVR1-8	0x040-0x05F	Address Comparator Value Registers 1-8, see the *Embedded Trace Macrocell Architecture Specification*
0x020 to 0x027	ETMACTR 1-8	0x080-0x09F	Address Comparator Access Type Registers 1-8, see the *Embedded Trace Macrocell Architecture Specification*
0x030[a]	ETMDCVR1[a]	0x0C0[a]	Data Comparator Value Register 1, see the *Embedded Trace Macrocell Architecture Specification*
0x032[a]	ETMDCVR3[a]	0x0C8[a]	Data Comparator Value Register 3, see the *Embedded Trace Macrocell Architecture Specification*
0x040[a]	ETMDCMR1[a]	0x100[a]	Data Comparator Mask Register 1, see the *Embedded Trace Macrocell Architecture Specification*
0x042[a]	ETMDCMR3[a]	0x108[a]	Data Comparator Mask Register 3, see the *Embedded Trace Macrocell Architecture Specification*

Table 3-4 Comparator registers (continued)

Register number	Name	Base offset	Description
0x06C	ETMCIDCVR1	0x1B0	Context ID Comparator Value 1 Register, see the *Embedded Trace Macrocell Architecture Specification*
0x06F	ETMCIDCMR	0x1BC	Context ID Comparator Mask Register, see the *Embedded Trace Macrocell Architecture Specification*
0x090	ETMVMIDCVR	0x240	VMID Comparator Value Register, see the *Embedded Trace Macrocell Architecture Specification*

a. In the Data Comparator register area, even number registers are reserved. For the ETM-A7 macrocell, reserved areas are:
Register 0x031, Data Comparator Value 2, at offset 0x0C4.
Register 0x033, Data Comparator Value 4, at offset 0x0CC.
Register 0x041, Data Comparator Mask 2, at offset 0x104.
Register 0x043, Data Comparator Mask 4, at offset 0x10C.
You must not write to these reserved register addresses. Reads from these addresses is UNKNOWN.

Counter, sequencer and other resource registers

Table 3-5 shows the counter, sequencer and other resource registers in register number order. These control:

- the two counters, and associated events
- the sequencer, and associated state change events
- trigger events
- EXTOUT external output events
- extended external input selection.

Table 3-5 Counter, sequencer and other resource registers

Register number	Name	Base offset	Description
0x002	ETMTRIGGER	0x008	Trigger Event Register, see the *Embedded Trace Macrocell Architecture Specification*
0x050, 0x051	ETMCNTRLDEVR1-2	0x140, 0x144	Counter Reload Event Registers 1-2, see the *Embedded Trace Macrocell Architecture Specification*
0x054, 0x055	ETMCNTENR1-2	0x150, 0x154	Counter Enable Event Registers 1-2, see the *Embedded Trace Macrocell Architecture Specification*
0x058, 0x059	ETMCNTRLDEVR1-2	0x160, 0x164	Counter Reload Event Registers 1-2, see the *Embedded Trace Macrocell Architecture Specification*
0x05C, 0x05D	ETMCNTVR1-2	0x170, 0x174	Counter Value Registers, see the *Embedded Trace Macrocell Architecture Specification*
0x060-0x065	ETMSQ*ab*EVR	0x180 -0x194	Sequencer State Transition Event Registers, see the *Embedded Trace Macrocell Architecture Specification*
0x067	ETMSQR	0x19C	Current Sequencer State Register, see the *Embedded Trace Macrocell Architecture Specification*

Table 3-5 Counter, sequencer and other resource registers (continued)

Register number	Name	Base offset	Description
0x068, 0x069	ETMEXTOUTEVR	0x1A0, 0x1A4	External Output Event Registers 1-2, see the *Embedded Trace Macrocell Architecture Specification*
0x07B	ETMEXTINSELR	0x1EC	*Extended External Input Selection Register* on page 3-23
0x07E	ETMTSEVR	0x1F8	Timestamp Event Register, see the *Embedded Trace Macrocell Architecture Specification*

CoreSight management registers

Table 3-6 shows the CoreSight management registers in register number order.

Table 3-6 CoreSight management registers

Register number	Name	Base offset	Description
0x3C0	ETMITCTRL	0xF00	Integration Mode Control Register, see the *Embedded Trace Macrocell Architecture Specification*
0x3E8	ETMCLAIMSET	0xFA0	Claim Tag Set Register, see the *Embedded Trace Macrocell Architecture Specification*
0x3E9	ETMCLAIMCLR	0xFA4	Claim Tag Clear Register, see the *Embedded Trace Macrocell Architecture Specification*
0x3EC	ETMLAR	0xFB0	Lock Access Register, see the *Embedded Trace Macrocell Architecture Specification*
0x3ED	ETMLSR	0xFB4	Lock Status Register, see the *Embedded Trace Macrocell Architecture Specification*
0x3EE	ETMAUTHSTATUS	0xFB8	Authentication Status Register, see the *Embedded Trace Macrocell Architecture Specification*
0x3F2	ETMDEVID	0xFC8	CoreSight Device Configuration Register, see the *Embedded Trace Macrocell Architecture Specification*
0x3F3	ETMDEVTYPE	0xFCC	CoreSight Device Type Register, see the *Embedded Trace Macrocell Architecture Specification*
0x3F4-0x3F7	Peripheral ID4-ID7	0xFD0-0xFDC	*Peripheral identification registers* on page 3-26
0x3F8-0x3FB	Peripheral ID0-ID3	0xFE0-0xFEC	
0x3FC-0x3FF	Component ID0-ID3	0xFF0-0xFFC	*Component identification registers* on page 3-28

Integration test registers

Table 3-7 shows the integration test registers in register number order.

Table 3-7 Integration test registers

Register number	Name	Base offset	Description
0x3B7	ITMISCOUT	0xEDC	*Integration Test Miscellaneous Outputs register* on page 3-31
0x3B8	ITMISCIN	0xEE0	*Integration Test Miscellaneous Input Register* on page 3-32
0x3BA	ITTRIGGERREQ	0xEE8	*Integration Test Trigger Request Register* on page 3-33
0x3BB	ITATBDATA0	0xEEC	*Integration Test ATB Data 0 Register* on page 3-34
0x3BC	ITATBCTR2	0xEF0	*Integration Test ATB Control Register 2* on page 3-35
0x3BD	ITATBCTR1	0xEF4	*Integration Test ATB Control Register 1* on page 3-36
0x3BE	ITATBCTR0	0xEF8	*Integration Test ATB Control Register 0* on page 3-37

3.5 Register descriptions

The following sections describe the implementation-defined ETM-A7 registers:

- *Main Control Register*
- *Configuration Code Register* on page 3-18
- *ASIC Control Register* on page 3-19
- *ID Register* on page 3-20
- *Configuration Code Extension Register* on page 3-21
- *Extended External Input Selection Register* on page 3-23
- *Power-Down Status Register* on page 3-24
- *Auxiliary Control Register* on page 3-25
- *ETM ID Register 2* on page 3-25
- *Peripheral identification registers* on page 3-26
- *Component identification registers* on page 3-28
- *Integration test registers* on page 3-29.

The *Embedded Trace Macrocell Architecture Specification* describes the other ETM-A7 registers.

3.5.1 Main Control Register

The ETMCR characteristics are:

Purpose Controls general operation of the ETM, such as whether tracing is enabled or coprocessor data is traced.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-2 on page 3-9.

Figure 3-1 shows the ETMCR bit assignments.

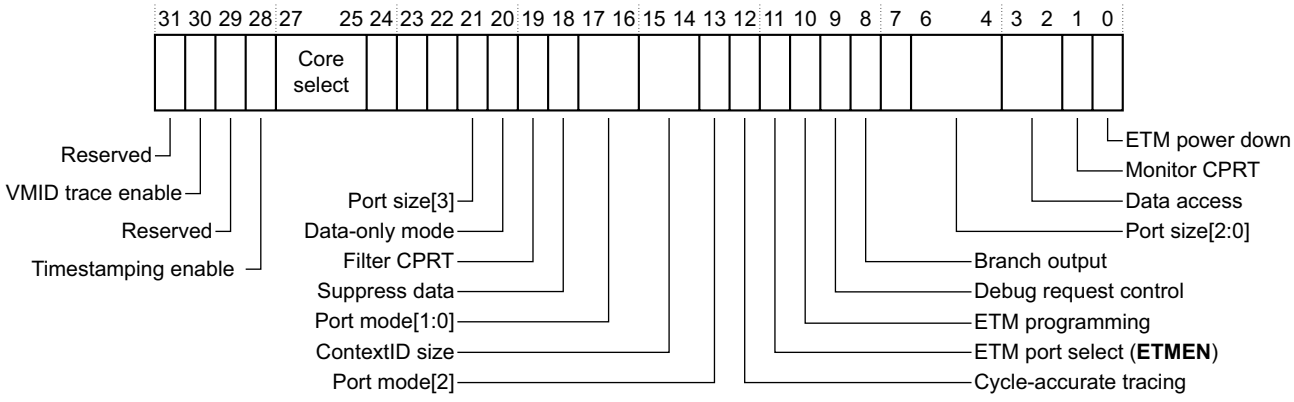


Figure 3-1 ETMCR bit assignments

Table 3-8 shows the ETMCR bit assignments.

Table 3-8 ETMCR bit assignments

Bits	Name	Description
[31]	-	Reserved, RAZ/WI.
[30]	VMID trace enable	**0** VMID tracing disable. **1** VMID tracing enable. The reset value is 0.
[29]	-	Reserved, RAZ/WI.
[28]	Timestamping enable	**0** Timestamping tracing disable. **1** Timestamping tracing enable. The reset value is 0.
[27:25]	Processor select	If an ETM is shared between multiple processors, selects which processor to trace. For the maximum value permitted, see bits[14:12] of the System Configuration Register. See the *Embedded Trace Macrocell Architecture Specification* for more information. To guarantee that the ETM is correctly synchronized to the new processor, you must update these bits as follows: 1. Set bit[10], ETM programming, and bit[0], ETM power down, to 1. 2. Change the processor select bits. 3. Set bit[0], ETM power down, to 0. 4. Perform other programming required as normal. The reset value is 0.
[24]	Instrumentation resources access control	Not supported, RAZ/WI.
[23]	Disable software writes	Not supported, RAZ/WI.
[22]	Disable register writes from the debugger	Not supported, RAZ/WI.
[21]	Port size[3]	Use this bit in conjunction with bits[6:4] in this table. The reset value is 0, corresponding to the 64-bit port size.
[20]	Data-only mode	Enables data-only tracing: **0** Instruction trace enabled. **1** Data-only tracing enabled. The reset value is 0.
[19]	Filter (CPRT)	Use this bit in conjunction with bit[1], the MonitorCPRT bit. For more information about the *Filter Coprocessor Register Transfers* (CPRT) in ETMv3.0 and later, see the *Embedded Trace Macrocell Architecture Specification*. The reset value is 0.
[18]	Suppress data	Use this bit with bit[7] to suppress data. For more information about data suppression, see the *Embedded Trace Macrocell Architecture Specification*. The reset value is 0.

Table 3-8 ETMCR bit assignments (continued)

Bits	Name	Description
[17:16]	Port mode[1:0]	In conjunction with bit[13], sets the trace port clocking mode. The ETM-A7 macrocell supports only dynamic mode, corresponding to the value `0b000`, but you can write other values to these bits, and a read of the register returns the value written. Writing another value to these bits has no effect on the ETM. bit[11] of the System Configuration Register indicates if these bits are set to select a supported clocking mode. The reset value is `0b00`. For more information about trace port clocking modes, see the *Embedded Trace Macrocell Architecture Specification*.
[15:14]	ContextIDsize	Controls Context ID tracing: `0b00` No Context ID tracing. `0b01` Context ID bits[7:0] traced. `0b10` Context ID bits[15:0] traced. `0b11` Context ID bits[31:0] traced. **Note** Only the number of bytes specified is traced even if the new value is larger than this. The reset value is `0b00`.
[13]	Port mode[2]	See the description of bits[17:16] in this table. The reset value is 0.
[12]	Cycle-accurate tracing	Selects cycle-accurate tracing: **1** Include a precise cycle count of executed instructions. This is achieved by adding extra information into the trace, giving cycle counts even when **TraceEnable** is inactive. The reset value is 0.
[11]	ETM port selection	Controls an external output, **ETMEN**: **0** **ETMEN** is LOW. **1** **ETMEN** is HIGH. You can use the **ETMEN** signal to control the routing of trace port signals to shared GPIO pins on your SoC, under the control of logic external to the ETM. Trace software tools must set this bit to 1 to ensure that trace output is enabled from this ETM. The reset value is 0.
[10]	ETM programming	Controls the mode of the ETM: **0** ETM in trace mode. **1** ETM in Programming mode. For more information about the ETM Programming bit and associated state, see the *Embedded Trace Macrocell Architecture Specification*. The reset value is 1.
[9]	Debug request control	Forces the appropriate processor in the Cortex-A7 MPCore device into Debug state: **0** On a trigger event **DBGRQ** is not set. **1** On a trigger event **DBGRQ** is set. When a trigger event occurs the **DBGRQ** output is asserted until the **DBACK** signal is observed. The reset value is 0.

Table 3-8 ETMCR bit assignments (continued)

Bits	Name	Description
[8]	Branch output	Enables the ETM to control the output of all branch addresses, even if the branch results from of a direct branch instruction: **0** Branch addresses not traced. **1** Branch addresses traced. This enables reconstruction of the program flow without having access to the memory image of the code being executed. The reset value is 0.
[7]	Stall processor	Not supported, RAZ/WI.
[6:4]	Port size[2:0]	In conjunction with bit[21] in this table, Specifies the port size. The port size determines how many external pins are available to output the trace information on **ATDATA[63:0]**. The ETM-A7 macrocell supports only the 64-bit port size, corresponding to a Port size[3:0] value of `0b0110`, but you can write other values to these bits, and a read of the register returns the value written. Writing other values to these bits has no effect on the ETM. Bit[10] of the System Configuration Register indicates if these bits are set to select an unsupported port size. See the *Embedded Trace Macrocell Architecture Specification* for more information. The reset value is `0b110`, corresponding to the 64-bit port size.
[3:2]	Data access	Configures the data tracing mode: `0b00` No data tracing. `0b01` Trace only the data portion of the access. `0b10` Trace only the address portion of the access. `0b11` Trace both the address and the data of the access. The reset value is `0b00`.
[1]	MonitorCPRT	Controls whether CPRTs are traced: **0** CPRTs not traced. **1** CPRTs traced. This bit is used with bit[19]. For more information about *Filter Coprocessor Register Transfers* (CPRT) in ETMv3.0 and later. see the *Embedded Trace Macrocell Architecture Specification*. The reset value is 0.
[0]	ETM power down	Enables the ETM power to be controlled externally: **0** ETM tracing is enabled. **1** ETM tracing is disabled. The reset value is 1. This bit must be cleared by the trace software tools at the beginning of a debug session. See *Control of ETM power down* for additional information on controlling ETM power down.

Control of ETM power down

To save power, you can use the **ETMPWRUP** signal, controlled by the ETM power down bit of the ETMCR, to gate the clock to the logic in the ETM interface of the processor. Also, when you set the ETM power down bit to 1, the clock to most of the logic in the ETM is gated, disabling ETM tracing and leaving the ETM block operating in a low-power mode.

Note

You must not use the **ETMEN** signal to gate the ETM clock or any other functionality required for basic operation. You can use the **ETMEN** signal to control functionality that is required only for off-chip tracing, such as multiplexing between two ETMs. Use the **ETMPWRUP** signal to control basic operation of the ETM.

3.5.2 Configuration Code Register

The ETMCCR characteristics are:

Purpose Indicates the configuration of the ETM.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-2 on page 3-9.

If the **MAXEXTOUT[1:0]** and **MAXEXTIN[2:0]** signals are all tied LOW, the ETMCCR has the value `0x8D014024`.

Figure 3-2 shows the ETMCCR bit assignments.

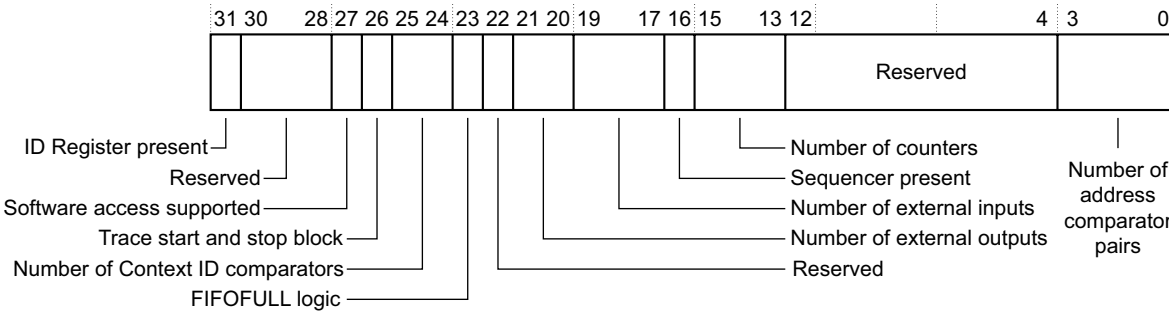


Figure 3-2 ETMCCR bit assignments

Table 3-9 shows the ETMCCR bit assignments.

Table 3-9 ETMCCR bit assignments

Bits	Name	Description
[31]	ID register present	ID Register: **1** Indicates that the ETMIDR, register `0x79`, is present. See *ID Register* on page 3-20 for more information.
[30:28]	-	Reserved, RAZ.
[27]	Software access	Indicates software access support: **1** Supports memory-mapped access to registers.
[26]	Trace start and stop block	Indicates if trace start and stop block is present: **1** Start and stop block is present.
[25:24]	Number of Context ID comparators	Indicates the number of Context ID comparators: `0b01` One Context ID comparator supported.
[23]	FIFOFULL logic	Not supported, RAZ.

Table 3-9 ETMCCR bit assignments (continued)

Bits	Name	Description
[22]	-	Reserved, RAZ.[a]
[21:20]	Number of external outputs	Indicates the number of external outputs that is present at the **MAXEXTOUT[1:0]** inputs: `0b010` Supports a maximum of two external outputs.
[19:17]	Number of external inputs	Indicates the number of external inputs that is present at the **MAXEXTIN[2:0]** inputs: `0b100` Supports a maximum of four external inputs.
[16]	Sequencer	Indicates sequencer support: **1** Supports a sequencer.
[15:13]	Counters	Indicates the number of counters: `0b010` Supports two counters.
[12:8]	Memory map decoders	Not supported, RAZ.
[7:4]	Data comparators	Indicates the number of data comparators: `0x2` Supports two data comparators.
[3:0]	Pairs of address comparators	Indicates the number of pairs of address comparators: `0x4` Supports four pairs of address comparators.

a. The *Embedded Trace Macrocell Architecture Specification* defines this as the most significant bit of the number of external outputs field, see the description of bits[21:20].

3.5.3 ASIC Control Register

The ETMASICCR characteristics are:

Purpose Controls the **ASICCTL[7:0]** signals.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-2 on page 3-9.

Figure 3-3 shows the ETMASICCR bit assignments.

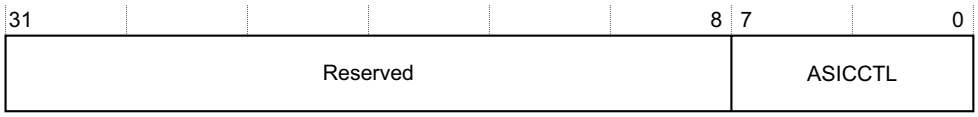


Figure 3-3 ETMASICCR bit assignments

Table 3-10 shows the ETMASICCR bit assignments.

Table 3-10 ETMASICCR bit assignments

Bits	Name	Description
[31:8]	-	Reserved.
[7:0]	ASICCTL	When a bit in this field is set to: **0** The corresponding bit of **ASICCTL[7:0]** is LOW. **1** The corresponding bit of **ASICCTL[7:0]** is HIGH.

3.5.4 ID Register

The ETMIDR characteristics are:

Purpose Identifies the implementation of the ETM.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes This register has the value `0x410CF25x`, where x depends on the release version of the macrocell, see the bits[3:0], Implementation revision field in Table 3-11 for more information.

See the register summary in Table 3-1 on page 3-5 and Table 3-2 on page 3-9.

Figure 3-4 shows the ETMIDR bit assignments.

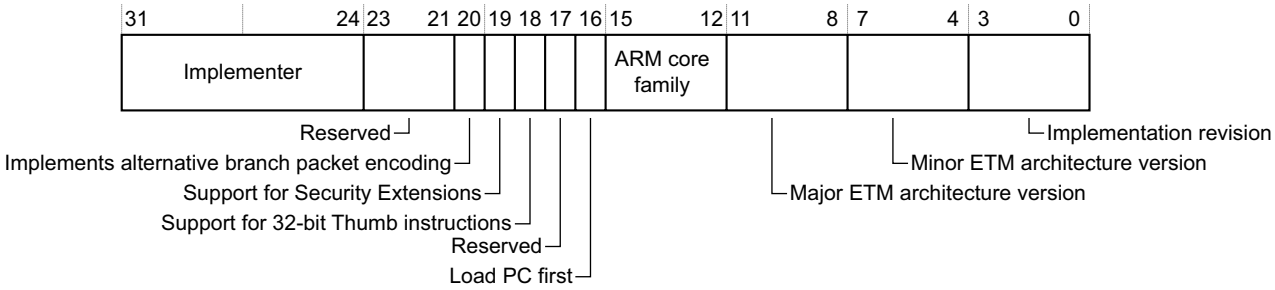


Figure 3-4 ETMIDR bit assignments

Table 3-11 shows the ETMIDR bit assignments.

Table 3-11 ETMIDR bit assignments

Bits	Name	Description
[31:24]	Implementer	Indicates implementer code: `0x41` ARM.
[23:21]	-	Reserved, RAZ.
[20]	Branch packet encoding	Indicates branch packet encoding support: **0** Supports the original branch packet encoding support.
[19]	Security Extensions	Indicates ARM architecture Security Extensions support: **1** Supports Security Extensions architecture.
[18]	32-bit Thumb instructions	Indicates 32-bit Thumb instructions support: **1** Supports 32-bit Thumb instructions.
[17]	-	Reserved, RAZ.
[16]	Load PC first	If an LSM[a] load operation with the PC, indicates where in the list the PC is loaded: **0** PC is not loaded first.
[15:12]	ARM processor family	Indicates what ARM profile the processor belongs to: `0b1111` The processor family is defined elsewhere.

Table 3-11 ETMIDR bit assignments (continued)

Bits	Name	Description
[11:8]	Major version number	Indicates the major version number of the ETM architecture: `0b0010` ETM v3.x.
[7:4]	Minor version number	Indicates the minor version number of the ETM architecture: `0b0101` ETM vx.5.
[3:0]	Implementation revision	Indicates the implementation revision: `0b0000` r0p0 release of the ETM -A7 macrocell.

a. See the *Embedded Trace Macrocell Architecture Specification* for a definition and list of LSM operations.

3.5.5 Configuration Code Extension Register

The ETMCCER characteristics are:

Purpose Indicates the configuration of the extended external input bus.

Usage constraints Read by software only.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-2 on page 3-9.

Figure 3-5 shows the ETMCCER bit assignments.

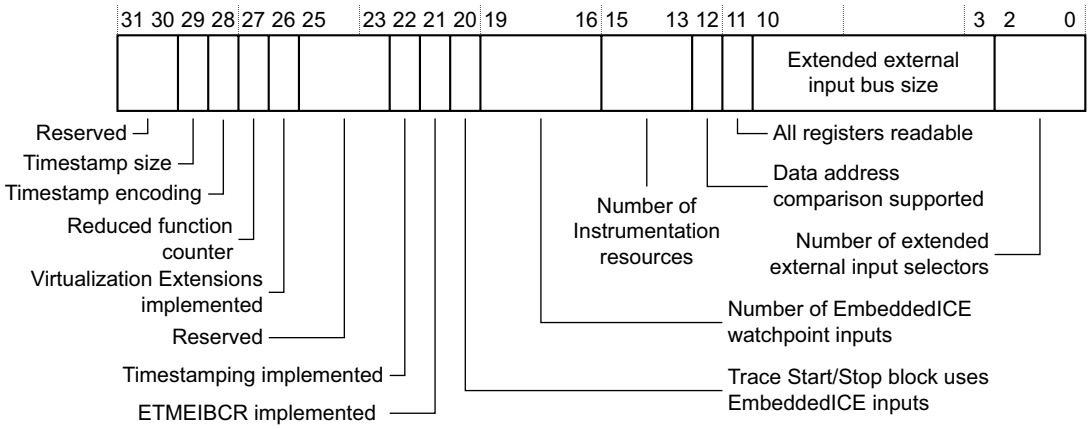


Figure 3-5 ETMCCER bit assignments

Table 3-12 shows the ETMCCER bit assignments.

Table 3-12 ETMCCER bit assignments

Bits	Name	Description
[31:30]	-	Reserved, RAZ.
[29]	Timestamp size	Indicates support for timestamp size: **1** Supports a 64-bit timestamp size.
[28]	Timestamp encoding.	Indicates the type of timestamp encoding support: **1** Supports binary encoded timestamp.

Table 3-12 ETMCCER bit assignments (continued)

Bits	Name	Description
[27]	Counter function	Indicates support for full or reduced counter function: **0** Supports full counter function.
[26]	Virtualization Extensions	Indicates support for Virtualization Extensions: **1** Supports Virtualization Extensions.
[25:23]	-	Reserved, RAZ.
[22]	Timestamping	Indicates support for timestamping support: **1** Supports timestamping and: • the Timestamp Event Register is implemented • bit[28] in the Main Control Register is writable.
[21]	ETMEIBCR implemented	Indicates support for ETMEIBCR: **1** No ETMEIBCR supported.
[20]	Trace start and stop block usage	Indicates if the start and stop block supports EmbeddedICE watchpoint inputs. **0** No EmbeddedICE watchpoint inputs supported.
[19:16]	EmbeddedICE watchpoint inputs	Indicates the number of EmbeddedICE watchpoint inputs supported: `0b0000` No EmbeddedICE watchpoint inputs supported.
[15:13]	Instrumentation resources supported.	Indicates the number of instrumentation resources supported: `0b000` No instrumentation resources supported.
[12]	Data address comparisons	Indicates support for data address comparisons: **0** No data address comparisons are supported.
[11]	All registers are readable.	All registers, except some integration test registers, are readable. See Table 3-7 on page 3-13 for information about accesses to integration test registers[a].
[10:3]	Size of extended external input bus	Indicates the number of PMUEVENT registers available.
[2:0]	Number of extended external input selectors	Indicates the number of extended external input selectors available.

a. Registers with names that start with IT are the Integration Test Registers, for example ITATBCTR1.

3.5.6 Extended External Input Selection Register

The ETMEXTINSELR Register characteristics are:

Purpose Specifies the extended external inputs, see the *Embedded Trace Macrocell Architecture Specification* for more information.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-5 on page 3-11.

Figure 3-6 shows the ETMEXTINSELR bit assignments.

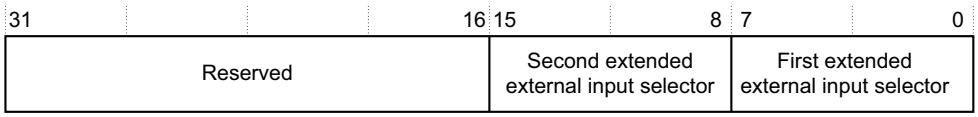


Figure 3-6 ETMEXTINSELR bit assignments

Table 3-13 shows the ETMEXTINSELR bit assignments.

Table 3-13 ETMEXTINSELR bit assignments

Bits	Name	Description	
[31:16]	-	Reserved, SBZP.	
[15:8]	Second extended external input selector	**bits[15:13]** **bits[12:8]**	Reserved, SBZP. Selection value for second external input.
[7:0]	First extended external input selector	**bits[7:5]** **bits[4:0]**	Reserved, SBZP. Selection value for first external input.

3.5.7 Power-Down Control Register

The ETMPDCR characteristics are:

Purpose Indicates when the ETM is used on different domains, the status of the trace registers domain must be on.

Usage constraints Default ETM single domain.

Configurations This register is only useful when the ETM is used in multiple domain.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-3 on page 3-10.

Figure 3-7 shows the ETMPDCR bit assignments.

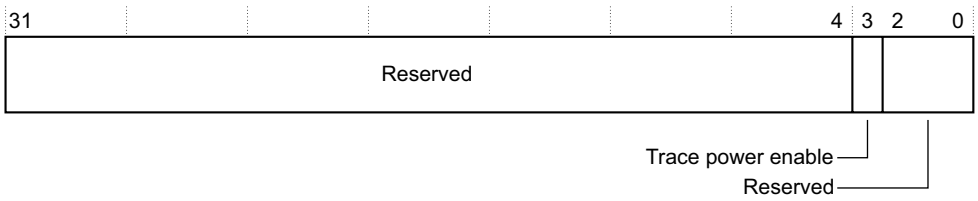


Figure 3-7 ETMPDCR bit assignments

Table 3-14 shows the ETMPDCR bit assignments.

Table 3-14 ETMPDCR bit assignments

Bits	Name	Description
[31:4]	-	Reserved, RAZ.
[3]	Trace power enable	When HIGH, power to the power domain containing the trace registers must be provided.
[2:0]	-	Reserved, RAZ.

Note

The trace registers power domain is always on because it is in a single domain by default.

3.5.8 Power-Down Status Register

The ETMPDSR characteristics are:

Purpose Indicates the power-down status of the ETM.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-2 on page 3-9.

Figure 3-8 shows the ETMPDSR bit assignments.

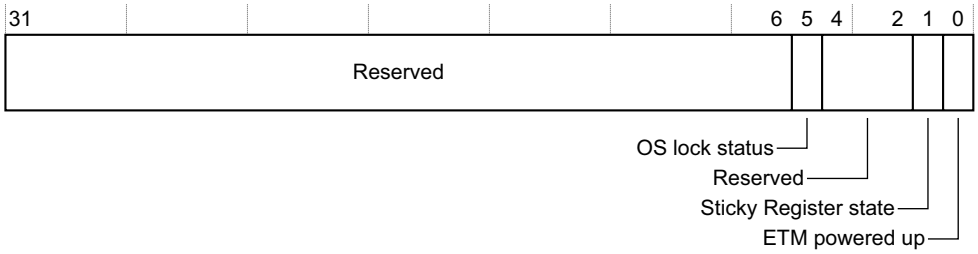


Figure 3-8 ETMPDSR bit assignments

Table 3-15 shows the ETMPDSR bit assignments.

Table 3-15 ETMPDSR bit assignments

Bits	Name	Description	
[31:6]	-	Reserved, RAZ.	
[5]	OS lock status	The value of this bit is the same as the value of bit[1] of the ETMOSLSR. This bit is UNKNOWN when the ETM is powered down.	
[4:2]	-	Reserved, RAZ.	
[1]	Sticky Register state[a]	**0**	Indicates that this register has been read after a reset.
		1	Indicates that this register has never been read after a reset.
[0]	ETM powered up[a]	The ETM registers are always accessible, RAO.	

a. The ETM-A7 macrocell does not support multiple power domains.

3.5.9 Auxiliary Control Register

The ETMAUXCR characteristics are:

Purpose Provides additional implementation-defined ETM controls.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-2 on page 3-9.

Figure 3-9 shows the ETMAUXCR bit assignments.

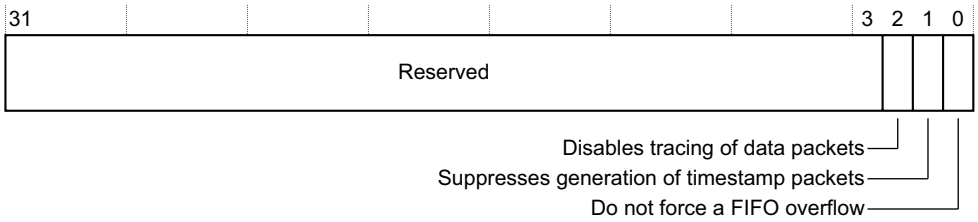


Figure 3-9 ETMAUXCR bit assignments

Table 3-16 shows the ETMAUXCR bit assignments.

Table 3-16 ETMAUXCR bit assignments

Bits	Name	Description
[31:3]	-	Reserved, RAZ.
[2]	Disables tracing of data packets	Specifies whether the ETM disables tracing of data packets from VFP or Advanced SIMD load or store instructions. **0** Not disabled. This is the reset value. **1** Disabled. This only suppresses the data packets. Comparators and other resources can still match on the data from these instructions
[1]	Suppresses generation of timestamp packets	Specifies whether the ETM suppresses generation of timestamp packets as the result of executing an `ISB` instruction: **0** Not suppressed. This is the reset value. **1** Suppressed.
[0]	Do not force FIFO overflow	Specifies whether a force FIFO overflow is sent if a periodic synchronization has not been output for two full synchronization periods **0** Force FIFO overflow . This is the reset value. **1** Do not force FIFO overflow

3.5.10 ETM ID Register 2

The ETMIDR2 characteristics are:

Purpose Provides an extension to the ETM ID register, ETMIDR.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-2 on page 3-9.

Figure 3-10 shows the ETMIDR2 bit assignments.

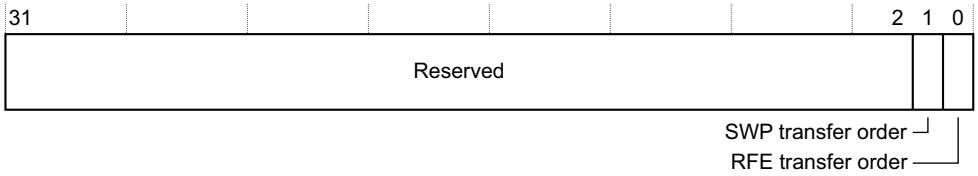


Figure 3-10 ETMIDR2 bit assignments

Table 3-17 shows the ETMIDR2 bit assignments.

Table 3-17 ETMIDR2 bit assignments

Bits	Name	Description
[31:2]	-	Reserved, RAZ.
[1]	SWP transfer order	Indicates the order of transfers for a `SWP` or `SWPB` instruction: **0** The Load transfer is traced before the Store transfer.
[0]	RFE transfer order	Indicates the order of transfers for the `RFE` instruction: **0** The PC transfer is traced before the CPSR transfer.

3.5.11 Peripheral identification registers

The ETMPIDR0-ETMPIDR7 characteristics are:

Purpose Provides the standard Peripheral ID required by all CoreSight components, see the *Embedded Trace Macrocell Architecture Specification* for more information.

Usage constraints Only bits[7:0] of each register are used. This means that ETMPIDR0-ETMPIDR7 define a single 64-bit *Peripheral ID*, as Figure 3-11 shows.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-6 on page 3-13.

Figure 3-11 shows the mapping between ETMPIDR0-ETMPIDR7 and the single 64-bit *Peripheral ID* value,

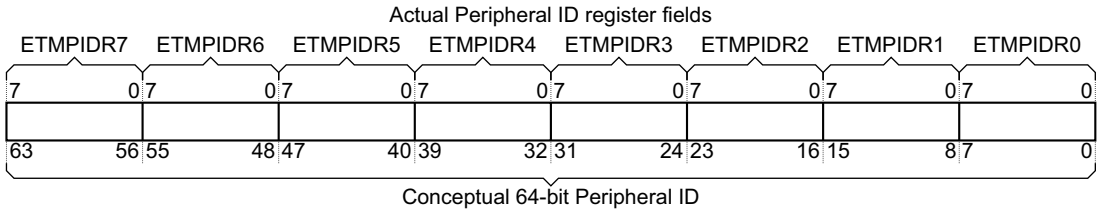


Figure 3-11 Mapping between ETMPIDR0-ETMPIDR7 and the Peripheral ID value

Figure 3-12 on page 3-27 shows the Peripheral ID bit assignments in the single conceptual Peripheral ID register.

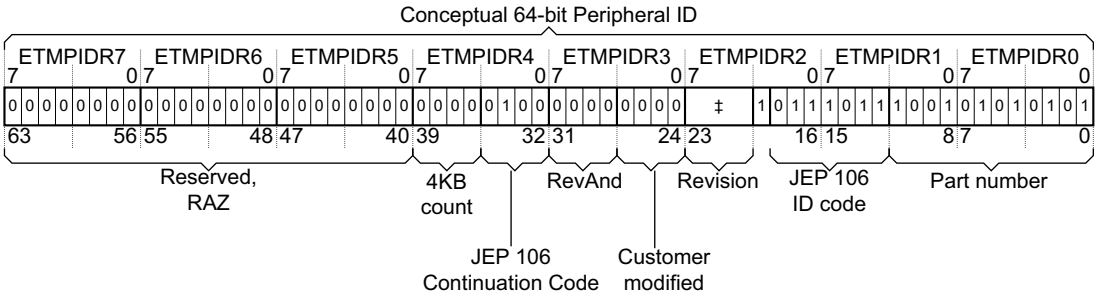


Figure 3-12 Peripheral ID fields

Table 3-18 shows the values of the fields when reading this set of registers. The *Embedded Trace Macrocell Architecture Specification* gives more information about many of these fields.

Table 3-18 ETMPIDR0-ETMPIDR7 bit assignments

Register	Register number	Register offset	Bits	Value	Description
ETMPIDR7	0x3F7	0xFDC	[31:8]	-	Reserved.
			[7:0]	0x00	Reserved.
ETMPIDR6	0x3F6	0xFD8	[31:8]	-	Reserved.
			[7:0]	0x00	Reserved.
ETMPIDR5	0x3F5	0xFD4	[31:8]	-	Reserved.
			[7:0]	0x00	Reserved.
ETMPIDR4	0x3F4	0xFD0	[31:8]	-	Reserved.
			[7:4]	0x0	n, where 2^n is number of 4KB blocks used.
			[3:0]	0x4	JEP 106 continuation code.
ETMPIDR3	0x3FB	0xFEC	[31:8]	-	Reserved.
			[7:4]	0x0	RevAnd (at top level). Manufacturer revision number.
			[3:0]	0x0	Customer Modified. 0x0 indicates ARM is the customer.
ETMPIDR2	0x3FA	0xFE8	[31:8]	-	Reserved.
			[7:4]	a	Revision number of the peripheral. This value is the same as the Implementation revision field of the ETMIDR, see *ID Register* on page 3-20.
			[3]	1	Always 1. Indicates that a JEDEC assigned value is used.
			[2:0]	0b011	JEP 106 identity code[6:4].

Table 3-18 ETMPIDR0-ETMPIDR7 bit assignments (continued)

Register	Register number	Register offset	Bits	Value	Description
ETMPIDR1	0x3F9	0xFE4	[31:8]	-	Reserved.
			[7:4]	0xB	JEP 106 identity code[3:0]
			[3:0]	0x9	Part Number[11:8]. Upper *Binary Coded Decimal* (BCD) value of Device Number.
ETMPIDR0	0x3F8	0xFE0	[31:8]	-	Reserved.
			[7:0]	0x56	Part Number[7:0]. Middle and Lower BCD value of Device Number.

a. See the Description column for details.

Note

In Table 3-18 on page 3-27, the *Peripheral identification registers* on page 3-26 are listed in order of register name, from most significant (ETMPIDR7) to least significant (ETMPIDR0). This does not match the order of the register offsets. Similarly, in Table 3-19 on page 3-29 the *Component identification registers* are listed in order of register name, from most significant (ETMCIDR3) to least significant (ETMCIDR0).

3.5.12 Component identification registers

The ETMCIDR0-ETMCIDR3 characteristics are:

Purpose Identifies the ETM as a CoreSight component. For more information, see the *Embedded Trace Macrocell Architecture Specification*.

Usage constraints Only bits[7:0] of each register are used. This means that ETMCIDR0-ETMCIDR3 define a single 32-bit Component ID, as Figure 3-13 shows.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-6 on page 3-13.

Figure 3-13 shows the mapping between ETMCIDR0-ETMCIDR3 and the single 32-bit *Component ID* value.

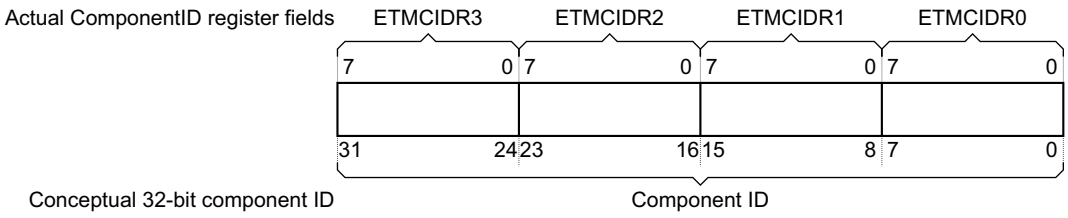


Figure 3-13 Mapping between ETMCIDR0-ETMCIDR3 and the Component ID value

Table 3-19 shows the Component ID bit assignments in the single conceptual Component ID register.

Table 3-19 ETMCIDR0-ETMCIDR3, bit assignments

Register	Register number	Register offset	Bits	Value	Description
ETMCIDR3	0x3FF	0xFFC	[31:8]	-	Unused, read UNDEFINED.
			[7:0]	0xB1	Component identifier, bits[31:24].
ETMCIDR2	0x3FE	0xFF8	[31:8]	-	Unused, read UNDEFINED.
			[7:0]	0x05	Component identifier, bits[23:16].
ETMCIDR1	0x3FD	0xFF4	[31:8]	-	Unused, read UNDEFINED.
			[7:4]	0x9	Component class, component identifier, bits[15:12].
			[3:0]	0x0	Component identifier, bits[11:8].
ETMCIDR0	0x3FC	0xFF0	[31:8]	-	Unused, read UNDEFINED.
			[7:0]	0x0D	Component identifier, bits[7:0].

3.5.13 Integration test registers

The following subsections describe the integration test registers. To access these registers, set bit[0] of the *Integration Mode Control Register* (ETMITCTRL) to 1.

- You can use the write-only integration test registers to set the outputs of some of the ETM signals. Table 3-20 shows the signals that can be controlled in this way.
- You can use the read-only integration test registers to read the state of some of the ETM input signals. Table 3-21 on page 3-30 shows the signals that can be read in this way.

See the *Embedded Trace Macrocell Architecture Specification* for more information on ETMITCTRL.

Table 3-20 Output signals that the Integration Test Registers can control

Signal	Register	Bits	Register description
AFREADY	ITATBCTR0	[1]	See *Integration Test ATB Control Register 0* on page 3-37
ATBYTES[2:0]	ITATBCTR0	[11:9]	See *Integration Test ATB Control Register 0* on page 3-37
ATDATA[63, 55, 47, 39 31, 23, 15, 7, 0]	ITATBDATA0	[8:0]	See *Integration Test ATB Data 0 Register* on page 3-34
ATID[6:0]	ITATBCTR1	[6:0]	See *Integration Test ATB Control Register 1* on page 3-36
ATVALID	ITATBCTR0	[0]	See *Integration Test ATB Control Register 0* on page 3-37
ETMDBGRQ	ITMISCOUT	[4]	See *Integration Test Miscellaneous Outputs register* on page 3-31
ETMSTANDBYWFX	ITMISCOUT	[5]	See *Integration Test Miscellaneous Outputs register* on page 3-31

Table 3-20 Output signals that the Integration Test Registers can control (continued)

Signal	Register	Bits	Register description
EXTOUT[1:0]	ITMISCOUT	[9:8]	See *Integration Test Miscellaneous Outputs register* on page 3-31
SYNCREQ	ITATBCTR2	[2]	See *Integration Test ATB Control Register 2* on page 3-35
TRIGGER	ITTRIGGERREQ	[0]	See *Integration Test Trigger Request Register* on page 3-33

Table 3-21 Input signals that the Integration Test Registers can read

Signal	Register	Bits	Register description
AFVALID	ITATBCTR2	[1]	See *Integration Test ATB Control Register 2* on page 3-35
ATREADY	ITATBCTR2	[0]	See *Integration Test ATB Control Register 2* on page 3-35
DBGACK	ITMISCIN	[4]	See *Integration Test Miscellaneous Input Register* on page 3-32
ETMWFXPENDING	ITMISCIN	[5]	See *Integration Test Miscellaneous Input Register* on page 3-32
EXTIN[3:0]	ITMISCIN	[3:0]	See *Integration Test Miscellaneous Input Register* on page 3-32

Using the integration test registers

Use the integration test registers to check integration. For example:

When bit[0] of ETMITCTRL is set to 1:

- Values written to the write-only integration test registers map onto the specified outputs of the macrocell. For example, writing `0x3` to ITMISCOUT[9:8] causes **EXTOUT[1:0]** to take the value `0x3`.
- Values read from the read-only integration test registers correspond to the values of the specified inputs of the macrocell. For example, if you read ITMISCIN[3:0] you obtain the value of **EXTIN[3:0]**.

When bit[0] of ETMITCTRL is set to 0:

- Reading an integration test register returns an UNPREDICTABLE value.
- The effect of attempting to write to an integration test register, other than the read-only Integration Test Registers, is UNPREDICTABLE.

Note

You must not attempt to write to an integration test register unless you have set bit[0] of ETMITCTRL to 1.

See the *Embedded Trace Macrocell Architecture Specification* for details of ETMITCTRL.

Integration Test Miscellaneous Outputs register

The ITMISCOUT register characteristics are:

Purpose Sets the state of the output pins shown in Table 3-22.

Usage constraints
- Available when bit[0] of ETMITCTRL is set to 1.
- The value of the register sets the signals on the output pins when the register is written.

Configurations Available in all configurations.

Attributes See the register summaries in Table 3-1 on page 3-5, Table 3-7 on page 3-13, and Table 3-21 on page 3-30.

Figure 3-14 shows the ITMISCOUT bit assignments.

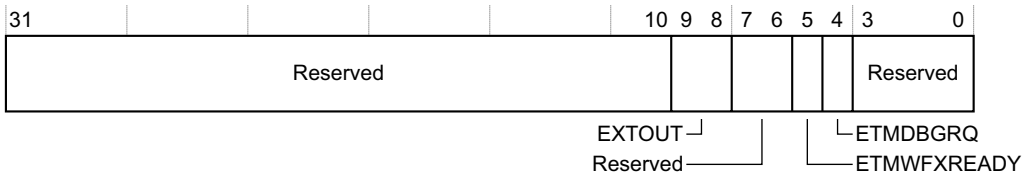


Figure 3-14 ITMISCOUT bit assignments

Table 3-22 shows the ITMISCOUT bit assignments.

Table 3-22 ITMISCOUT bit assignments

Bits	Name	Description
[31:10]	-	Reserved. Write as zero.
[9:8]	EXTOUT	Drives the **EXTOUT[1:0]** output pins[a].
[7:6]	-	Reserved. Write as zero.
[5]	ETMWFXREADY	Drives the **nETMWFXREADY** output pin[a].
[4]	ETMDBGRQ	Drives the **ETMDBGRQ** output pin[a].
[3:0]	-	Reserved. Write as zero.

a. When a bit is set to 0, the corresponding output pin is LOW.
When a bit is set to 1, the corresponding output pin is HIGH.
The ITMISCOUT bit values correspond to the physical state of the output pins.

Integration Test Miscellaneous Input Register

The ITMISCIN Register characteristics are:

Purpose Reads the state of the input pins shown in Table 3-23.

Usage constraints
- Available when bit[0] of ETMITCTRL is set to 1.
- The values of the register bits depend on the signals on the input pins when the register is read.

Configurations Available in all configurations.

Attributes See the register summaries in Table 3-1 on page 3-5, Table 3-7 on page 3-13, and Table 3-21 on page 3-30.

Figure 3-15 shows the ITMISCIN bit assignments.

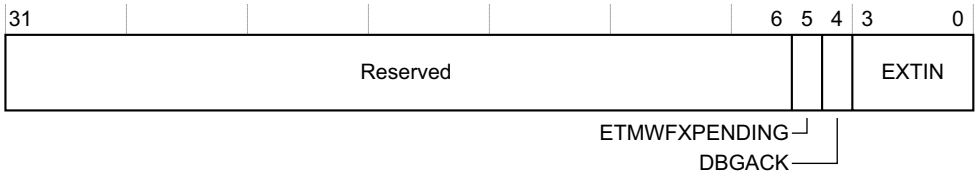


Figure 3-15 ITMISCIN bit assignments

Table 3-23 shows the ITMISCIN bit assignments.

Table 3-23 ITMISCIN bit assignments

Bits	Name	Description
[31:6]	-	Reserved. Read UNDEFINED.
[5]	ETMWFXPENDING	Returns the value of the **ETMWFXPENDING** input pin[a].
[4]	DBGACK	Returns the value of the **DBGACK** input pin[a].
[3:0]	EXTIN	Returns the value of the **EXTIN[3:0]** input pins[a].

a. When a bit is set to 0, the corresponding input pin is LOW.
When a bit is set to 1, the corresponding input pin is HIGH.
The ITMISCIN bit values always correspond to the physical state of the input pins.

Integration Test Trigger Request Register

The ITTRIGGERREQ Register characteristics are:

Purpose Sets the **TRIGGER** output pin shown in Table 3-24.

Usage constraints
- Available when bit[0] of ETMITCTRL is set to 1.
- The values of the register bits set the signals on the output pin when the register is written.

Configurations Available in all configurations.

Attributes See the register summaries in Table 3-1 on page 3-5, Table 3-7 on page 3-13, and Table 3-21 on page 3-30.

Figure 3-16 shows the ITTRIGGERREQ bit assignments.

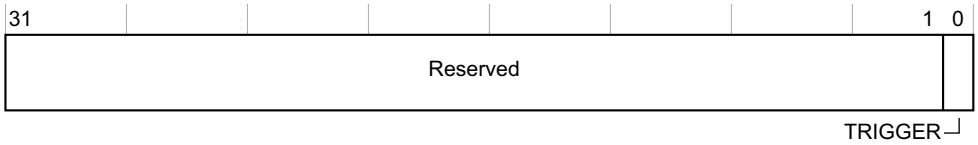


Figure 3-16 ITTRIGGERREQ bit assignments

Table 3-24 shows the ITTRIGGERREQ bit assignments.

Table 3-24 ITTRIGGERREQ bit assignments

Bits	Name	Description
[31:1]	-	Reserved. Write as zero.
[0]	TRIGGER	Drives the **TRIGGER** output pin[a].

a. When a bit is set to 0, the corresponding output pin is LOW. When a bit is set to 1, the corresponding output pin is HIGH. The ITTRIGGERREQ bit values always correspond to the physical state of the output pins.

Integration Test ATB Data 0 Register

The ITATBDATA0 Register characteristics are:

Purpose Sets the state of the ATDATA output pins shown in Table 3-25.

Usage constraints
- Available when bit[0] of ETMITCTRL is set to 1.
- The values of the register bits set the signals on the output pins when the register is written.

Configurations Available in all configurations.

Attributes See the register summaries in Table 3-1 on page 3-5, Table 3-7 on page 3-13, and Table 3-21 on page 3-30.

Figure 3-17 shows the ITATBDATA0 bit assignments.

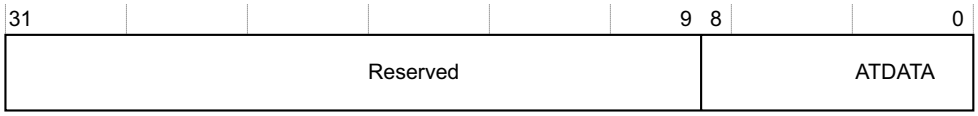


Figure 3-17 ITATBDATA0 bit assignments

Table 3-25 shows the ITATBDATA0 bit assignments.

Table 3-25 ITATBDATA0 bit assignments

Bits	Name	Description
[31:9]	-	Reserved. Write as zero.
[8:0]	ATDATA	Drives the **ATDATA[63, 55, 47, 39, 31, 23, 15, 7, 0]** output pins[a].

a. When a bit is set to 0, the corresponding output pin is LOW.
When a bit is set to 1, the corresponding output pin is HIGH.
The ITATBDATA0 bit values always correspond to the physical state of the output pins.

Integration Test ATB Control Register 2

The ITATBCTR2 characteristics are:

Purpose Reads the state of the **AFVALID**, **ATREADY**, and **SYNCREQ** input pins from the ATB bus, as shown in Table 3-26.

Usage constraints
- Available when bit[0] of ETMITCTRL is set to 1.
- The values of the register bits depend on the signals on the input pins when the register is read.

Configurations Available in all configurations.

Attributes See the register summaries in Table 3-1 on page 3-5, Table 3-7 on page 3-13, and Table 3-21 on page 3-30.

Figure 3-18 shows the ITATBCTR2 bit assignments.

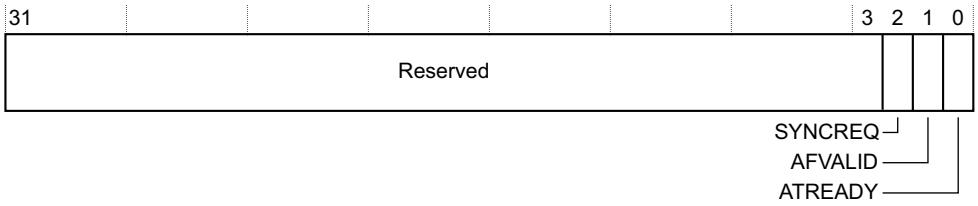


Figure 3-18 ITATBCTR2 bit assignments

Table 3-26 shows the ITATBCTR2 bit assignments.

Table 3-26 ITATBCTR2 bit assignments

Bits	Name	Description
[31:3]	-	Reserved. Read UNDEFINED.
[2]	SYNCREQ	Returns the value of the **SYNCREQ** input pin.
[1]	AFVALID	Returns the value of the **AFVALID** input pin[a].
[0]	ATREADY	Returns the value of the **ATREADY** input pin[a].

a. When a bit is set to 0, the corresponding input pin is LOW.
When a bit is set to 1, the corresponding input pin is HIGH.
The ITATBCTR2 bit values always correspond to the physical state of the input pins.

Integration Test ATB Control Register 1

The ITATBCTR1 characteristics are:

Purpose Sets the state of the **ATID** output pins shown in Table 3-27.

Usage constraints
- Available when bit[0] of ETMITCTRL is set to 1.
- The values of the register bits set the signals on the output pins when the register is written.

Configurations Available in all configurations.

Attributes See the register summaries in Table 3-1 on page 3-5, Table 3-7 on page 3-13, and Table 3-21 on page 3-30.

Figure 3-19 shows the ITATBCTR1 bit assignments.

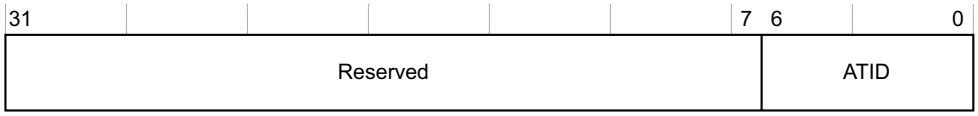


Figure 3-19 ITATBCTR1 bit assignments

Table 3-27 shows the ITATBCTR1 bit assignments.

Table 3-27 ITATBCTR1 bit assignments

Bits	Name	Description
[31:7]	-	Reserved. Write as zero.
[6:0]	ATID	Drives the **ATID[6:0]** output pins[a].

a. When a bit is set to 0, the corresponding output pin is LOW. When a bit is set to 1, the corresponding output pin is HIGH. The ITATBCTR1 bit values always correspond to the physical state of the output pins.

Integration Test ATB Control Register 0

The ITATBCTR0 characteristics are:

Purpose Sets the state of the output pins shown in Table 3-28.

Usage constraints
- Available when bit[0] of ETMITCTRL is set to 1.
- The values of the register bits set the signals on the output pins when the register is written.

Configurations Available in all configurations.

Attributes See the register summaries in Table 3-1 on page 3-5, Table 3-7 on page 3-13, and Table 3-21 on page 3-30.

Figure 3-20 shows the ITATBCTR0 bit assignments.

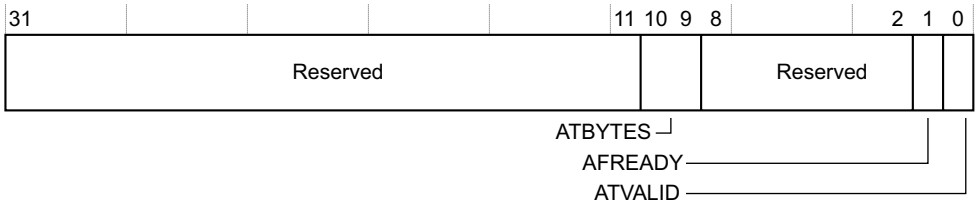


Figure 3-20 ITATBCTR0 bit assignments

Table 3-28 shows the ITATBCTR0 bit assignments.

Table 3-28 ITATBCTR0 bit assignments

Bits	Name	Description
[31:12]	-	Reserved. Write as zero.
[11:9]	ATBYTES	Drives the **ATBYTES[2:0]** output pins[a].
[8:2]	-	Reserved. Write as zero.
[1]	AFREADY	Drives the **AFREADY** output pin[a].
[0]	ATVALID	Drives the **ATVALID** output pin[a].

a. When a bit is set to 0, the corresponding output pin is LOW. When a bit is set to 1, the corresponding output pin is HIGH. The ITATBCTR0 bit values always correspond to the physical state of the output pins.

Appendix A
Signal Descriptions

This appendix describes the signals used in the macrocell. It contains the following section:

- *Signal descriptions* on page A-2.

A.1 Signal descriptions

Table A-1 shows the ETM-A7 macrocell signals in alphabetical order.

Table A-1 ETM-A7 signals

Signal	Type	Description
AFREADY	Output	ATB interface FIFO flush finished.
AFVALID	Input	ATB interface FIFO flush request.
ASICCTL[7:0]	Output	Contents of ASICCTL Register.
ATBYTES[2:0]	Output	Size of **ATDATA**.
ATCLKEN	Input	Clock enable for ATB interface.
ATDATA[63:0]	Output	ATB interface data.
ATID[6:0]	Output	ATB interface trace source ID.
ATREADY	Input	**ATDATA** can be accepted.
ATVALID	Output	ATB interface data valid.
CLK	Input	ETM clock. Same as Cortex-A7 MPCore processor clock.
CLKCHANGE	Input	Clock change indicator input. It is used when either the processor clock period or timestamp period changes.
CORESELECT[2:0]	Output	ETMA7 does not support multiple processor sharing the same ETM.
DBGACK	Input	Indicates that the processor is in debug state. This signal is connected to the processor general purpose **DBGACK** output, so that it can be used to determine when **ETMDBGRQ** can be deasserted. It is also used for other purposes in the ETM, and care must be taken to ensure the timing of this signal is appropriate because it does not come through the main interface between the processor and the ETM.
DBGEN	Input	Invasive debug enable. When HIGH, indicates that invasive debug is enabled.
DFTRSTDISABLE	Input	Reset synchronization bypass DFT signal.
DFTSE	Input	Scan enable DFT signal.
ETMCID[31:0]	Input	Current value of the processor Context ID Register.
ETMDA[31:0]	Input	Address for data transfer.
ETMDBGRQ	Output	Request from the macrocell for the processor to enter debug state. This must be ORed with any ASIC-level **DBGRQ** signals before being connected to the processor **EDBGRQ** input.
ETMDCTL[10:0]	Input	Data control signals.
ETMDD[63:0]	Input	Contains the data value for load, store, or coprocessor instructions.
ETMEN	Output	Enable signal for trace output from the ETM, driven by bit[11] of the ETMCR.
ETMIA[31:1]	Input	Address for executed instruction.
ETMICTL[20:0]	Input	Instruction control signals.

Table A-1 ETM-A7 signals (continued)

Signal	Type	Description
ETMPWRUP	Output	When HIGH, indicates that the macrocell is in use. When LOW: • external logic supporting the macrocell can be clock-gated to conserve power • the Cortex-A7 MPCore processor disables the interface • logic within the macrocell is clock-gated to conserve power.
ETMPWRUPREQ	Output	This signal is not used in the ETM-A7 macrocell because it is in a single power domain shared with the rest of the CoreSight debug system.
ETMSTANDBYWFX	Output	Indicates that the macrocell FIFO is empty and that the Cortex-A7 MPCore processor can be put in Standby mode.
ETMVMID[7:0]	Input	Current value of the processor VMID.
ETMWFXPENDING	Input	Indicates that the Cortex-A7 MPCore processor is about to go into Standby mode, and that the ETM must drain its FIFO.
EXTIN[3:0]	Input	External input resources.
EXTOUT[1:0]	Output	External outputs.
FIFOPEEK[7:0]	Output	For validation purposes only. Indicates when various events occur before being written to the FIFO.
MAXCORES[2:0]	Input	Number of processors the ETM can trace when in share mode. Ignored for ETMA7 since share mode not supported.
MAXEXTIN[2:0]	Input	Number of external inputs the ASIC supports, maximum four. These signals determine the value bits[19:17] in the ETMCCR, see *Configuration Code Register* on page 3-18.
MAXEXTOUT[1:0]	Input	Number of external outputs the ASIC supports, maximum two. These signals determine the value bits[22:20] in the ETMCCR, see *Configuration Code Register* on page 3-18.
NIDEN	Input	Non-invasive debug enable. When HIGH, indicates that non-invasive debug is enabled.
nSYSPORESET	Input	Power-on reset. This is the main reset.
PADDRDBG[11:2]	Input	Debug APB address bus.
PADDRDBG31	Input	Indicates an external debug request from the *Debug Access Por*t (DAP): • **PADDRDBG31** at logic 1 indicates an access from hardware (JTAG) • **PADDRDBG31** at logic 0 indicates an access from software.
PCLKENDBG	Input	Debug APB clock enable.
PENABLEDBG	Input	The Debug APB interface is enabled for a transfer.
PMUEVENT[29:0]	Input	Gives the status of the performance monitoring events. Used as extended external inputs.
PRDATADBG[31:0]	Output	Debug APB read data.
PREADYDBG	Output	Used to extend Debug APB transfers.
PSELDBG	Input	Debug APB slave select signal.

Table A-1 ETM-A7 signals (continued)

Signal	Type	Description
PSLVERRDBG	Output	Debug APB slave error.
PWDATADBG[31:0]	Input	Debug APB write data.
PWRITEDBG	Input	Debug APB transfer direction: **0** Read. **1** Write.
SYNCREQ	Input	Request for periodic synchronization.
TRIGGER	Output	Trigger request status signal. Asserted for one clock cycle when a trigger occurs.
TSVALUEB[63:0]	Input	Timestamp value input bus.

Appendix B
Revisions

This appendix describes the technical changes between released issues of this book.

Table B-1 Issue A

Change	Location	Affects
No changes, first release	-	-