IMDB: A Low-Cost In-Module Disturbance Barrier for Mitigating Write Disturbance Errors in Phase-Change Memory

Hyokeun Lee[1], Seungyong Lee[1], Moonsoo Kim[1], Hyun Kim[2], and Hyuk-Jae Lee[1]

[1]Seoul National University, Seoul, Republic of Korea

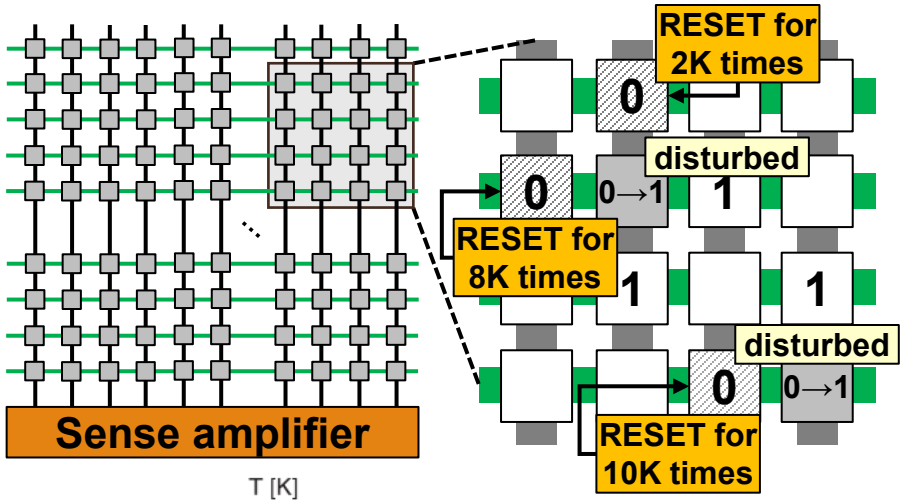
[2]Seoul National University of Science and Technology, Seoul, Republic of Korea

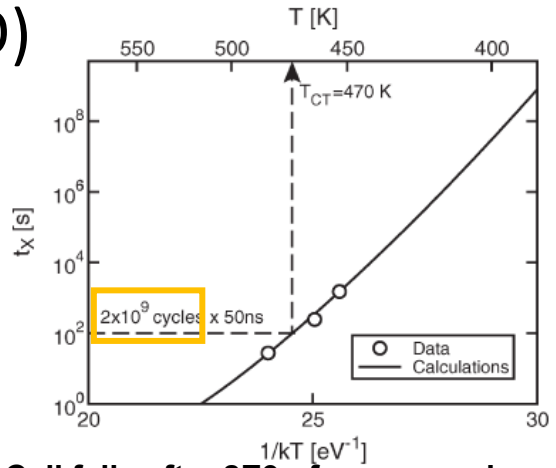
About the presenter

- Pursuing MSc and PhD in Dept. of ECE, Seoul National University, Seoul, Republic of Korea (2016-)
- Computer Architecture and Parallel Processing Lab.
- Area of Interests
  - Computer architecture
  - Memory controller design
  - Reliability issues on phase-change memories
- Contacts: harrylee365@gmail.com/hklee@capp.snu.ac.kr

Problem: Write Disturbance Error (WDE) in Phase-change memory (PCM)

- About PCM: Identify RESET and SET with the **resistance** of cell phase (amorphous & crystalline)
- Cells are crystallized under **high temperature** environment for **a long time**
  - Cells on idle amorphous state are vulnerable!
  - Appears as 0→1 flip-errors logically
- Acute phenomenon (X), **Chronic phenomenon** (O)
  - WDE is NOT a RANDOM problem
  - WDE occurs with **gradual crystallization**
  - Russo et al. declare WDE occurs under **a number of RESETs** →called "WDE limitation number"
- Manufacturers specify **that number** as 10K in recent works→ Guarantee no WDE before 10K of RESET on neighbors!





Cell fails after 2E9 of programming under 470K

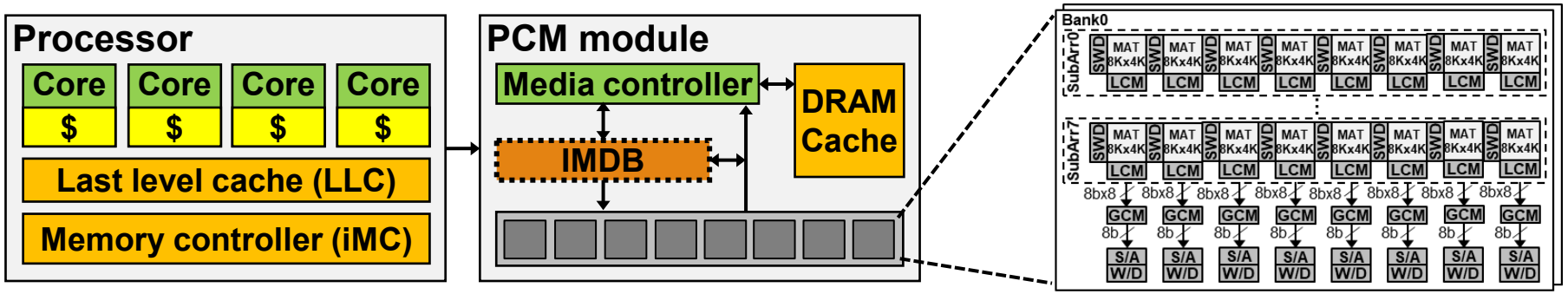
Motivations

- Treats WDE as “encoding” problem
  - Converts WDE-vulnerable pattern → **“less” vulnerable** patterns
  - WDE rate variates with workloads + relying on ECC
- Requires significant overhead when “deferring” correction
  - **Extra device** to temporally “record” error position
  - Relying on a high-overhead **verify-n-correction (VnC)**
- Extra supercapacitors are required to flush volatile data if “write cache” is adopted
- **Knowledge of WDE limitation number is NOT leveraged yet**

Idea of In-Module Disturbance Barrier (IMDB)

- Rewrite vulnerable data "**on-demand**"
- Record the number of **1-to-0 flips in a data word**
  - Data are NOT recorded basically → NO burden on supercapacitors
  - Need counter on each address? → Hold WDE-vulnerable addresses in a table
- No modifications on the processor: modification only **in PCM module**

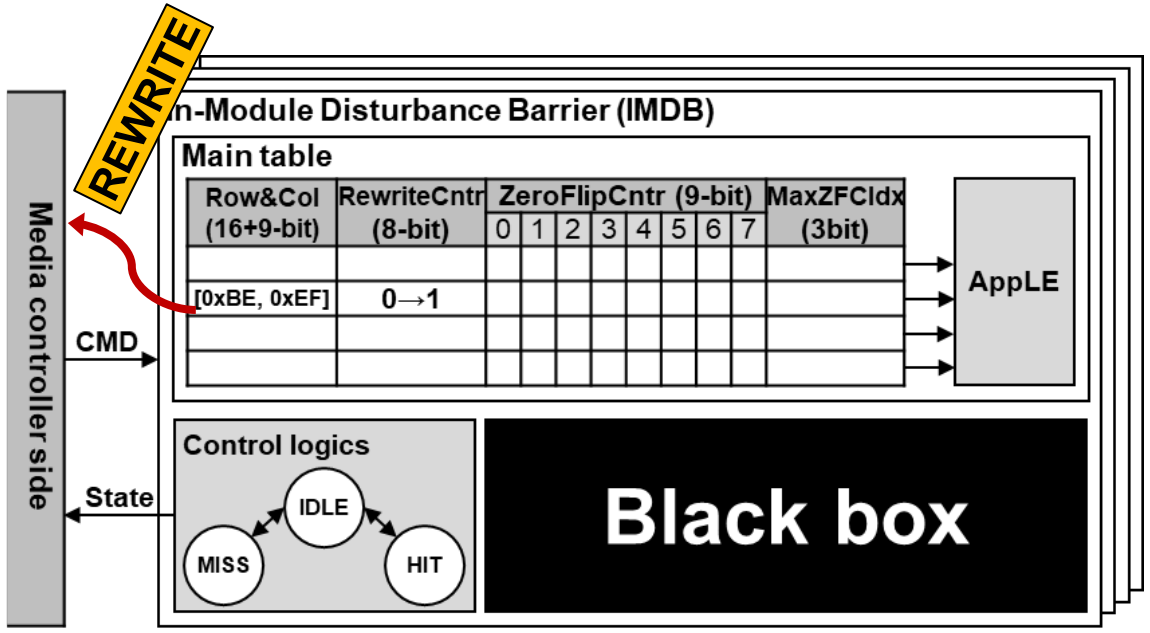
  → Desirable solution to both vendors of processor & memory



System layout in this paper. Proposed module is added to the PCM module

Deeper view of IMDB

- Main table: **SRAM-based table** hold WDE-vulnerable addresses
  - **ZeroFlipCntr:** Counts the number of 1→0 flips in a WRITE CMD data
  - Generate REWRITE CMD before ZeroFlipCntr reaches **threshold**
  - threshold=WDE limitation #/2 (two wordlines disturbs a cell)
- **"Sparsely"** gets WRITE CMD
  - Newly insert WRITE CMD with the probability of 1/64
- 512 entries assumed in the paper

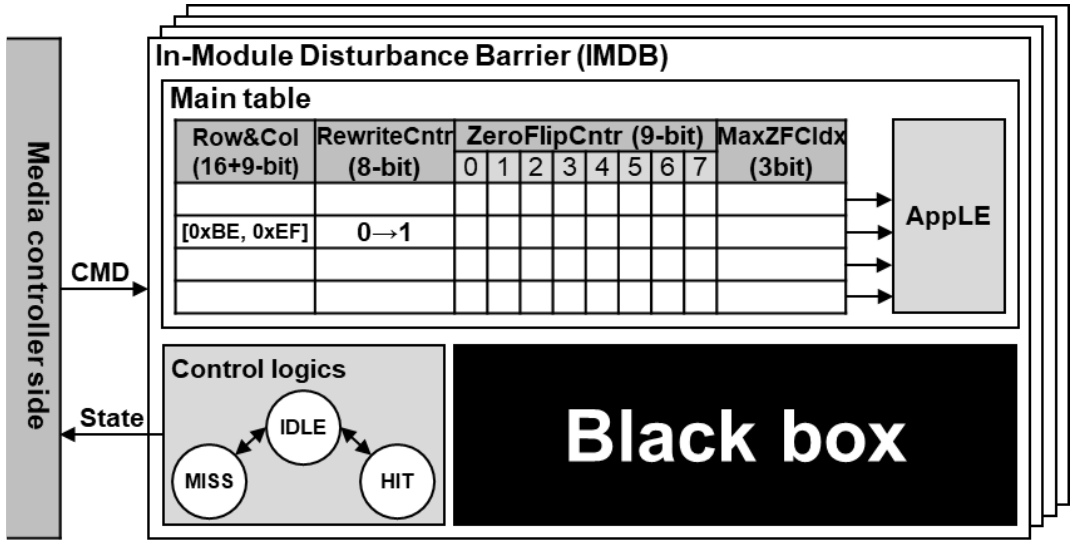


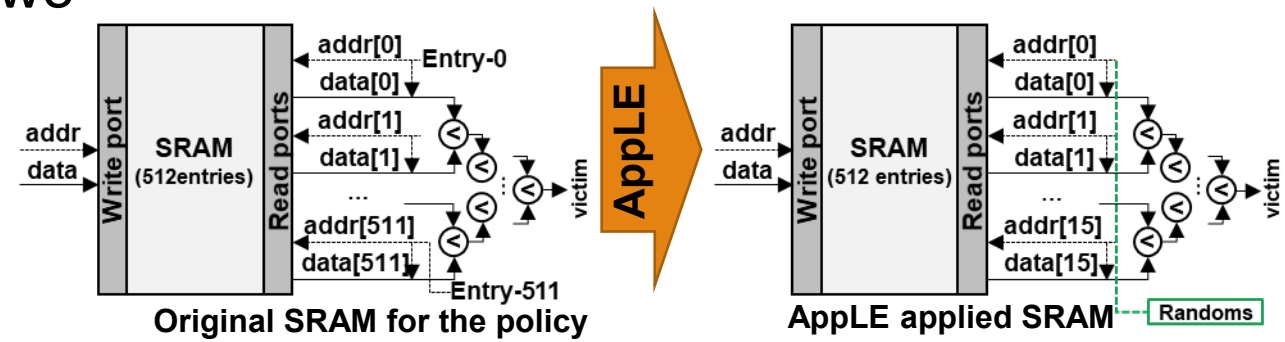
Main table of IMDB

Deeper view of IMDB

- Replacement policy
  - Replace the entry with MIN(ZeroFlipCntr[MaxZFCIdx])
  - MaxZFIdx: index of MAX(ZeroFlipCntr)
  - Get MIN(RewriteCntr) if more than two MIN(ZeroFlipCntr)
- A large amount of read ports and comparators on the SRAM
  - **Approximate Lowest number Estimator (AppLE)**
  - Few entries as a “group”

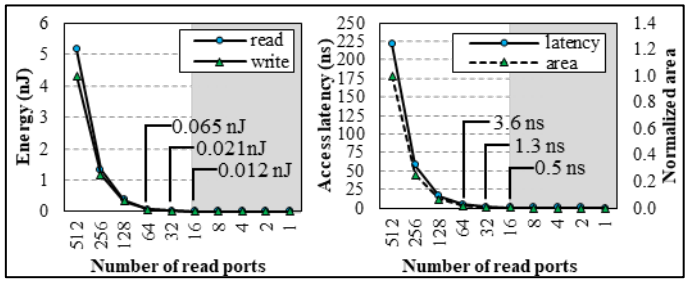
  → 1 group - 1 read port on the SRAM
  - Each read port is fed by a randomizer





Original SRAM for the policy

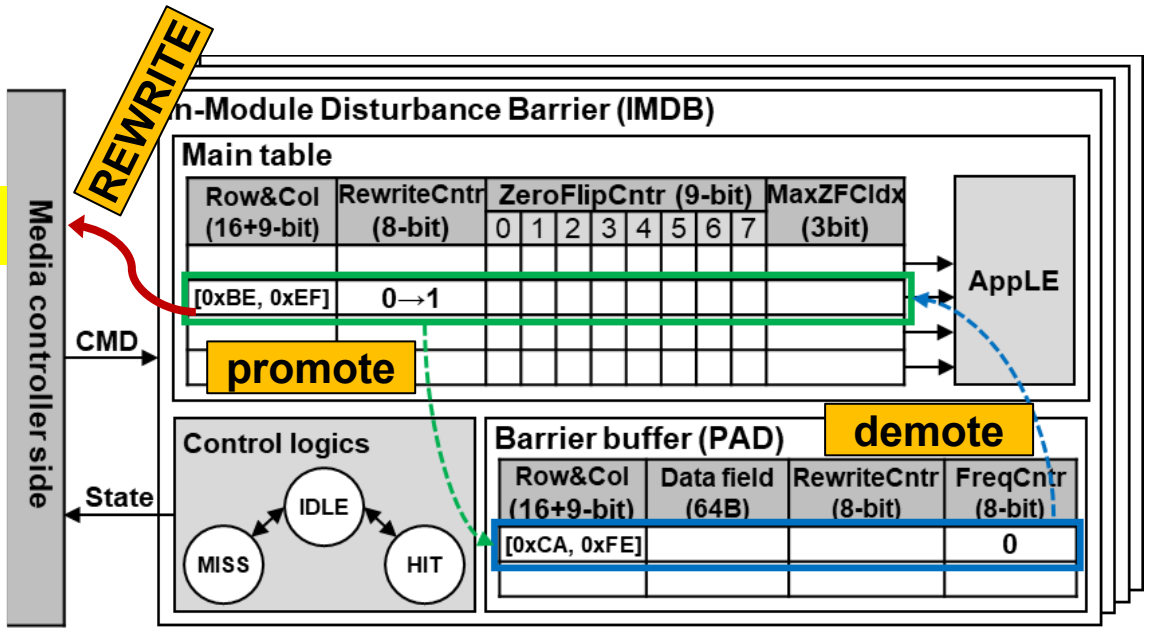
AppLE applied SRAM



Energy, area, latency vs. # of read ports on SRAM

Deeper view of IMDB

- **Barrier buffer**: an SRAM holding extremely WDE-vulnerable addresses along with data
  - Adopt **practical address detector (PAD)** from the work of Qureshi et al.
- Once REWRITE is generated, entry is **promoted** to the barrier buffer
- Barrier buffer is full → swap entries between two tables
- 16 entries as previous work does
  - 2% of total flush time constraint (100us in Optane devices)



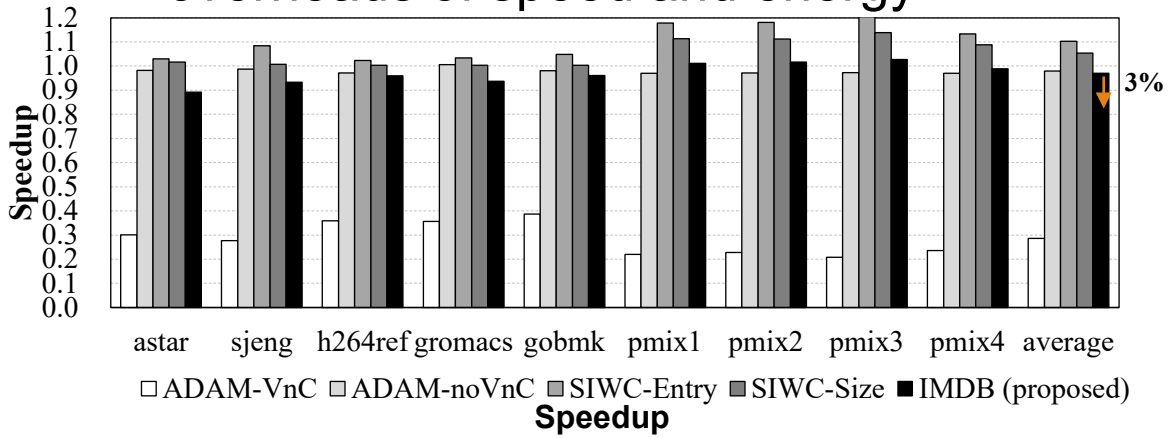
Migration between the main table and the barrier buffer

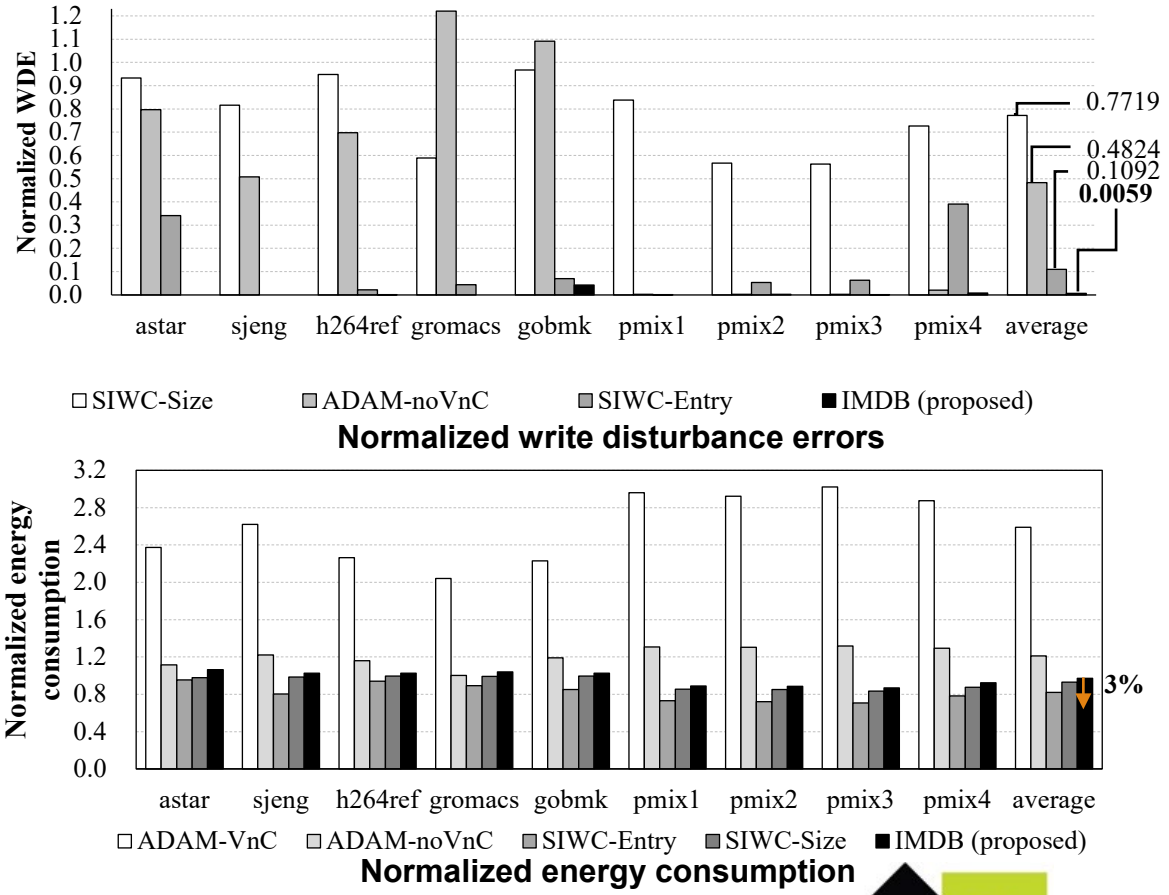
M. K. Qureshi et al., "Practical and secure pcm systems by online detection of malicious write streams," in Proceedings of the 17th International Symposium on High-Performance Computer Architecture (HPCA), 2011.

Experimental Results

- WDE
  - 81.3× lower than ADAM-noVnC
  - 18.4 × lower than SIWC
- Speed & energy: both are 3% lower than the baseline

  → VnC fully eliminates WDE but with high overheads of speed and energy





Conclusion & Future Works

- Conclusion
  - A table-based mitigating WDE with on-demand way is firstly proposed
  - Effectively reduces the number of read ports on SRAM incurred by the replacement policy
  - Significantly reduces WDEs with negligible speed degradation and energy overhead as compared with previous works
- Future works
  - Sensitivity analysis on the entries numbers of main table and barrier buffers
  - Comparison with other state-of-art replacement policy (*i.e.,* LRU)
  - Sensitivity analysis on the number of groups in *AppLE*

Questions