





HYOKEUN LEE

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EDUCATION

-
- Seoul National University**, Seoul, South Korea *Sep. 2016 - Aug. 2021*
Ph.D. Electrical and Computer Engineering
Advisor: Dr. Hyuk-Jae Lee; Co-advisor: Dr. Hyun Kim
Dissertation: Mitigating Disturbance Errors and Enhancing RMW Performance for PCM
- Seoul National University**, Seoul, South Korea *Sep. 2011 - Aug. 2016*
B.S. Electrical and Computer Engineering

WORK EXPERIENCE

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- Secure and Advanced Computer Architecture Group**, North Carolina State University *Feb. 2023 - Present*
- Postdoctoral researcher
- Mentor: Dr. Amro Awad
- Inter-university Research Center (ISRC)**, Seoul National University, South Korea *Sep. 2021 - Jan. 2023*
- Postdoctoral researcher
- Mentor: Dr. Hyuk-Jae Lee
- I served the mandatory military service as a Technical Research Personnel (until Feb. 2023). ISRC is one of the designated research centers for mandatory service in South Korea.

RESEARCH INTERESTS

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- Computer architecture, memory system, disaggregated memory, computer architecture security, Compute-Express Link (CXL), non-volatile memory, phase-change memory

SKILLS

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- Programming:** C++, C, Verilog, Python
Software & Tools: **Architecture simulators:** McSimA+, MacSim, gem5, NVMain, PCMCsim, DRAMsim3
Commercial software: ModelSim, Vivado, Quartus, Design Compiler
Language: **English:** Professional working proficiency
Korean: Native proficiency
Chinese: Bilingual proficiency

RESEARCH ACTIVITIES (PROJECTS)

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- Optimization of Type-3 Compute Express Link (CXL) Add-In Card (AIC) Memory** *Feb. 2022 - Jan. 2023*
- Sponsor: SK Hynix, South Korea
- Developing an in-house simulation platform for CXL memory devices
- Breaking down the performance of the CXL-attached system under various scenarios
- Optimization of memory-centric workloads (e.g., NLP) on the CXL-attached system
- Development of Open Convergence Memory Solution and Platform for Next-Generation Memories** *April. 2020 - Dec. 2022*
- Sponsor: Ministry of Trade, Industry & Energy (MOTIE), South Korea
- Developing a high-performance and low-power PCM-based computer architecture for CNN inference
- DRAM/PRAM Heterogeneous Memory Architecture and Controller IC Design Technology R&D** *July. 2017 - Dec. 2021*
- Sponsor: Ministry of Trade, Industry & Energy (MOTIE), South Korea
- Constructed reliable PRAM technologies concerning endurance and write/read disturbance errors
- Developed an FPGA-based heterogeneous memory system emulation platform

Architecture Exploration of a Hardwired PCM Controller

- Sponsor: SK Hynix, South Korea July. 2020 - June. 2021
- Characterized the performance of the in-house PCM controller simulator developed in the previous year
- Minimized the performance overhead of accessing the DRAM-based address translation table in the PCM controller

PRAM Memory Scheduler Modeling and its Verification against RTL

- Sponsor: SK Hynix, South Korea July. 2019 - June. 2020
- Developed an in-house, functional- and cycle-accurate PCM controller simulator
- Validated functionality and cycle accuracy against the industrial RTL simulation trace

Schemes for Managing Metadata in PCRAM Software Wear-leveling

- Sponsor: SK Hynix, South Korea July. 2017 - June. 2018
- Developed a PCRAM simulation environment using NVMain and gem5
- Minimized the performance overhead of the read-modify-write module in a PCRAM system
- Enhanced the lifetime of PCRAM with the table-based and static wear-leveling

Management on Non-volatile Memory Systems

- Sponsor: SK Hynix, South Korea Sep. 2016 - June. 2017
- Developed a hot address-based wear-leveling for PRAM

Development of Parallel Processing Techniques for Computational Imaging

- Sponsor: Korea Electrotechnology Research Institute (KERI), South Korea Jan. 2016 - Nov. 2017
- Developed an algorithm for improving the image quality under surgery environment
- Accelerated the above algorithm using FPGA

PUBLICATIONS

Journal

- Hyokeun Lee, Seungyong Lee, Byeongki Song, Moonsoo Kim, Seokbo Shim, Hyuk-Jae Lee, and Hyun Kim, "An In-Module Disturbance Barrier for Mitigating Write Disturbance in Phase-Change Memory," IEEE Transactions on Computers, April. 2023.
- Hyokeun Lee, Hyuk-Jae Lee, and Hyun Kim, "A Read Disturbance Tolerant Phase Change Memory System for CNN Inference Workloads," Journal of Semiconductor Technology and Science, Aug. 2022.
- Moonsoo Kim, Hyokeun Lee, Hyun Kim, and Hyuk-Jae Lee, "WL-WD: Wear-Leveling Solution to Mitigate Write Disturbance Errors for Phase-Change Memory," IEEE Access, Feb. 2022.
- Seungyong Lee, Hyokeun Lee, Hyuk-Jae Lee, Hyun Kim, "Evaluation of Various Workloads in Filebench Suitable for Phase-change Memory," IEIE Transactions on Smart Processing & Computing, April. 2021.
- Hyokeun Lee, Hyunmin Jung, Hyuk-Jae Lee, and Hyun Kim, "Bit-width Reduction in Write Counters for Wear Leveling in a Phase-change Memory System," IEIE Transactions on Smart Processing & Computing, Oct. 2020.
- Jinwoo Park, Hyokeun Lee, Boyeal Kim, Dong-Goo Kang, Seung Oh Jin, Hyun Kim, and Hyuk-Jae Lee, "A Low-Cost and High-Throughput FPGA Implementation of the Retinex Algorithm for Real-Time Video Enhancement," IEEE Transactions on Very Large Scale Integration Systems, Jan. 2020.
- Hyokeun Lee, Moonsoo Kim, Hyunchul Kim, Hyun Kim, and Hyuk-Jae Lee, "Integration and Boost of a Read-Modify-Write Module in Phase Change Memory System," IEEE Transactions on Computers, Dec. 2019.
- Sunwoong Kim, Hyunmin Jung, Woojae Shin, Hyokeun Lee, and Hyuk-Jae Lee, "HAD-TWL: Hot Address Detection-based Wear Leveling for Phase-Change Memory Systems with Low Latency," IEEE Computer Architecture Letters, July. 2019.

Conference

- Hyokeun Lee, Hyungsuk Kim, Seokbo Shim, Seungyong Lee, Dosun Hong, Hyuk-Jae Lee, and Hyun Kim, "PCMsim: An Accurate Phase-Change Memory Controller Simulator and its Performance Analysis," IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), 2022.

- Hyeong Gi Seong, Hyekeun Lee, Hyun Kim, and Hyuk-Jae Lee, "Analysis of Hardware Prefetchers Suitable for CNN Applications," IEEE/IEIE International Conference on Consumer Electronics-Asia (ICCE-Asia), Nov. 2021.
- Hyekeun Lee, Seungyong Lee, Moonsoo Kim, Hyun Kim, and Hyuk-Jae Lee, "IMDB: A Low-Cost In-Module Disturbance Barrier for Mitigating Write Disturbance Errors in Phase-Change Memory," Design Automation Conference (DAC, work-in-progress session), July. 2020.
- Hyekeun Lee, Donghyeon Lee, and Hyuk-Jae Lee, "A Predictive Initialization of Hidden State Parameters in a Hidden Markov Model for Hand Gesture Recognition," IEEE/IEIE International Conference on Consumer Electronics-Asia (ICCE-Asia), June. 2018.

PATENTS

- "Mitigating Write Disturbance Errors of Phase-Change Memory Module," US Patent, No. 11462266, Oct. 2022. (Granted)
- "Semiconductor Memory Device Performing Command Merging and Operating Method Thereof," US Patent, No. 11055025, July. 2021. (Granted)
- "Semiconductor Device for Managing Cold Addresses of Nonvolatile Memory Device," US Patent, No. 10877698, Dec. 2020. (Granted)
- "Semiconductor Device for Managing Wear Leveling Operation of a Nonvolatile Memory Device," US Patent, No. 10713159, July. 2020. (Granted)

PROFESSIONAL ACTIVITIES

2023

- Reviewer, IEEE Conference on Artificial Intelligence Circuits and Systems (AICAS)
- Reviewer, IEIE Transactions on Smart Processing and Computing

2022

- Session Chair, The 40th IEEE International Conference on Computer Design (ICCD)
- Program Committee, The 40th IEEE International Conference on Computer Design (ICCD)
- Reviewer, Elsevier Microelectronics Journal
- Reviewer, IEEE Conference on Artificial Intelligence Circuits and Systems (AICAS)

2021

- Reviewer, Material Research Bulletin, Journal, Elsevier
- Reviewer, IEEE /IEIE International Conference on Consumer Electronics Asia (ICCE-ASIA)
- Reviewer, IEIE Transactions on Smart Processing and Computing

REFERENCE

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