ZILONG LYU

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EDUCATION

Georgia Institute of Technology Aug. 2018 - May 2020
M.S. in Computer Science *Atlanta, US*

Tsinghua University Aug. 2014 - July 2018
B.E. in Electronic Engineering (87.3/100) *Beijing, China*

SKILLS

Languages	**C++**, **Java**, **C#**, Python, JavaScript
Courses	**Data Structures & Algorithms**, **OOP**, Computer Vision, Database, Networks
Others	**MATLAB**, Git, MySQL

EXPERIENCE

Microsoft (STC Asia) June 2017 - Sept. 2017
Software Engineer Intern - Relevance & News Group *Beijing, China*

· Labeling is significant to classification of polyphony words in Text-to-Speech. To Improve accuracy and save labeling cost, the sampling strategy needs to be improved.
· Designed and conducted experiments to verify the feasibility of a strategy named Active Learning. Extracted ambiguous samples for correction using Max-Entropy method based on CRF model.
· Used **C#** to create an application for annotation, and integrated Active Learning into the process of annotating by dynamically selecting samples to be labeled by linguistic engineers.
· Reduced 17% classification error with same labeling cost after implementing Active Learning.

DiCarlo Lab, TU Delft Nov. 2016 - Feb. 2017
Research Intern *Delft, Netherlands*

· Participated in design and electromagnetic simulation of radio elements and quantum devices.
· Replaced shape-dependent algorithm using **MATLAB** to support boundary extraction for arbitrary shapes, which greatly improved the efficiency of data processing.

PROJECTS

IEEE1588 Clock Synchronization Feb. 2018 - June 2018
Software Simulation of clock synchronization based on IEEE1588 protocol

· Enable message packaging and exchanging based on UDP Multicasting.
· Used **C++** to implement logic of local state machines which supports IEEE1588 Protocol.
· Eliminated time drift between network nodes and completed clock synchronization.

Greedy Snake June 2016 - June 2016
*Computer game created with **Java***

· Used **Java** to implement core logic of greedy snake.
· Used **Swing** to create graphical interfaces.
· Applied **Socket** and Server-Client Model to enable multi-player mode.

Processor Design June 2016 - July 2016
Design and simulation of a basic processor on FPGA

· Used **Verilog** to implement fundamental functions of processor on FPGA.
· Used **MIPS assembly** to build a basic operating system which can run simple programs.