Design of Low-Power Fault-Tolerant SRAM for Baby Wearable Health Monitoring

Report submitted to GITAM (Deemed to be University) as a partial fulfillment of the requirements for the award of the Degree of Bachelor of Technology in ELECTRONIC AND COMMUNICATION ENGINEERING

Name	Register Number
1. M REDDY SEKHAR	- BU22EECE0100186
2. LAASYA PRIYA RAJA	- BU22EECE0100154
3. VAISHNAVI D	- BU22EECE0100539

DEPARTMENT OF ELECTRICAL, ELECTRONICS AND COMMUNICATION ENGINEERING
GITAM SCHOOL OF TECHNOLOGY
GITAM (DEEMED TO BE UNIVERSITY)
BENGALURU -561203

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DECLARATION

We declare that the project work contained in this report is original and it has been done by me under the guidance of my project guide.

Name: Dr.S.Karthick

Date: 2/09/2025

Signature of the Student: (M REDDY SEKHAR LAASYA PRIYA RAJA VAISHNAVI)

Department of Electrical, Electronics and Communication Engineering
GITAM School of Technology, Bengaluru-561203

GITAM
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CERTIFICATE

This is to certify that (M Reddy Sekhar, lasya Priya raja,vaishnavi) bearing(Regd.No.:BU22EECE0100186,BU22EECE0100154,BU22EECE0100539)has satisfactorily completed Mini Project Entitled in partial fulfillment of the requirements as prescribed by University for VIIth semester, Bachelor of Technology in "Electrical, Electronics and Communication Engineering" and submitted this report during the academic year 2025-2026.

[Signature of the Guide]

Dr. Karthick sekhar

[Signature of HOD]

Dr. Prithvi Sekhar Pagala

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Chapter 1: Introduction

1.1 Overview of the problem statement

Wearable health monitoring devices such as smart watches, fitness trackers, and biomedical patches have become an essential part of modern healthcare systems. These devices continuously acquire physiological signals including heart rate, blood pressure, oxygen saturation, and motion activity, and often process the data locally before transmitting it to a smartphone or a cloud platform. To achieve reliable real-time monitoring while operating under strict battery constraints, the underlying hardware must provide **ultra-low power consumption**, **high reliability**, and **compact area efficiency**.

1.2 Objectives and goals

Main Goals

- Achieve ultra-low leakage and active power.
- Enable stable operation at near-threshold voltages (0.5–0.7 V).
- Integrate fault-tolerance mechanisms (ECC, redundancy).
- Improve stability against process variation and aging.
- Validate with simulations (SNM, delay, power, Monte-Carlo).

Additional Goals

- Extend battery life of wearable devices.
- Ensure reliable long-term health monitoring

Chapter 2 : Literature Review

Title and Author	Problem statement	Methodology	Result
Design of a SRAM memory cell with enhanced stability and variability for embedde d biomedica l applicatio ns , Sagar Juneja a , M. Elangovan b , Kulbhushan Sharma	There is a need for highly efficient on-chip memories for modern embedded and biomedical devices, where SRAM cells dominate chip area and power use. SRAM cells must be resilient against soft errors and other issues	The proposed 11-transistor (11T) LCTG FinFET-based SRAM cell was designed in Cadence Virtuoso using 18 nm FinFET devices. The design incorporates a transmission gate (TG) for a fast, stable write path , leakage control transistors for power efficiency , a PPN inverter structure , and a decoupled read path for stability	The proposed 11T LCTG cell has the best Figure of Merit (FOM) when balancing delay, statics, power, and area. The write stability (WSNM) and read stability (RSNM) of the cell are superior to other SRAM cells. The design also has the smallest write delay and second-lowest hold power. Monte Carlo and PVT analyses show lower variability and high robustness.

Title and Author	Problem statement	Methodology	Result
A FinFET Based Low Power Static Random Access Memory Cell With Improved Stability Gautam Rana1 ,Ashish Sachde va2 M. Elangovan3 Kulbhushan Sh arma	The demand for ultra-low power SRAM is growing. Existing SRAM designs face challenges like high write power in 11T cells, read disturbance in 8T cells, and trade-offs between write ability and read stability	The proposed FC8T SRAM cell was designed and simulated using 18 nm FinFET models in Cadence Virtuoso. The design features separate read/write paths, a read decoupled design, and a feedback-cutting mechanism. The Fin number in pull-down transistors was optimized to reduce leakage. The performance was compared to conventional 6T, 8TRD, 10TST, and 10TMST cells	The proposed FC8T SRAM cell has significant reductions in write power (up to 1.88x lower) and read power (up to 34% lower). It also shows improved write stability (WSNM up to 1.85x higher) and read stability (RSNM up to 2.27x higher). It also has a lower read delay compared to 10T designs.
SHRCO: Design of an SRAM with High Reliability and Cost Optimizatio n for Safety Critical Applications	ang Chang School of Computer Science and Technology Anhui University Hefei, China 690491839@q q.com Gaoyang Shan Department of Software and Computer Engineering Ajou University	he proposed SHRCO SRAM cell uses 18 transistors: 12 for storage and 6 for parallel access. It features separated, error-interceptive feedback paths. Fault injection simulations using a double exponential current source model with HSPICE were used to analyze SNU/DNU self recovery principles.	he SHRCO cell offers complete self recoverability from all single node upsets. It can also recover from double node upsets in 16 total node pairs. The design achieves an average read time saving of 28% and write time saving of 3% compared to existing radiation hardened SRAM cells

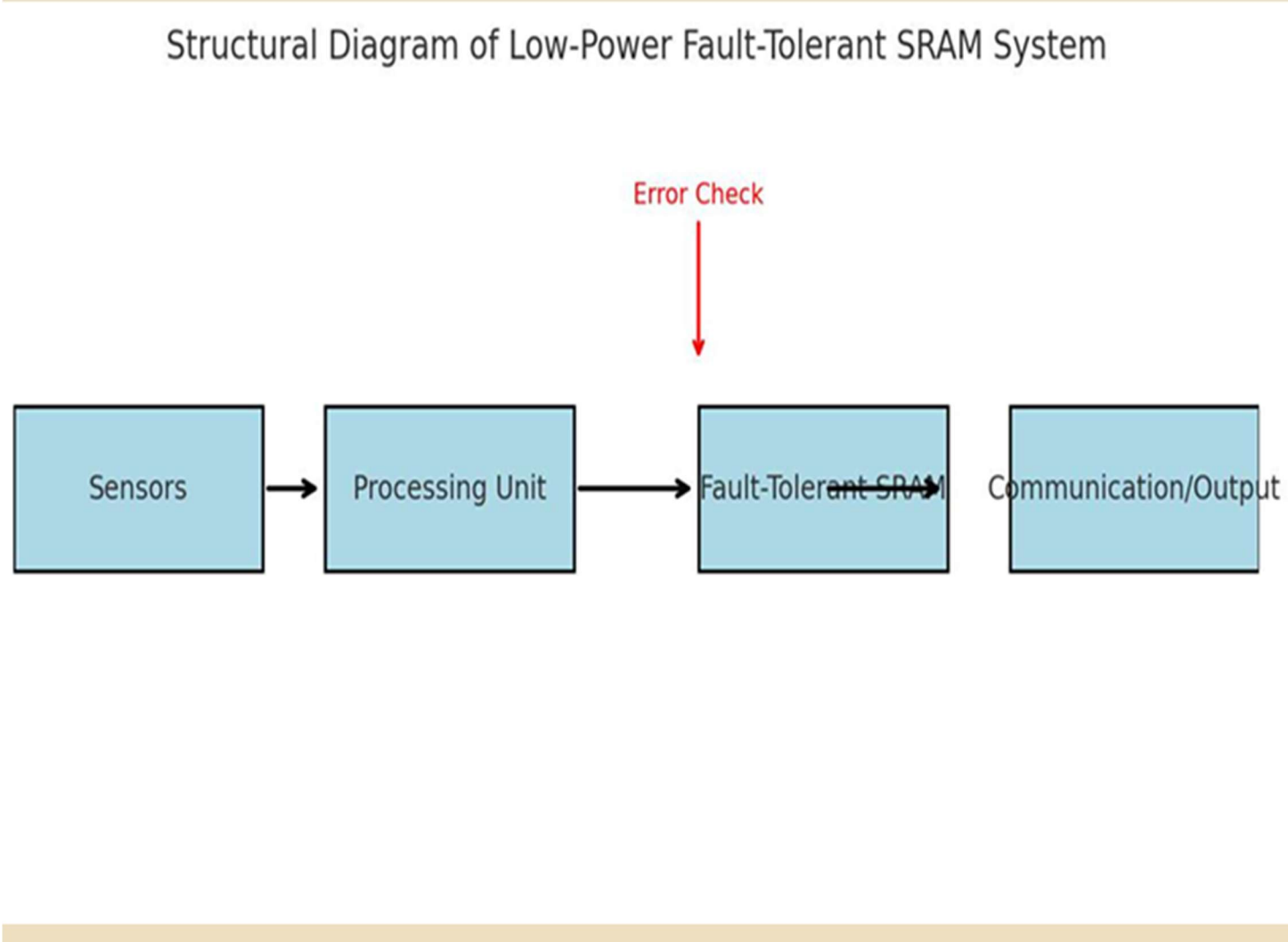
Title and Author	Problem statement	Methodology	Result
Investigati on of stability parameter s of a gate-stack junctionle ss double gate transistor (GS JLDGT) based 6T and 3T SRAM in the presence of traps	Traditional SRAM designs face reliability challenges from interface trap charges at the oxide semiconductor interface, which affect performance and stability. This is especially true at elevated temperatures.	The study proposes a GS-JLDGT structure to build both 6T and 3T SRAM cells. The structure was simulated using the Silvaco ATLAS 3D device simulator. The impact of different trap profiles (uniform and step function) and temperature scenarios (200-500 K) on transfer characteristics and stability margins (SNM, RNM, SVNM, etc.) was analyzed.	Both the 6T and 3T structures show performance degradation in the presence of interface trap charges, with the degradation intensifying at higher temperatures . Uniform trap profiles were found to be more detrimental. The 3T SRAM design reduces
CNTFET based leakage control static approximat e full adder circuit for high performanc e multimedia applications	The need for high-speed, low power digital circuits in portable devices necessitates improved full adder (FA) designs.	The proposed 11T-LCSAFA design modifies a mirror adder circuit to reduce transistors and implement complementary logic with a leakage control transistor based inverter. The circuit was simulated using a 32 nm Stanford CNTFET model in the Cadence Virtuoso Tool. The performance was compared to four contemporary approximate FA circuits. A 4-bit ripple carry adder (RCA) was also	The proposed 11T-LCSAFA design has a power dissipation of 3.132 nW and a propagation delay of 3.743 ps at 500 mV. It outperforms contemporary designs in propagation delay (TD), power dissipation (PD), power delay product (PDP), and energy delay product (EDP). The 4-bit RCA implemented with the design has a maximum propagation delay of 39.929 ps and a

		implemented using the proposed design	power dissipation of 23.37 nW.

Chapter 3 : Architecture

Structural Diagram

Block Diagram/Pin Diagram
Resource



Behaviour Diagram

Flow chart/ State machine

Resource –

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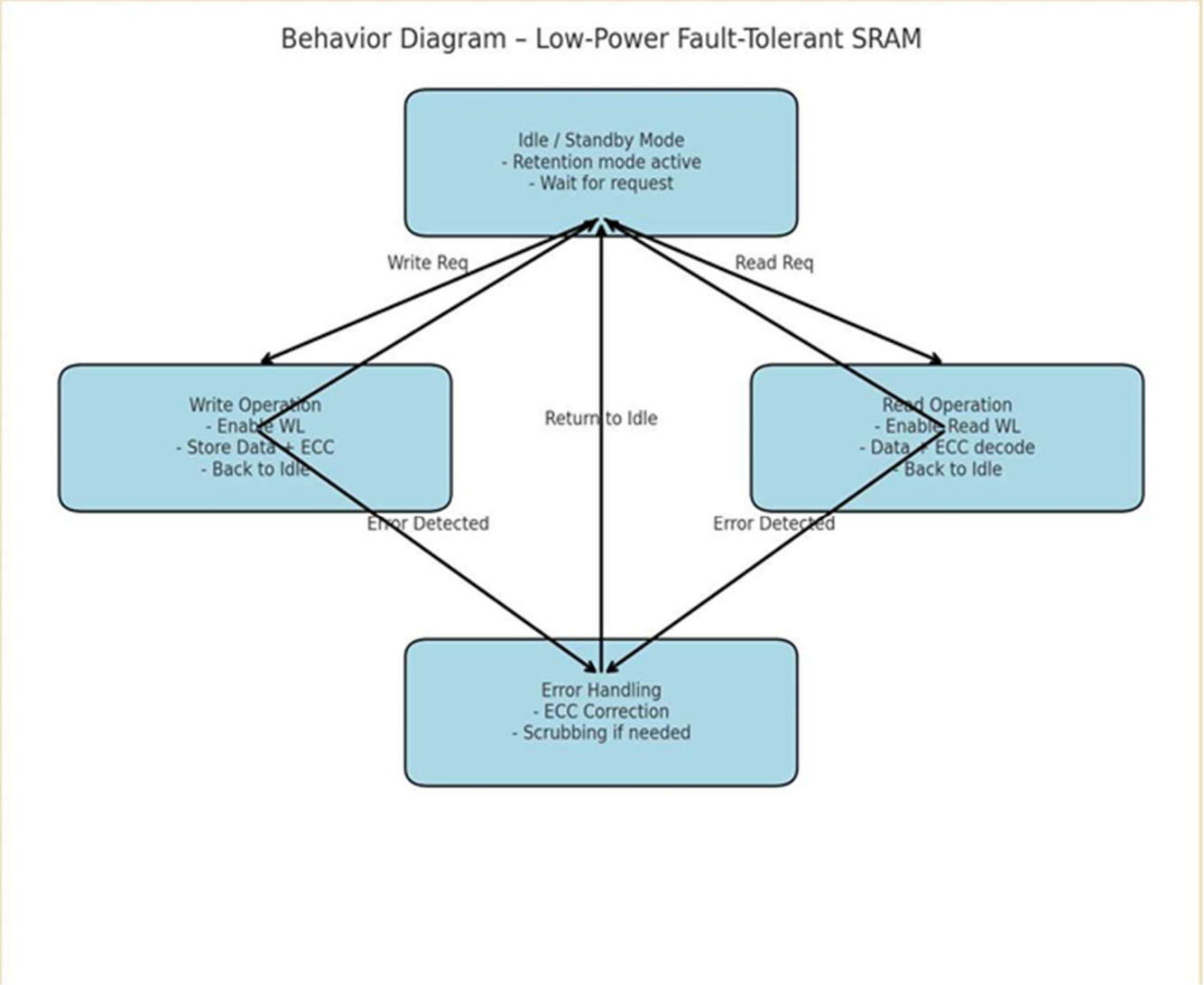

Chapter 4 : Use Cases & Testing

Use Cases Heart-Rate Monitoring
SRAM stores continuous heart-rate samples
Requires low power and error-free storage . Motion Data Buffering
Temporary storage for accelerometer/gyroscope signals
Needs fast write and reliable retention. Audio/Event Detection
Save short audio clips (baby cry, fall detection).
Must work in low-voltage always-on mode Wearable Device Settings
Retains calibration and user configuration.
nsures safe wake-up from sleep mode

Test Cases Hold Stability Test
Measure Static Noise Margin (SNM) at 0.5–0.7 V.
Ensure cell retains data correctly in standby mode. Read Operation Test
Verify read speed and stability using decoupled read port.
Confirm no read-disturb errors at low supply voltage. Write Operation Test
Check write margin and delay.
Validate data overwrite even with weak pull-up devices . .
Fault Tolerance Test
Inject single-bit errors → ECC must correct.
Inject double-bit errors → ECC must detect and flag.
Variation & Reliability Test
Run Monte-Carlo simulations for process variation. Test across temperature (−40°C to 85°C). Leakage & Retention Test

Chapter 5: Conclusion

The project's objective is to design a low-power, fault-tolerant SRAM cell for use in wearable health monitoring devices. The design will combine FinFET, CNTFET, and junctionless FET transistors to achieve key goals, including ultra-low leakage and active power, and stable operation at near-threshold voltages of 0.5–0.7 V. Additionally, it aims to integrate fault-tolerance mechanisms like ECC and redundancy to improve stability against process variation and aging. The project plan includes simulating the basic SRAM and analyzing its power consumption and stability metrics. The proposed SRAM is intended to extend battery life and ensure reliable long term health monitoring for applications such as heart rate monitoring, motion data buffering, and event detection

Chapter 6 : Future Work

Provides reliable memory support for wearable baby health monitoring systems.
Improves battery life through low power consumption.
Increases trust in medical IoT devices by ensuring fault tolerance.

Future work:

scaling the design to larger memory arrays, integrating with biomedical sensors, and optimizing for AI-driven health analytics

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Bengaluru City Office No 5/1, First Floor, Prestige Terraces, Union Street, Infantry Road, Bengaluru - 560003 Karnataka, India

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