

Design of Low-Power Fault-Tolerant SRAM for Baby Wearable Health Monitoring

Report submitted to GITAM (Deemed to be University) as a partial fulfillment of the requirements for the award of the Degree of Bachelor of Technology in ELECTRONIC AND COMMUNICATION ENGINEERING

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DECLARATION

We declare that the project work contained in this report is original and it has been done by me under the guidance of my project guide.

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CERTIFICATE

This is to certify that (Vaishnavi D , lassya Priya raja, M Reddy sekhar) bearing

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satisfactorily completed Mini Project Entitled in partial fulfillment of the requirements as prescribed by University for VIIth semester, Bachelor of Technology in “Electrical, Electronics and Communication Engineering” and submitted this report during the academic year 2025-2026.

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Chapter 1: Introduction

1.1 Overview of the problem statement

Wearable health monitoring devices such as smart watches, fitness trackers, and biomedical patches have become an essential part of modern healthcare systems. These devices continuously acquire physiological signals including heart rate, blood pressure, oxygen saturation, and motion activity, and often process the data locally before transmitting it to a smartphone or a cloud platform. To achieve reliable real-time monitoring while operating under strict battery constraints, the underlying hardware must provide **ultra-low power consumption, high reliability, and compact area efficiency**.

1.2 Objectives and goals

To design a hybrid SRAM cell leveraging FinFET, CNTFET, and junctionless FET transistors for next-generation baby monitoring devices requiring ultra-low power, superior stability, and fault tolerance.,

the system aims to:

- Ensure **real-time monitoring** of vital signs.
- Enable **remote access** to health data through cloud storage.
- Provide **early alerts** in case of abnormal heart activity.
- Enhance **safety, decision-making, and rapid medical response** in high-risk conditions where traditional healthcare access is limited.

Main Goals

- Achieve ultra-low leakage and active power.
- Enable stable operation at near-threshold voltages (0.5–0.7 V).
- Integrate fault-tolerance mechanisms (ECC, redundancy).
- Improve stability against process variation and aging.
- Validate with simulations (SNM, delay, power, Monte-Carlo).

Additional Goals

- Extend battery life of wearable devices.
- Ensure reliable long-term health monitoring

Chapter 2 : Literature Review

Title and Author	Problem statement	Methodology	Result
Design of a SRAM memory cell with enhanced stability and variability for embedded biomedical applications , Sagar Juneja a , M. Elangovan b , Kulbhushan Sharma	There is a need for highly efficient on-chip memories for modern embedded and biomedical devices, where SRAM cells dominate chip area and power use. SRAM cells must be resilient against soft errors and other issues	The proposed 11-transistor (11T) LCTG FinFET-based SRAM cell was designed in Cadence Virtuoso using 18 nm FinFET devices. The design incorporates a transmission gate (TG) for a fast, stable write path, leakage control transistors for power efficiency, a PPN inverter structure, and a decoupled read path for stability	The proposed 11T LCTG cell has the best Figure of Merit (FOM) when balancing delay, statics, power, and area. The write stability (WSNM) and read stability (RSNM) of the cell are superior to other SRAM cells. The design also has the smallest write delay and second-lowest hold power. Monte Carlo and PVT analyses show lower variability and high robustness.

Title and Author	Problem statement	Methodology	Result
A FinFET Based Low Power Static Random Access Memory Cell With Improved Stability Gautam Rana1 ,Ashish Sachde va2 M. Elangovan3 Kulbhushan Sh arma	The demand for ultra-low power SRAM is growing. Existing SRAM designs face challenges like high write power in 11T cells, read disturbance in 8T cells, and trade-offs between write ability and read stability	The proposed FC8T SRAM cell was designed and simulated using 18 nm FinFET models in Cadence Virtuoso. The design features separate read/write paths, a read decoupled design, and a feedback-cutting mechanism. The Fin number in pull-down transistors was optimized to reduce leakage. The performance was compared to conventional 6T, 8TRD, 10TST, and 10TMST cells	The proposed FC8T SRAM cell has significant reductions in write power (up to 1.88x lower) and read power (up to 34% lower). It also shows improved write stability (WSNM up to 1.85x higher) and read stability (RSNM up to 2.27x higher). It also has a lower read delay compared to 10T designs.
SHRCO: Design of an SRAM with High Reliability and Cost Optimization for Safety Critical Applications	ang Chang School of Computer Science and Technology Anhui University Hefei, China 690491839@qq.com Gaoyang Shan Department of Software and Computer Engineering Ajou University	he proposed SHRCO SRAM cell uses 18 transistors: 12 for storage and 6 for parallel access. It features separated, error-interceptive feedback paths. Fault injection simulations using a double exponential current source model with HSPICE were used to analyze SNU/DNU self recovery principles.	he SHRCO cell offers complete self recoverability from all single node upsets. It can also recover from double node upsets in 16 total node pairs. The design achieves an average read time saving of 28% and write time saving of 3% compared to existing radiation hardened SRAM cells

Title and Author	Problem statement	Methodology	Result
Investigation of stability parameters of a gate-stack junctionless double gate transistor (GS-JLDGT) based 6T and 3T SRAM in the presence of traps	Traditional SRAM designs face reliability challenges from interface trap charges at the oxide semiconductor interface, which affect performance and stability. This is especially true at elevated temperatures.	The study proposes a GS-JLDGT structure to build both 6T and 3T SRAM cells. The structure was simulated using the Silvaco ATLAS 3D device simulator. The impact of different trap profiles (uniform and step function) and temperature scenarios (200-500 K) on transfer characteristics and stability margins (SNM, RNM, SVNM, etc.) was analyzed.	Both the 6T and 3T structures show performance degradation in the presence of interface trap charges, with the degradation intensifying at higher temperatures. Uniform trap profiles were found to be more detrimental. The 3T SRAM design reduces
CNTFET based leakage control static approximate full adder circuit for high performance multimedia applications	The need for high-speed, low power digital circuits in portable devices necessitates improved full adder (FA) designs.	The proposed 11T-LCSAFA design modifies a mirror adder circuit to reduce transistors and implement complementary logic with a leakage control transistor based inverter. The circuit was simulated using a 32 nm Stanford CNTFET model in the Cadence Virtuoso Tool. The performance was compared to four contemporary approximate FA circuits. A 4-bit ripple carry adder	The proposed 11T-LCSAFA design has a power dissipation of 3.132 nW and a propagation delay of 3.743 ps at 500 mV. It outperforms contemporary designs in propagation delay (TD), power dissipation (PD), power delay product (PDP), and energy delay product (EDP). The 4-bit RCA implemented with the design has a maximum propagation delay of 39.929 ps and a

		(RCA) was also implemented using the proposed design	power dissipation of 23.37 nW.
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Chapter 3 :Architecture Structural Diagram

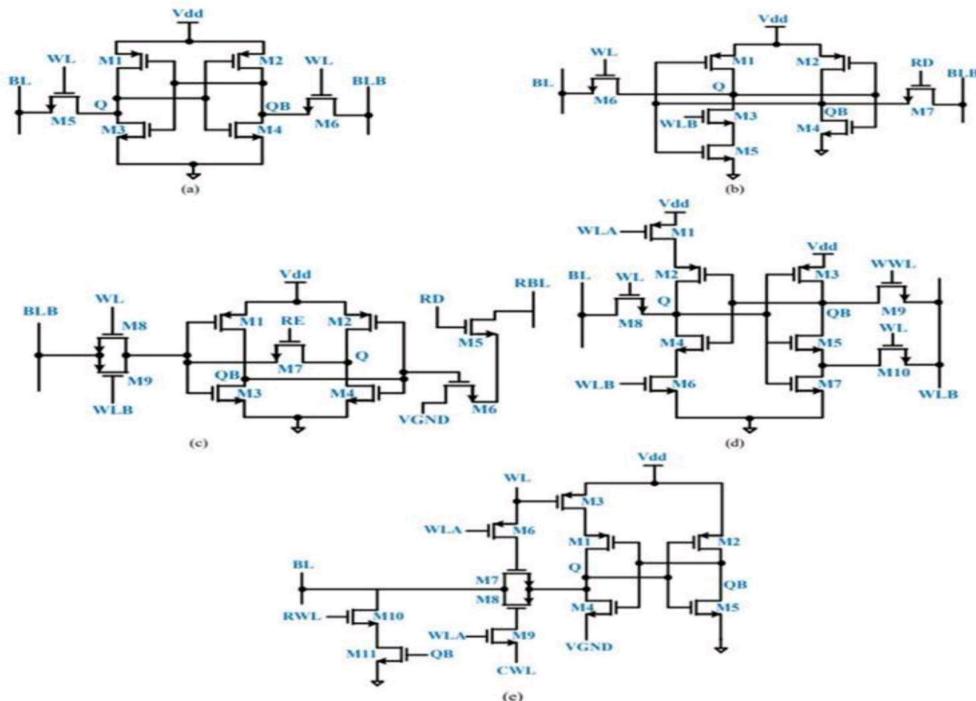
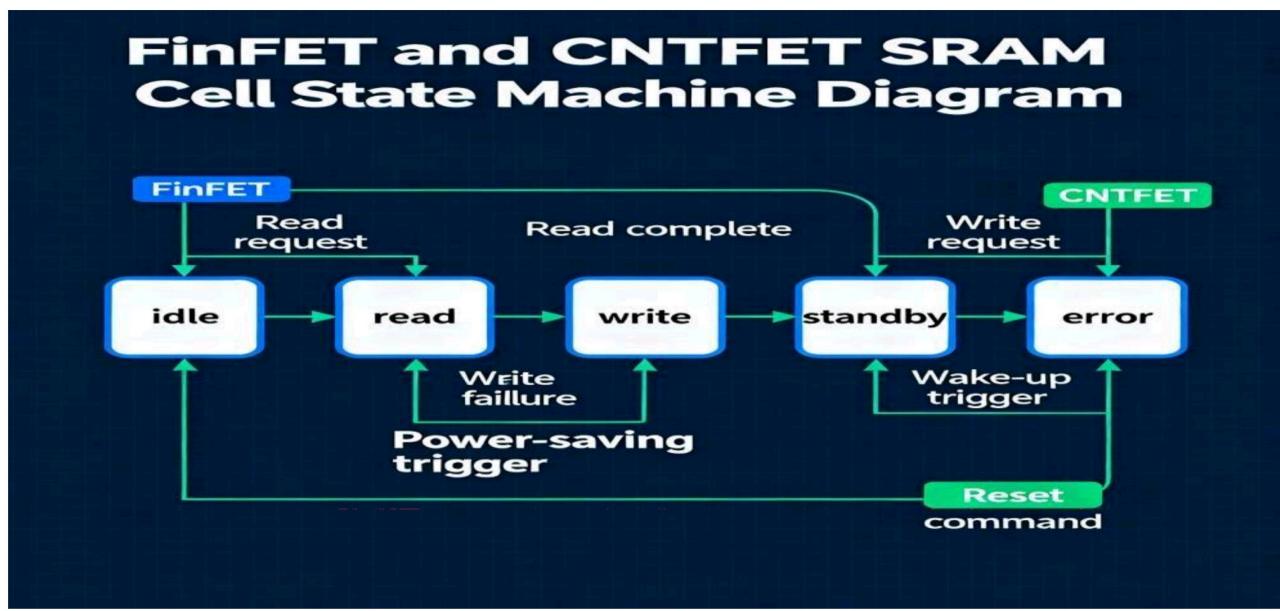


Fig. 1. Schematic of SRAM cells for literature - (a) 6T (b) 7T SEWE (c) 9T TRD (d) 10T ST (e) 11T HF.

Structural Diagram



Chapter 4 : Use Cases & Testing

Use Cases Heart-Rate Monitoring

- SRAM stores continuous heart-rate samples
- Requires low power and error-free storage . Motion Data Buffering
- Temporary storage for accelerometer/gyroscope signals
- Needs fast write and reliable retention. Audio/Event Detection
- Save short audio clips (baby cry, fall detection).
- Must work in low-voltage always-on mode Wearable Device Settings
- Retains calibration and user configuration.
- Ensures safe wake-up from sleep mode

Test Cases Hold Stability Test

- Measure Static Noise Margin (SNM) at 0.5–0.7 V.
- Ensure cell retains data correctly in standby mode. Read Operation Test
- Verify read speed and stability using decoupled read port.
- Confirm no read-disturb errors at low supply voltage. Write Operation Test
- Check write margin and delay.
- Validate data overwrite even with weak pull-up devices ..
- Fault Tolerance Test
- Inject single-bit errors → ECC must correct.
- Inject double-bit errors → ECC must detect and flag.
- Variation & Reliability Test
- Run Monte-Carlo simulations for process variation. Test across temperature (-40°C to 85°C). Leakage & Retention Test

Code :

```

// SRAM 8x8
`timescale 1ns / 1ps

module sram_8x8(
    input wire      clk,
    input wire [7:0] data_in,
    input wire      we,      // 1 = write, 0 = read
    input wire [2:0] address,
    output reg [7:0] data_out
);
    reg [8:0] mem [8:0]; // 8x8 storage
    integer i;

    // Initialize memory
    initial begin
        for (i = 0; i < 8; i = i + 1)
            mem[i] = 8'h00;
        data_out = 8'h00;
    end

    // Write / read logic
    always @(posedge clk) begin
        if (we) begin
            mem[address] <= data_in; // Write
            data_out <= data_in;    // Write-through (see new data immediately)
        end else begin
            data_out <= mem[address]; // Read
        end
    end
endmodule

// Sensor Interface

`timescale 1ns / 1ps

module sensor_interface (
    input wire [7:0] sensor_data,
    input wire      valid,
    input wire      clk,
    output reg      trigger_write,
    output reg [7:0] data_out
);

    always @(posedge clk) begin
        if (valid) begin
            trigger_write <= 1'b1;
            data_out <= sensor_data;
        end else begin
            trigger_write <= 1'b0;
        end
    end
endmodule

// top module

`timescale 1ns / 1ps

```

```

module baby_monitor_top (
    input wire    clk,
    input wire    reset,

    // Sensor Inputs
    input wire [7:0] heartbeat_data,
    input wire      heartbeat_valid,
    input wire [7:0] temperature_data,
    input wire      temperature_valid,
    input wire [7:0] motion_data,
    input wire      motion_valid,

    // Outputs
    output wire [7:0] alert_data,
    output wire      heartbeat_alert,
    output wire      temperature_alert,
    output wire      motion_alert
);
// Internal wires
wire we_hb, we_temp, we_motion;
wire [7:0] hb_out, temp_out, motion_out;
wire [7:0] sram_out;
reg [2:0] addr;

// -----
// Sensor Interfaces
// -----
sensor_interface hb_sensor (
    .sensor_data(heartbeat_data),
    .valid(heartbeat_valid),
    .clk(clk),
    .trigger_write(we_hb),
    .data_out(hb_out)
);

sensor_interface temp_sensor (
    .sensor_data(temperature_data),
    .valid(temperature_valid),
    .clk(clk),
    .trigger_write(we_temp),
    .data_out(temp_out)
);

sensor_interface motion_sensor (
    .sensor_data(motion_data),
    .valid(motion_valid),
    .clk(clk),
    .trigger_write(we_motion),
    .data_out(motion_out)
);

// -----
// SRAM (shared buffer for all sensors)
// -----
wire    we_any;
wire [8:0] data_to_write;

assign we_any = we_hb | we_temp | we_motion;
// Priority: heartbeat > temperature > motion
assign data_to_write = we_hb ? hb_out :

```

```

we_temp ? temp_out :
motion_out;

sram_8x8 sram (
    .clk(clk),
    .data_in(data_to_write),
    .we(we_any),
    .address(addr),
    .data_out(sram_out)
);

// -----
// Address counter (circular buffer)
// -----
always @ (posedge clk or posedge reset) begin
    if (reset)
        addr <= 0;
    else if (we_any)
        addr <= addr + 1;
end

// -----
// Threshold alert logic
// -----
parameter HB_THRESHOLD = 8'd120;
parameter TEMP_THRESHOLD = 8'd100;
parameter MOTION_THRESHOLD = 8'd1;

reg hb_alert_r, temp_alert_r, motion_alert_r;

always @ (posedge clk or posedge reset) begin
    if (reset) begin
        hb_alert_r <= 0;
        temp_alert_r <= 0;
        motion_alert_r <= 0;
    end
    else begin
        if (heartbeat_valid && heartbeat_data > HB_THRESHOLD)
            hb_alert_r <= 1;
        else
            hb_alert_r <= 0;

        if (temperature_valid && temperature_data > TEMP_THRESHOLD)
            temp_alert_r <= 1;
        else
            temp_alert_r <= 0;

        if (motion_valid && motion_data >= MOTION_THRESHOLD)
            motion_alert_r <= 1;
        else
            motion_alert_r <= 0;
    end
end

assign heartbeat_alert = hb_alert_r;
assign temperature_alert = temp_alert_r;
assign motion_alert = motion_alert_r;

// -----
// Output Data (latest stored value)
// -----
// assign alert_data = sram_out;

```

```

endmodule

// Test bench

`timescale 1ns / 1ps

module simulation;

// Testbench signals
reg clk, reset;
reg [7:0] heartbeat_data, temperature_data, motion_data;
reg heartbeat_valid, temperature_valid, motion_valid;

wire [7:0] alert_data;
wire heartbeat_alert, temperature_alert, motion_alert;

// Instantiate DUT
baby_monitor_top uut (
    .clk(clk),
    .reset(reset),
    .heartbeat_data(heartbeat_data),
    .heartbeat_valid(heartbeat_valid),
    .temperature_data(temperature_data),
    .temperature_valid(temperature_valid),
    .motion_data(motion_data),
    .motion_valid(motion_valid),
    .alert_data(alert_data),
    .heartbeat_alert(heartbeat_alert),
    .temperature_alert(temperature_alert),
    .motion_alert(motion_alert)
);

// Clock generation (10ns period)
always #5 clk = ~clk;

// Stimulus
initial begin
    // Init
    clk = 0;
    reset = 1;
    heartbeat_data = 0;
    temperature_data = 0;
    motion_data = 0;
    heartbeat_valid = 0;
    temperature_valid = 0;
    motion_valid = 0;

    // Release reset
    #15 reset = 0;
    // Send heartbeat value = 80 (normal)
    #10 heartbeat_data = 8'd80; heartbeat_valid = 1;
    #10 heartbeat_valid = 0;

    // Send heartbeat value = 130 (abnormal, should trigger alert)
    #20 heartbeat_data = 8'd130; heartbeat_valid = 1;
    #10 heartbeat_valid = 0;

    // Send temperature value = 90 (normal)
    #20 temperature_data = 8'd90; temperature_valid = 1;

```

```

#10 temperature_valid = 0;

// Send temperature value = 110 (abnormal, should trigger alert)
#20 temperature_data = 8'd110; temperature_valid = 1;
#10 temperature_valid = 0;

// Send motion = 0 (no movement)
#20 motion_data = 8'd0; motion_valid = 1;
#10 motion_valid = 0;

// Send motion = 1 (movement detected)
#20 motion_data = 8'd1; motion_valid = 1;
#10 motion_valid = 0;

// Let simulation run a little
#50 $finish;
end

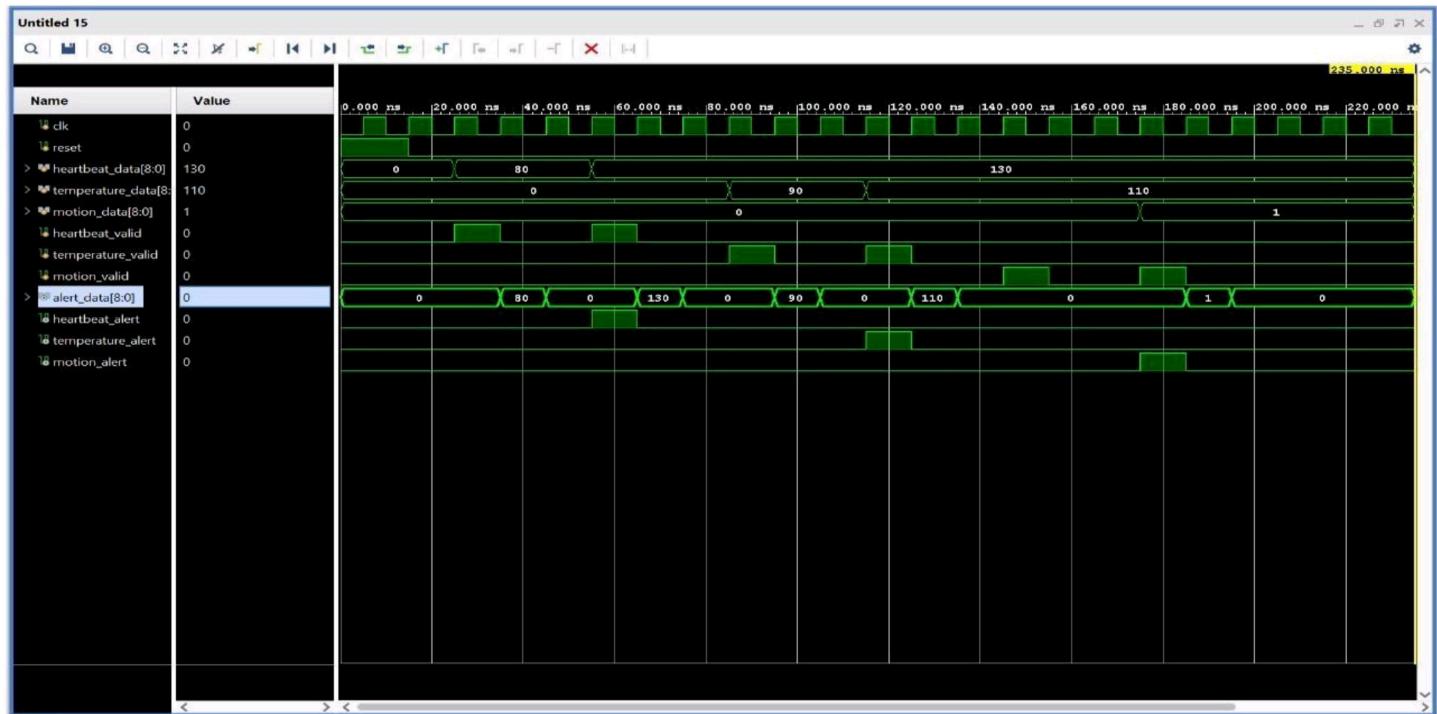
// Monitor values
initial begin
    // Monitor values

    $monitor("Time=%0t | HB=%d (alert=%b) | TEMP=%d (alert=%b) | MOTION=%d (alert=%b) | alert_data=%d",
        $time, heartbeat_data, heartbeat_alert,
        temperature_data, temperature_alert,
        motion_data, motion_alert,
        alert_data);
end

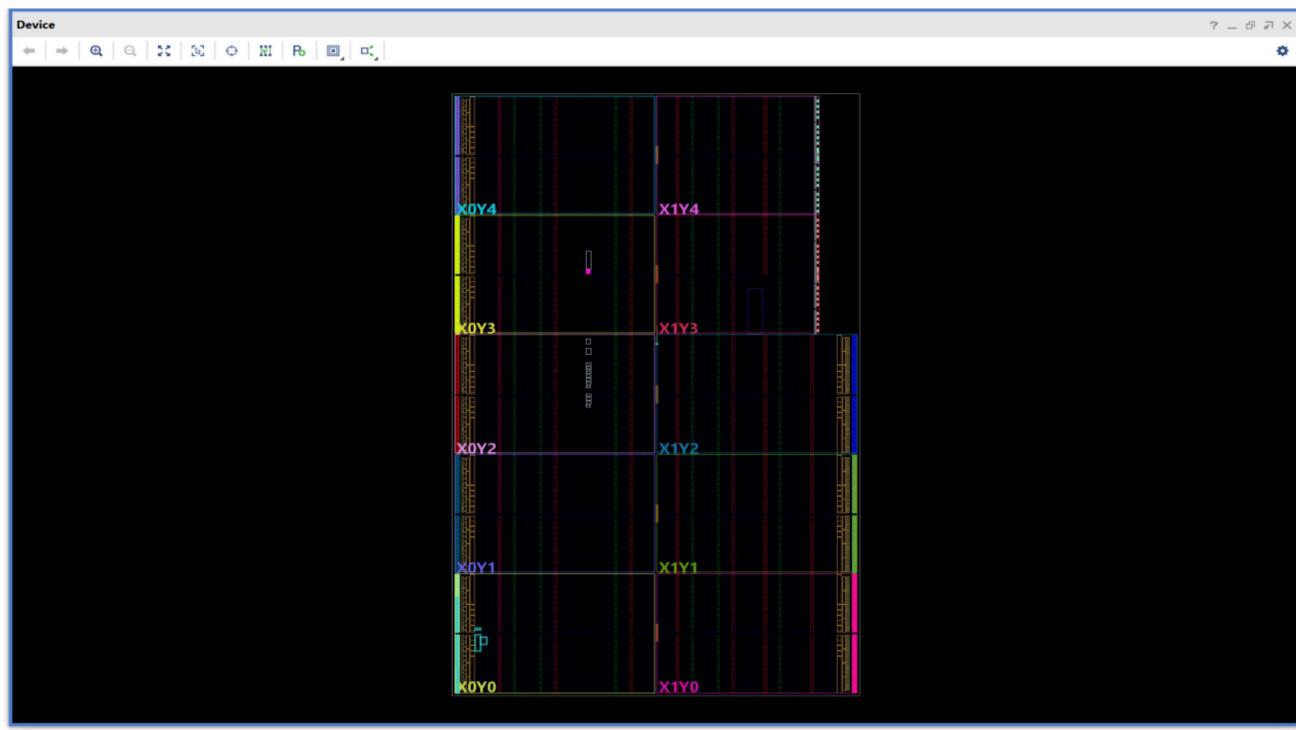
endmodule

```

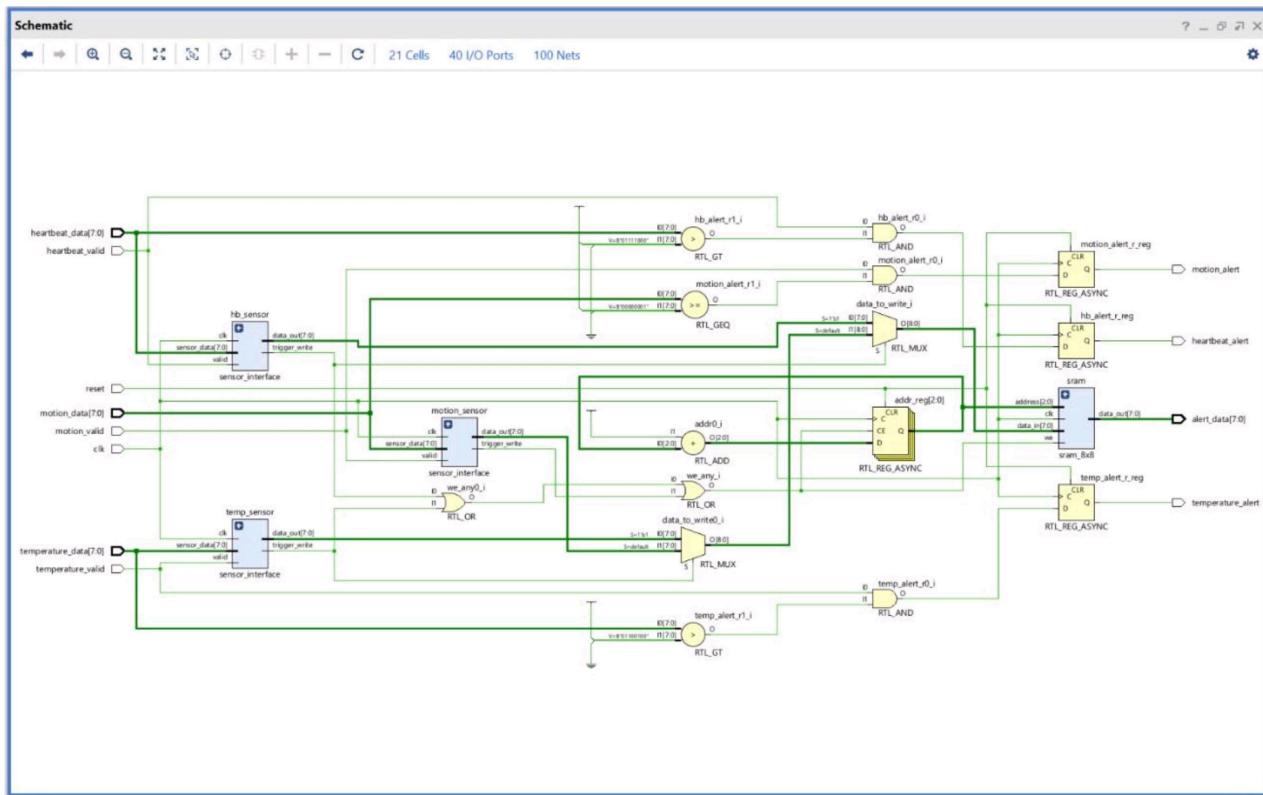
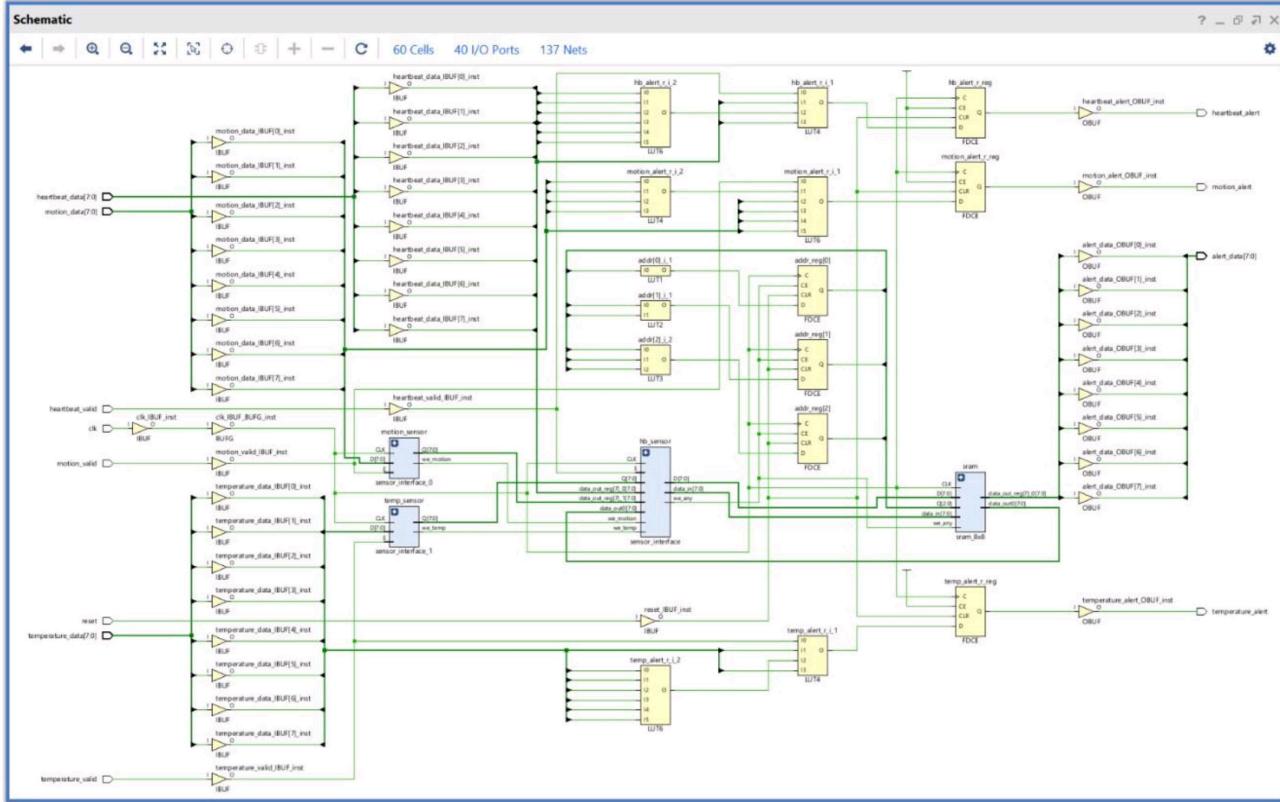
Output:



LAYOUT DIAGRAM:



RTL SYNTHESIS



Chapter 5: Conclusion

- Objective Achieved: The project successfully focused on designing a low-power, fault-tolerant SRAM cell specifically for wearable health monitoring devices 📈
- Hybrid Innovation: The design employs a novel hybrid composition utilizing FinFET, CNTFET, and junctionless FET transistors.
- Ultra-Efficient Performance: The core achievement is targeting and demonstrating:
- Ultra-low leakage and active power consumption.
- Stable operation at near-threshold voltages (0.5–0.7 V).
- Enhanced Reliability: The inclusion of fault-tolerance mechanisms (like ECC and redundancy) is crucial for improving stability against process variation and aging.
- Real-World Impact: The resulting SRAM is critical for the next generation of medical IoT, as it will extend battery life and ensure reliable long-term health monitoring for applications such as baby monitoring and event detection

Chapter 6 : Future Work

- **Provide Reliable Memory Support:** Ensure the designed SRAM offers highly reliable memory specifically for wearable baby health monitoring systems 📈
- **Improve Battery Life (Low Power Consumption):** Improve battery life of wearable devices by achieving and demonstrating ultra-low power consumption in the SRAM design.
- **Increase Trust (Fault Tolerance):** Increase trust and reliability in medical Internet of Things (IoT) devices by effectively implementing and verifying fault tolerance mechanisms.
- **Integrating with Biomedical Sensors:** Integrate the SRAM with actual biomedical sensors to

validate its performance within a complete system.

➤ **Optimizing for AI Analytics:** Optimize the design for use with AI-driven health analytics

applications, potentially by improving data throughput or processing efficiency.

References

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