



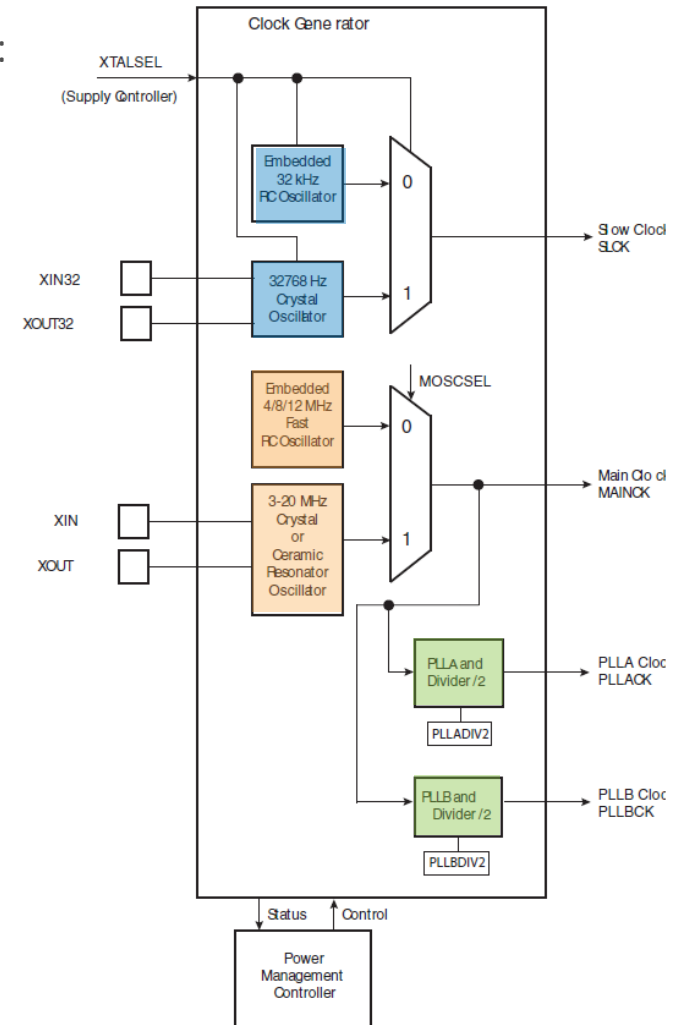
SAM4S Power Management Controller (PMC)

SAM4S Power Management Controller (PMC)

Clock Generator

The clock generator provides the following clocks:

- **Slow Clock (SLCK) sources:**
 - On-chip 32KHz RC oscillator (20KHz-44KHz)
 - Xtal 32KHz oscillator featuring bypass mode
- **Main Clock (MAINCK) sources:**
 - On-chip 4/8/12 MHz RC oscillator (Fast RC)
 - 8/12 MHz calibrated in production
 - Trimming capability
 - Xtal and Ceramic 3-20 MHz oscillator featuring bypass mode
- **PLLA/PLLB Clocks (PLLACK/PLLBCK) sources:**
 - Integrated RC filters
 - One dedicated to USB



SAM4S Power Management Controller (PMC)

Fast RC Trimming

- Possibility to compensate frequency drift due to derating factors such as temperature and voltage by measuring and trimming on the fly the Fast RC frequency
- Oscillator Calibration Register: PMC_OCR

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
SEL12	CAL12						
15	14	13	12	11	10	9	8
SEL8	CAL8						
7	6	5	4	3	2	1	0
SEL4	CAL4						

SEL	CAL
0	Factory Trimmed default calibration value ($\pm 5\%$ for 8/12MHz; $\pm 30\%$ for 4MHz)
1	User Calibration value (reset after each power up) <i>Frequency deviation vs. Trimming code in the Electricals (8/12MHz only)</i>

- Trimming capability on operating oscillator frequency
 - i.e. for example, when running on 8 MHz, it is possible to change the CAL8 value if SEL8 is set in PMC_OCR.

SAM4S Power Management Controller (PMC)

Main Frequency Counter

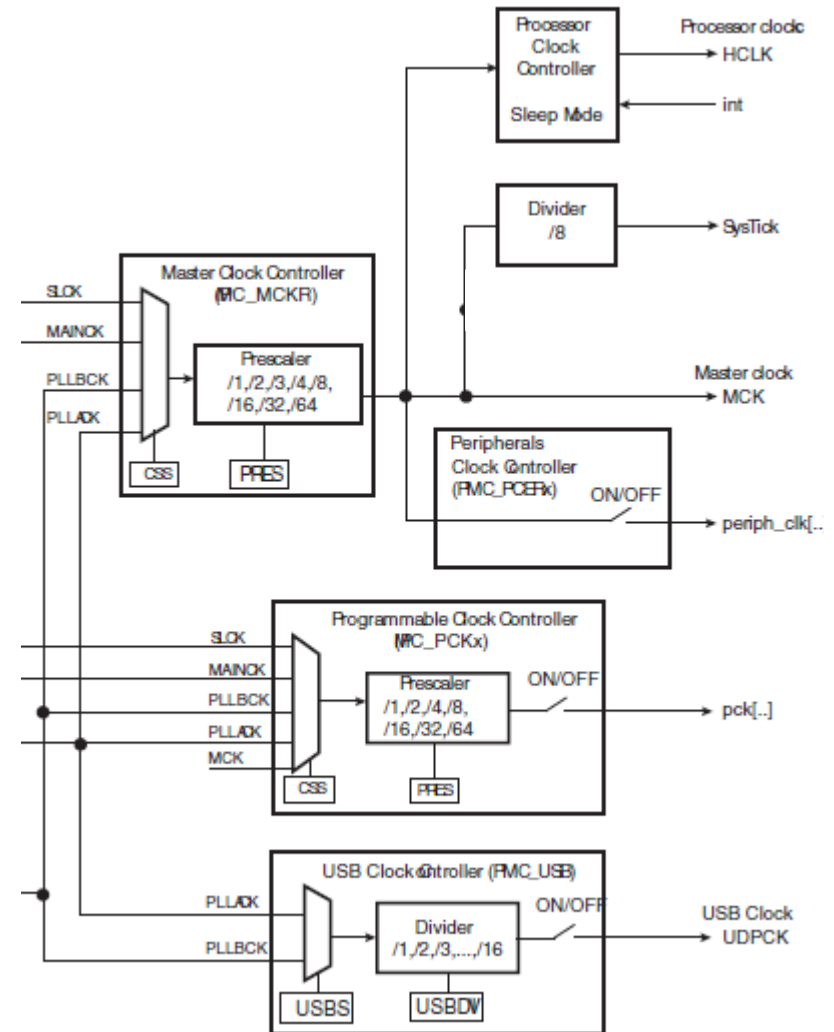
- Provides the frequency of the main clock (MAINCK)
 - Counter is incremented at main clock speed during 16 slow clock cycles
- Used to determine Fast RC, 3/20MHz crystal or ceramic resonator-based oscillator frequency

SAM4S Power Management Controller (PMC)

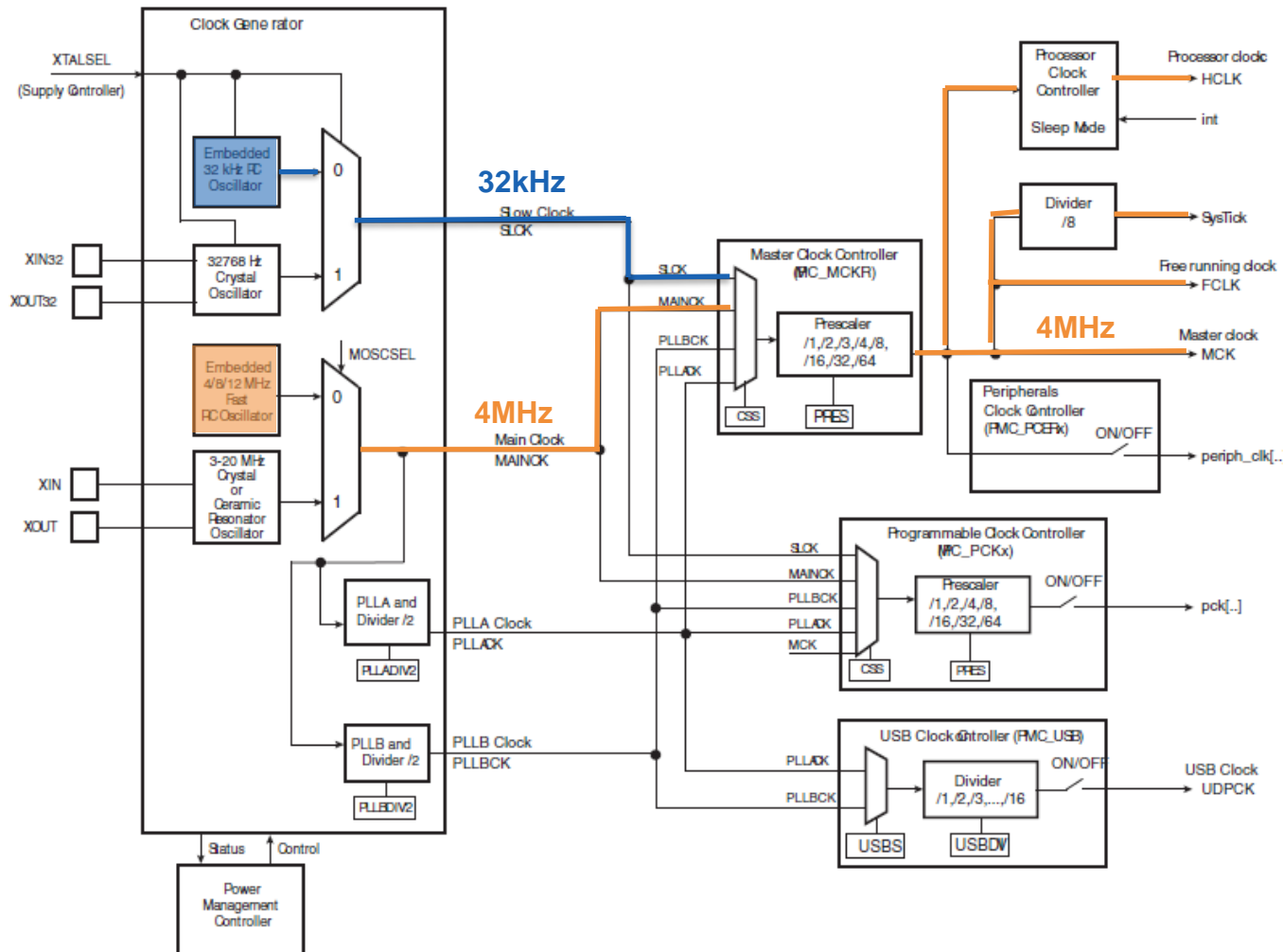
Power Management Controller

- The PMC controls the following clocks:

- HCLK:
 - Processor clock
- MCK:
 - Master clock (Bus Clock)
- Peripheral Clocks
 - USART, SPI Clocks...
- PCKx:
 - Programmable Clock Outputs on PCKx pins
- UDPCK:
 - USB Device clock
- Systick



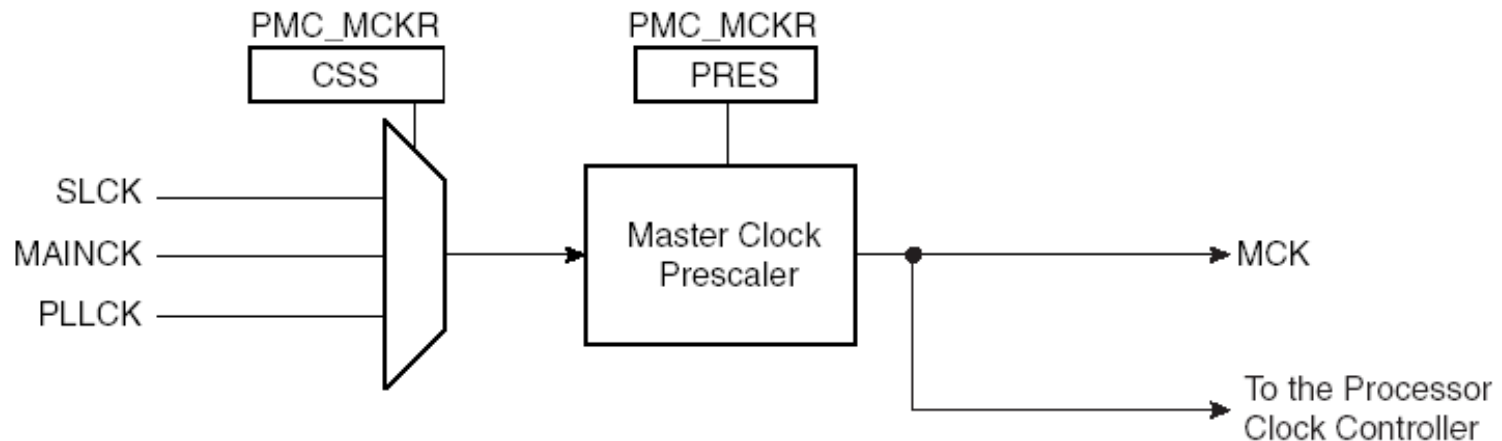
Clocks Startup Configuration



SAM4S Power Management Controller (PMC)

Master Clock Controller (MCK)

- Master Clock Controller Register (PMC_MCKR) provides selection and division of the Master Clock (MCK)
 - CSS selects the clock: SLCK, MAINCK or PLLCK
 - PRES divides the selected clock by 1, 2, 4, 8, 16, 32 or 64



SAM4S Power Management Controller (PMC)

Processor Clock Controller (HCLK)

- HCLK = MCK
- HCLK is automatically:
 - Disabled by entering any low power mode using the Wait for Interrupt instruction (WFI) or Wait for Event (WFE)
 - Re-enabled by any triggered interrupts or by a reset of the product.

SAM4S Power Management Controller (PMC)

Peripheral Clock Controller

- User Peripheral clocks can be individually enabled or disabled:
 - by setting their corresponding bit in the PMC peripheral clock enable/disable register (PMC_PCER/PMC_PCDR)

// Enable all peripheral clocks

AT91C_BASE_PMC->PMC_PCER = 0xFFFFFFFF;

// Disable all peripheral clocks

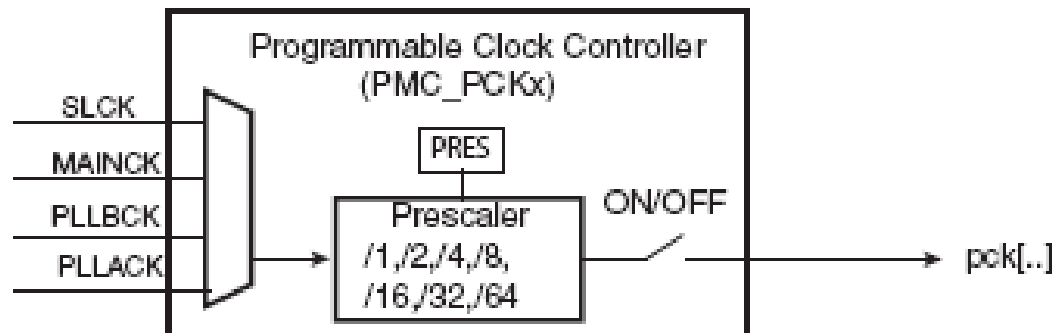
AT91C_BASE_PMC->PMC_PCDR = 0xFFFFFFFF;

- When enabled, the user peripherals are clocked @ MCK.
- Some peripherals are continuously clocked
 - SUPC, RSTC, RTC, RTT, WDT, PMC, EEFC0/1 (peripherals ID #0-#7)
- After reset, peripheral clocks are disabled by default to reduce power consumption

SAM4S Power Management Controller (PMC)

Programmable Clock outputs (PCKx)

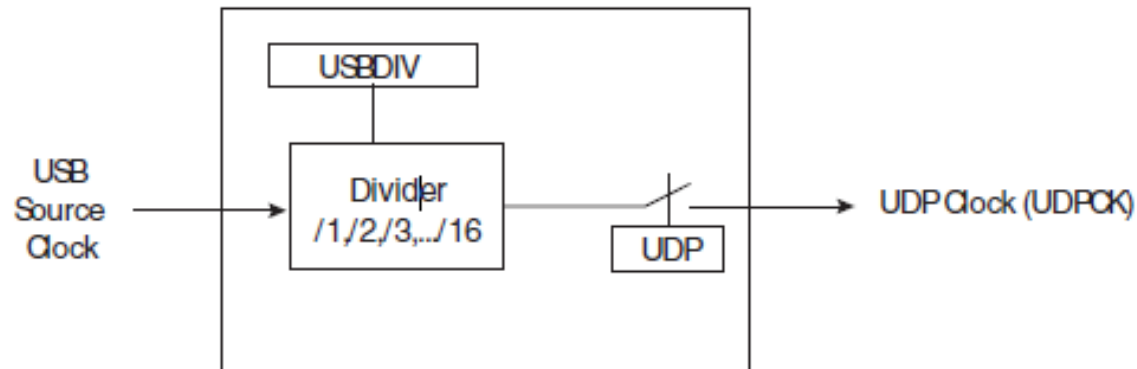
- SAM4S features up to 3 programmable clock outputs
 - PCK0, PCK1 and PCK2 which are multiplexed with I/Os
- Interest is to remove use of external crystals/oscillators.
- Programmable clocks can be enabled or disabled:
 - by setting their corresponding bit in the PMC system clock enable/disable register (PMC_SCER/PMC_SCDR)



SAM4S Power Management Controller (PMC)

USB Device Clock Controller

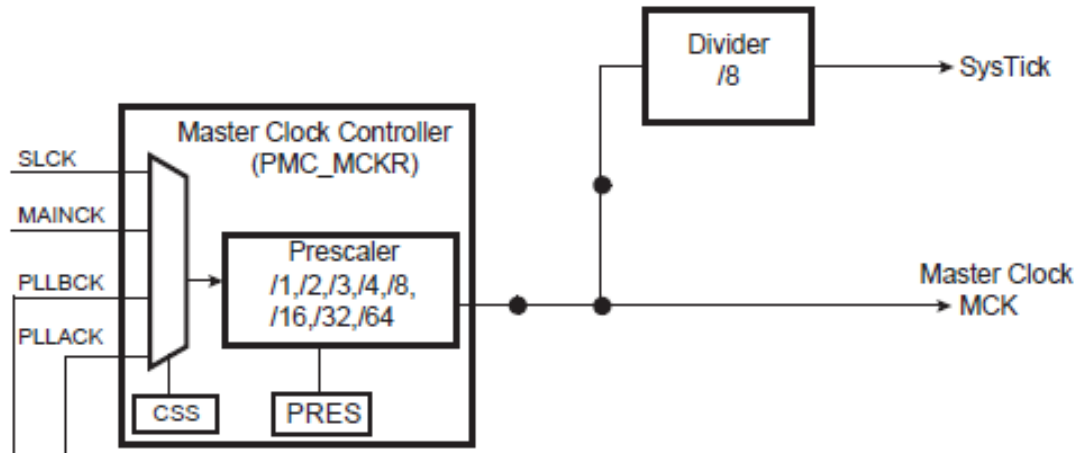
- The user must program one PLL to generate a UDPCK frequency equal to 48MHz.
- UDPCK is the PLL Output (PLLCK) divided by 1,2,... to 16 (USBDIV field)
 - Right divider must be chosen based on PLL Output Frequency range
- User can select either PLLA or PLLB output as USB clock source



SAM4S Power Management Controller (PMC)

Systick

- 24-bit count-down timer embedded in the Cortex-M4
- Divider by 8 embedded in the SAM4S PMC
 - Allows generation of a time base of 1 ms with SysTick clock equal to 1 MHz (ie. when MCK=8MHz).



SAM4S Power Management Controller (PMC)

Main Clock Failure Detector

- Monitors the main crystal oscillator or ceramic resonator-based oscillator to identify an eventual failure.
 - No need for CPU intervention
- Automatically switches the master clock source (MCK) on main clock (MAINCK) with Fast RC as main clock source
 - $MCK = MAINCK = \text{Fast RC}$
- Puts PWM outputs in safe mode
 - A clock failure detection activates a fault output connected to the PWM
 - PWM can force its outputs and protect the driven device



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