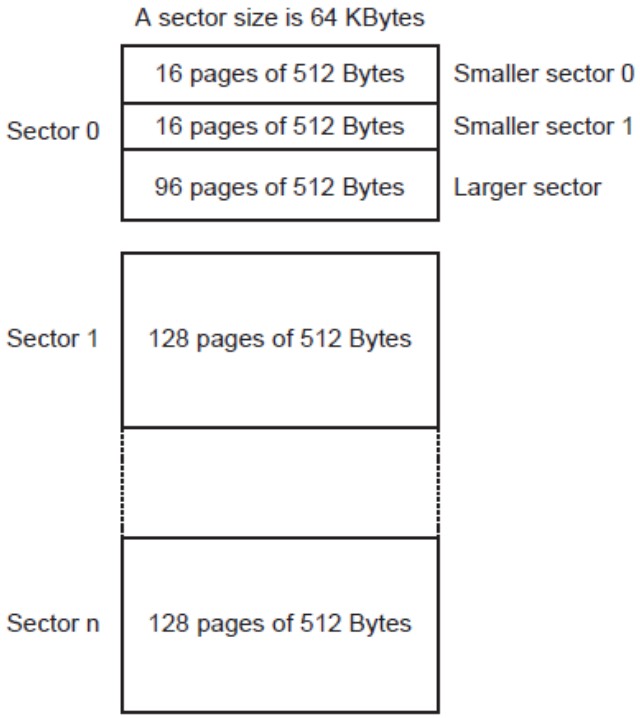
SAM4S Enhanced Embedded Flash Controller (EEFC)

Enhanced Embedded Flash Controller

- The Enhanced Embedded Flash Controller ensures the interface of the Flash block.
- It manages the programming, erasing, locking and unlocking sequences of the Flash using a full set of commands.
- One of the commands returns the embedded Flash descriptor definition that informs the system about the Flash organization, thus making the software generic.

Embedded Flash Organization

- One or two memory planes (banks)
- The memory is organized in sectors:
  - Each sector has a size of 64 Kbytes
  - Each Sector is organized in pages of 512 Bytes.
- First sector (sector 0) is divided into 3 smaller sectors.
  - 2 smaller sectors of 8 kB (16 pages each)
  - 1 smaller sector of 48 kB (96 pages)
- Other sectors are composed by 128 pages of 512 bytes



Flash Speed

- Dual Power Supply Flash: VDDCORE / VDDIO
- The user needs to set the number of wait states depending on the frequency and the power supplies:

Table 43-58. Embedded Flash Wait State VDDCORE Set at 1.2V and VDDIO 1.62V to 3.6V @ 85°C

FWS	Read Operations	Maximum Operating Frequency (MHz)
0	1 cycle	17
1	2 cycles	34
2	3 cycles	52
3	4 cycles	69
4	5 cycles	87
5	6 cycles	104
6	7 cycles	121

Table 42-54. Embedded Flash Wait State VDDCORE set at 1.20V and VDDIO 2.7V to 3.6V @ 85C

FWS	Read Operations	Maximum Operating Frequency (MHz)
0	1 cycle	21
1	2 cycles	42
2	3 cycles	63
3	4 cycles	84
4	5 cycles	105
5	6 cycles	123

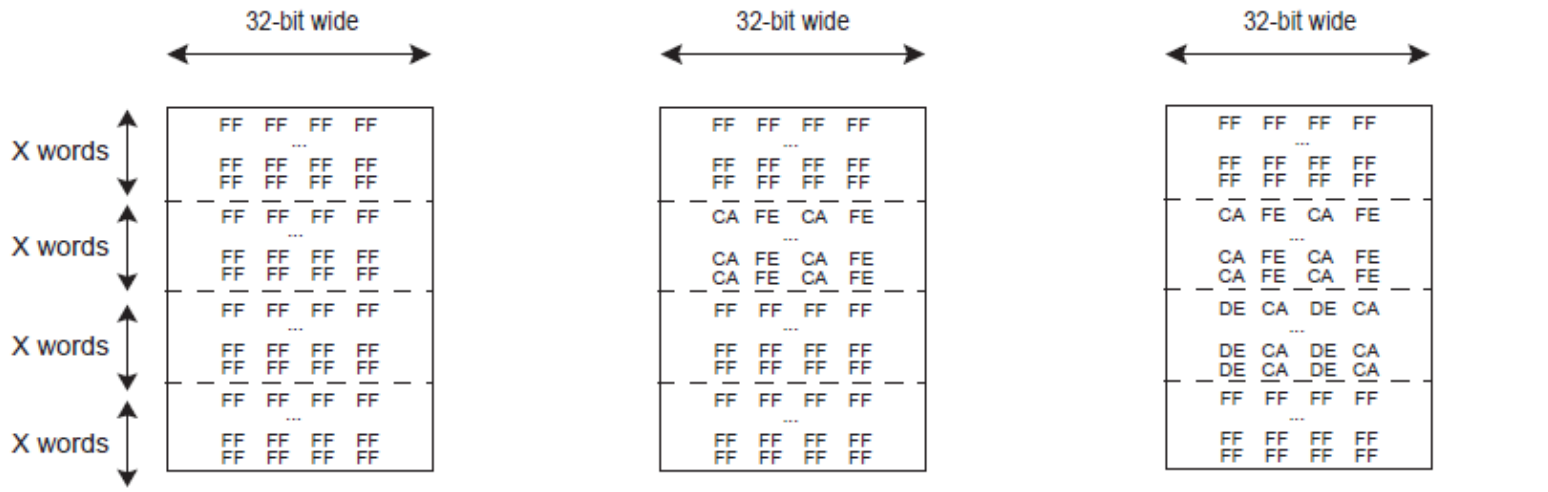
Flash Read Operations

- Flash memory is accessible through 8-, 16- and 32-bit reads.
- By default the read accesses of the Flash are performed through a 64- or 128-bit wide memory interface which enables better system performance especially when 2 or 3 wait state needed.
- **Code Read Optimization**
  - A system of 2 x 128-bit or 2 x 64-bit **prefetch buffers** are added in order to optimize **sequential** Code Fetch
- **Code Loops Optimization**
  - When a jump is inserted in the code, the pipeline of the sequential optimization is broken and becomes inefficient.
  - In this case, the loop code read optimization takes over from the sequential code read optimization to avoid insertion of wait states.
- **Data Read Optimization**
  - One 128-bit (or 64-bit) **data read buffer** to store the requested data plus all the data contained in the 128-bit (64-bit) aligned data to speed up sequential data reads.

Flash Programming

- A page erase can be automatically done before a page write using EWP command

- **Partial Page Programming**:
  - By using the WP command, a page can be programmed in several steps if it has been erased before



Step 1.
Erase All Flash
So Page Y erased

Step 2.
Programming of the second part of Page Y

Step 3.
Programming of the third part of Page Y

Flash Erasing

- Erasing the memory can be performed as follows:
  - On a 512-byte page inside a sector of 8 kB (smaller sectors only)
  - On a 4-Kbyte Block inside a sector
  - On a sector
  - On chip

Flash Protection

- Flash Command Keyword protection
  - All commands are protected by the same keyword (0x5A)
  - If a command is not sent with the keyword, the command is aborted
- Lock bits: Flash Protection from accidental erasing/writing
  - A lock region is composed by several consecutive pages
  - Each lock region has its associated lock bit
  - If an erase or program command occurs on a locked region, the command is aborted.
- Security bit: Flash Protection from JTAG accesses
  - Prevent external accesses to the internal bus system, either through the ICE interface or through the FFPI interface.
  - This bit can be reset only by an external hardware ERASE request to the chip (ERASE pin).
  - Hardware ERASE will erase firstly the flash content then the Security Bit which ensures code confidentiality

General Purpose NVM bits (GPNVM bits)

- Do not interfere with the embedded Flash memory plane(s)
- The SAM4S(D) features up to three GPNVM bits:
  - GPNVM bit 0: Security Bit
  - GPNVM bit 1: Boot Mode selection (ROM or Flash)
  - GPNVM bit 2: Flash Selection (Flash 0 or Flash 1) – **SAM4SD only**

GPNVMBit[#]	Function
0	Security bit
1	Boot mode selection
2	Flash selection (Flash 0 or Flash 1)

- Asserting ERASE pin clears the GPNVM Bits

Flash Commands

- The Enhanced Embedded Flash Controller offers a set of commands

Command	Value	Mnemonic
Get Flash Descriptor	0x00	GETD
Write page	0x01	WP
Write page and lock	0x02	WPL
Erase page and write page	0x03	EWP
Erase page and write page then lock	0x04	EWPL
Erase all	0x05	EA
Erase Pages	0x07	EPA
Set Lock Bit	0x08	SLB
Clear Lock Bit	0x09	CLB
Get Lock Bit	0x0A	GLB
Set GPNVM Bit	0x0B	SGPB
Clear GPNVM Bit	0x0C	CGPB
Get GPNVM Bit	0x0D	GGPB
Start Read Unique Identifier	0x0E	STUI
Stop Read Unique Identifier	0x0F	SPUI
Get CALIB Bit	0x10	GCALB
Erase Sector	0x11	ES
Write User Signature	0x12	WUS
Erase User Signature	0x13	EUS
Start Read User Signature	0x14	STUS
Stop Read User Signature	0x15	SPUS

128 bits Unique Identifier

User Signature of 512-bytes