



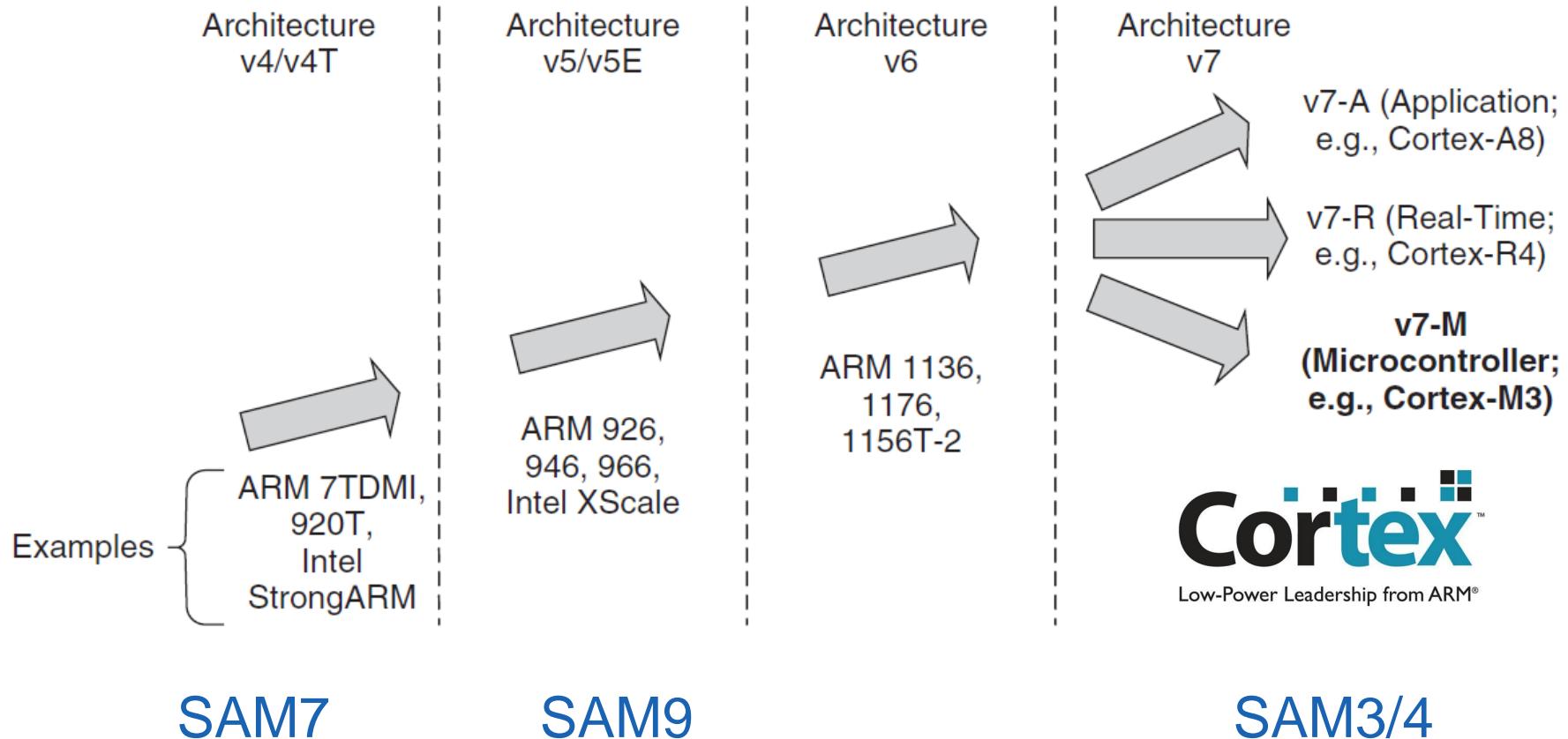
Atmel SAM3/SAM4 Flash MCU

Technical Overview

Quick Introduction to Cortex-M3 & Cortex-M4



Evolution of ARM Processor Architecture

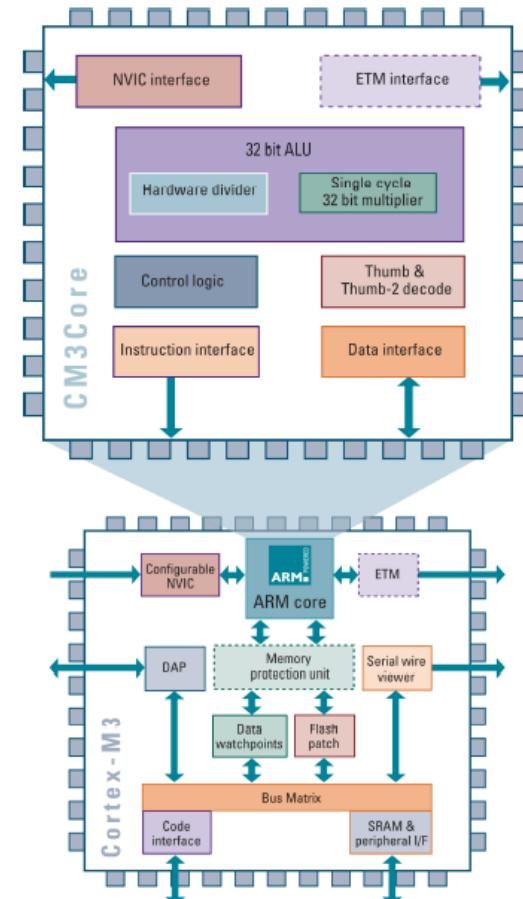


ARM Cortex Family

- Architecture version v7 is divided into three profiles:
 - A profile, designed for high-performance application platforms
 - R profile, designed for high-end embedded systems in which real-time performance is needed
 - M profile, designed for deeply embedded microcontroller-type systems
- Cortex-M3 is the first ARM processor based on the ARMv7-M architecture
 - Designed to achieve high system performance in power and cost-sensitive embedded applications such as microcontrollers

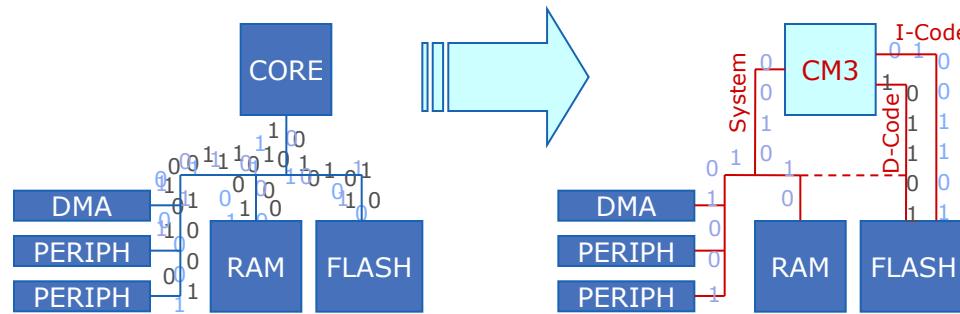
Cortex-M3 Processor Overview

- Hierarchical processor integrating core and advanced system peripherals
- Cortex-M3 core
 - Harvard architecture
 - 3-stage pipeline w. branch speculation
 - Thumb®-2 and traditional Thumb
 - ALU w. H/W divide and single cycle multiply
- Cortex-M3 processor
 - Configurable interrupt controller
 - Bus matrix
 - Advanced debug components
 - Optional MPU & ETM



System Architecture Benefits

- Harvard architecture
 - Separate buses for instructions and data speeding application execution



- Thumb-2 Instruction Set Architecture
 - Blend of 16 and 32-bit instructions that delivers significant benefits in terms of ease of use, code size and performance
- 3-stage pipeline + branch speculation
 - When a branch instruction is encountered, the decode stage also includes a speculative instruction fetch

Other Benefits

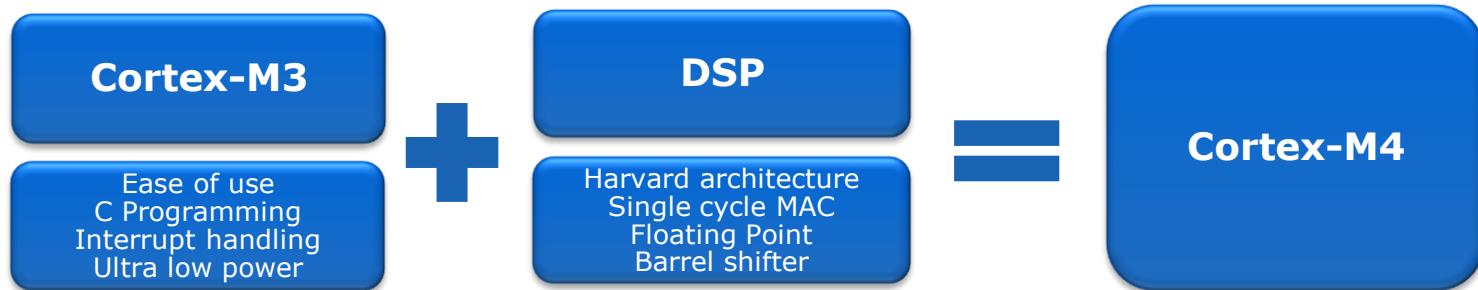
- Complete hardware support for interrupts for low latency interrupt handling (NVIC Controller)
 - Interrupt Service Routines (ISRs) are purely written in C
- Advanced ALU with support for hardware multiply and divide
 - Single cycle 32-bit Multiply
- Integrated atomic bit manipulation for improved data storage
- Reduced pin debug & Trace interfaces
 - Serial Wire Interface (SWI) (2 pins) in addition to JTAG (5 pins)
- Embedded sleep control and power-down modes
- Optional MPU & ETM
 - MPU: support up to 8 regions with different protection rules

SAM3 Series Cortex-M3 Implementation

	SAM3U	SAM3S	SAM3N	SAM3X/A
Revision	r2p0	r2p0	r2p0	r2p0
MPU	Yes	Yes	No	Yes
IRQ#	30	30	34	30
IRQ Priority Level	16	16	16	16
Debug Level	3	3	3	3
Trace Level	1	1	1	1

Why Cortex-M4?

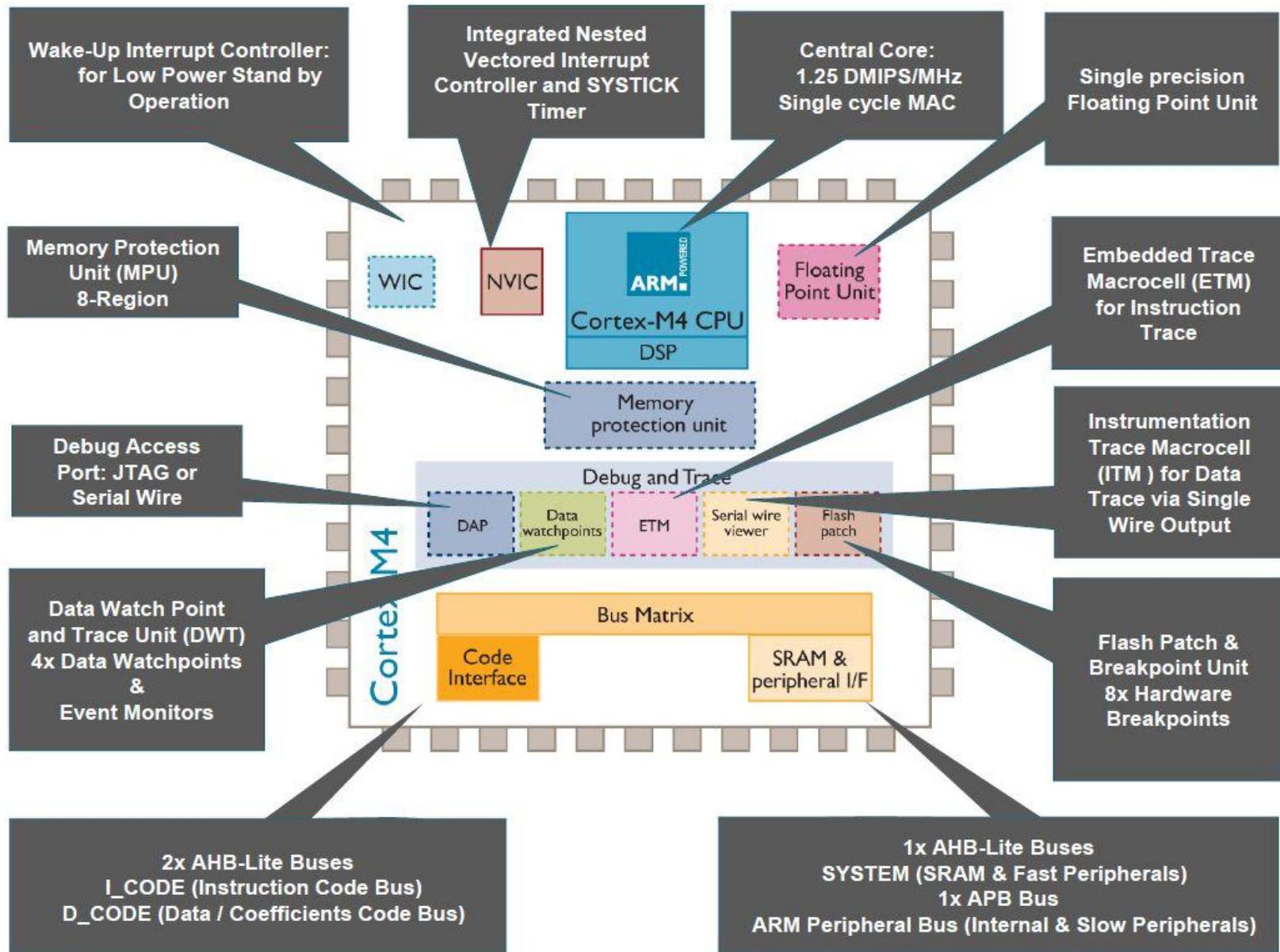
- Designed for applications requiring more computational performance
- Cortex-M4 frees CPU resources in case digital signal processing task are used (less active cycles are needed)
- Cortex M4 features:
 - A single-cycle multiply-accumulate unit (MAC)
 - Optimized single instruction multiple data (SIMD) instructions, saturating arithmetic instructions
 - Optional single precision Floating-Point Unit (FPU)



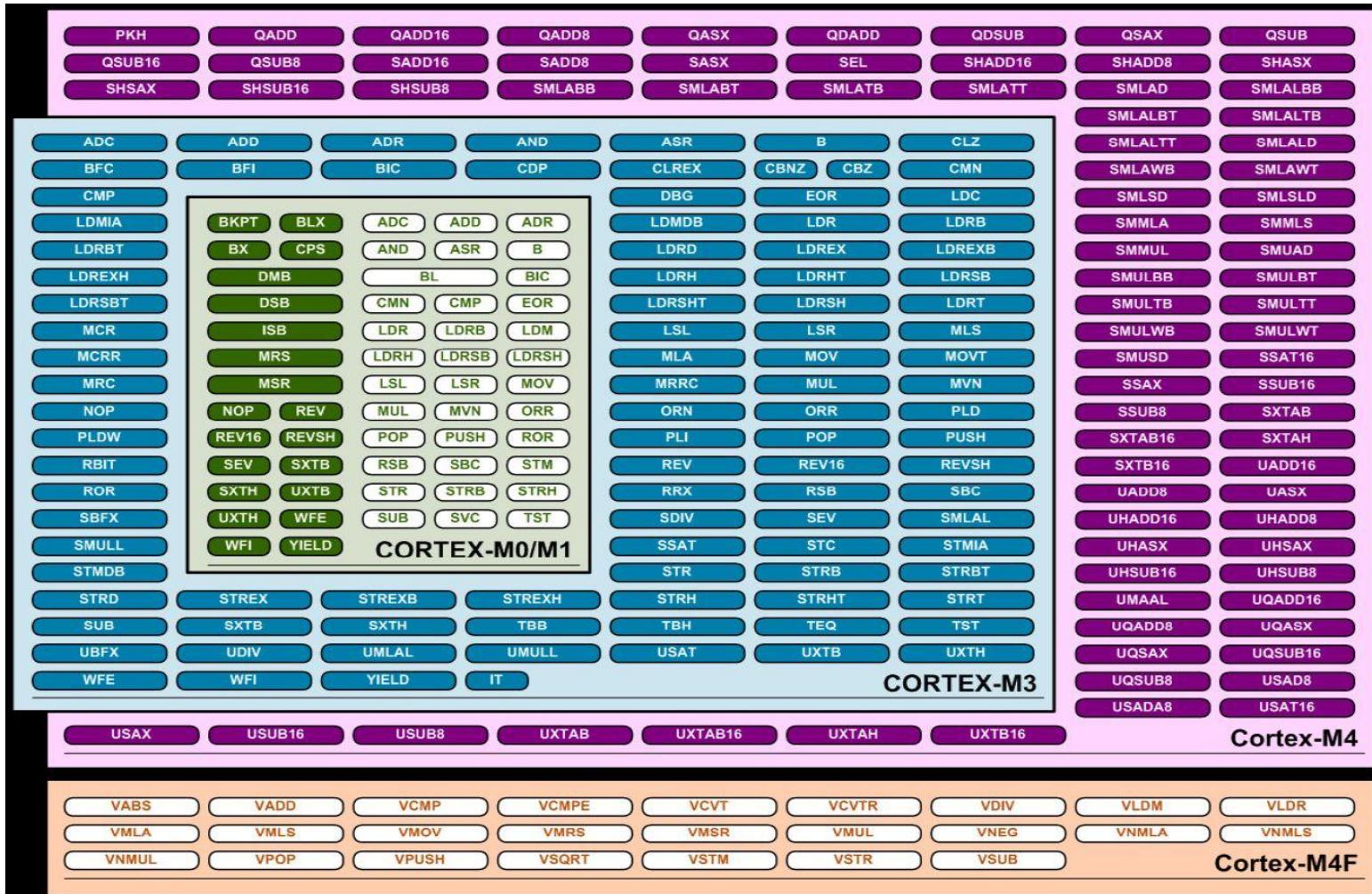
Cortex-M4 vs. Cortex-M3

	Cortex-M3	Cortex-M4
Architecture	ARMv7-M (Harvard)	ARMv7-M (Harvard)
ISA Support	Thumb / Thumb-2	Thumb / Thumb-2
DSP Extensions	NA	Single cycle 16, 32-bit MAC Single cycle dual 16-bit MAC 8, 16-bit SIMD arithmetic Hardware Divide (2-12 cycles)
Optional Floating Point Unit	NA	Single precision floating point unit IEEE 754 compliant
Pipeline	3-stage + branch speculation	3-stage + branch speculation
Interrupts	NMI + 1 to 240 interrupts	NMI + 1 to 240 interrupts
Interrupt Latency	12 cycles (6 when Tail Chaining)	12 cycles (6 when Tail Chaining)
Sleep Modes	Integrated (3)	Integrated (3)
Memory Protection	8 regions MPU	8 regions MPU
Dhrystone	1.25DMIPS/MHz	1.25DMIPS/MHz

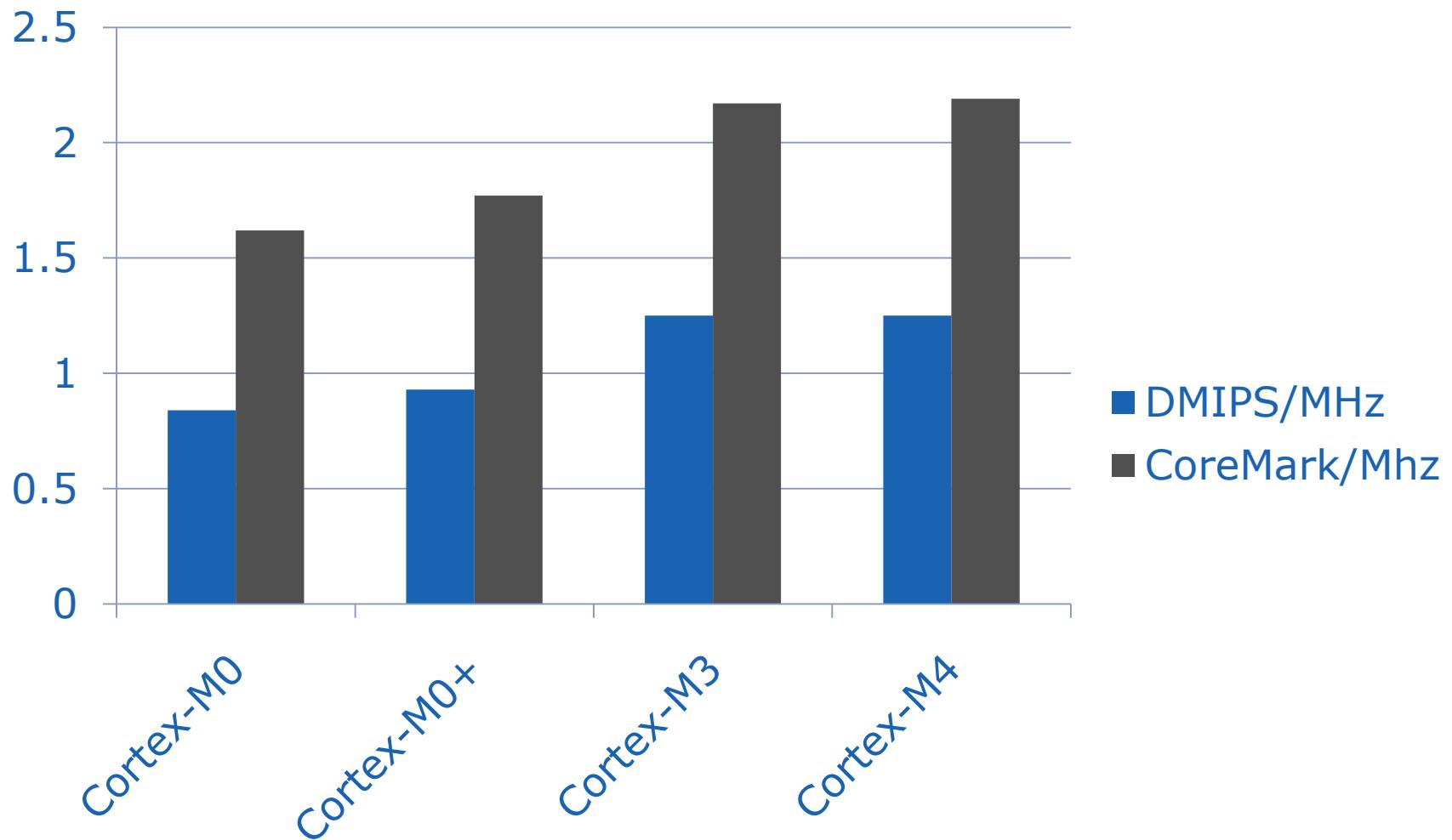
Cortex-M4 Processor Overview



Cortex-M4 Instruction Set



Performance Efficiency



Single Cycle Multiply Accumulate Instructions

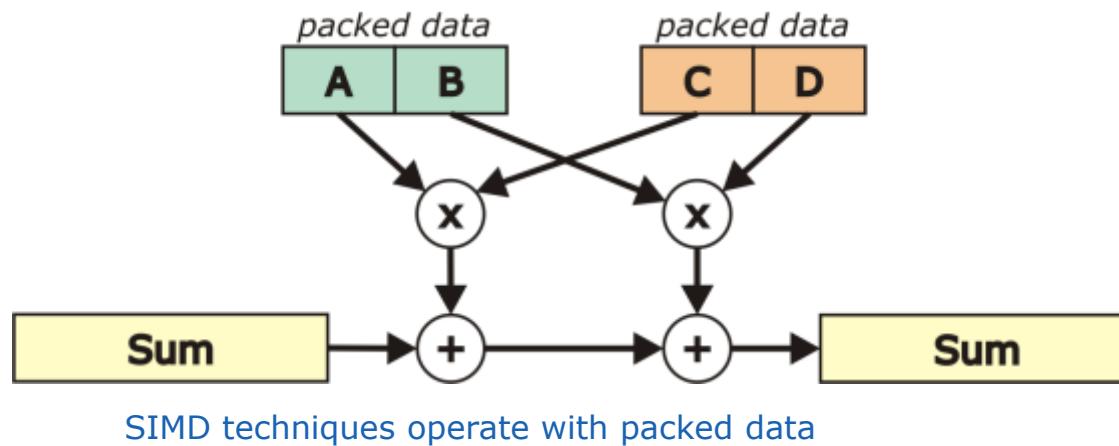
- Cortex-M4 features 32-bit hardware multiply-accumulate (MAC) unit
 - Makes digital signal processing more efficient and greatly reduces the consumption of CPU resources
 - Capable of accomplishing an operation of up to $32 \times 32 + 64 -> 64$ or two operations of 16×16 in a single cycle
- Main features:
 - Wide range of multiply-accumulate instructions
 - Choice of 16 or 32 bit multiply and 32 or 64 bit accumulate
 - All instructions execute in a single cycle

MAC Instructions

OPERATION	INSTRUCTION
$16 \times 16 = 32$	SMULBB, SMULBT, SMULTB, SMULTT
$16 \times 16 + 32 = 32$	SMLABB, SMLABT, SMLATB, SMLATT
$16 \times 16 + 64 = 64$	SMLALBB, SMLALBT, SMLALTB, SMLALTT
$16 \times 32 = 32$	SMULWB, SMULWT
$(16 \times 32) + 32 = 32$	SMLAWB, SMLAWT
$(16 \times 16) \pm (16 \times 16) = 32$	SMUAD, SMUADX, SMUSD, SMUSDX
$(16 \times 16) \pm (16 \times 16) + 32 = 32$	SMLAD, SMLADX, SMLSD, SMLSX
$(16 \times 16) \pm (16 \times 16) + 64 = 64$	SMLALD, SMLALDX, SMLSX, SMLSX
$32 \times 32 = 32$	MUL
$32 \pm (32 \times 32) = 32$	MLA, MLS
$32 \times 32 = 64$	SMULL, UMULL
$(32 \times 32) + 64 = 64$	SMLAL, UMLAL
$(32 \times 32) + 32 + 32 = 64$	UMAAL
$32 \pm (32 \times 32) = 32$ (upper)	SMMLA, SMMLAR, SMMLS, SMMLSR
$(32 \times 32) = 32$ (upper)	SMMUL, SMMULR

Single Instruction Multiple Data (SIMD)

- Several instructions operate on “packed” data types
 - Byte or halfword quantities packed into words
 - Allows more efficient access to packed structure types
 - SIMD instructions can act on packed data:
 - Quad (4 parallel) 8-bit adds or subtracts
 - Dual (2 parallel) 16-bit adds or subtracts
 - All instructions execute in a single cycle
- SIMD extensions perform multiple operations in one cycle
$$\text{Sum} = \text{Sum} + (\mathbf{A} \times \mathbf{C}) + (\mathbf{B} \times \mathbf{D})$$



Typical DSP Algorithms

- **DSP operations – MAC is key operation**
 - Most operations are dominated by MACs
 - These can be on 8, 16 or 32 bit operations
- FIR Filters
 - Data communications
 - Echo cancellation (adaptive versions)
 - Smoothing data
- IIR filters
 - Audio equalization
 - Motor control
- FFT
 - Audio compression
 - Spread spectrum communication
 - Noise removal

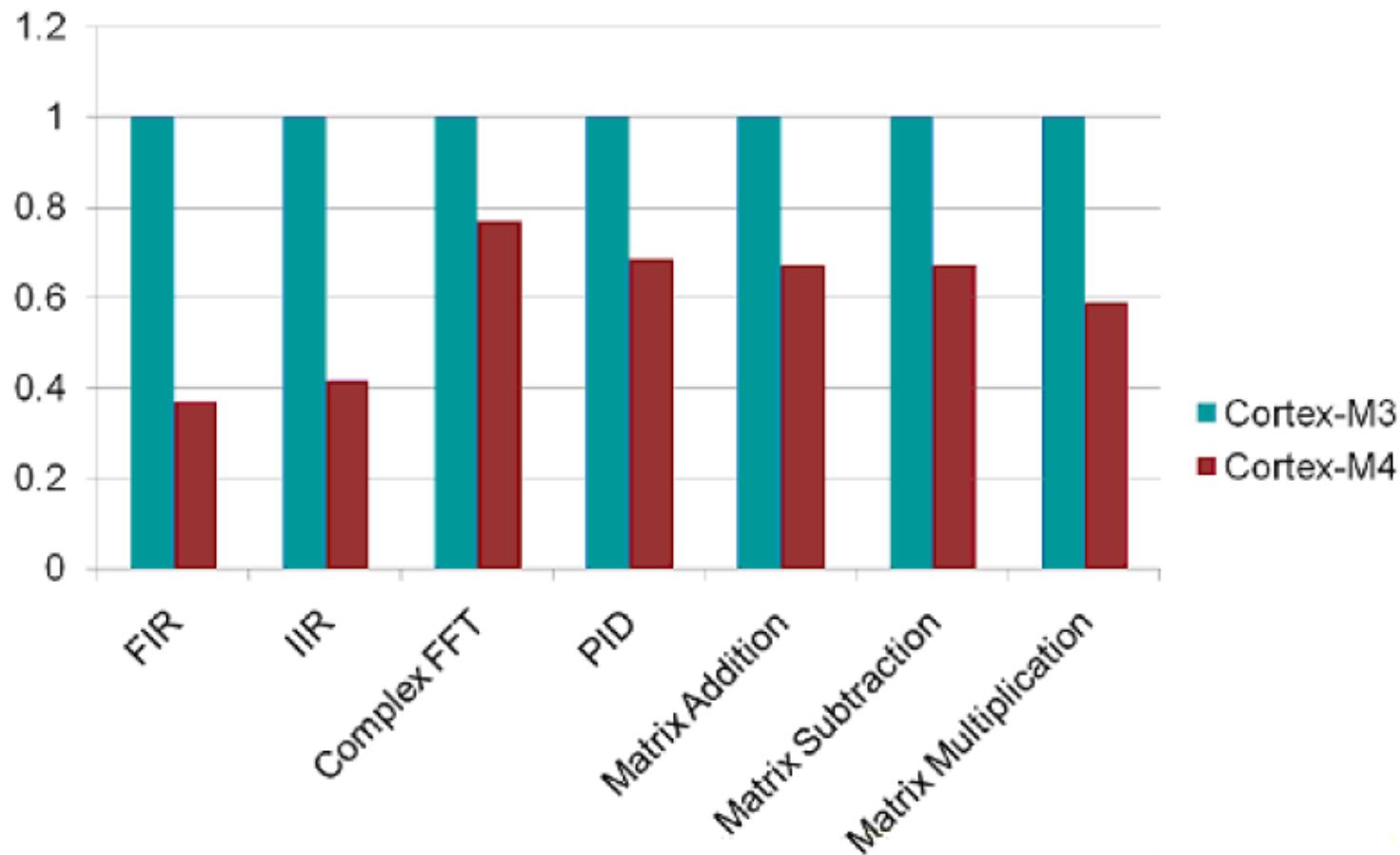
$$y[n] = \sum_{k=0}^{N-1} h[k]x[n-k]$$

$$\begin{aligned}y[n] = & b_0x[n] + b_1x[n-1] + b_2x[n-2] \\& + a_1y[n-1] + a_2y[n-2]\end{aligned}$$

$$\begin{aligned}Y[k_1] &= X[k_1] + X[k_2]e^{-j\omega} \\Y[k_2] &= X[k_1] - X[k_2]e^{-j\omega}\end{aligned}$$

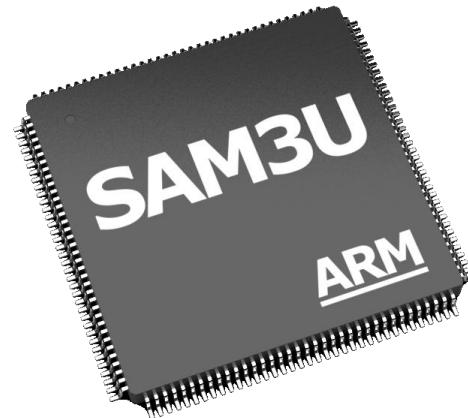
Digital Signal Processing Performance

Relative cycle count



SAM3U Series

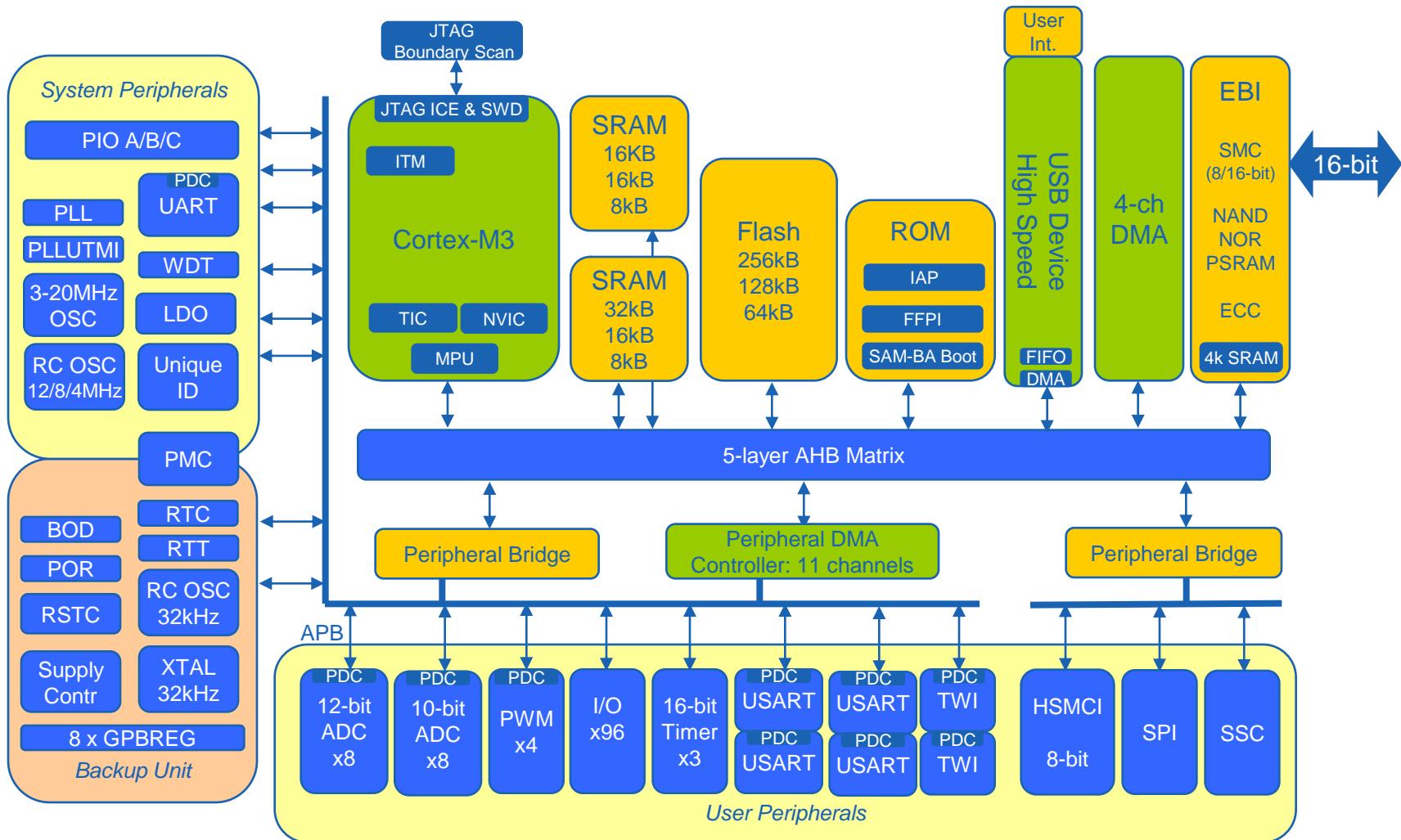
First Cortex-M3 Flash
Microcontroller with High-speed
USB and embedded Phy



SAM3U – Benefits

- High-speed Bridging
 - Sustains 100Mbps+ data rates between multiple high-speed peripherals including High-speed USB 2.0, SDIO/SDCard 2.0, MMC 4.3 and EBI
- High performance
 - A 96MHz max frequency allows designers to build more feature-rich applications
- Market's lowest operating voltage at 1.62V
 - Extended operation time when running from batteries
- First Cortex-M3 MCU with Dual-bank Flash with boot bank select
 - Secure self-programming including the boot program
- High-end 12-bit 1Msps Analog-to-Digital Converter
 - On-chip Programmable Gain Amplifier and differential input support reduces external component count and real estate
- Better code protection
 - Hardware security, including external memory scrambling and unique 128-bit ID

SAM3U Series

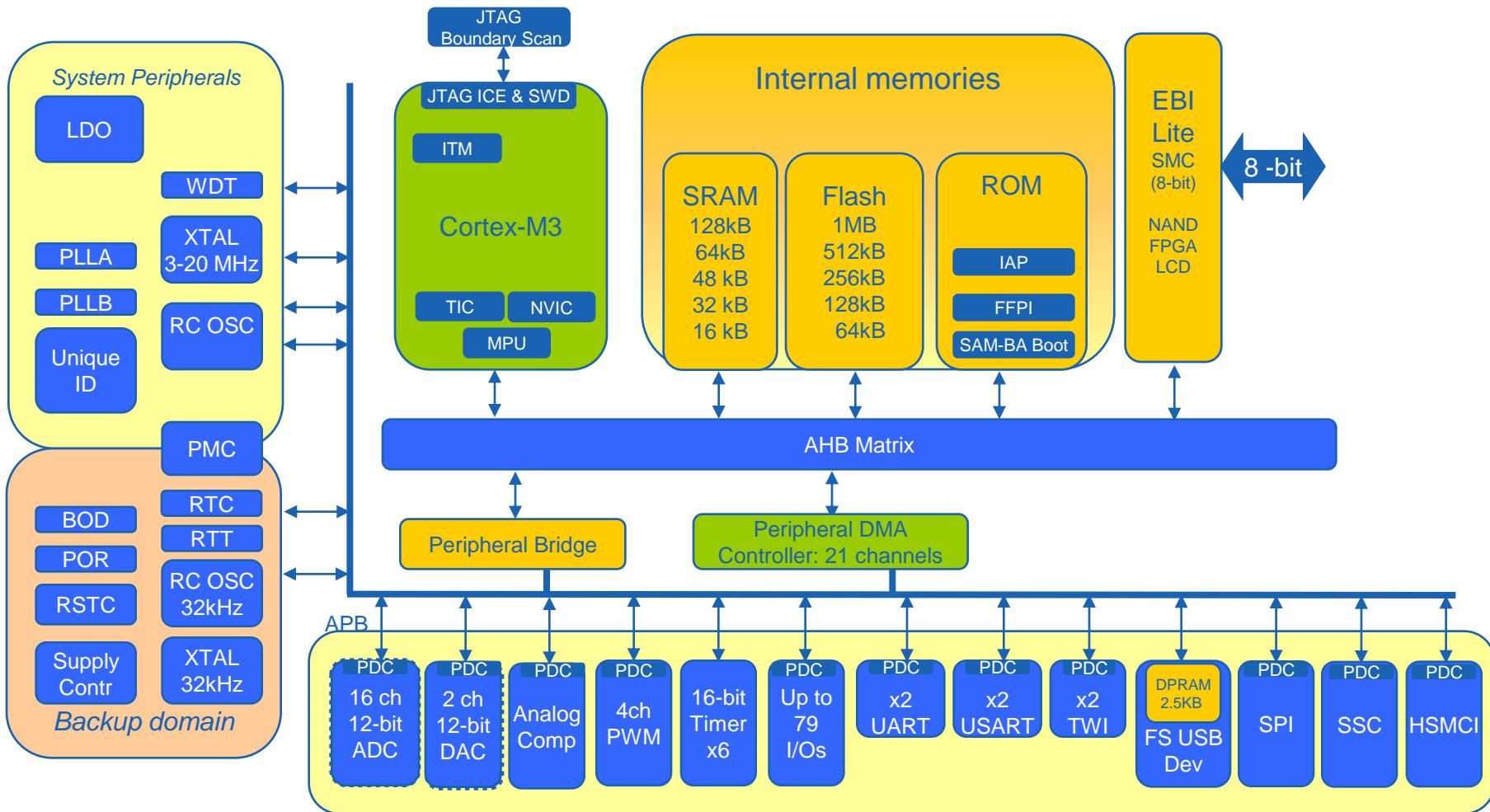


SAM3S Series

Highly-integrated Cortex-M3 Flash MCUs



SAM3S Series



System Architecture

- Cortex-M3 vs ARM7TDMI
 - 1.25DMIPS/MHz versus 0.9DMIPS/MHz,
 - NVIC reducing interrupt latency,
 - Thumb-2 instruction set for better performance and code density,
- AHB/APB AMBA Architecture
 - 4-layer matrix maximizing system bandwidth.
- 100MHz maximum frequency.
- 128-bit wide Flash access,
 - Ensuring single clock cycle execution for sequential accesses at maximum speed with 2 wait states,
 - Unique-ID – 128-bit factory programmed.
- Two on-chip PLLs,
 - Allowing CPU maximum frequency at 100MHz when using USB.

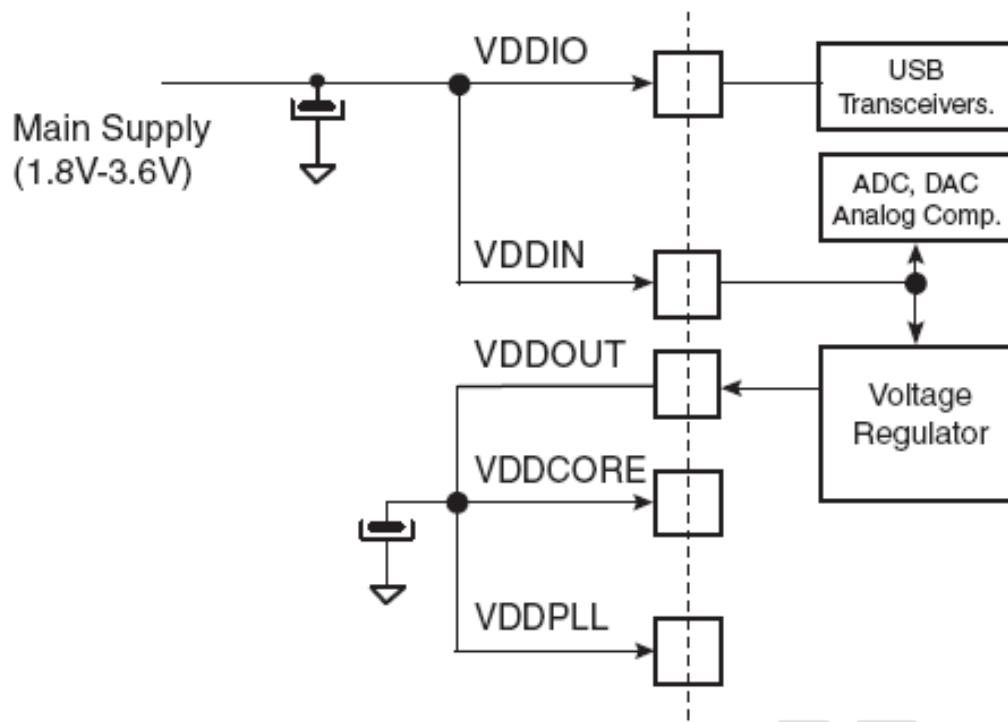
System Control

- NRST pin is configured as an input pin by default allowing to control the reset line externally at first power-up.
- BOD on VDDCORE is enabled by default.
- POR on VDDIO.
- Supply monitor on VDDIO,
 - Programmable threshold from 1.9V to 3.4V by steps of 100mV,
 - Continuous or periodic sampling modes available,
 - Can generate a reset of the core or an interrupt.
- Main oscillator clock failure detection,
 - Automatically switch to on-chip 4/8/12MHz RC.

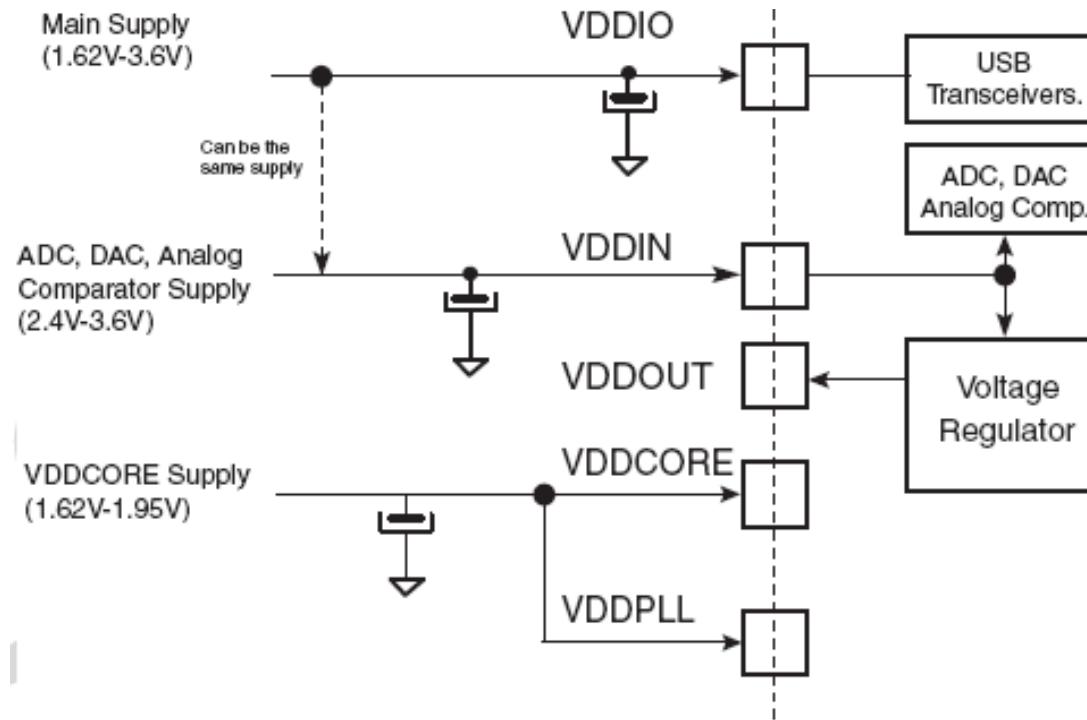
System Clock Sources

- Slow Clock – SLCK
 - On-chip 32KHz RC oscillator (20KHz-44KHz)
 - Xtal 32KHz oscillator featuring bypass mode
 - Selection is made through XTALSEL bit in SUPC_CR
- Main Clock – MAINCK
 - On-chip 4/8/12 MHz RC oscillator
 - 8 and 12 MHz calibrated in production
 - +/-5% in worst case conditions
 - Xtal and Ceramic 3-20 MHz oscillator featuring bypass mode
- PLLA/PLLB Clock – PLLACK PLLBCK
 - Input frequency: 3.5-20 MHz
 - Output frequency: 60 to 130 MHz
 - Integrated RC filter

Single Power Supply Scenario



Dual Power Supply Scenario

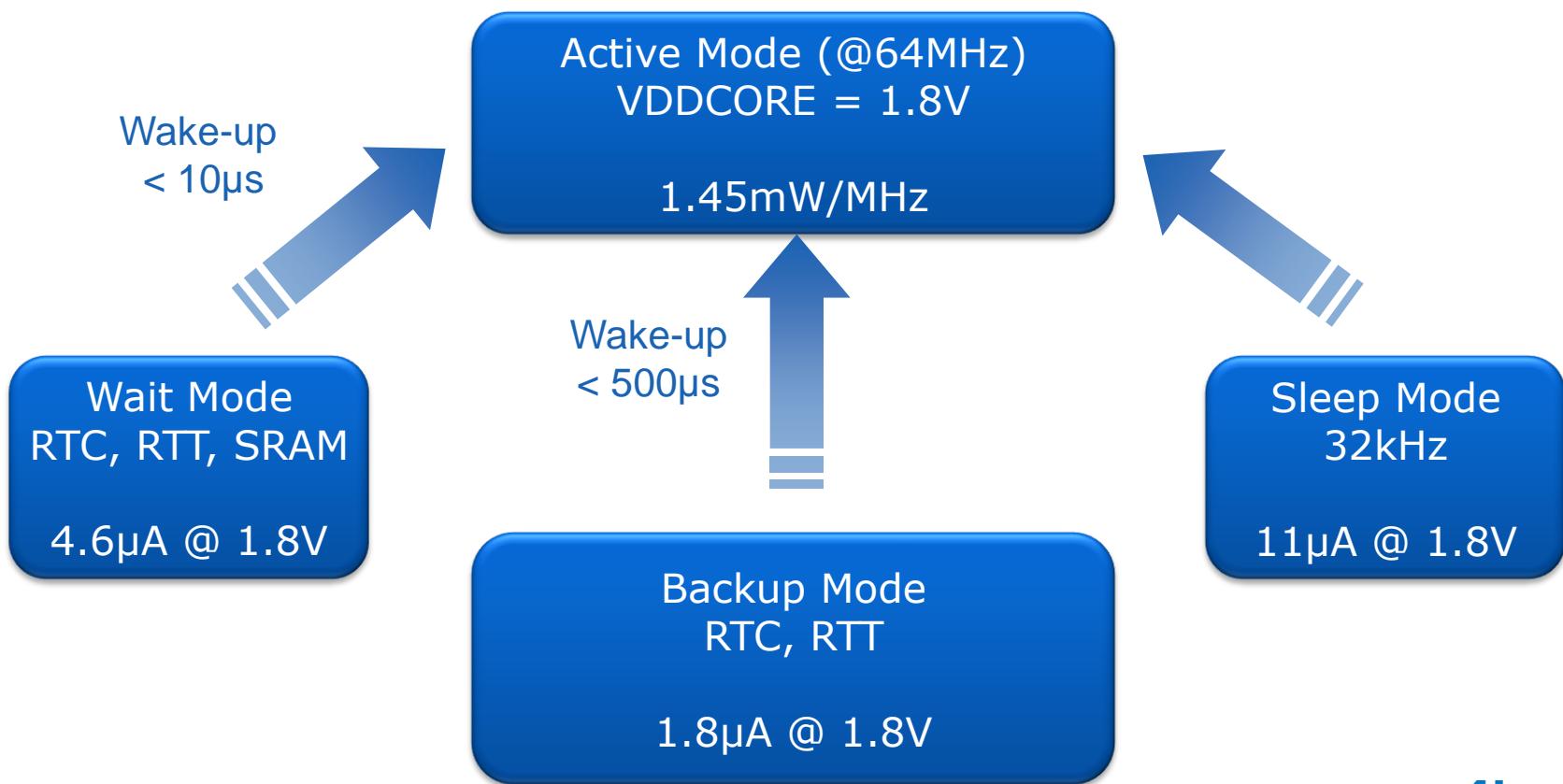


Advanced Power Management

- Operating voltage down to 1.62V.
- New low power modes including Wait mode ensuring 10 μ s wake-up time and backup mode with sub 3 μ A power consumption,
- Better power figures versus SAM7S up to 1MHz because the sense amplifiers of the Flash are automatically put to sleep after completion of the read cycle.
- A self-adapting regulator scales current consumption as a function of current draw without any software handling.
- Voltage regulator <1 μ A backup mode.

Extended Supply Range and Low Power

- 1.62V to 3.6V extended supply range
 - True $1.8V \pm 10\%$ operation
 - Lowest Cortex-M3 MCU operating supply voltage at 1.62V



Low Power Modes Summary Table

	Backup	Wait	Sleep
SUPC, 32kHz, POR, Backup registers, RTC, RTT	ON	ON	ON
Regulator	OFF	ON	ON
Core Memories Peripherals	OFF (not powered)	Powered (but not clocked)	Powered (but not clocked)
Mode entry	WFE+SLEEPDEEPbit = 1	WFE+SLEEPDEEPbit = 0 +LPM bit =1	WFI+SLEEPDEEPbit = 0 +LPM bit =0
Potential wake-up sources	WUP0-15 pins BOD alarm RTC alarm RTT alarm	Fast start-up through WUP0-15 pins RTC alarm RTT alarm USB wake-up	Any Interrupt (with WFI) WUP0-15 pins RTC alarm RTT alarm USB wake-up
Core at wake-up	Reset	Clocked back	Clocked back
PIO state while in low power mode	Previous state saved	Previous state saved	Previous state saved
PIO state at wake-up	Input with pull-up	Unchanged	Unchanged
Consumption	2.5 μ A typical	15 μ A typical)	17 μ A typical at 500 Hz
Wake-up time	200 μ s typical	<10 μ s	Depends on Clock



Improving Signal Integrity & PCB Design

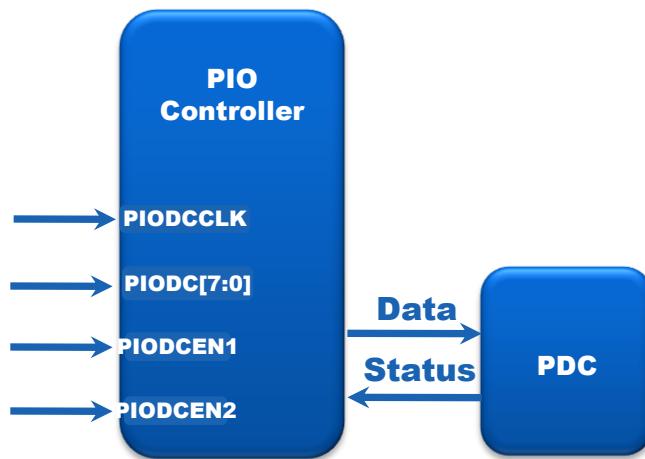
- On-Die Termination
 - 36 ohms embedded termination resistors.
- On-chip PLL filters.
- Integrated Pull-up on USB DDP signal and pull-down on USB DDM and DDP signals.
- Programmable pull-up and pull-down resistors on I/Os.

Parallel Input/Output Controller (PIO)

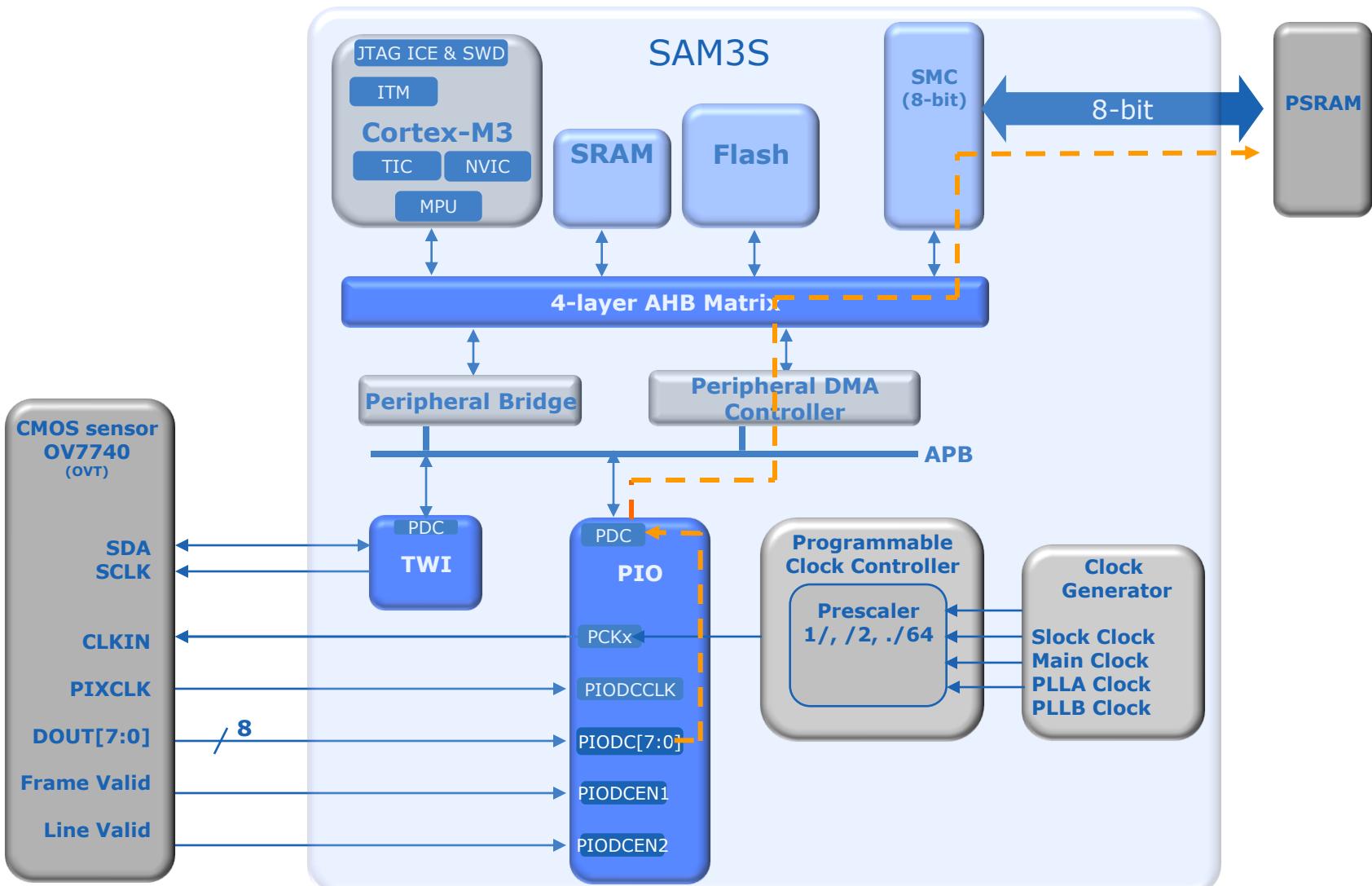
- Programmable pull-up and pull-down resistor (100K)
- Programmable Schmitt Trigger
- Programmable Filtering/Debouncing
- On-Die Termination (ODT)
- Input Edge/Level Interrupt
- 8-bit Parallel Capture Mode with PDC support
- Extended multiplexing
 - System I/Os are now multiplexed; TDI, TDO, TMS, TCK, ERASE, DDM, DDP, XIN and XOUT.
 - Analog I/Os AD4 to AD7 are also multiplexed.

PIO Parallel Capture Mode

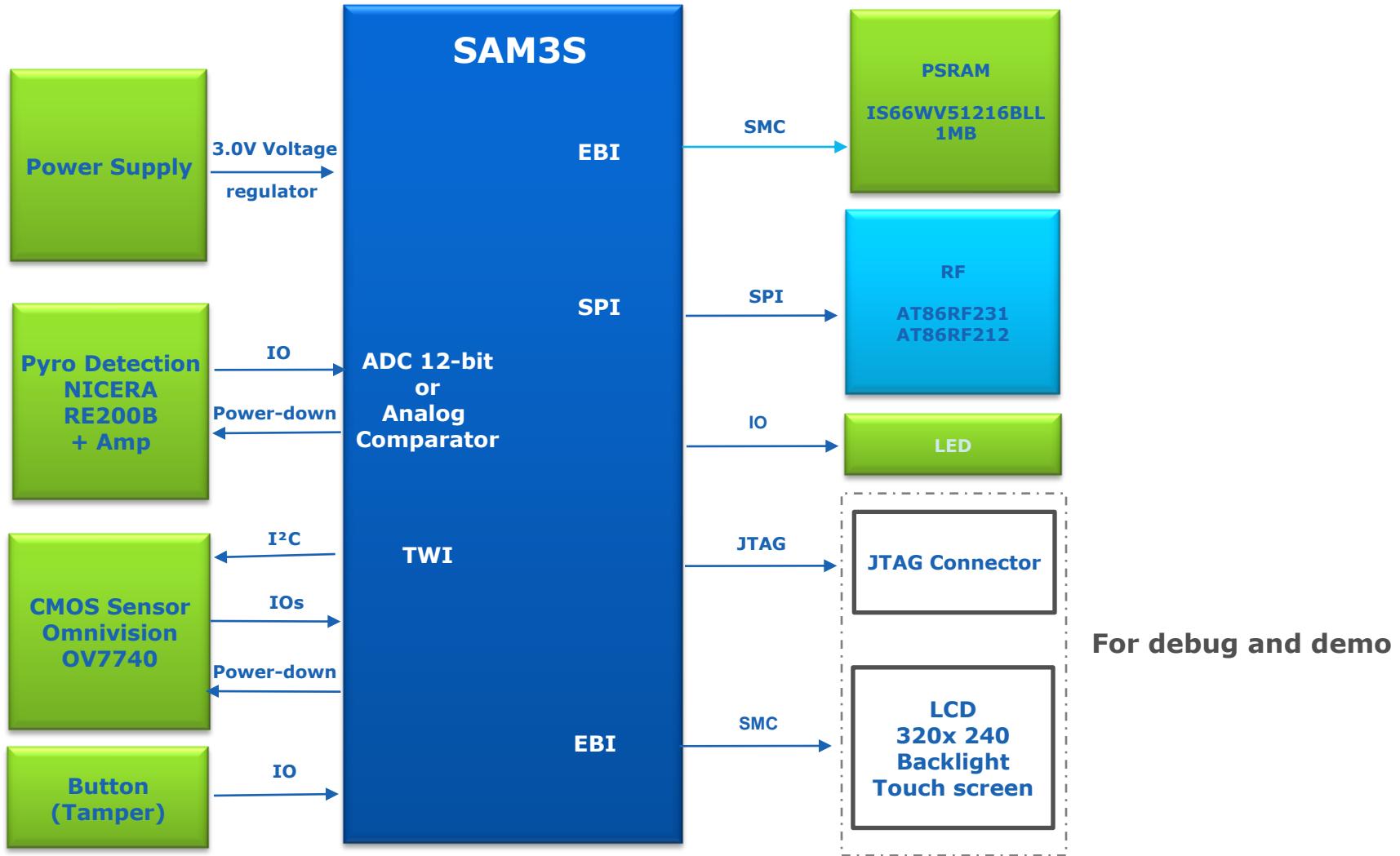
- Capture data from a CMOS digital CMOS image sensor, a high speed parallel ADC, a DSP synchronous port.
- Can be linked to a receiver PDC channel to transfer data without CPU intervention,
 - Byte / Half-word / Word Transfer,
 - Up to MCK/4 data rate in Always sampling mode and MCK/3 in half sampling mode.



Parallel Capture Mode Example



PIR Reference Design Block Diagram

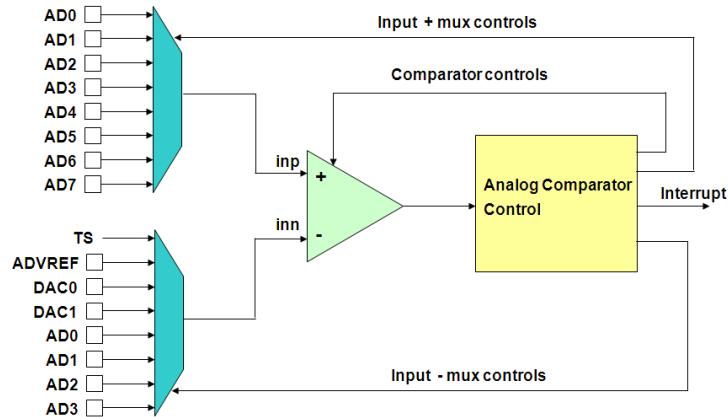


Timers

- Real Time Clock (RTC)
 - Complete time-of-day clock and two hundred year calendar.
- Real Time Timer (RTT)
- PWM Controller
 - Designed for motor control support.
- Timer/counter
 - Quadrature decoder logic,
 - 2-bit gray up/down counter to generate a 2-bit gray count waveform for stepper motor.

Analog Peripherals

- Analog comparator
 - 16 Selectable inputs,
 - Configurable hysteresis, edge detection and polarity,
 - High-speed or low-power options for settling time and consumption trade-off,
 - Can generate interrupt or PWM fault event.
- ADC
 - 12-bit ADC, 1Msps instead of 384Ksps,
 - 2-bit programmable gain, differential mode and temperature sensor.
- 2-channel 12-bit DAC
 - Up to 2MHz Conversion Rate with 50MHz
 - Multiple trigger sources: Free running, PWM event line, Timer output or external trigger
 - PDC support



Serial Communication Improvements

- UDP
 - 8 USB endpoints with maximum endpoint size up to 512 bytes.
- USART
 - Supports SPI and Manchester modes.
- TWI
 - Supports Slave and Multi Master modes with PDC.
- SPI
 - Improved I/Os characteristics for 48Mbps maximum data rate.

External Memory Interfaces

- External Bus Interface (100-pin version only)
 - 8-bit data bus, 4 chip select lines (16MB per CS lines), 24-bit address lines,
 - Off-Chip Memory Scrambling/Unscrambling capability
 - Interfacing Capabilities:
 - NOR Flash, SLC NAND Flash, LBA-NANDTM (MLC NAND + ECC + Bad Block Mgt), Static Asynchronous RAM, PSRAM, External LCD controller, External Ethernet Controller or any Memory Mapped Peripherals.



- High Speed MCI
 - Compliant with Multimedia Card Specification 4.3; 1-bit/4-bit.
 - Compliant with SD Memory Card Specification 2.0; 1-bit/4-bit.
 - Compliant with SDIO Specification 2.0; 1-bit/4-bit.
 - Compliant with CE-ATA Specification 1.1.
 - 32Mbps maximum data rate.

Other Peripherals

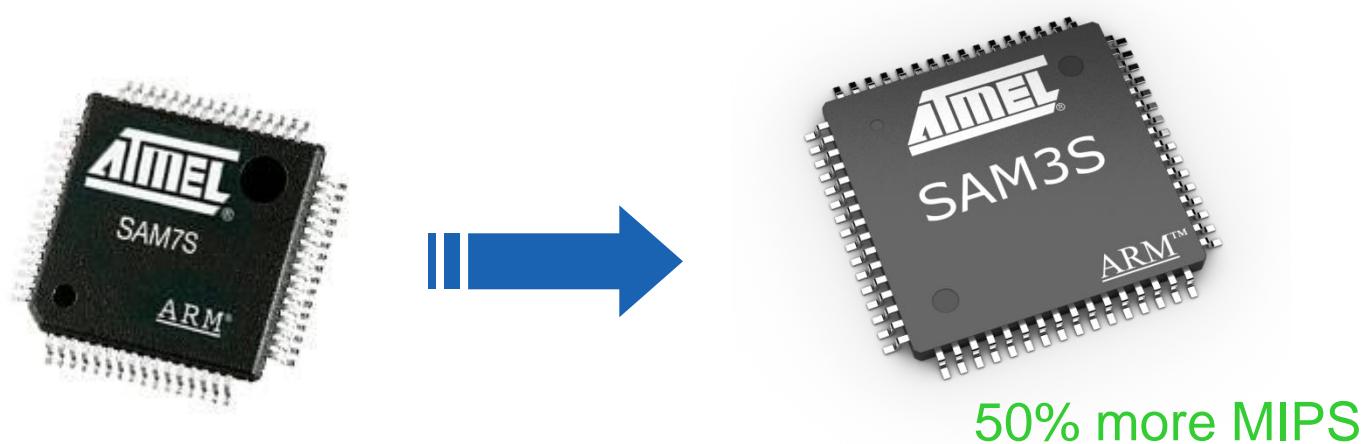
- CRC Unit
 - Cyclic Redundancy Check engine to perform a checksum computation on any memories; on-chip Flash, on-chip SRAM or off-chip memory.
 - Three polynomials:
 - CCIT802.3; Polynom 0x04C11DB7,
 - CRC-32C (CASTAGNOLI); Polynom 0x1EDC6F41,
 - CCIT16; Polynom 0x1021.
 - DMA channel reading a programmable amount of data and computes CRC on the fly.
 - Reference CRC register for comparison with interrupt capability.

Safety & Security Features

- Hardware CRC with DMA and Flash ECC guarantees memory integrity.
- Memory protection unit improves code protection and secures multi-application/task execution.
- Unique 128-bit ID and scrambled external bus interface ensure software confidentiality.
- Crystal Oscillator failure detection & automatic fallback to RC Osc.
- Protected mode for peripherals configuration registers.
- I/Os configuration for peripherals can be locked.

Improvements to Best-selling SAM7S Series

- The SAM3S is the ideal upgrade path for the SAM7S and SAM7SE
 - Migration path to Cortex-M3 processor
 - 50 percent raw performance increase over the SAM7S series
 - Renewed upwards compatible peripheral set
- In its 64-pin version, the SAM3S is pin-to-pin compatible with the SAM7S, preserving prior made investments in hardware



Pin to pin compatibility with SAM7S?

- SAM7S series package offering:



- SAM3S series is available in 100-pin, 64-pin and 48-pin QFP/QFN packages,
 - In its 64-pin version, the SAM3S is pin-to-pin compatible with the SAM7S,
 - In its 48-pin version, there is only one pin which differs from SAM7S.
- SAM3S hardware changes:
 - I/Os are not 5V Tolerant,
 - XIN level in bypass mode is 3.3V and not 1.8V.

SAM3S8/SD8 comparison table

Features	SAM3S4/2/1	SAM3S(D)8
Core	Cortex M3 + MPU	Cortex M3 + MPU
Supply	1.62 to 3.6V	1.62 to 3.6V
Max Freq	64MHz	64MHz
SRAM	Up to 48kB	64kB
FLASH	64 to 256kB	512kB (Dual bank for SAM3SD8)
PDC	22	Up to 24 (for SAM3SD8)
USB	FS Dev	FS Dev
CAN	-	-
Ethernet	-	-
ADC	16x 12-bit	16x 12-bit
DAC	2x 12-bit	2x 12-bit
EBI	Yes (8-bit data)	Yes (SDRAM)
Package	48, 64, 100	64,100

SAM3S8/SD8 Memories improvement

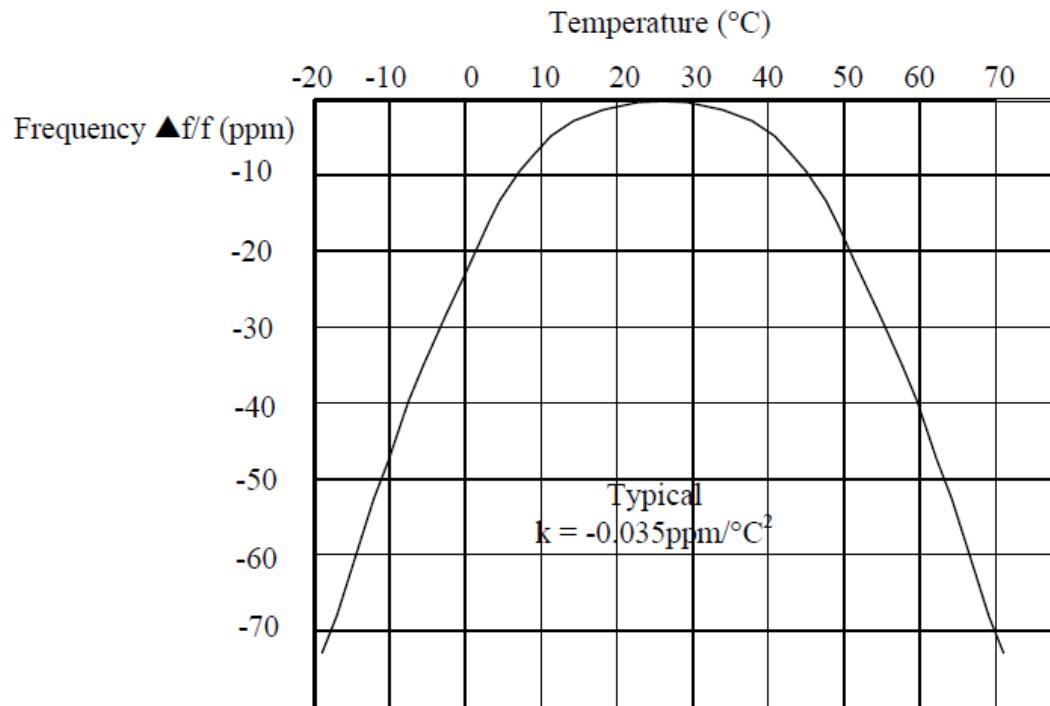
- Flash memory size is 512kbytes:
 - Single Bank for SAM3S8
 - Dual Bank for SAM3SD8
 - Only One EEFC to handle the two banks.
 - Possible to read while programming (but not possible to read or write the two banks at the same time)
 - Can erase by plane
 - EEFC improvement:
 - One-by-one lock bit
- RAM memory size is 64kbytes versus 48kbytes

SAM3S8/SD8 ADC automatic hardware calibration

- Automatic hardware calibration added to improve the ADC:
 - auto-calibration enable using the AUTOCAL bit in ADC Control Register(ADC_CR)
 - automatic calibration sequence on all enabled channels
 - wait for End Of CALibration bit (EOCAL)
 - calibration data is stored in the internal ADC memory
 - after a new conversion, the converted value is a calibrated value
- ADC automatic calibration need to be done :
 - After setting the gain and offset of all enabled channels
 - If the gain and offset settings are modified for a given channel
 - After changing the ADC reference voltage (ADVREF pin)
 - After a software reset, a power up, or wake-up from Backup mode as the calibration data in the ADC memory is lost
- ADC automatic calibration do NOT need to be done AGAIN:
 - For a new channel with the same setting as the one already calibrated
 - After changing the ADC running mode (Normal or sleep mode)

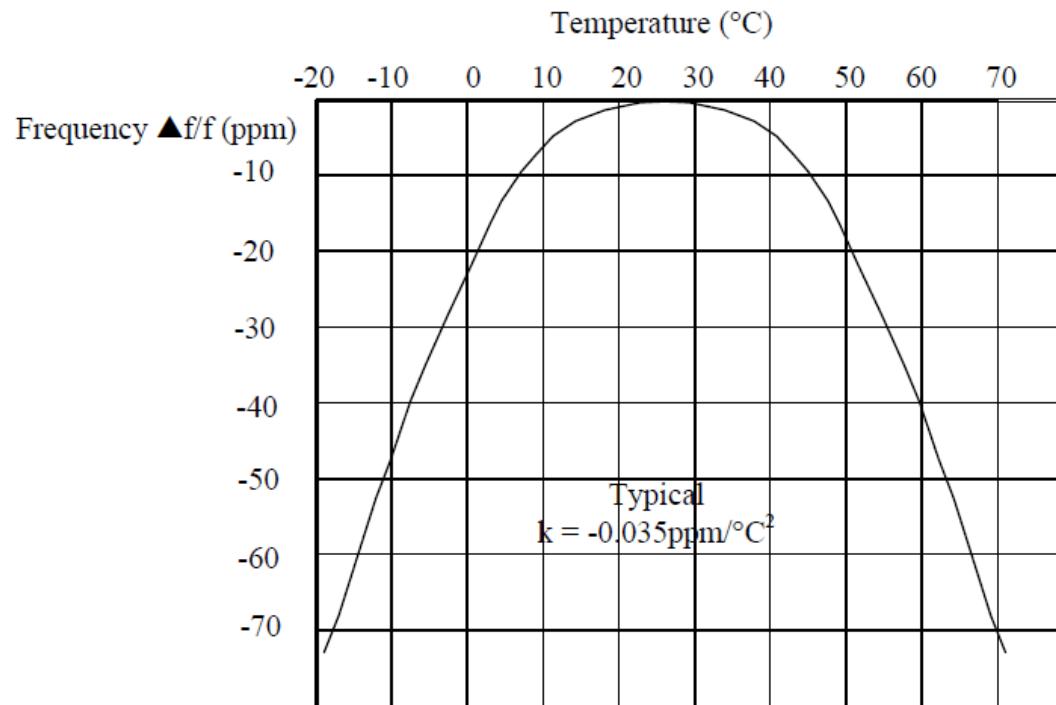
SAM3S8/SD8 RTC Trimming capability 1/4

- The RTC clock source
 - Internal RC 32kHz
 - 32.7678kHz external crystal(gives better frequency accuracy)
- Crystal error sources
 - Drift at room temperature (typically +/-20ppm)
 - Temperature variations



SAM3S8/SD8 RTC Trimming capability 2/4

- For an application where a very accurate RTC is required you can:
 - measure in production at room temperature the quartz deviation and compensate it via this trimming capability
 - compensate the temperature deviation by measuring the temperature (using internal TS or external)



SAM3S8/SD8 RTC Trimming capability 3/4

- Crystal drift correction:
 - The calibration circuitry acts by slightly modifying the 1 Hz clock period from time to time
 - By Adding positive or negative correction in a range of 1.5ppm to 1950ppm.
 - Can obtain a crystal drift:
 - below 1 ppm for a initial crystal drift between 1.5 ppm to 90 ppm
 - below 2 ppm for a initial crystal drift between 90 ppm to 130 ppm
 - below 5 ppm for a initial crystal drift between 130 ppm to 200 ppm
 - i.e. after correcting a drift of 20ppm in the crystal should have maximum drift of 1ppm

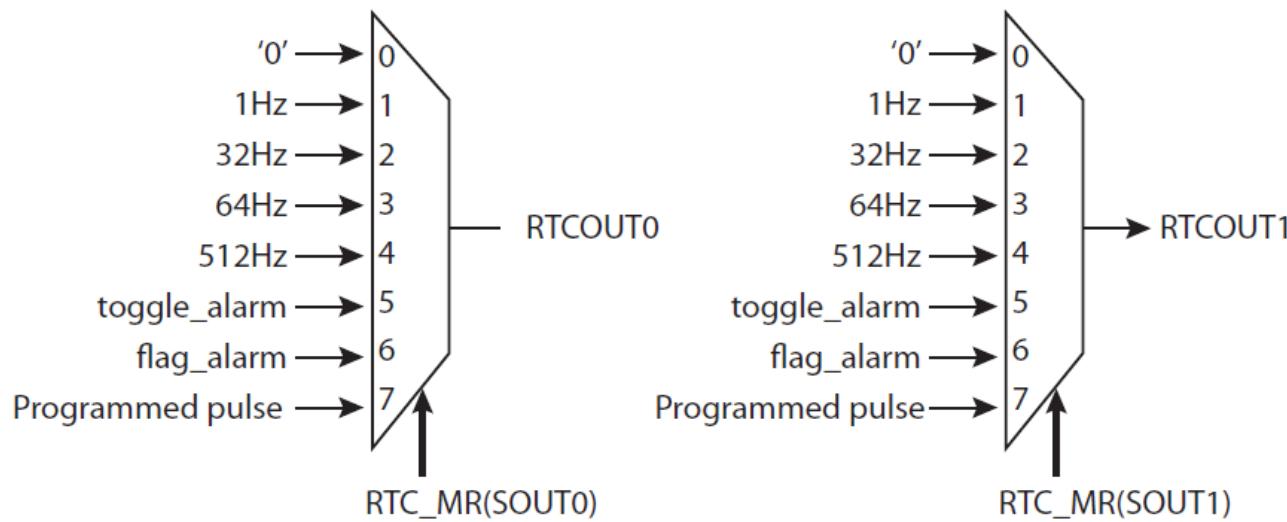
SAM3S8/SD8 RTC Trimming capability 4/4

- Register to configure: RTC Mode Register RTC_MR
 - NEGPPM: NEГative PPM Correction (negative or positive correction)
 - HIGHPPM: HIGH PPM Correction (set for ppm correction above 30ppm)
 - CORRECTION: correction value to add given by the formulas:
- Formulas:
 - HIGHPPM=0 (correction below 30 ppm) CORRECTION = $[3906 / (20 * \text{ppm})] - 1$
 - HIGHPPM=1 (correction above 30 ppm) CORRECTION = $(3906 / \text{ppm}) - 1$
- Example: need a crystal correction of +100ppm:
 - NEGPPM =0
 - HIGHPPM =1
 - CORRECTION = $(3906 / 100) - 1 \# 38$ (rounded)

SAM3S8/SD8 RTC Waveform generation 1/2

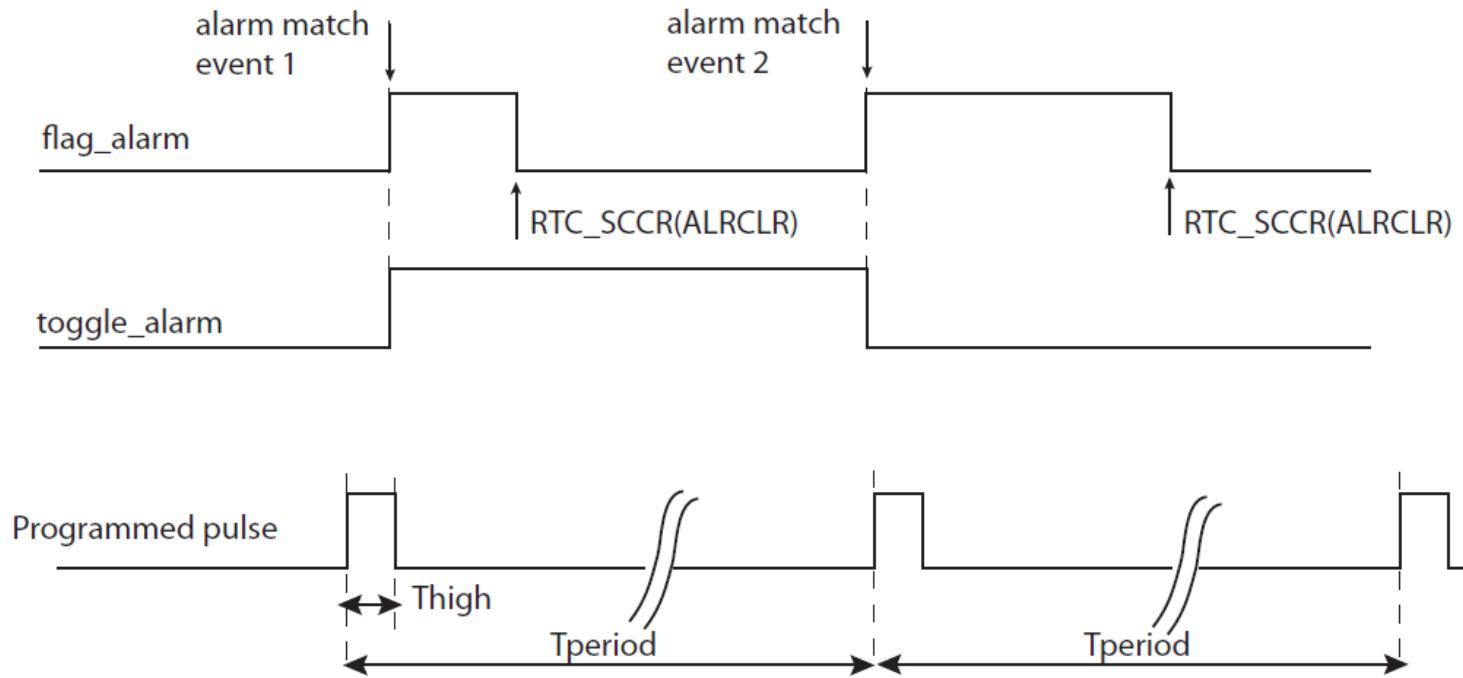
- Avoid to wake-up the MCU from low power modes to drive the PIO (Extra function) to generate periodic action like:
 - blink a dot on a Segment LCD
 - to activate periodically an external sensor
 - a tamper function...
- Up to 2 waveforms can be generated RTCOUT0 and RTCOUT1
 - 7 possibilities driver sources
 - independent source selection registers

Figure 5-1. Waveform generation



SAM3S8/SD8 RTC Waveform generation 2/2

- Flag alarm, Toggle alarm and Pulse sources details

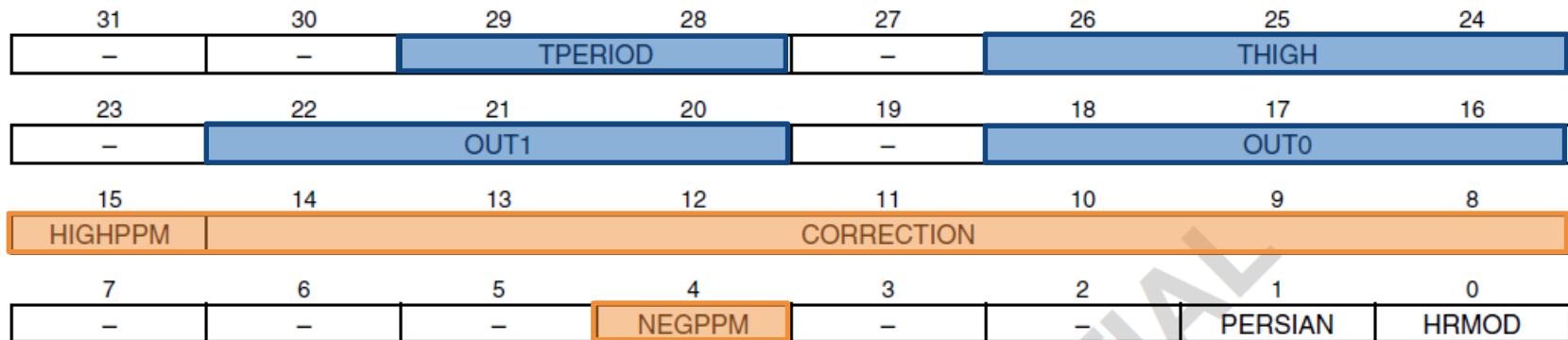


- **Thigh** and **Tperiod** are set in the RTC Mode Register `RTC_MR`
 - $\text{Thigh} = 15.2\mu\text{s} / 30.5\mu\text{s} / 122\mu\text{s} / 488\mu\text{s} / 967\mu\text{s} / 3.91\text{ms} / 15.6\text{ms} / 31.2\text{ms}$
 - $\text{Tperiod} = 125\text{ms} / 250\text{ms} / 500\text{ms} / 1\text{S}$

SAM3S8/SD8 RTC Mode Register

Registers to configure for Waveform generator

- TPERIOD: Period of the Output Pulse
- THIGH: High Duration of the Output Pulse
- OUT1 & OUT2: RTCOUT1 & RTCOUT0 Outputs Source Selection



Registers to configure for RTC trimming Correction

- NEGPPM: NEGative PPM Correction (set negative or positive correction)
- HIGHPPM: HIGH PPM Correction (set for ppm correction above 30ppm)
- CORRECTION: correction value to add

PERSIAN: RTC with Persian calendar available

HRMOD: 12 or 24 hour Mode (same as SAM3S)

SAM3S8/SD8 Fast RC trimming

- Possibility to measure and trim on the fly the Fast RC (4/8/12 MHz) frequency with external 32.768 kHz crystal
 - Possibility to get accuracy lower than 1%
- Fast RC oscillator trimming bits are in the PMC_OCR register.

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
SEL12				CAL12			
15	14	13	12	11	10	9	8
SEL8				CAL8			
7	6	5	4	3	2	1	0
SEL4				CAL4			

SELx: select the factory trimmed default calibration value or the calibration value write in CALx
CALX: calibration value enter by the user (value reset after each power up or peripheral reset)

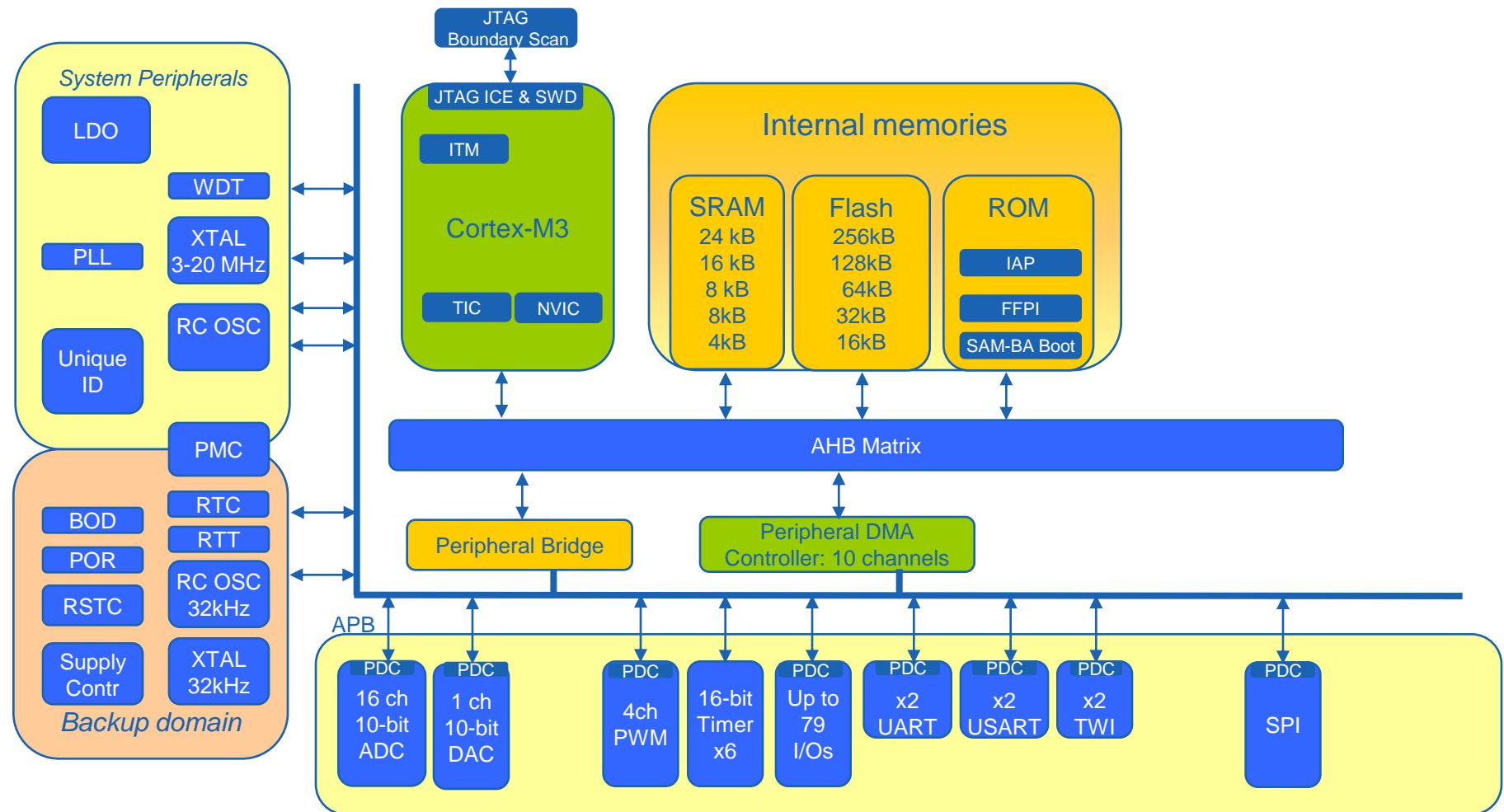
- Trimming not possible on operating oscillator frequency
 - i.e. running frequency is 8 MHz, we can adjust the 4 MHz and 12 MHz frequencies but not 8 MHz.

SAM3N Series

Entry level and low cost SAM3
Cortex-M3 series
Pin-to-pin compatible with the
SAM3S series

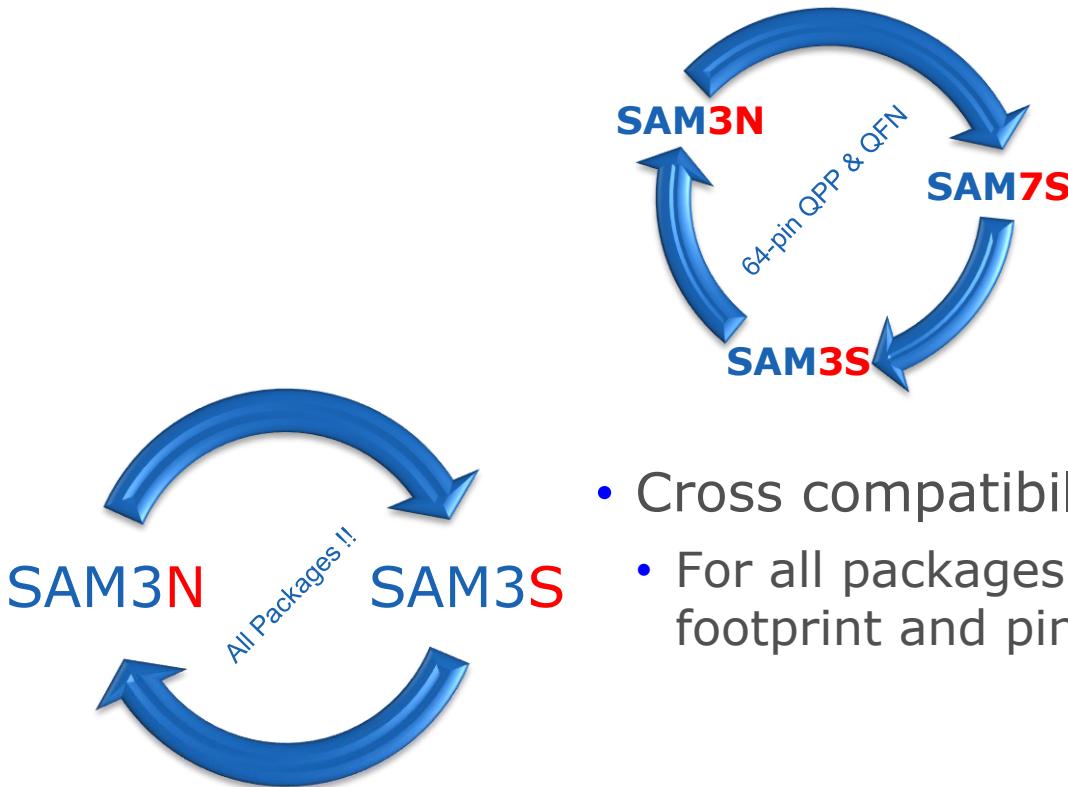


SAM3N Series



Drop in replacements

- Cross compatibility between Families
 - For 64-pin QFP & QFN package
 - SAM7S & SAM3S are footprint and pinout compatible
 - SAM7S & SAM3N are footprint and pinout compatible
 - SAM7S series support Full Speed USB device whereas SAM3N don't (pins are IOs)



- Cross compatibility within Family
 - For all packages, SAM3S and SAM3N are footprint and pinout compatible

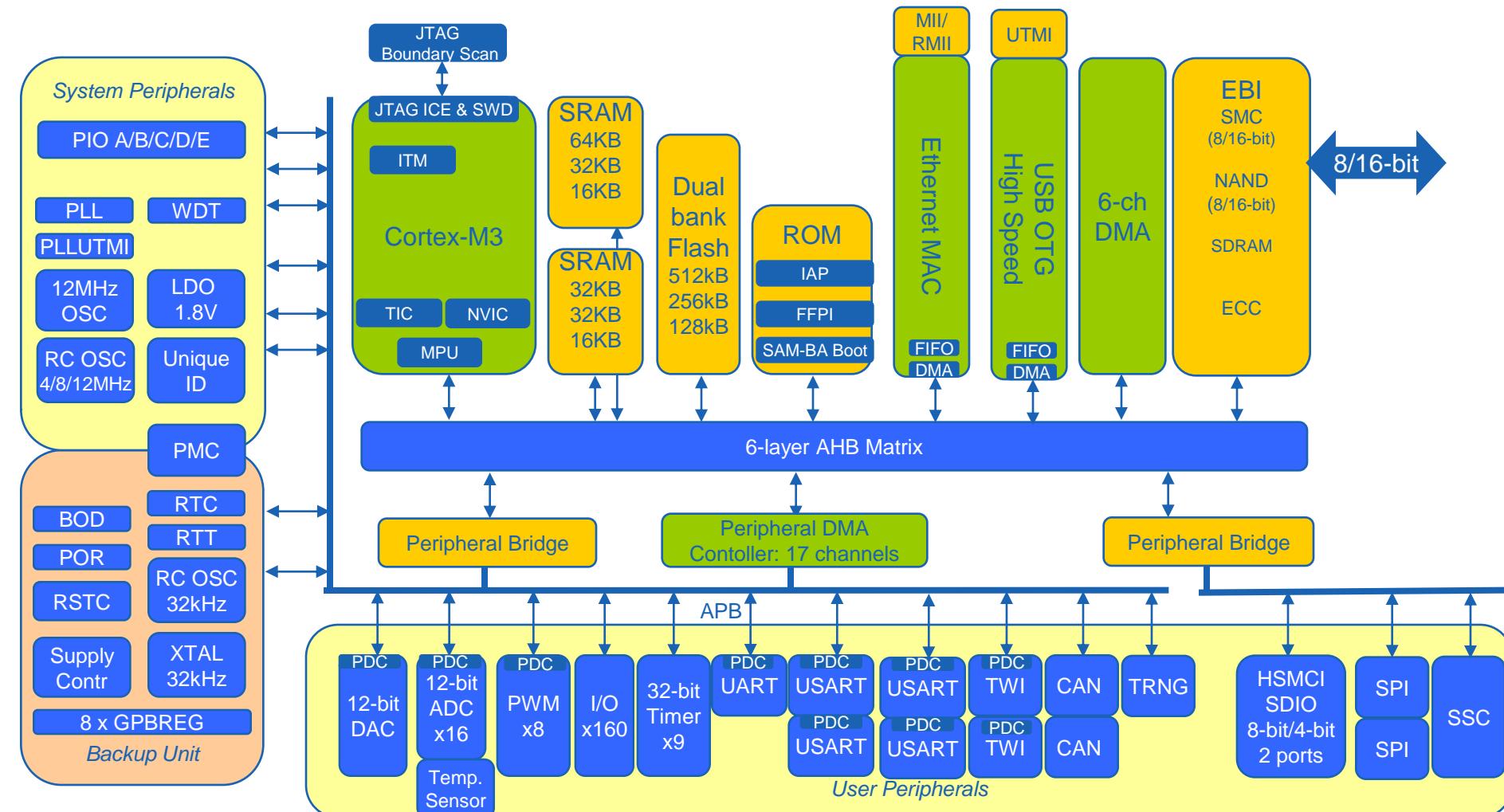
SAM3S vs SAM3N Resume table

Features	SAM3S	SAM3N
Core	Cortex-M3 + MPU	Cortex-M3
Supply	1.62V to 3.6V	1.62V to 3.6V
Max Frequency	100MHz	48 MHz (62 MHz if VDDCORE = 1.8V)
SRAM	Up to 128kB	Up to 24kB
FLASH	64kB to 1 MB	16 to 256kB
PDC	21	10
USB	FS Dev	No
HSMCI	Yes	No
SSC	Yes	No
Analog Comparator	Yes	No
PIO Capture Mode	Yes	No
ADC	15 x 12-bit (+Temp.)	16 x 10-bit
DAC	2 x 12-bit	1 x 10-bit
EBI	Yes (8-bit data)	-
Package (QFP, QFN, BGA)	48, 64, 100	48, 64, 100

SAM3X/A Series

Connectivity

SAM3X/A Series



SAM3X/A Family

	SAM3X	SAM3X	SAM3X	SAM3A
Pinout	208/217pin	144 pin	100 pin	100 pin
DAC channels	2			
ADC channels	15 + internal Temp Sensor			
Timer	9 + Systic + PWM + RTT			
Timer on PIO	3	6	6	9
I/O	166	111	70	
EMAC	✓ RMII/MII	✓ RMII/MII	✓ RMII	✗
HSMCI/SDIO	4bit-8bit 2 ports	8bit	4bit	4bit
CAN	2			
TWI	2	2	2	2
SPI	2 +4USART	1 +4USART	1 +3USART	1 +3USART
PWM channels	8	8	4	8
U(S)ART	4USART 1UART	3USART 2UART	3USART 1UART	3USART 1UART
SSC	✓			
EBI	8/16bit SDRAM	8/16bit	✗	✗

SAM3X/A New Features

- EBI
 - Same NFC and SMC versus SAM3U (SAM3X only)
- Ethernet MAC
 - Built-in 128-bytes FIFO and Dedicated DMA enable maximum throughput
- USB OTG HS with on-chip transceivers
 - Up to 480 Mbits/s
 - 10 Bidirectional endpoints
 - 4kB dual port RAM
- 2 CAN Controllers
 - 8 mailboxes per controller
- ADC 12 bit and 12-bit DAC : same as SAM3S

SAM3X/A New Features (cont.)

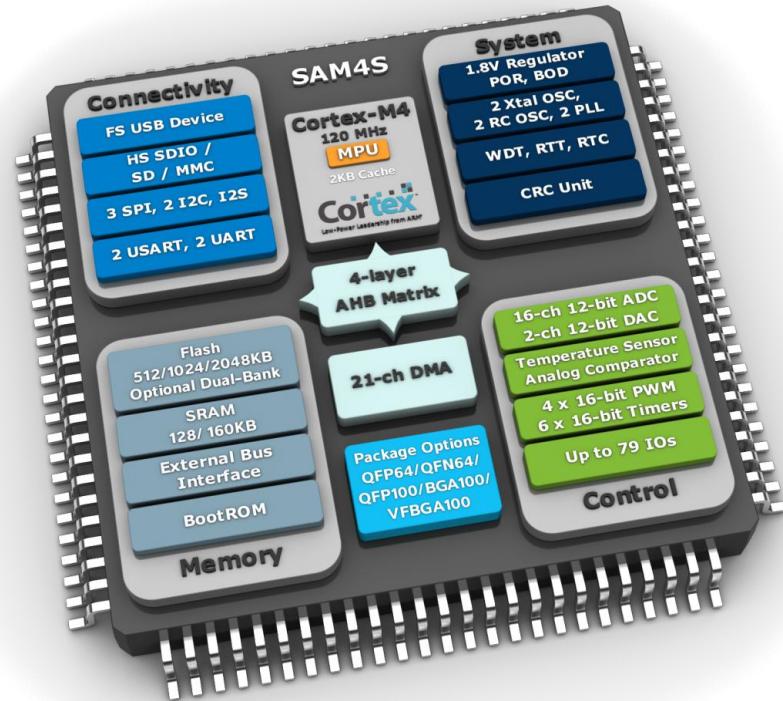
- TRNG (True Random Number Generator)
 - Provides a 32-bit RN every 84 clock cycles
- USART:
 - USART0 with LIN
- T/C:
 - 32 bits
- HSMCI
 - 1 x 8-bit slot and 1 x 4-bit slot (one controller)
- NRST pin in input by default
- All Flash version in dual bank version

SAM4S Series



SAM4S

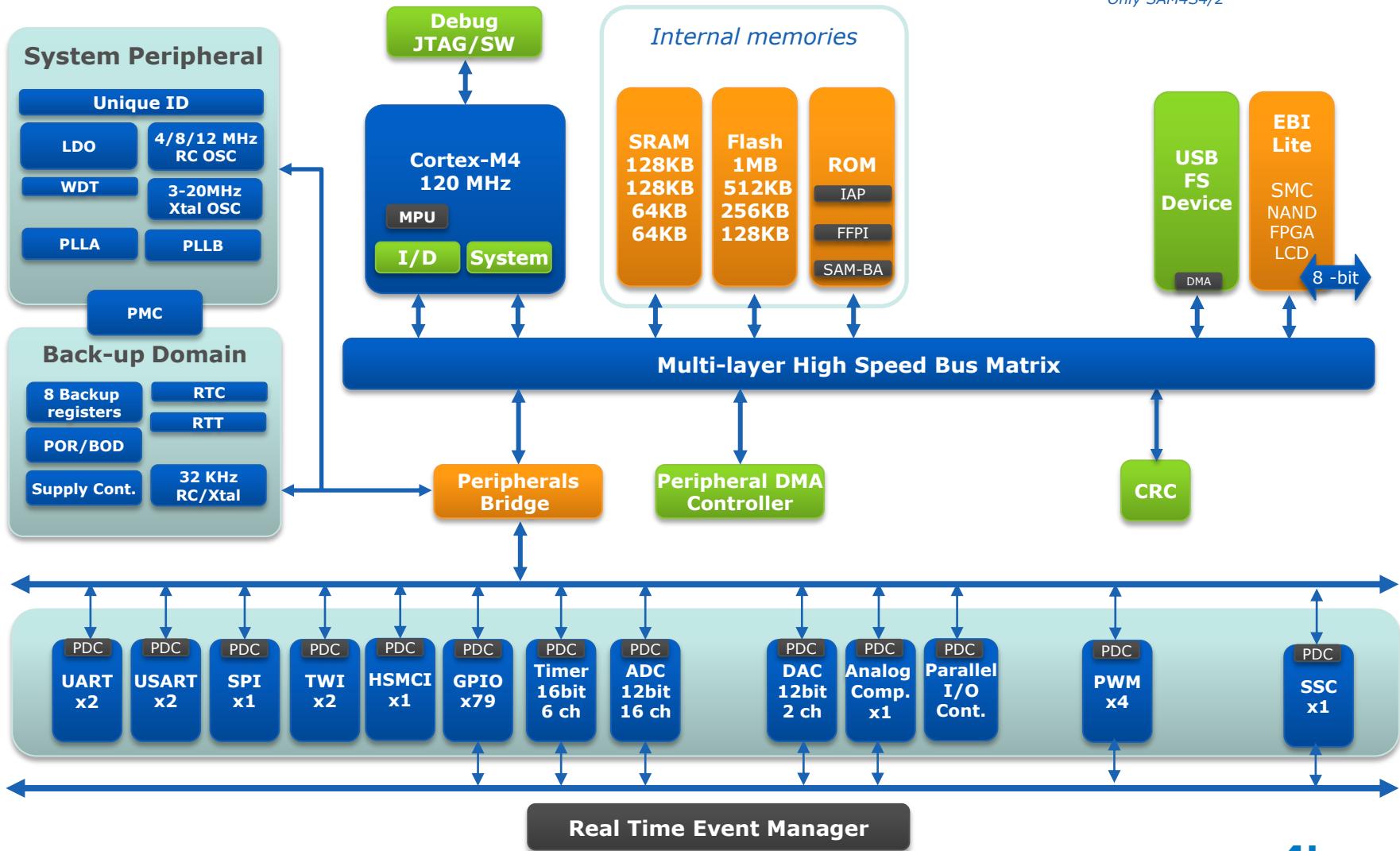
- Cortex-M4 processor running up to 120MHz
- Up to 2MB of Flash and 160KB of SRAM
- SAM7S/SAM3S/SAM3N Pin-to-pin compatible
- Very Low Power consumption
 - 200 μ A/MHz
 - 20 μ A in Wait Mode
 - 1 μ A in Backup Mode
- Parallel IO capture (CMOS interface)
- High data rate serial communication interfaces
 - High Speed USB Device
 - SDIO/SD/MMC
 - 4 UARTs, 3 SPI, 2 I2C and I2S



SAM4S Block Diagram

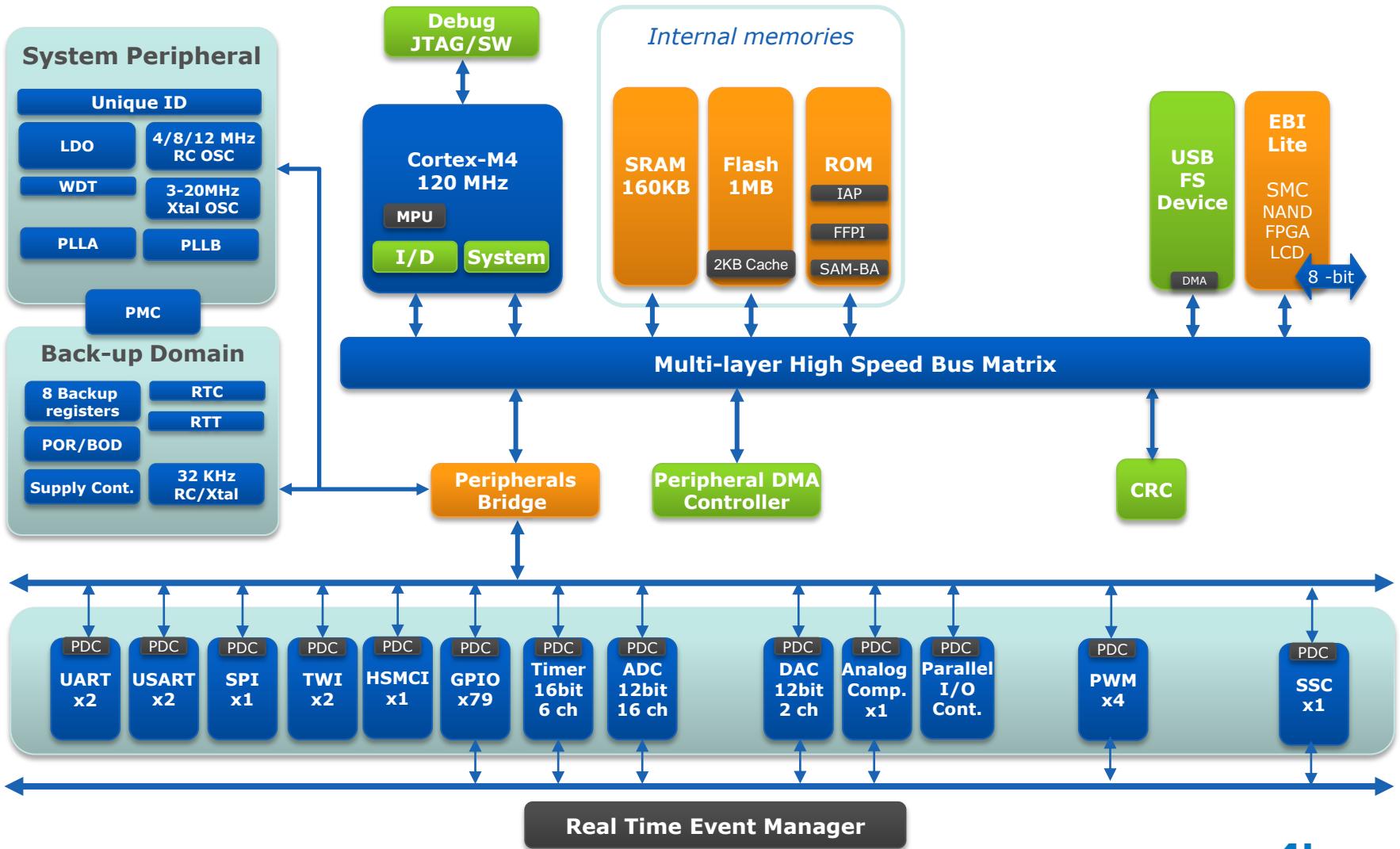
Package	General Purpose
LQFP/QFN48 (*)	180µA/MHz
LQFP/QFN64	~20µA - Full SRAM
LQFP/TFBGA100	1µA - Backup
VFBGA100	CMOS int.
WLCSP64	

* Only SAM4S4/2

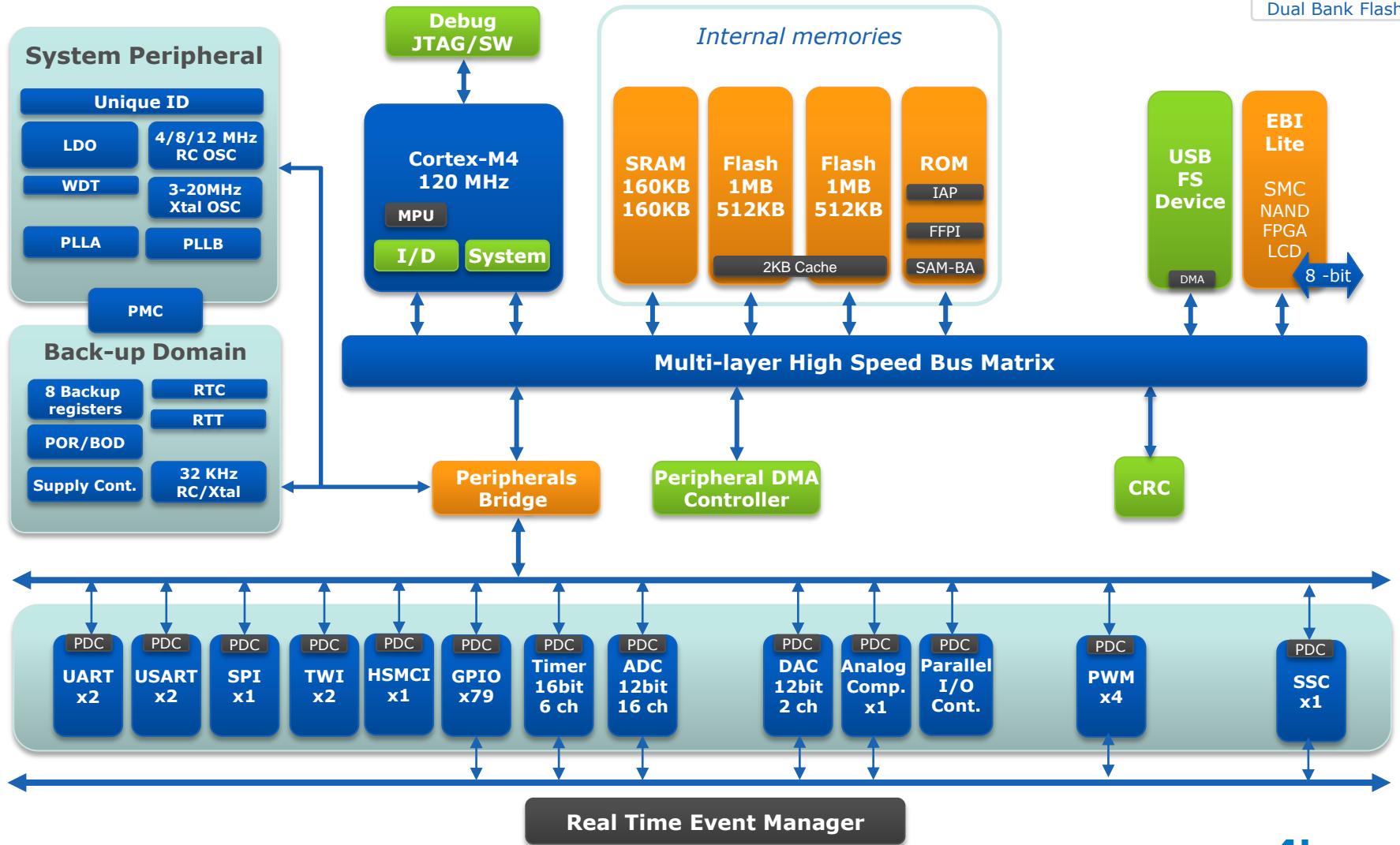


SAM4SA Block Diagram

Package	General Purpose
LQFP/QFN64	180µA/MHz
LQFP/TFBGA100	~20µA - Full SRAM
VFBGA100	1µA - Backup
	CMOS int.
	Cache



SAM4SD Block Diagram



Package

LQFP/QFN64
LQFP/TFBGA100
VFBGA100

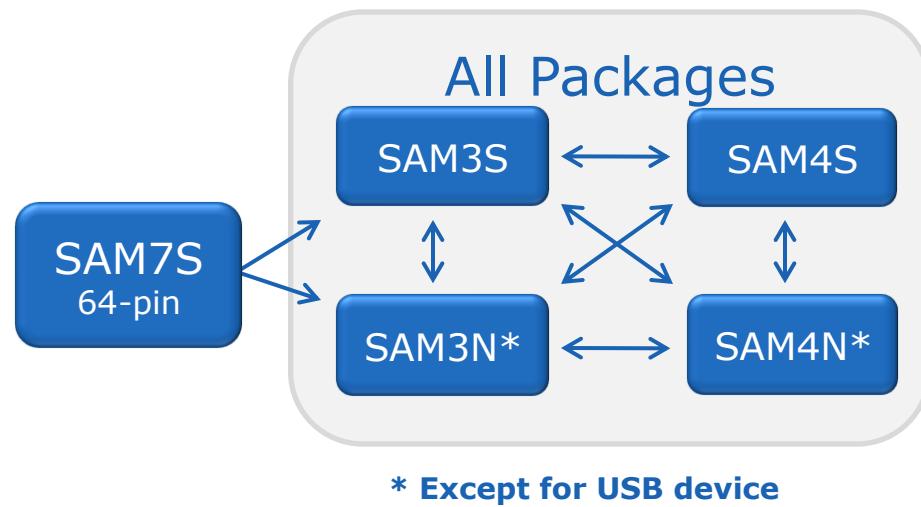
General Purpose

180 μ A/MHz
~20 μ A - Full SRAM
1 μ A - Backup
CMOS int.
Cache
Dual Bank Flash

Pin to pin compatibility

- Seamless migration path between SAM7S, SAM3N, SAM3S, SAM4S, SAM4N

Form, Fit & Function Compatibility



DSP extension

- Cortex M4 features
 - A single-cycle multiply-accumulate unit (MAC)
 - Optimized single instruction multiple data (SIMD) instructions, saturating arithmetic instructions
 - Optional single precision Floating-Point Unit (FPU)
- Designed for applications requiring more computational performance
- Releases CPU resources in case of DSP task are used

More memory density

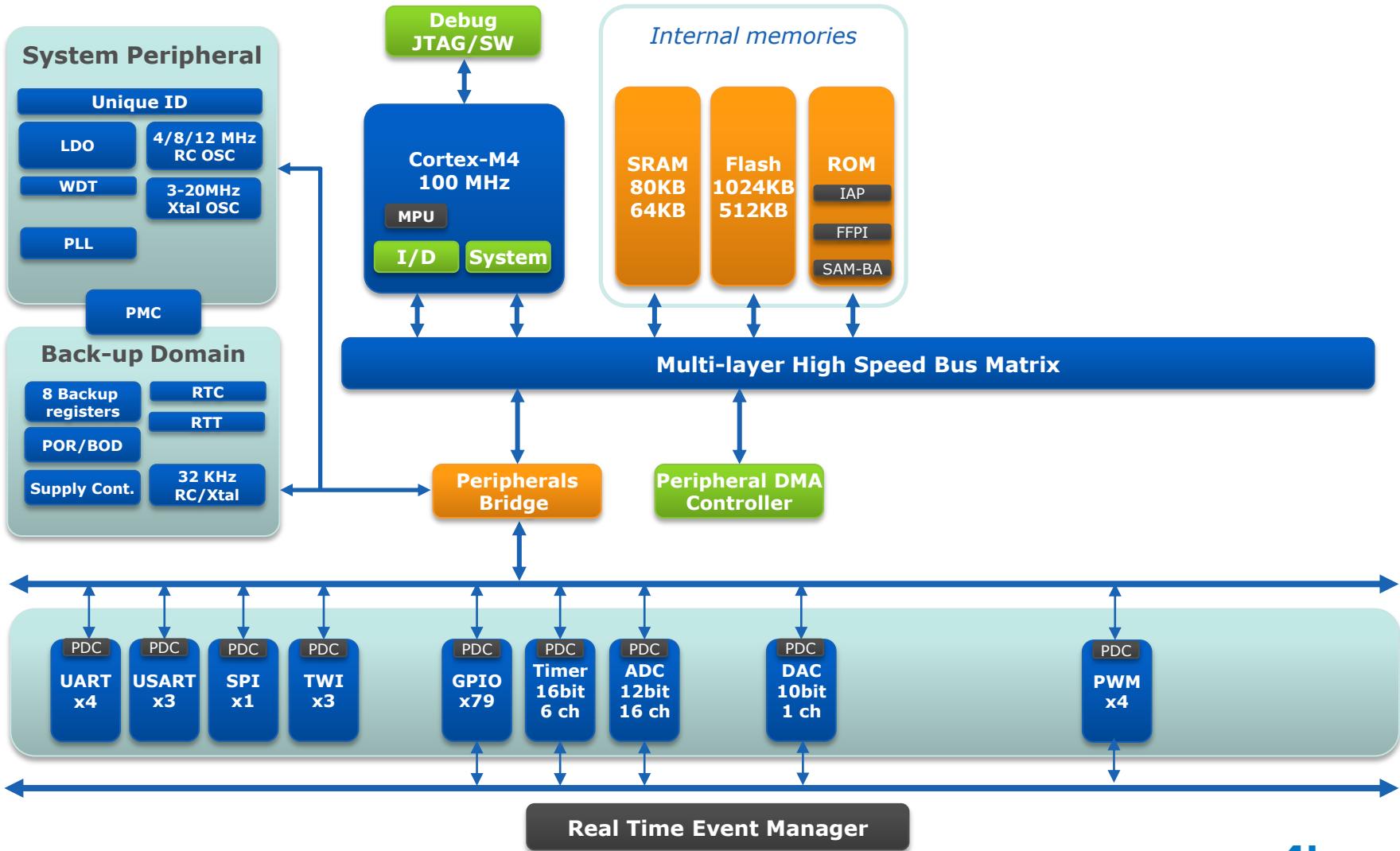
	SAM4S8/16	SAM4SA16	SAM4SD16/32
Core	Cortex-M4	Cortex-M4	Cortex-M4
Frequency	120MHz	120MHz	120MHz
Cache	-	2KB	2KB
Flash	512KB/1MB Single bank	1MB Single bank	1MB/2MB Dual bank
Flash access	64/128-bit	64/128-bit	64/128-bit
SRAM	128K	160K	160K

- Boot bank selection capability for SAM4SD16/32
- 2KB Cache Memory (SAM4SA and SAM4SD)
 - Fast Execution Out of Flash @120MHz
 - CoreMark/MHz = 2.14
 - CoreMark = 256.8

SAM4N Series

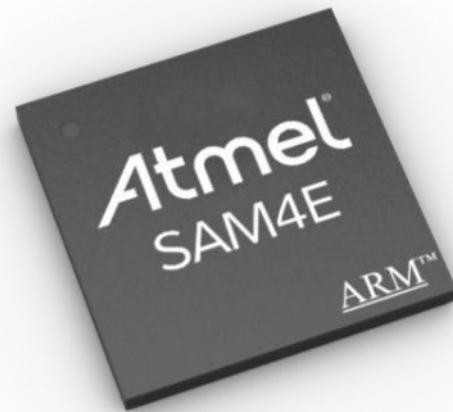
SAM4N Block Diagram

Package	General Purpose
LQFP/QFN48 (*)	170µA/MHz
LQFP/QFN64	~20µA - Full SRAM
LQFP/TFBGA100	1µA - Backup
VFBGA100	
* Only SAM4N8	



SAM4E Series

Connectivity

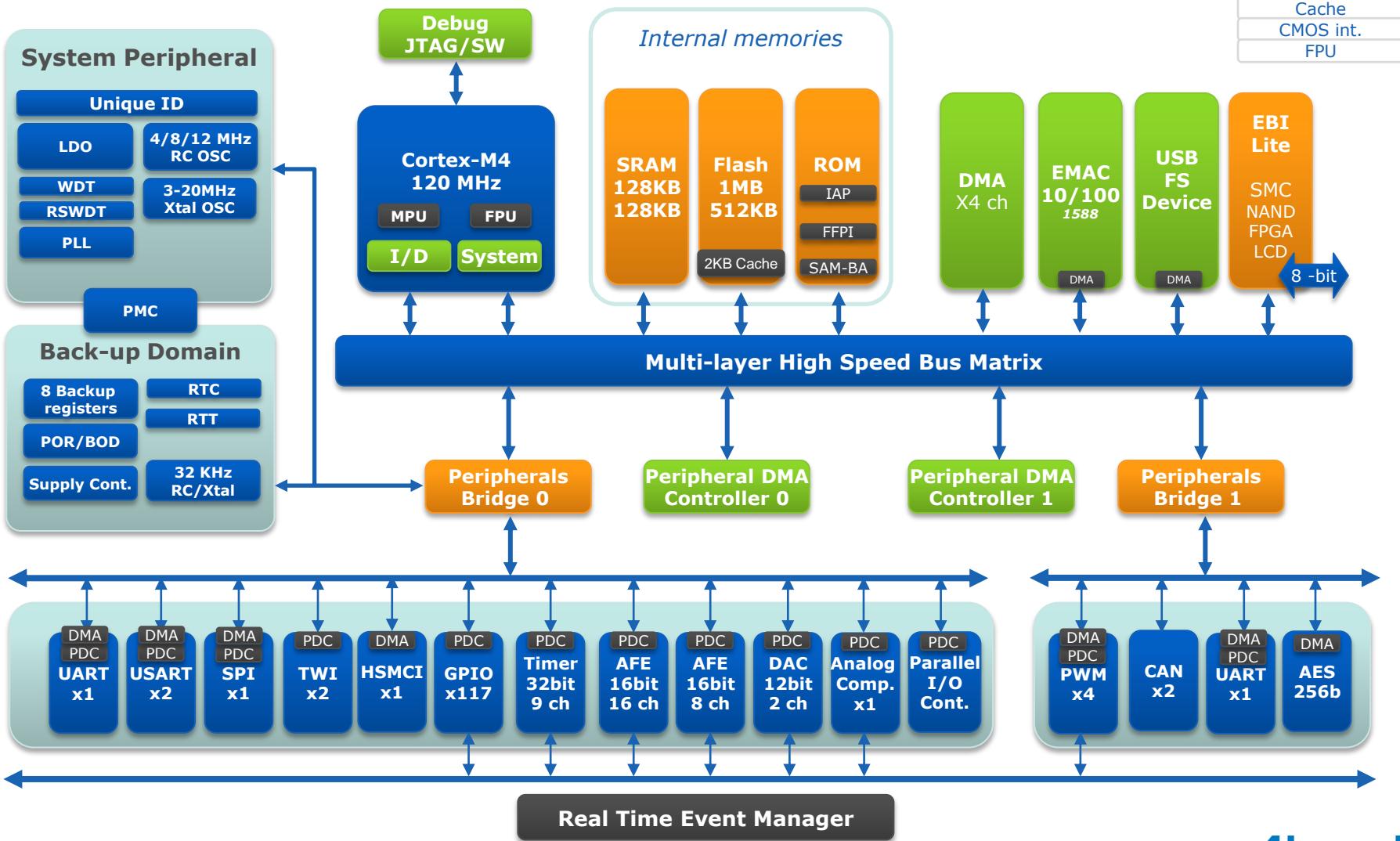


SAM4E in a nutshell

- **High Performance**
 - 120 MHz Cortex-M4F (FPU)
 - Dual HS bridge architecture
 - 2KB cache on flash
 - Real time Event
- **Connectivity**
 - Ethernet with IEEE 1588 support
 - Dual CAN ports
- **Advanced Analog**
 - Two Analog Front End (AFE)
 - ADC with 16-bit enhanced mode @ 4Ksps
 - Offset error correction
 - Gain error correction

SAM4E	
Frequency	120 MHz
Flash	512 KB - 1MB
SRAM	128 KBytes
EMAC	1
CAN	2
USART	4
SPI	3
I ² C	2
Crypto	AES256
Parallel Capture (CMOS int.)	Yes
2x 12-bit ADC @1Msps with Analog Front End	Up to 24 channels
12-bit DAC	Up to 2 channels
Timers/PWMs (Motor control)	9/4
MCI/SDIO	Yes
USB	FS Device
Ext Bus Interface	Yes
GPIO	Up to 117
Pin count	100 – 144
Package	QFP, BGA

SAM4E Block Diagram

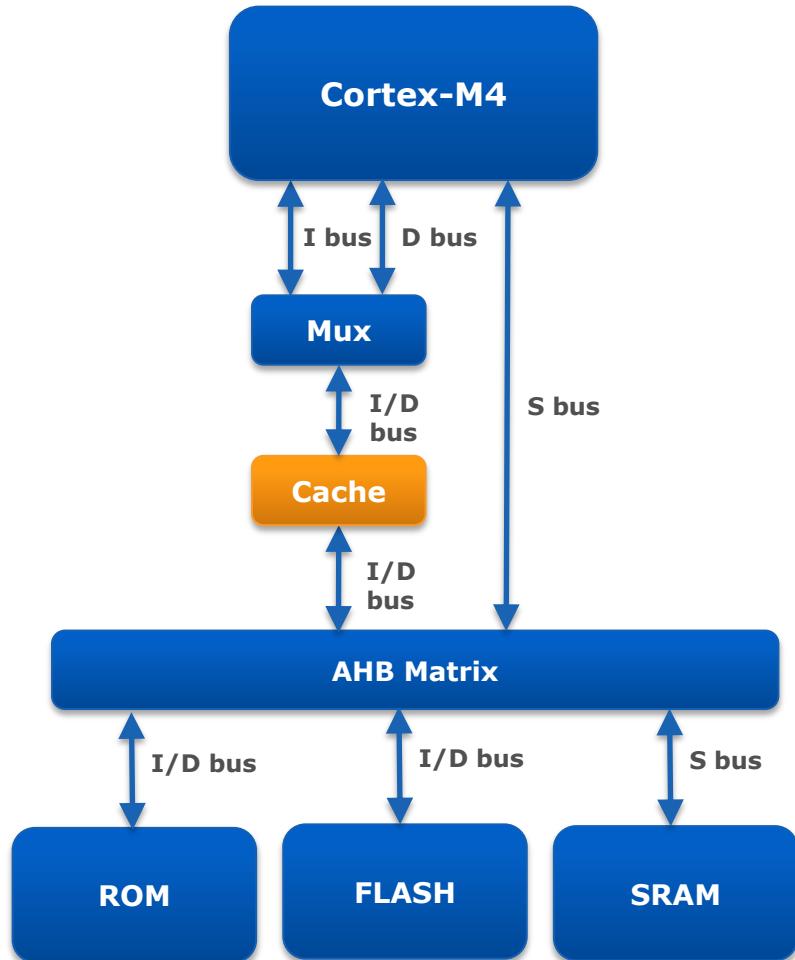


Performance highlights

- 120MHz core frequency with hardware Floating Point Unit (FPU)
 - Single cycle add/subtract/multiply floating point operations
- Dual high speed peripheral bridges
 - PDC and DMA capability
- 2KB cache on flash
 - Zero wait state access at full speed
- Real Time Event manager
 - Direct Peripheral to Peripheral connection
 - No CPU intervention

SAM4E Cache system overview

- 2Kbytes of 4-way consecutive cache with monitor system
- Advantage
 - Compensate wait state penalty at high frequency
 - Reduce power consumption
- Drawback
 - Not suitable for deterministic tasks execution (Real Time Applications)



Cache System Benefits

- Compensate wait state penalties

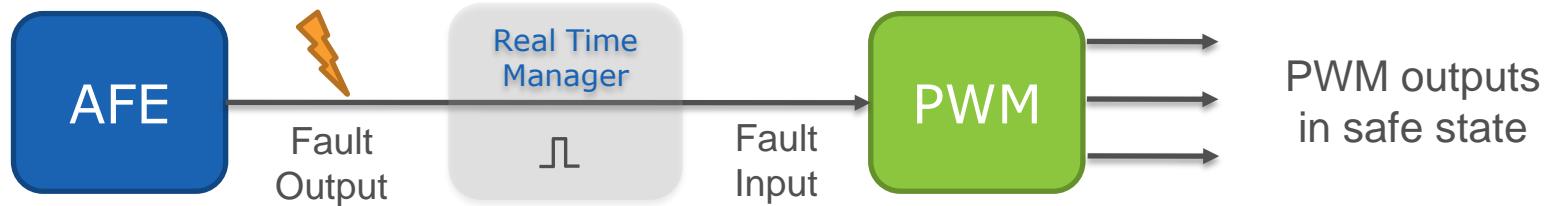
WS@Core Frequency	Coremark IAR 6.50 (Coremark/MHZ)
0WS@21MHz	3.38
5WS@123MHz (cache disabled)	2.03
5WS@123MHz (cache enabled)	3.33

- Reduce power consumption
 - A write or read access to cache requires less current than a direct access to flash
 - If recurrent code is accessed from cache a reduction of consumption can be observed

Core Frequency	I _{VDDIN} (mA)	I _{VDDCORE} (mA)
123MHz (cache disabled)	21.5	24.1
123MHz (cache enabled)	18.5	20.6

Real Time Event Management Overview

- Inter-peripheral communication
 - Events generated by peripherals (Event Generators) are directly routed to other peripherals (Event Managers)



- Latency free event handling without CPU intervention
- Only One Manager can be connected to one Generator at the same time
- Peripherals need to have their clock enabled
 - Not usable in WAIT and BACKUP low power modes

SAM4E Ethernet Controller Highlights

- 10Mbps and 100Mbps operations
- MII mode support only
- Two 128 bytes FIFO
- MDIO interface for external PHY management
- Supports Wake-on-LAN
- IEEE 1588 support
 - Precision Time Protocol frames recognition



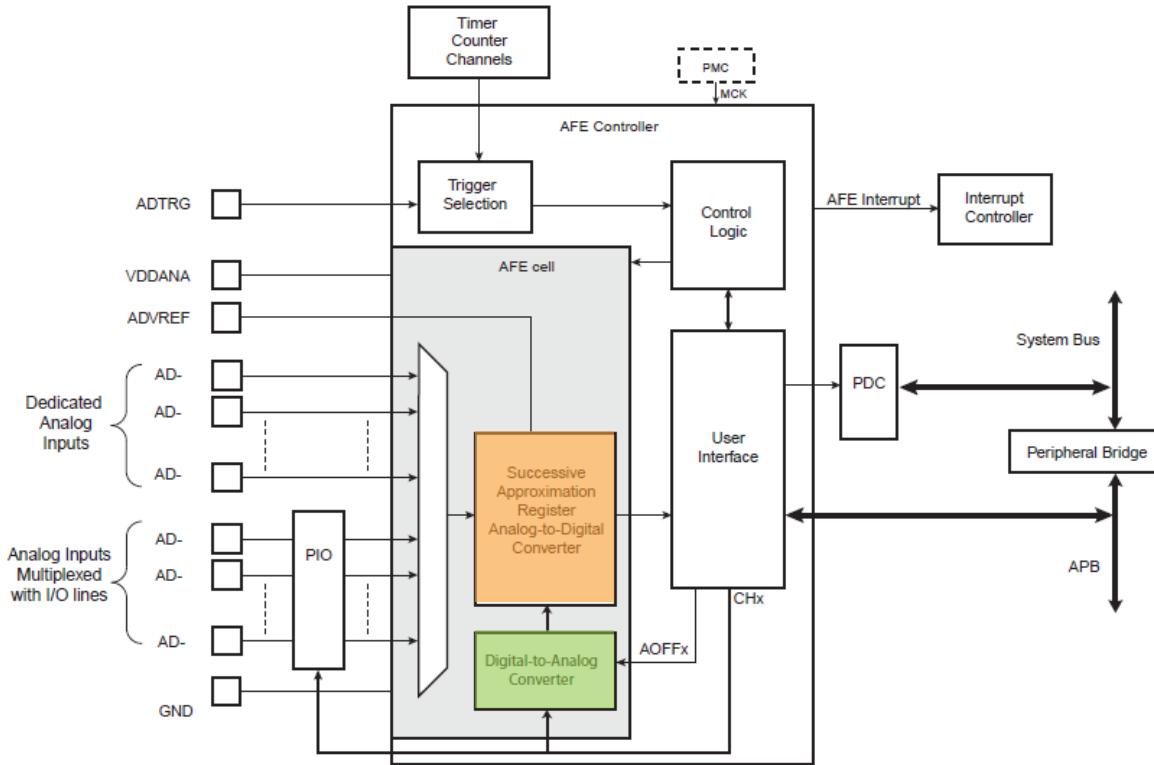
Advanced Analog Features



- Two Analog Front End controller (AFE)
 - 2 x 12-channel of 12-bit resolution with 1Msps sampling rate
 - Enhanced resolution mode gives up to 16-bit resolution at 4ksps
 - Auto-calibration
 - Offset and gain compensation
 - Single-ended and differential input modes
 - PDC support
- Digital-to-Analog controller (DAC)
 - 2-channel 12-bit resolution
 - PDC support
- Analog comparator

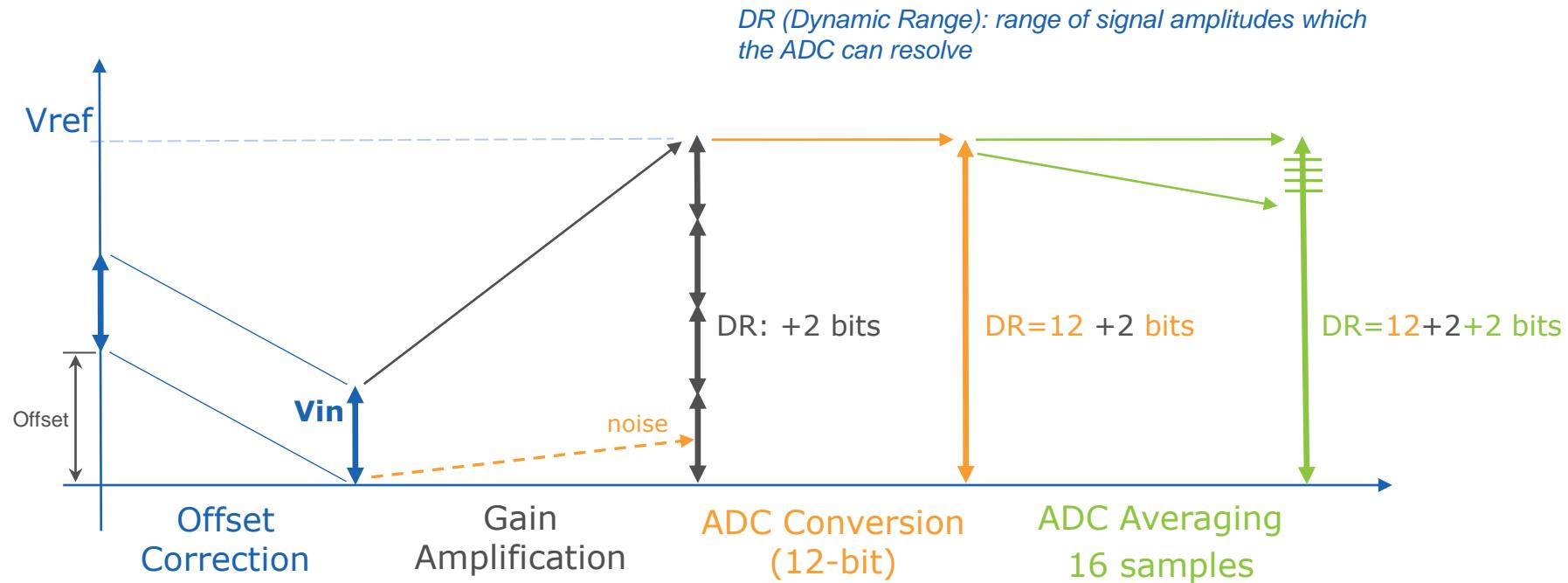
Analog Front End

- Each Analog Front End is made of:
 - One Successive Approximation **ADC**
 - + one PGA (Programmable Gain Amplifier)
 - + one **DAC** in feedback for offset correction of ADC input



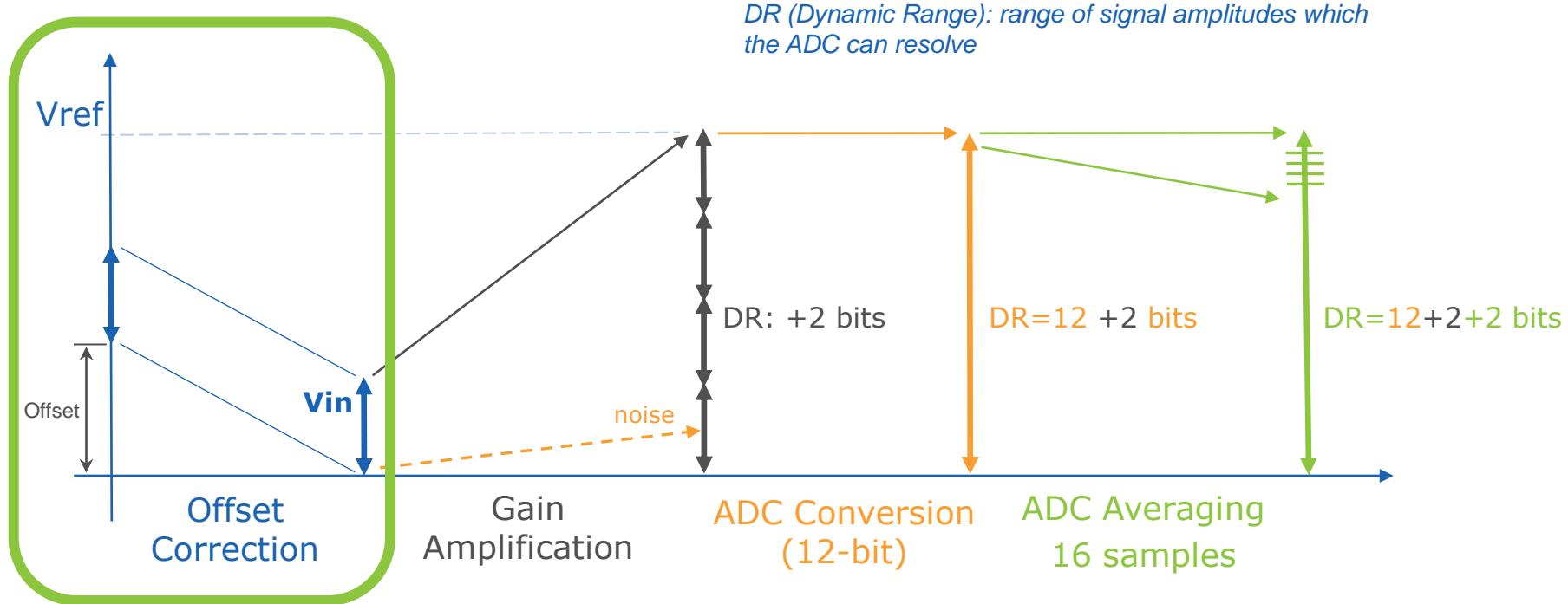
How resolution is increased?

- Resolution is increased by:
 - Correcting the offset
 - Amplifying the gain
 - Then performing digital averaging



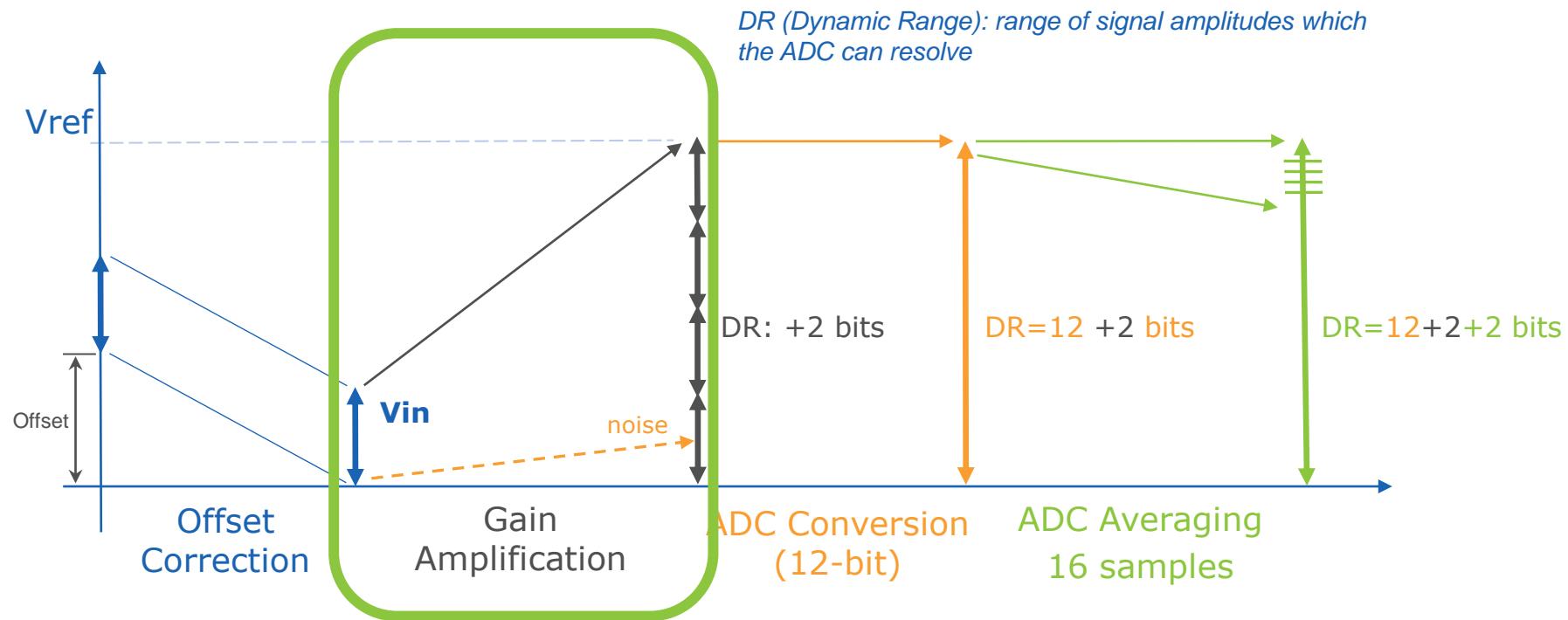
How resolution is increased?

- Offset correction (Single ended mode only)
 - Allows use of the full voltage range
 - Avoid saturation when amplifying the gain



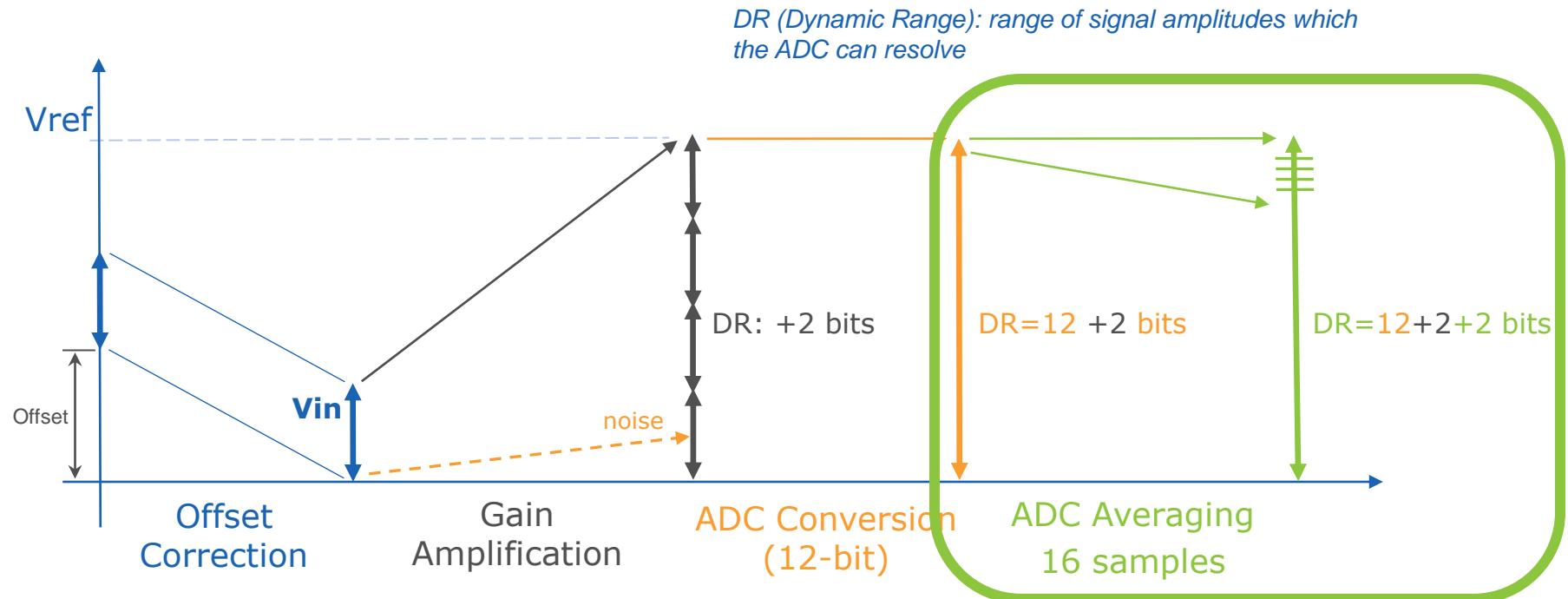
How resolution is increased?

- Gain Amplification
 - Amplify low-amplitude signals before conversion
 - Improve dynamic range



How resolution is increased?

- Digital averaging (Enhanced Resolution Mode is enabled)
 - Increase signal-to-noise ratio, adding resolution bits
 - Noise must be present in the signal (1 to 2 LSB)
 - If not, add noise to the signal



SAM4L Series

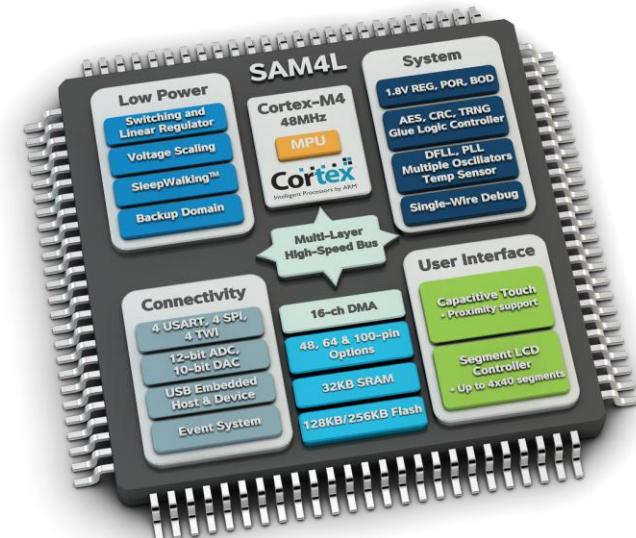
First Cortex-M4 Flash MCU
with PicoPower technology



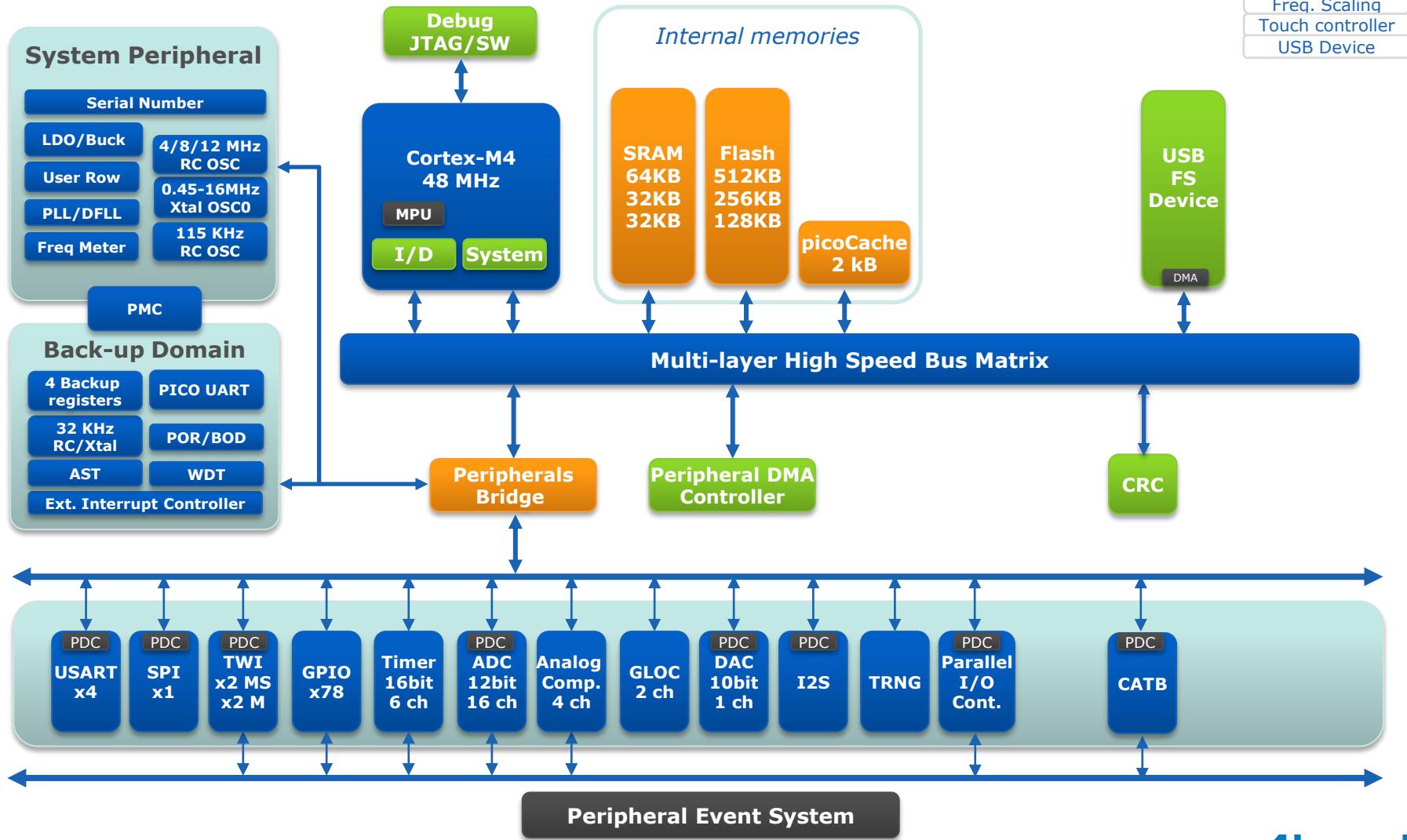
Introducing SAM4L

The world's most power efficient Cortex-M4

- Optimized for Low-Power Applications
 - Industry's lowest power consumption
 - Active mode: down to 95 μ A/MHz
 - RAM retention mode : 1.5 μ A
 - 1.8 – 3.6V operation
 - No degraded performance (up to 48 MHz)
 - Fast wakeup
 - 1.5 μ s
- Integrated Hardware QTouch®
 - Wake up from deep sleep with a touch of a button or proximity
- Integrated LCD
 - 4x40 Segment LCD



SAM4LS Block Diagram



Package

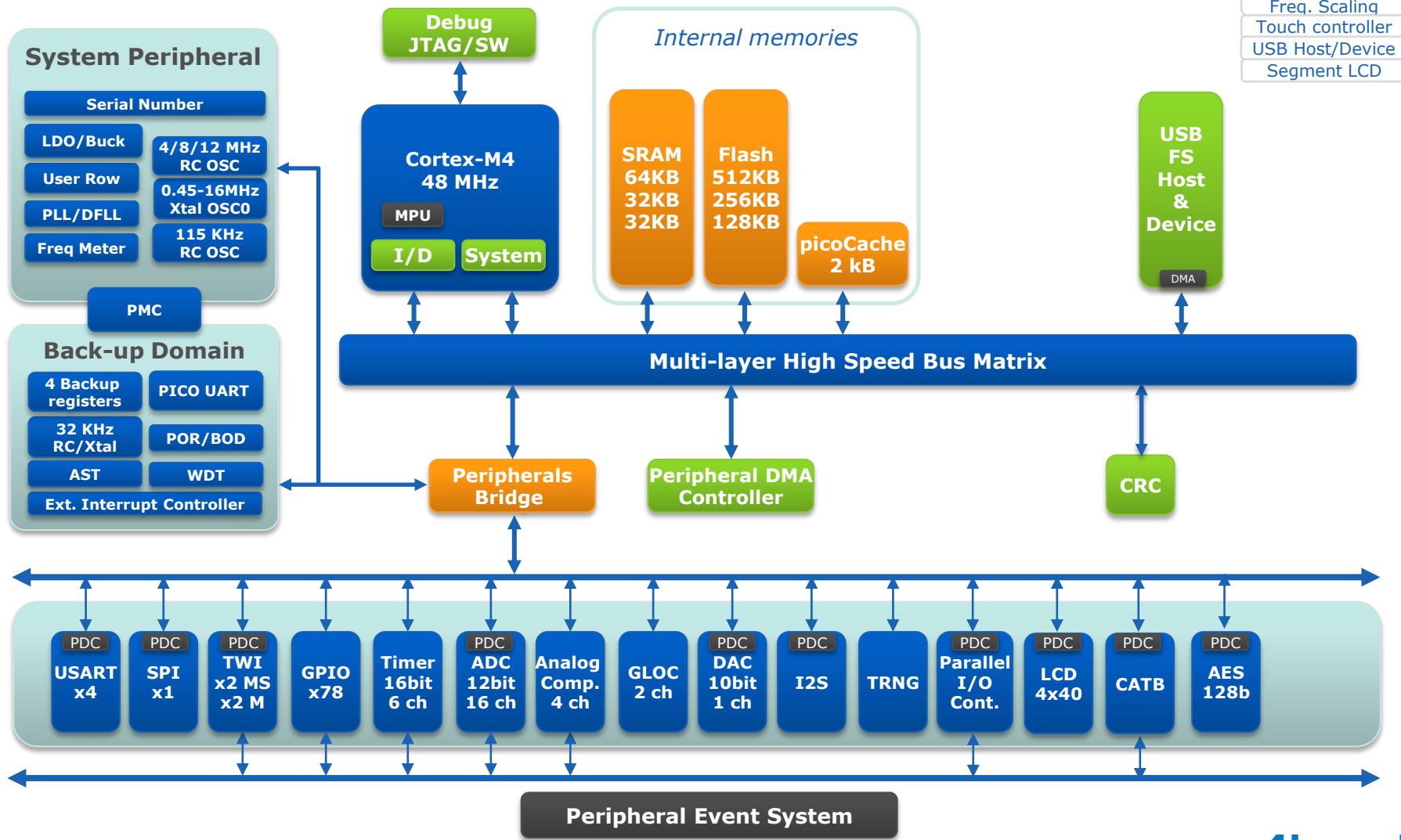
LQFP/QFN48
LQFP/QFN64
LQFP/VFBGA100
WLCSP64 (*)

* Only SAM4L4/2

picoPower

90µA/MHz
1.5µA - Full SRAM
0.5µA - Backup
SleepWalking
Dynamic Freq. Scaling
Touch controller
USB Device

SAM4LC Block Diagram



Package

LQFP/QFN48
LQFP/QFN64
LQFP/VFBGA100
WLCSP64 (*)

* Only SAM4L4/2

picoPower

90µA/MHz
1.5µA - Full SRAM
0.5µA - Backup
SleepWalking
Dynamic Freq. Scaling
Touch controller
USB Host/Device
Segment LCD

SAM3/4 Family Ecosystem

Major Third Parties

- Development Tools:
 - Atmel Studio 6, IAR EWARM, Keil MDK and Code sourcery GNU
- Operating Systems:
 - IAR PowerPac, FreeRTOS, Segger embOS and Micrium µC/OS-II.
- In-System Flash Programming
 - Atmel Studio 6 Flash loader through JTAG/ICE
 - IAR EWARM Flash loader through JTAG/ICE
 - Keil MDK Flash loader through JTAG/ICE
 - SAM-BA through serial, USB or JTAG/ICE
 - Segger J-Flash through JTAG/ICE
- Gang Programming Solutions
 - DataIO, System General, BP Microsystem...



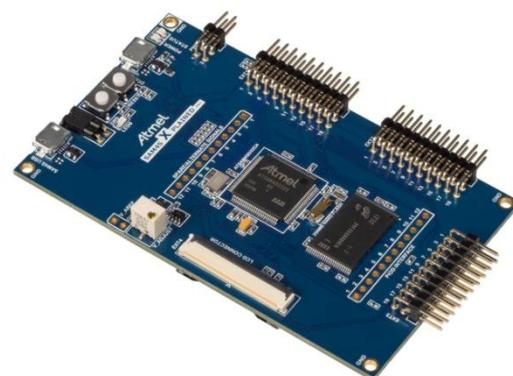
Evaluation Kit for Each Series



SAM3S-EK



SAM3U-EK



SAM4S Xplained Pro

Demo Kit for Each Series

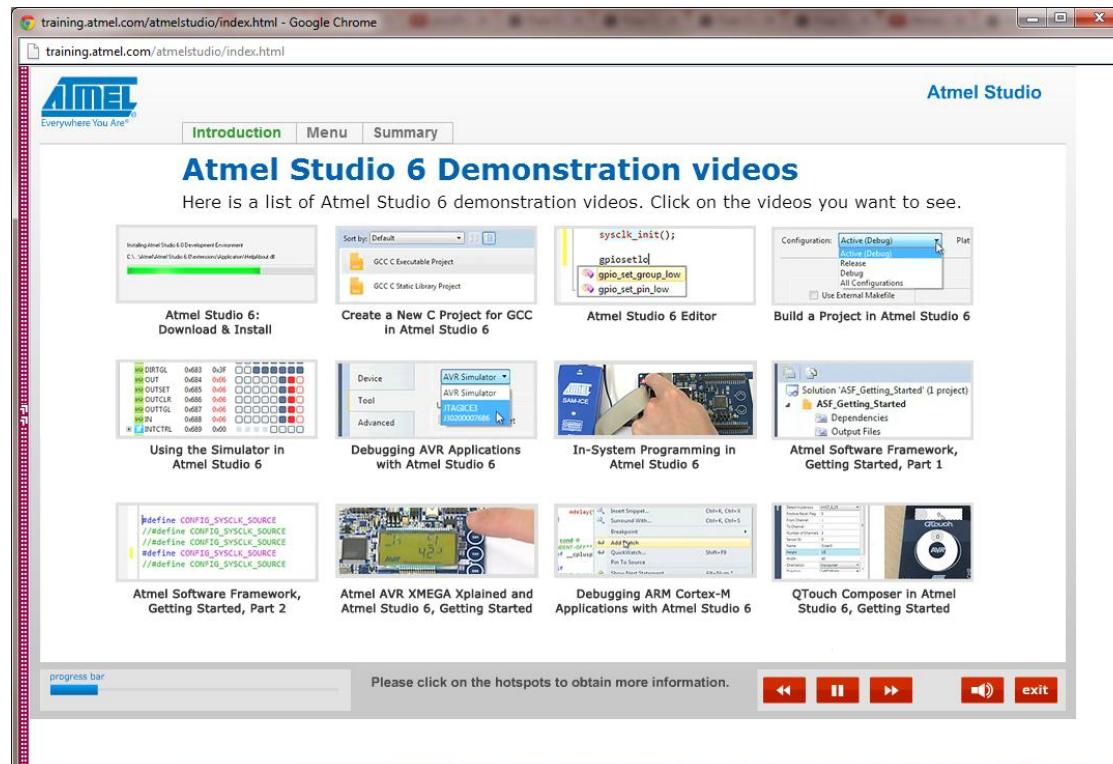
- Based on FreeRTOS
- USB Mass Storage
- Slide Show
- Power Consumption
- Parameters
 - LCD Backlight
 - Temperature
 - Date and Time
- Image Viewer
- QTouch
- Audio with embedded ADC and DAC
 - Register and re-play voice
 - Play melody
- USB audio card



Product Dependant

Atmel Studio

- Integrated Development Platform (IDP)
 - Seamless and easy-to-use environment
 - Full tool chain: write, build and debug applications written in C/C++ or assembly, powerful predictive editor. (**Free!!**)
 - Introductory e-learning at:
<http://training.atmel.com/atmelstudio/index.html>



The screenshot shows a web browser displaying the 'Atmel Studio 6 Demonstration videos' page. The page features a title 'Atmel Studio 6 Demonstration videos' and a subtitle 'Here is a list of Atmel Studio 6 demonstration videos. Click on the videos you want to see.' Below the subtitle, there are several video thumbnails arranged in a grid. The thumbnails include:

- Atmel Studio 6: Download & Install
- Create a New C Project for GCC In Atmel Studio 6
- Atmel Studio 6 Editor
- Build a Project in Atmel Studio 6
- Using the Simulator in Atmel Studio 6
- Debugging AVR Applications with Atmel Studio 6
- In-System Programming in Atmel Studio 6
- Atmel Software Framework, Getting Started, Part 1
- Atmel Software Framework, Getting Started, Part 2
- Atmel AVR XMEGA Xplained and Atmel Studio 6, Getting Started
- Debugging ARM Cortex-M Applications with Atmel Studio 6
- QTouch Composer in Atmel Studio 6, Getting Started

At the bottom of the page, there is a progress bar and a message: 'Please click on the hotspots to obtain more information.' Below the message are navigation buttons: back, forward, volume, and exit.



DOWNLOAD NOW

www.atmel.com/atmelstudio

Atmel Software Framework

- Rich set of proven drivers and code modules developed by Atmel experts to reduce customer design-time.
- Simplifies the usage of MCUs providing an abstraction to the hardware and high-value middlewares.
- >4000 Example projects

ASF is **code-size**-optimized:

- » Multiple ANSI-C compilers supported.
- » Architecture-optimized by Atmel experts.



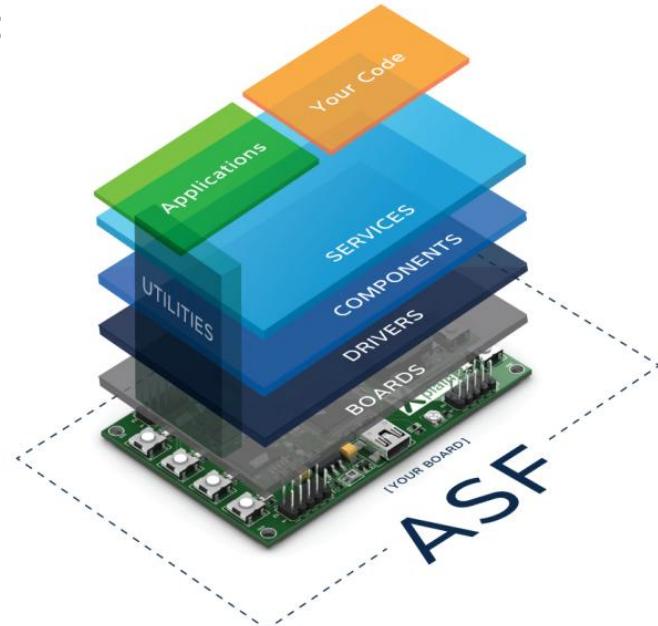
ASF is **performance**-optimized:

- » DMA for communication.
- » Interrupt-driven drivers.
- » Chip-specific features in stacks.



ASF is **low-power**-optimized:

- » Clock masking API, Sleep management API.
- » Support for hardware SleepWalking™ Event controller.
- » Dynamic frequency and voltage scaling.



<http://ASF.atmel.com>

SAM3 Series Software Package (IAR, Keil and GCC)

Project	Description	PDF	KEIL	IAR	GNU
at91lib	At91lib documentation.				
General-shell-project	SAM3U Demo project using general shell.				
basic-adc-project	Voltage acquisition demonstration				
basic-bitbanding-project	Show bit banding feature on SAM3 micro-controllers.				
basic-fatfs-nandflash-project	Demo based on Open Source FAT filesystem reading/writing files to Nandflash				
basic-fatfs-project	Demo based on Open Source FAT filesystem: FatFs				
basic-fatfs-sdcard-project	Demo based on Open Source FAT filesystem reading/writing files to a SD card				
basic-internalflash-project	Demonstrates the features of the Embedded Flash Controller (EFC/EEFC).				
basic-nandflash-project	Erases and writes an external NandFlash memory chip.				
basic-parallel-lcd-project	This example demonstrates how to use parallel LCD.				
basic-pwm2-project	Makes one or more LEDs glow using a PWM signal, duty cycles are updated by PDC.				
basic-rtc-project	Demonstrates basic usage of the Real-Time Clock (RTC) peripheral.				
basic-rtt-project	Demonstrates basic usage of the Real-Time Timer (RTT) peripheral.				
basic-sdcard-project	Performs read and write tests on a SD card connected to the evaluation board.				
basic-sdmmc-project	Performs initial, read, write, boot mode, boot partition access tests on a SD/MMC card connected to the evaluation board.				
basic-sdmmc-test-project	SD/MMC card test collections to the evaluation board.				
basic-slowclock-project	Switch the slow clock from the internal RC oscillator to the external 32.768kHz crystal, and inversely.				
basic-ssc-i2s-wm8731-project	Plays sound with the SSC in I2S mode, through an on-board WM8731 Codec.				
basic-touchscreen-project	Enables the user to draw on the LCD with a stylus using the touchscreen.				
basic-twi-eeprom-project	Reads and writes an external TWI serial EEPROM.				
basic-twi-tempsensor-project	Operate tempsensor using twi				
basic-usart-hw-handshaking-project	Regulates the speed of a USART file transfer using RTS/CTS hardware handshaking.				
getting-started-project	Details basic operations with AT91SAM device				
test-chip-id-project	Read and print chip's ID and features				
test-power-consumption-sam3-project	Test the core consumption of sam3				
	This software acts as a bridge between a USART and IISART connections. A virtual				

Useful Information on atmel.com

- Hardware files for evaluation kits,
 - BOM, schematics and PCB files;
- Schematics Check List Application Notes
 - http://www.atmel.com/dyn/products/app_notes_v2.asp?family_id=605#Design_Considerations
- Ibis models for Signal Integrity (SI) simulation
- BSD files for boundary scan test
- MCU Support Center (FAQs, technical support...)
 - <http://support.atmel.no/bin/customer>

SAM3/4 Series on AT91.com

- Easy access to all relevant information and community resources including discussion forums

Product Selection Table

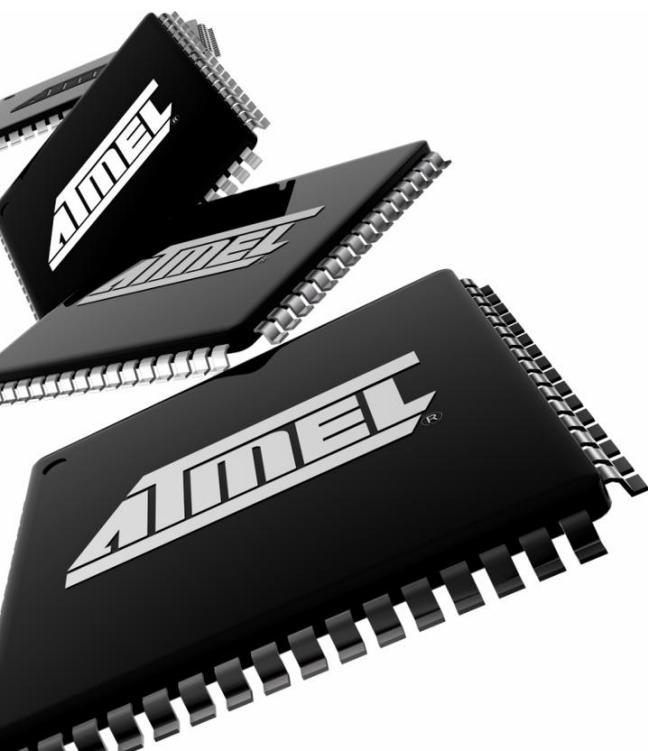
Product Name	Flash	SRAM	Clock Speed	Package
SAM3S4C	256 Kbytes	48 Kbytes	64 MHz	LQFP100 / BGA100
SAM3S4B	256 Kbytes	48 Kbytes	64 MHz	LQFP64 / QFN64
SAM3S4A	256 Kbytes	48 Kbytes	64 MHz	LQFP48 / QFN48
SAM3S2C	128 Kbytes	32 Kbytes	64 MHz	LQFP100 / BGA100
SAM3S2B	128 Kbytes	32 Kbytes	64 MHz	LQFP64 / QFN64
SAM3S2A	128 Kbytes	32 Kbytes	64 MHz	LQFP48 / QFN48
SAM3S1C	64 Kbytes	16 Kbytes	64 MHz	LQFP100 / BGA100
SAM3S1B	64 Kbytes	16 Kbytes	64 MHz	LQFP64 / QFN64
SAM3S1A	64 Kbytes	16 Kbytes	64 MHz	LQFP48 / QFN48

Datasheet	SAM3S Datasheet
Evaluation Kit	SAM3S Evaluation Kit
Software Package	SAM3S Software Package
In-System-Programing (ISP)	AT91-ISP
PCB Schematic Checklist	N/A
PLL Filter Calculator	PLL Filter Calculator (ZIP file)

Product Name	QFP Package		QFN Package		BGA Package	
	IBIS	BSD	IBIS	BSD	IBIS	BSD
SAM3S4C	LQFP100_IBIS	LQFP100_BSD	N/A	N/A	BGA100_IBIS	BGA100_BSD
SAM3S4B	LQFP64_IBIS	LQFP64_BSD	QFN64_IBIS	QFN64_BSD	N/A	N/A
SAM3S4A	LQFP48_IBIS	LQFP48_BSD	QFN48_IBIS	QFN48_BSD	N/A	N/A

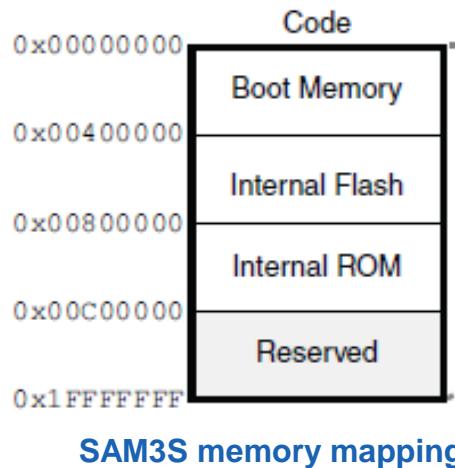
SAM3S Series Technical Data - AT91SAM3S04

SAM3/4 Boot Strategies & Programming solutions



Boot Strategies (except SAM4L)

- SAM3 and SAM4 provide 2 possibilities
 - Boot from the embedded ROM (**SAM-BA Boot**)
 - Boot from the embedded flash (**User application**)
- The boot selection is done by setting/clearing the GPNVM1 bit
 - Specific commands in the EEFC
 - Asserting the ERASE pin will clear GPNVM bits.
 - Processor reset needed



SAM-BA Boot Overview

- SAMBA Boot is the internal programming interface for any internal/external memory.
- SAMBA Boot initialize the device as follow:
 - 1. Stack setup
 - 2. Setup the Embedded Flash Controller
 - 3. External Clock detection (crystal or external clock on XIN)
 - 4. If external crystal or clock with supported frequency, allow USB activation
 - 5. Else, does not allow USB activation and use internal 12 MHz RC oscillator
 - 6. Main oscillator frequency detection if no external clock detected
 - 7. Switch Master Clock on Main Oscillator
 - 8. C variable initialization
 - 9. PLLA setup: PLLA is initialized to generate a 48 MHz clock
 - 10. PLLB setup in case of USB activation allowed
 - 11. Disable of the Watchdog
 - 12. Initialization of UART0 (115200 bauds, 8, N, 1)
 - 13. Initialization of the USB Device Port (in case of USB activation allowed)
 - 14. Wait for one of the following events
 - Check if USB device enumeration has occurred
 - Check if characters have been received in UART0
 - 15. Jump to SAM-BA Monitor

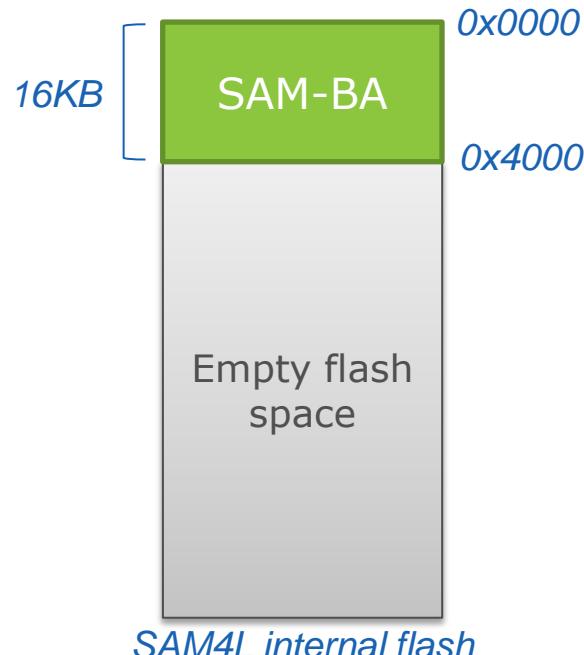
SAM-BA Boot: Hardware & Software constraints

- SAM-BA Boot uses the first 2048 bytes of the SRAM for variables and stacks. The remaining available size can be used for user's code.
- USB requirements: External Crystal or External Clock with frequency of (product dependant):
 - 11,289 MHz
 - 12,000 MHz
 - 16,000 MHz
 - 18,432 MHz
- UART0 requirements: None
 - URXD0 (PA9) and UTXD0 (PA10) are driven during execution
- External clock must be a 1.8V square wave signal
 - Check « schematic checklist » app note for more details

SAM-BA Boot Overview on SAM4L

Difference with other SAM4 devices

- SAM4L devices comes pre-loaded with SAM-BA boot in flash
 - SAM-BA boot stored in ROM on other SAM4 devices
- By default SAM-BA flash region [0x0000 to 0x4000] is locked
 - Unlock SAM-BA flash region before erasing it if whole flash capacity is needed for user application



Programming solutions

- Development Tools such as Atmel Studio, IAR, Keil integrate their own flash loaders utility to flash the application during debug phase.

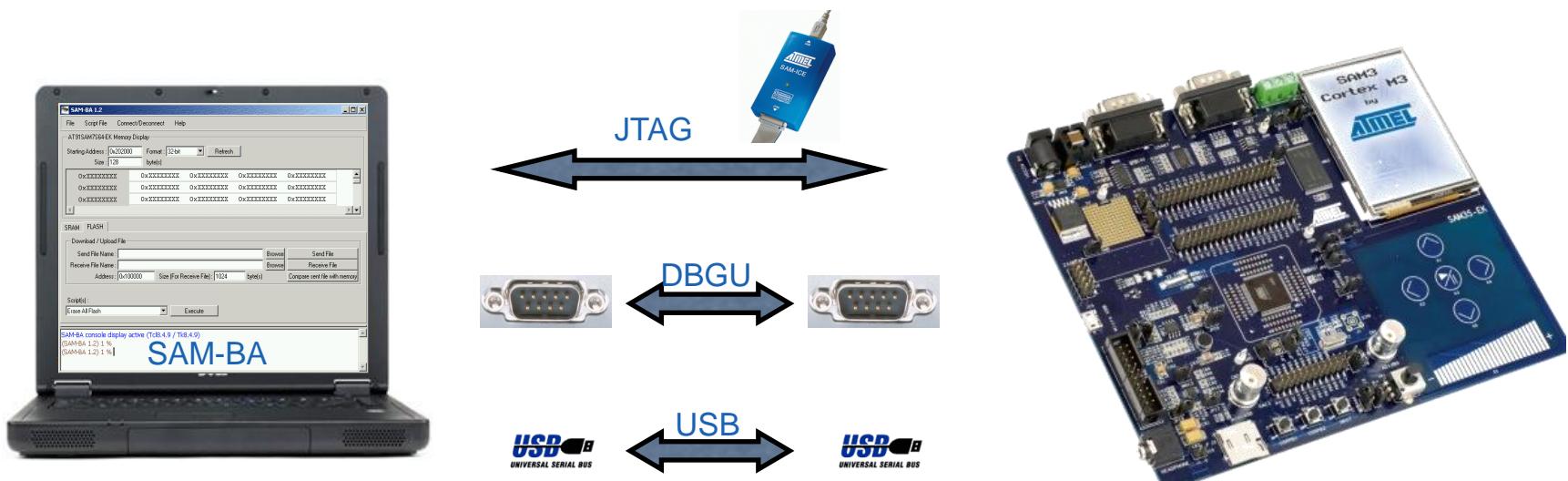


- J-Flash from Segger can be used to program the on-chip flash memory
- SAM-BA.dll: Atmel's Free solution for customers to create their own GUI Interfaces
- Gang Programmers: support for our whole flash-based microcontroller thanks to our FFPI.



SAM-BA GUI

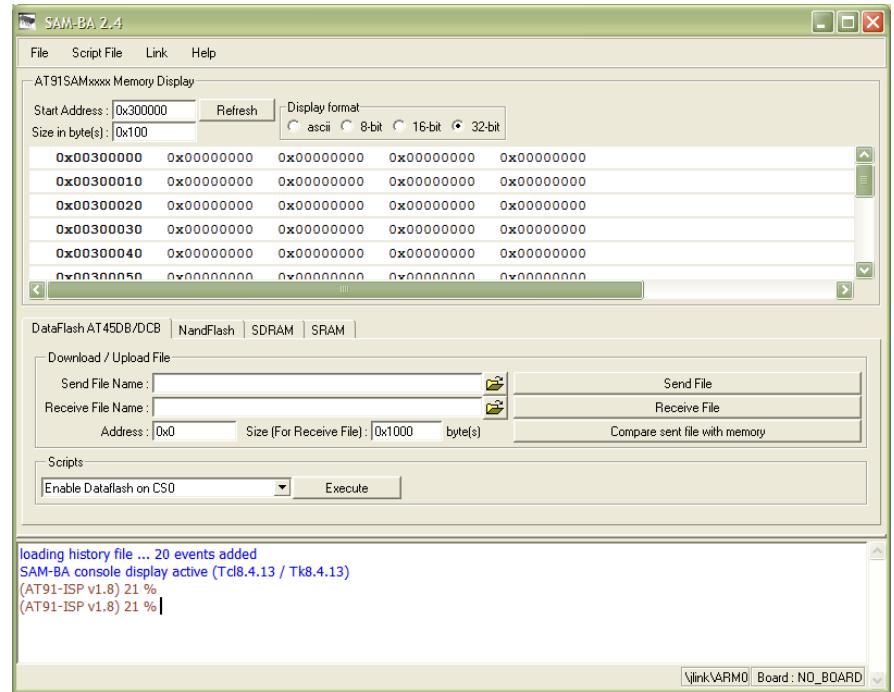
- SAM-BA UI provides In-System Programming solutions for on-chip and/or on-board memories
- Support many communication channels
 - USB, Serial (DBGU) with SAM-BA Boot running out of the target
 - JTAG ICE Port (no need for SAM-BA boot)
- Customizable
 - Other ISP solution can use SAMBA_DLL (Custom GUI)
 - Add support for custom boards or memories



SAM-BA GUI

- Customizing SAM-BA is possible by adding or modifying TCL scripts files

Create your own board
Add memory modules
Modify Memory Algorithms



- Command Line Mode: allows memory programming without any GUI interaction

IAP - In Application Programming

- The IAP feature is a function located in internal ROM
 - Can be called at any time by user application and executed out of ROM
- Allows flash programming while the code is running out of flash
 - No need to have programming routines in SRAM
- When called, this function sends the desired FLASH command to the EEFC and waits for the Flash to be ready
- This function takes one argument in parameter: the command to be sent to the EEFC
- The IAP function entry point is retrieved by reading the NMI vector in ROM (0x00800008).



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