



SAM4S Low Power Modes

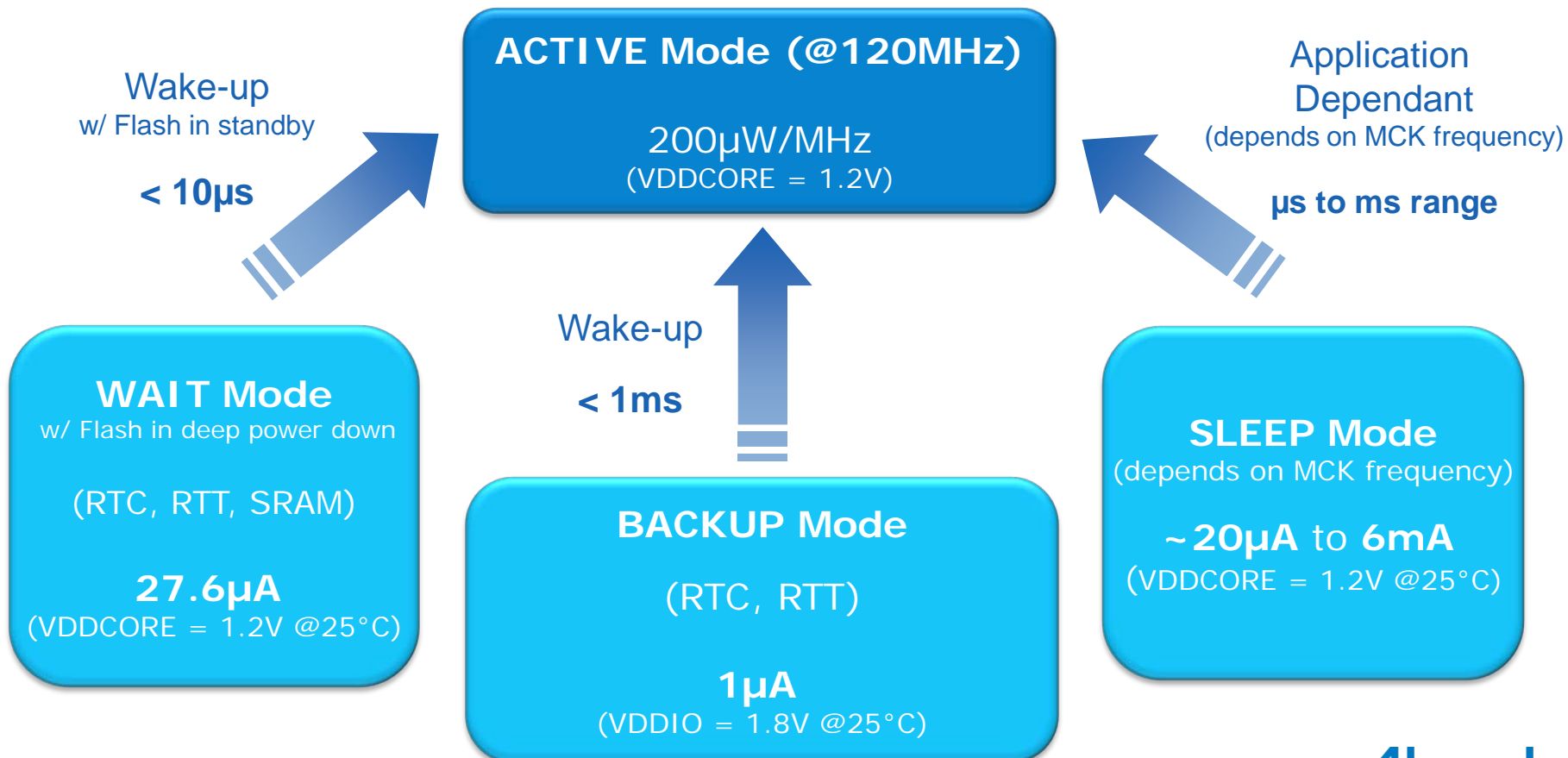
SAM4S Low Power Modes

Introduction

- The SAM4S embeds:
 - A Power Management Controller (PMC) to control clocking of the system.
 - A Supply Controller (SUPC) to control supply voltages and manage the different low power modes.
- Provides a wide range of low power modes allowing to choose the best trade-off between:
 - Power Consumption
 - Wake-up time
 - Clock frequency
 - Wake-up sources
 - Context saving (SRAM retention)

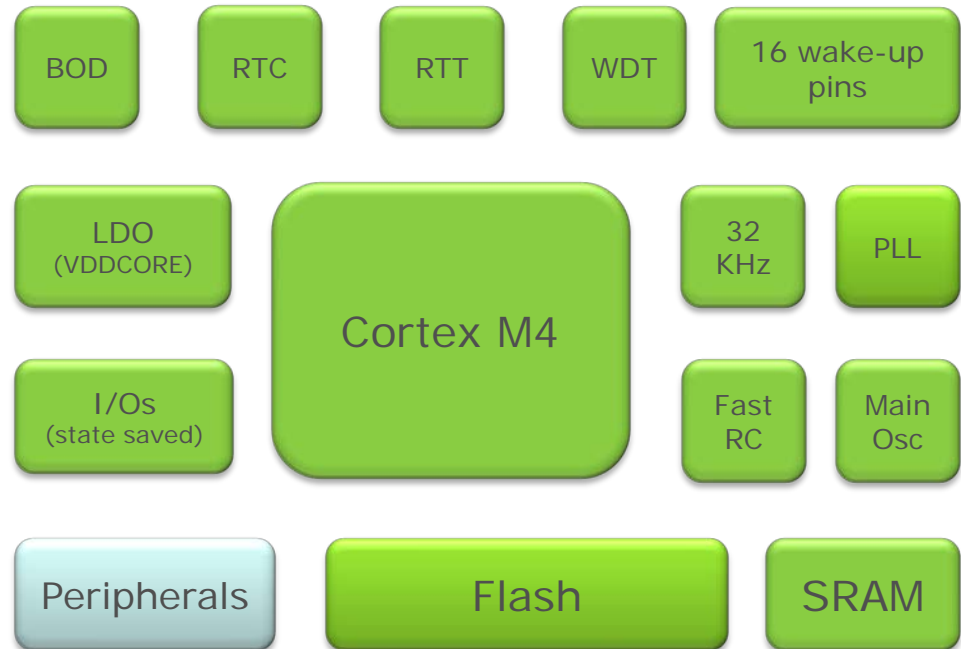
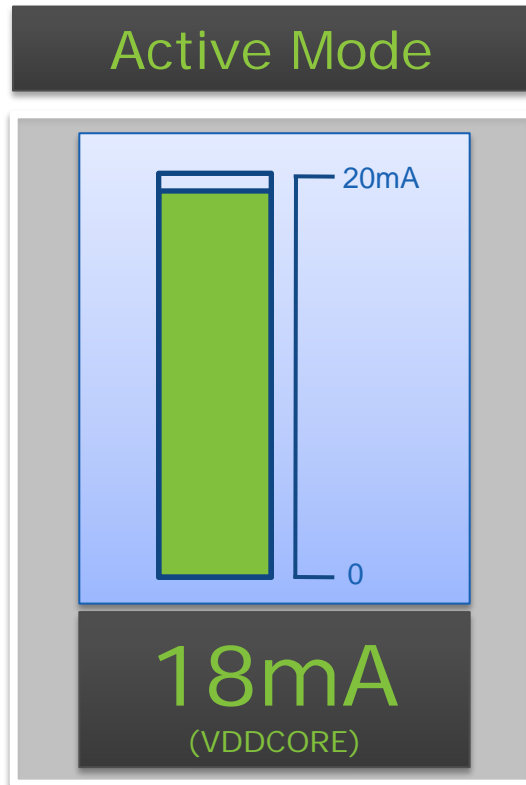
Extended Supply Range and Low Power Modes

- Operates from 1.62V to 3.6V extended supply range.
 - True $1.8V \pm 10\%$ operation (no Analog, no USB)



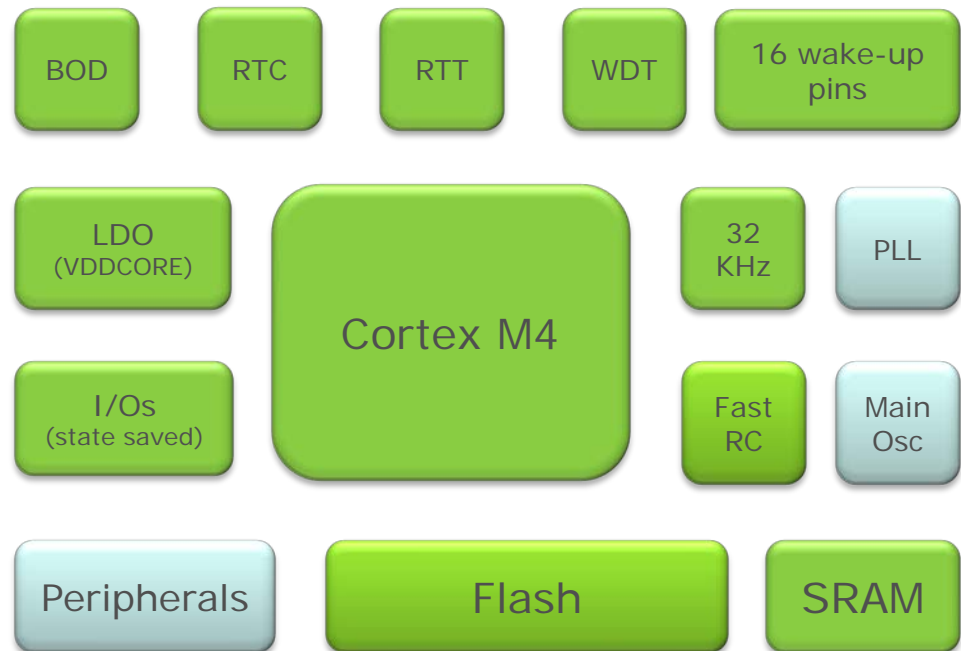
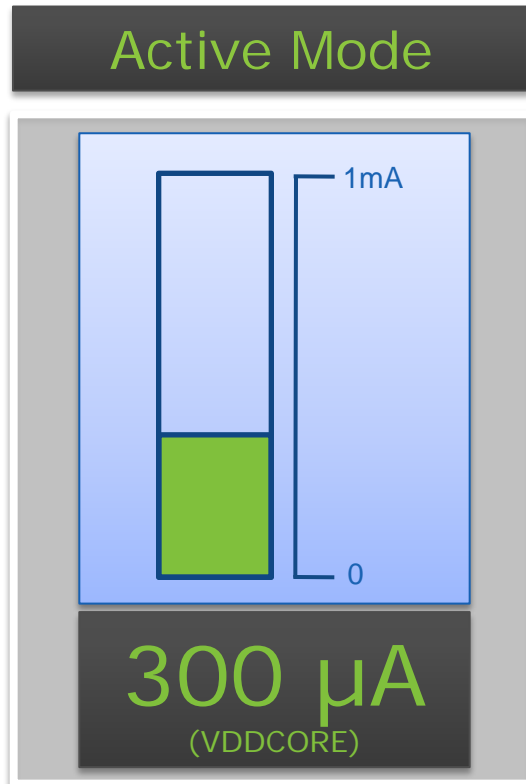
SAM4S Active Mode

MCK@120MHz / VDDCORE@1.2V (64-bit Flash Access)



SAM4S Active Mode

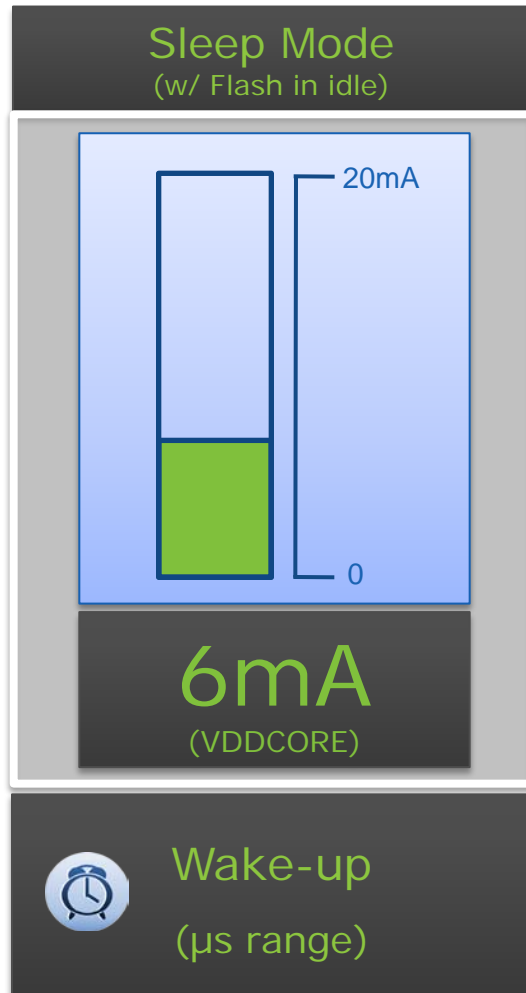
MCK@500kHz / VDDCORE@1.2V (64-bit Flash Access)



SAM4S Sleep Mode

MCK@120MHz / VDDCORE@1.2V (64-bit Flash Access)

Interrupts wake-up capability



* At least, one must be enabled for interrupt



Any Interrupts

Not Clocked

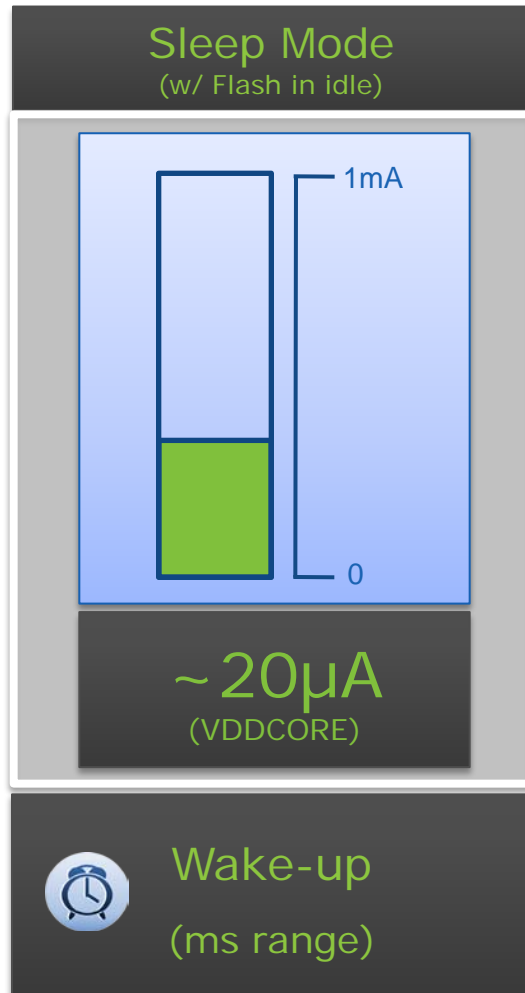
Clocked

Not Powered

SAM4S Sleep Mode

MCK@500Hz / VDDCORE@1.2V (64-bit Flash Access)

Interrupts wake-up capability



* At least, one must be enabled for interrupt



Any Interrupts

Not Clocked

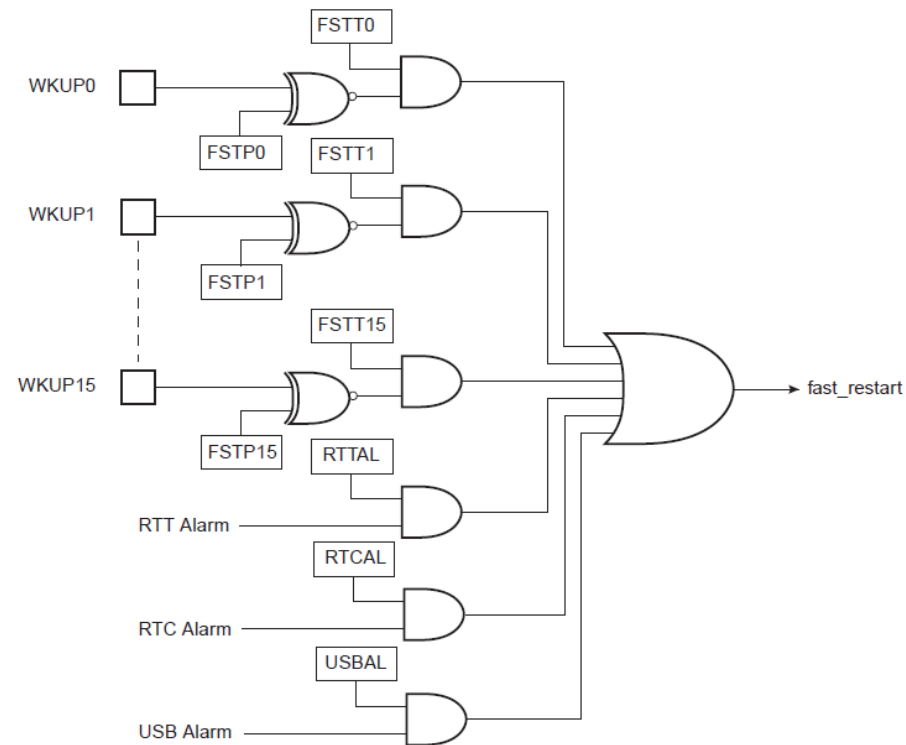
Clocked

Not Powered

SAM4S Wait Mode

Fast Startup

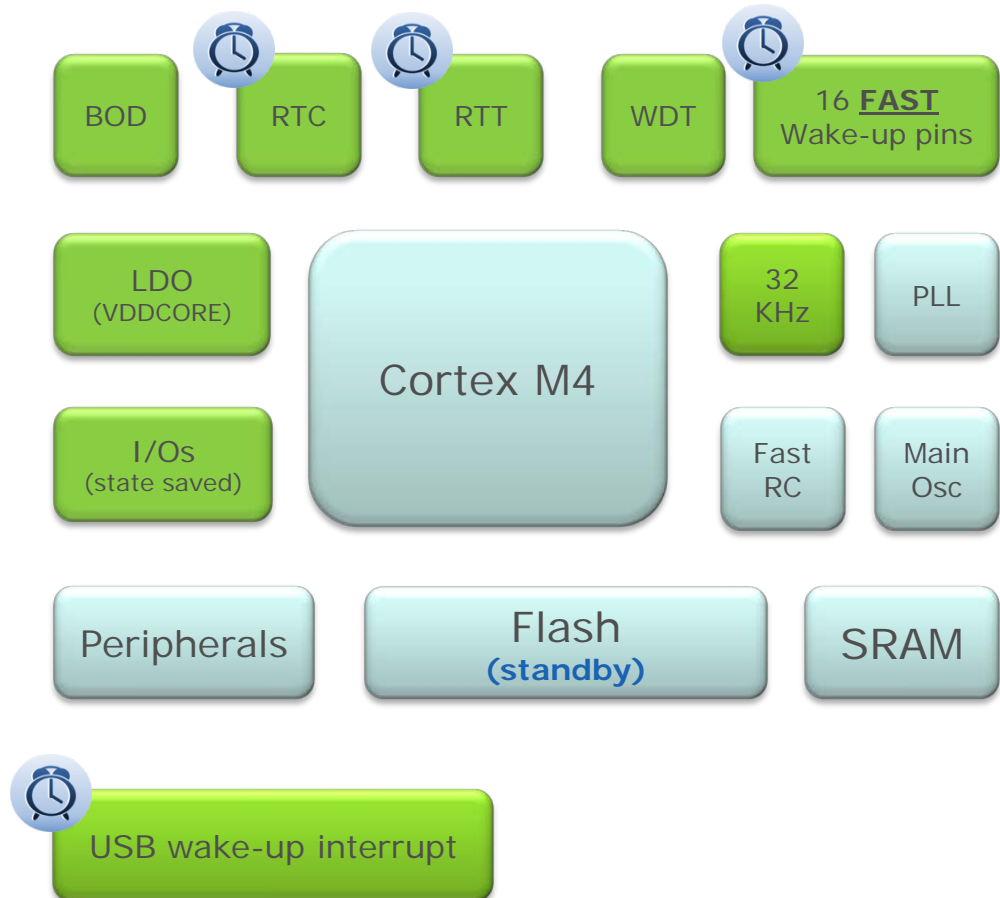
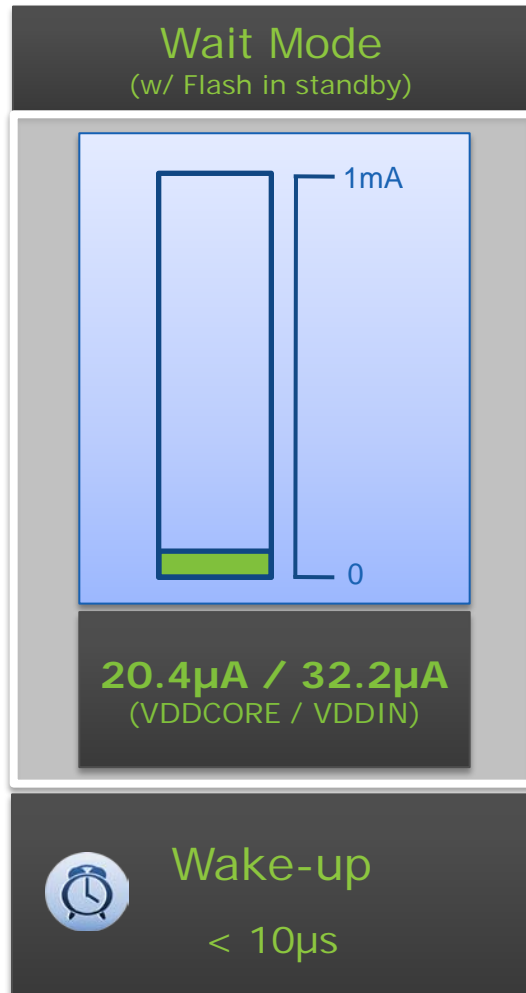
- SAM4S allows the processor to restart in a few microseconds while the processor is in Wait mode.
- Occurs upon detection of a low level on one of the wake-up inputs:
 - WKUP0 to 15
 - USB wake-up
 - RTC alarm
 - RTT alarm
- fast_restart signal fully asynchronous
- fast_restart assertion allows PMC to:
 1. Restart 4MHz Fast RC
 2. Switch Master Clock (MCK) on the Fast RC
 3. Restart Processor Clock (HCLK)



SAM4S Wait Mode w/ Flash in standby mode

MCK stopped / VDDCORE@1.2V

Fastest Wake-up
with SRAM retention



Not Clocked

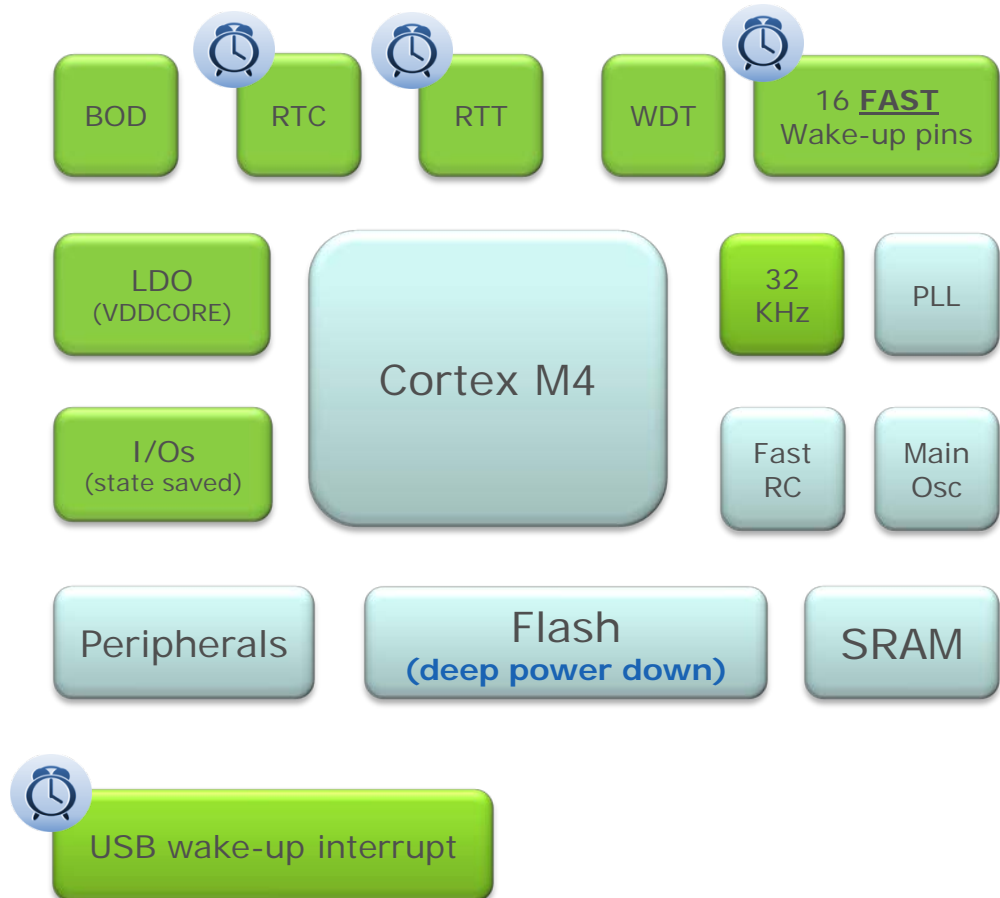
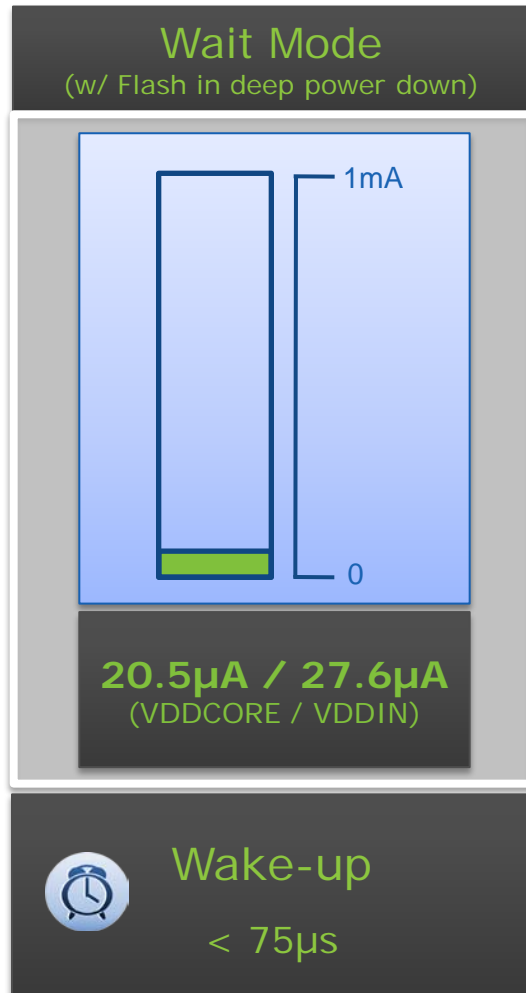
Clocked

Not Powered

SAM4S Wait Mode w/ Flash in deep power down mode

MCK stopped / VDDCORE@1.2V

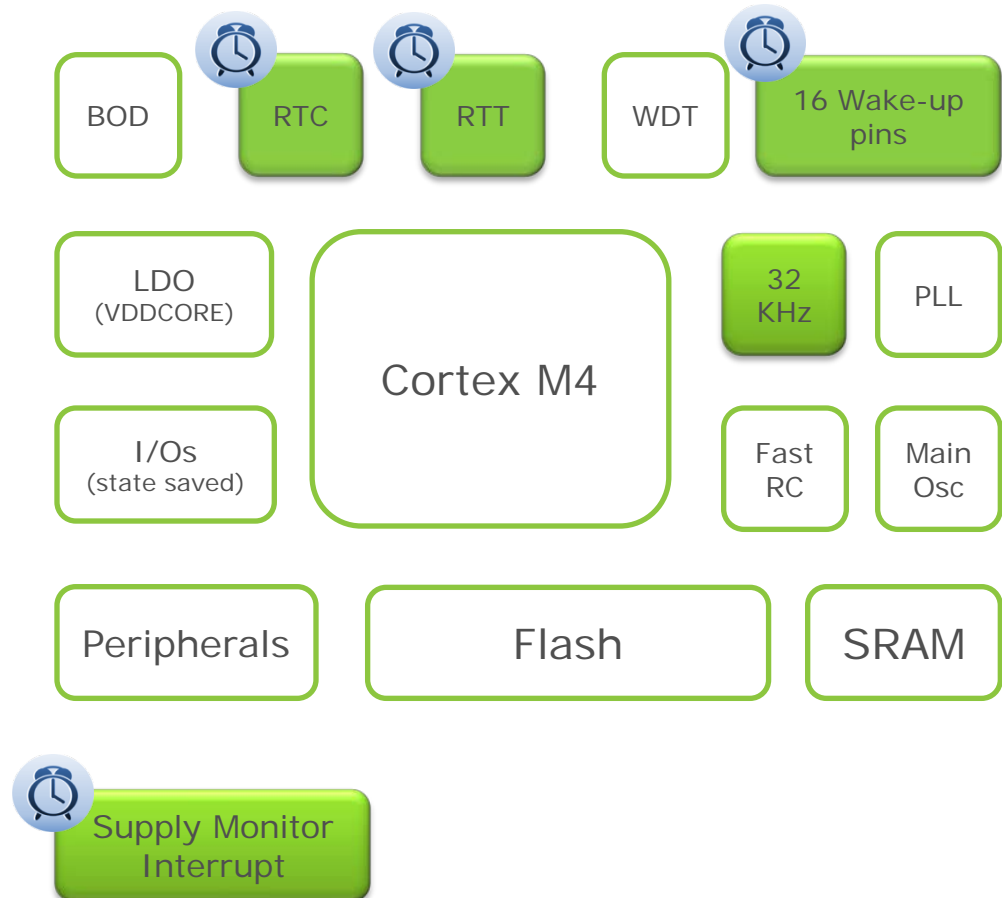
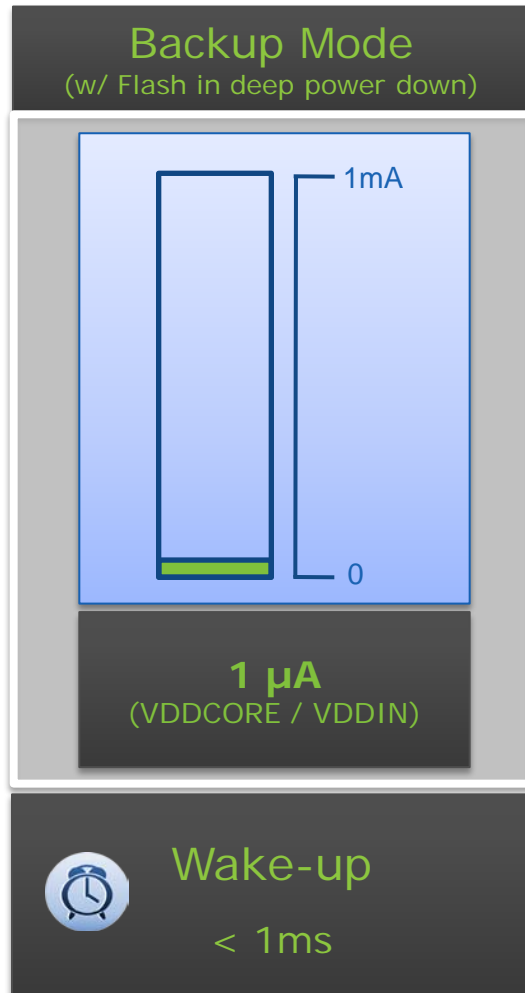
Lowest Power Consumption
with SRAM retention



SAM4S Backup Mode

MCK stopped / VDDCORE powered down

Lowest Power Consumption



SAM4S Low Power Modes Summary Table

| | Backup | Wait | Sleep |
|---|--|--|---|
| SUPC, 32kHz, POR, Backup Regs, RTC, RTT | ON | ON | ON |
| Regulator | OFF | ON | ON |
| Core Memories Peripherals | OFF (not powered) | Powered (but not clocked) | Powered (but not clocked) |
| Mode entry | SLEEPDEEP bit = 1 + VROFF bit = 1 | SLEEPDEEP bit = 0 + WAITMODE bit = 1 + LPM bit = 1 + FLPM bits = 00 or 01 | WFI + SLEEPDEEP bit = 0 + LPM bit = 0 |
| Potential wake-up sources | WUP0-15 pins SM alarm RTC alarm RTT alarm | Fast start-up WUP0-15 pins, RTC alarm RTT alarm USB wake-up | Any Interrupts (WFI) |
| Core at wake-up | Reset | Clocked back | Clocked back |
| PIO state while in low power mode | Previous state saved | Previous state saved | Previous state saved |
| PIO state at wake-up | Input with pull-up | Unchanged | Unchanged |
| Consumption | 1 μ A typical | 20.4 μ A typical | Depends on Clock |
| Wake-up time | 1ms typical | < 10 μ s | Depends on Clock |



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