

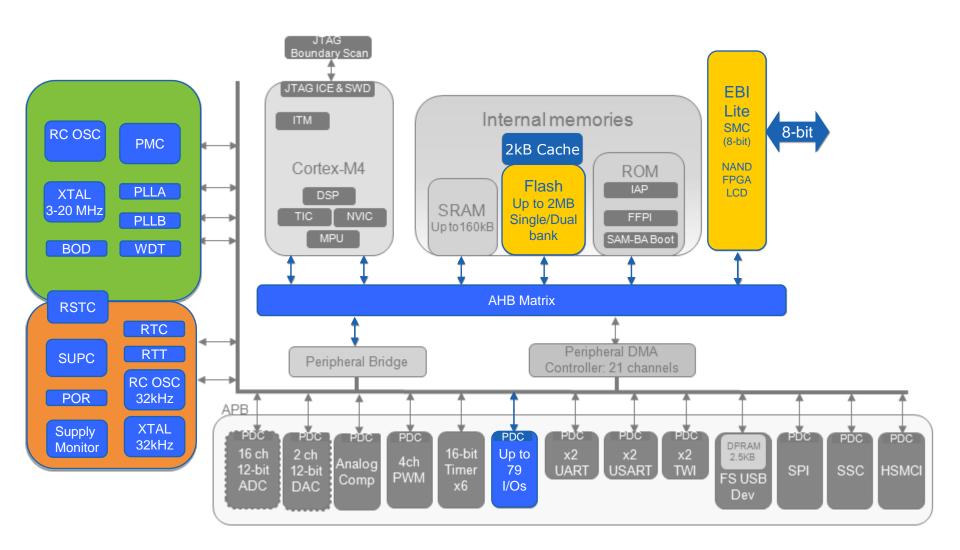
## **SAM4S System Peripherals**

#### **Presentation Outline**

- SAM4S System Peripherals Block Diagram
- AHB Matrix
- System Controller
  - Supply Controller
  - Reset Controller
  - Power Management Controller
  - Watchdog Timer
  - Real Time Clock and Real Time Timer
- Static Memory Controller
- PIO Controllers



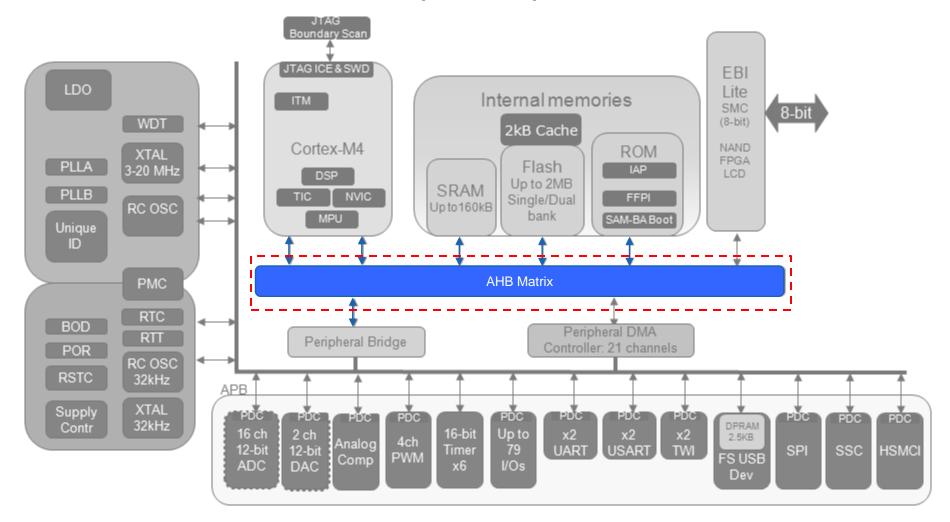
# **SAM4S System Peripherals Block Diagram**





#### **AHB Matrix**

(MATRIX)





#### **AHB Matrix**

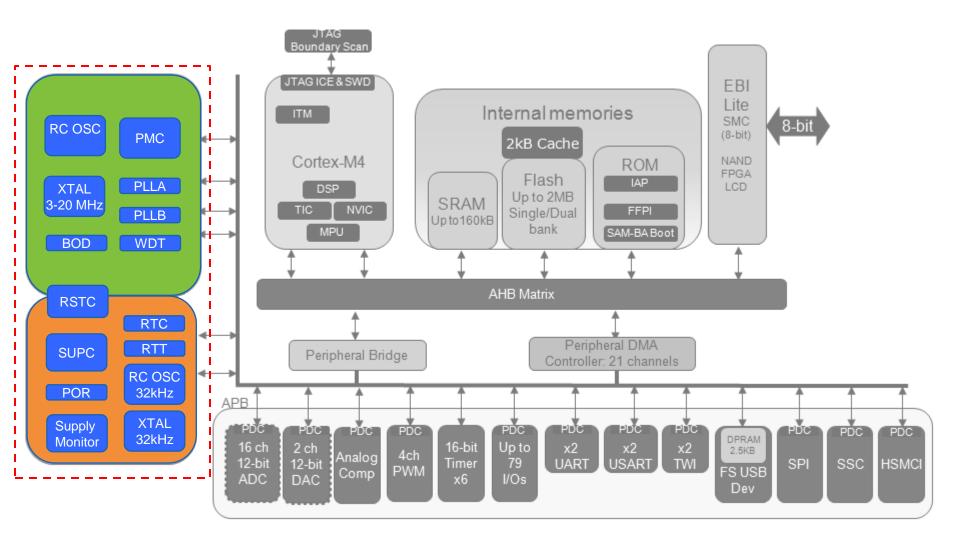
#### Overview

 The 4-layer Bus Matrix increases the system bandwidth by enabling parallel access paths between multiple AHB masters and slaves in the system

Ш		Masters	0	1	2	3
	Slaves		Cortex-M4 I/D Bus	Cortex-M4 S Bus	PDC	CRCCU
	0	Internal SRAM	-	Х	X	X
	1	Internal ROM	X	-	X	X
	2	Internal Flash	X	-	1	X
	3	3 External Bus Interface		Х	X	X
	4 Peripheral Bridge		-	X	X	-

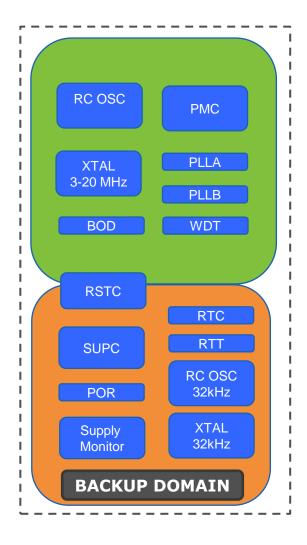
 The AHB Matrix Embeds an Arbitrary system (round robin, fixed priority) and speculative bus granting system for performance improvement according to application peripherals usage.







#### Overview



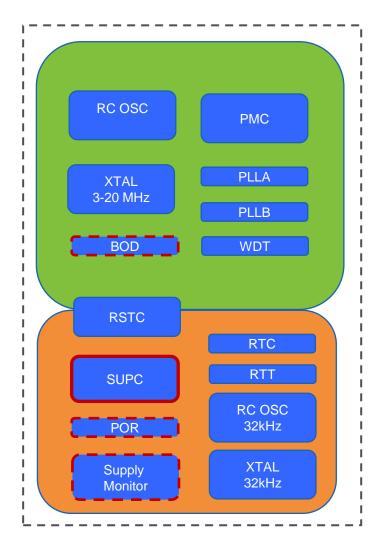
- The System controller (SYSC) is a set of peripherals and controllers that allows handling of key elements of the system :
  - System clocks control (32KHz, PLL, Main clock...)
  - Low Power modes management
  - System reliability (Resets, POR, BOD, Watchdog...)
- Part of the peripherals are supplied by the BACKUP power supply.



Supply Controller (SUPC)



#### Overview



- Controls the embedded voltage regulator and the different power domains of the microcontroller.
- Manages device start-up & power supplies monitoring (POR, BOD, Supply Monitor).
- Controls system Slow clock generation.



#### SAM4S Power Domain

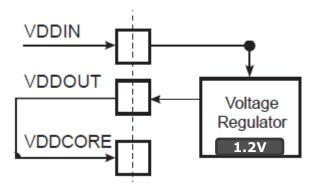
- VDDIN (1.62V to 3.6V): Powers the internal Voltage Regulator, ADC, DAC and Analog Comparator.
- **VDDCORE** (1.08V to 1.32V): Powers the core, the embedded memories and the peripherals.
- **VDDIO** (1.62V to 3.6V): Powers the Backup part, Peripherals I/O lines (Input/Output Buffers), USB transceiver, 32 kHz crystal oscillator its pads.
- **VDDPLL** (1.08V to 1.32V): Powers PLLA, PLLB, the Fast RC and the 3-20MHz main oscillator.



### Internal Voltage Regulator

The voltage regulator is designed to supply the internal core power

supply: VDDCORE.

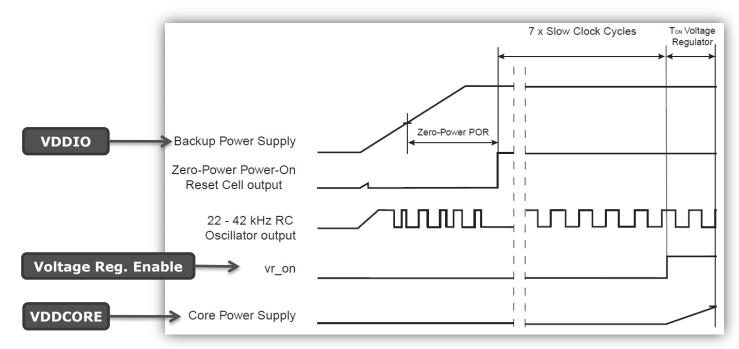


- It features two operating modes:
  - Normal mode: consumes less than 500μA.
  - Standby mode (Backup mode): consumes less than 1μA.
- In normal mode, the regulator has an automatic mode which adjusts its quiescent current depending on the required load current.
  - Quiescent current can go down to 5μA (Wait mode use).



Zero-Power On Reset (POR)

- At startup, the POR maintains its output low as long as the Backup Power Supply (VDDIO) has not reached its target voltage.
  - i.e Supply Controller is reset.

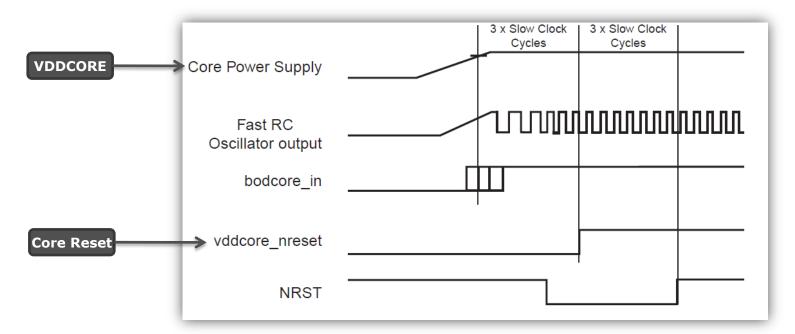


 Then, the Supply controller is started and the MCU voltage regulator is enabled after 7 slow clock cycles.



Brown Out Detector (BOD)

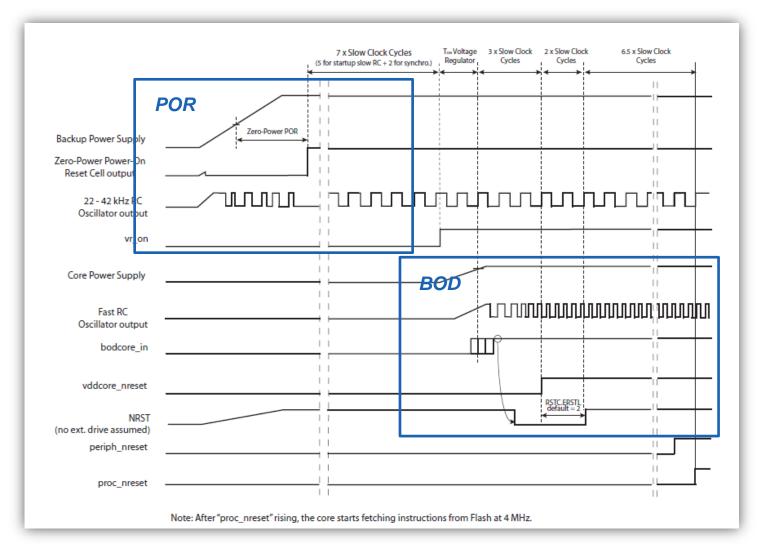
- The Brownout Detector monitors VDDCORE (enabled by default).
  - It releases the core reset at start up 3 cycles after VDDCORE is stabilized.



• It can also generates a core reset if any core voltage drops are detected for more than one Slow Clock cycle.



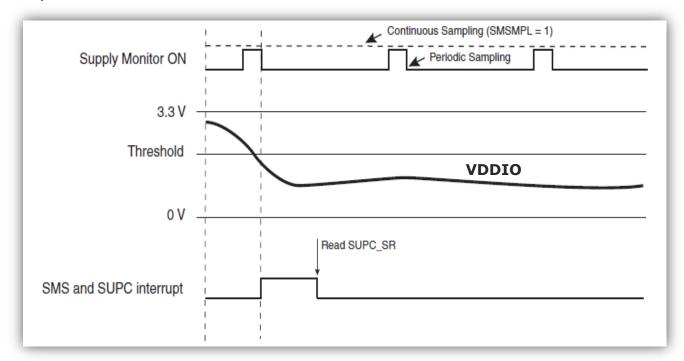
Startup Sequence (General Reset)





### Supply Monitor

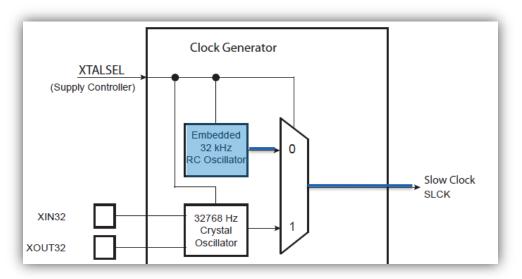
- Prevents the system from falling into an unpredictable state by resetting the core if VDDIO drops below a programmable threshold (from 1.9V to 3.4V).
  - Continuous or Periodic sampling (32, 256, 2048 Slow Clock periods)
  - Can also wake-up the core power supply from SAM4S backup mode.
- Disabled by default





#### Slow Clock Generator

- Supplied as soon as VDDIO is established.
- Several Slow Clock sources are possible:
  - Internal 32 kHz RC Oscillator
  - External 32 kHz crystal on XIN32/XOUT32
  - External clock on XIN32 (bypass mode)
- By default, the internal 32kHz RC is enabled.





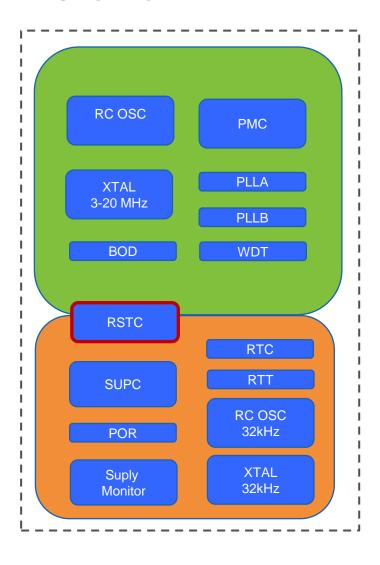
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Reset Controller (RSTC)



#### **SAM4S Reset Controller**

#### Overview



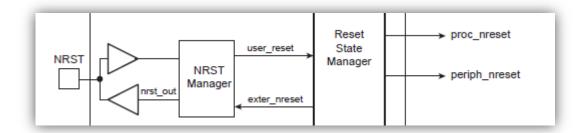
- Manages all Resets of the System, including:
  - General Reset
  - Backup Reset
  - Watchdog reset
  - User reset (NRST pin)
  - Software reset (NRST pin)
- Embeds
  - NRST pin Manager
  - Reset State Manager
    - Status of the latest reset



#### **SAM4S Reset Controller**

### NRST pin Manager

Manages NRST pin in input or output.



- NRST pin in Input mode (enabled by default)
  - Allows MCU to be reset by external components (i.e. User Reset)
  - The user reset is programmable and an interrupt can be generated
- NRST pin in Output mode
  - Allows MCU to reset external components (i.e. Software Reset)
  - The NRST line is driven to low level during a programmable time



#### **SAM4S Reset Controller**

#### Reset State Manager

- The Reset State Manager handles the different reset sources and generates the internal reset signals.
- It reports the reset status in the RSTTYP field of the Status Register

RSTTYP in RSTC_SR	Reset Type	Comments
0	General Reset	First Power up Reset
1	Backup Reset	Return from backup mode
2	Watchdog Reset	Watchdog fault occurred
3	Software Reset	Processor reset required by SW
4	User Reset	NRST pin detected low

 Update of the RSTTYP field is performed when processor reset is released

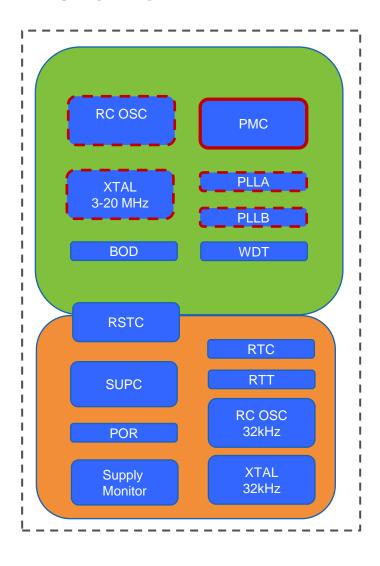


Power Management Controller (PMC)



# **SAM4S Power Management Controller**

#### Overview



- Allows to optimize power consumption by controlling all the clocks of the system.
- Main features:
  - Clock Generator
  - System clocks generation/control
  - Main Crystal Clock Failure Detector to identify an oscillator defect.
  - Possibility to trim the 4/8/12 MHz
    Fast RC Oscillator.

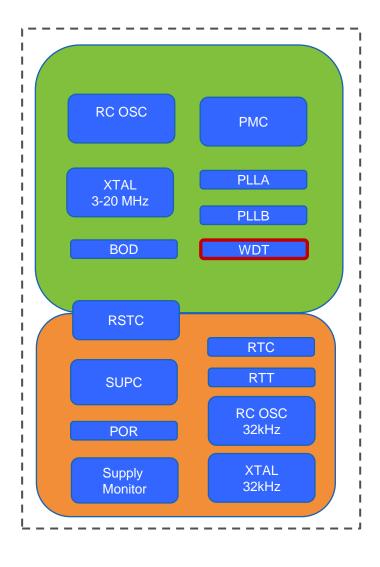


Watchdog Timer (WDT)



## **Watchdog Timer**

#### Overview



- The Watchdog Timer (WDT) can be used to prevent system lock-up if the software becomes trapped in a deadlock.
  - 12-bit down counter based on 32KHz clock
  - Enabled by default after start-up with a period set to its maximum (i.e. 16 seconds).
  - Generates a processor, peripherals and NRST pin resets or a processor reset only.



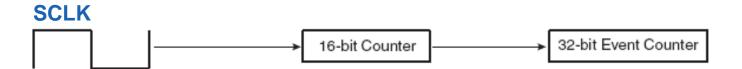
Real Time Clock and Real Time Timer



# **Real Time Timer (RTT)**

#### Overview

- The Real-Time Timer is built around a 32-bit counter fed by the Slow Clock divided by a programmable 16-bit value:
  - RTPRES field of Real-time Mode Register (RTT\_MR)



 It generates a periodic interrupt and/or triggers an alarm on a programmed value.



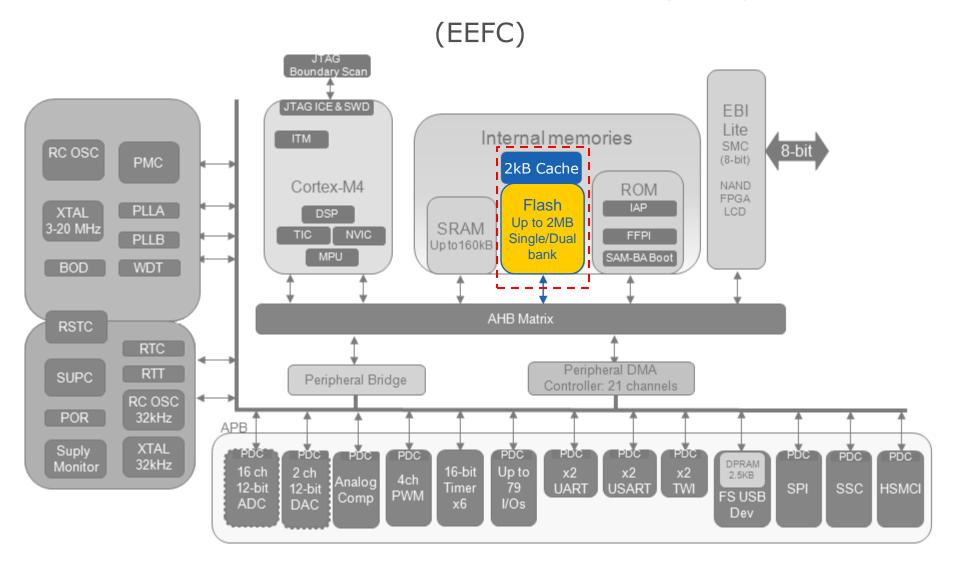
# **Real Time Clock (RTC)**

#### Overview

- Two Hundred Year Gregorian or Persian Calendar with Programmable Periodic Interrupt
- Full Asynchronous Design based on external 32Khz crystal
- Crystal Oscillator drift correction circuitry to compensate temperature variation.
- Waveform Generation capability (1Hz, 32Hz, 64Hz and 512Hz) on RTC Output dedicated pins (RTCOUT0/1).
- On-The-Fly Time and Date Validity Check



#### **Enhanced Embedded Flash Controller**

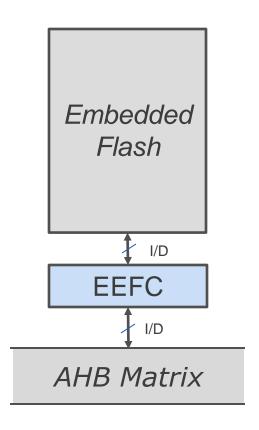




#### **Enhanced Embedded Flash Controller**

#### Overview

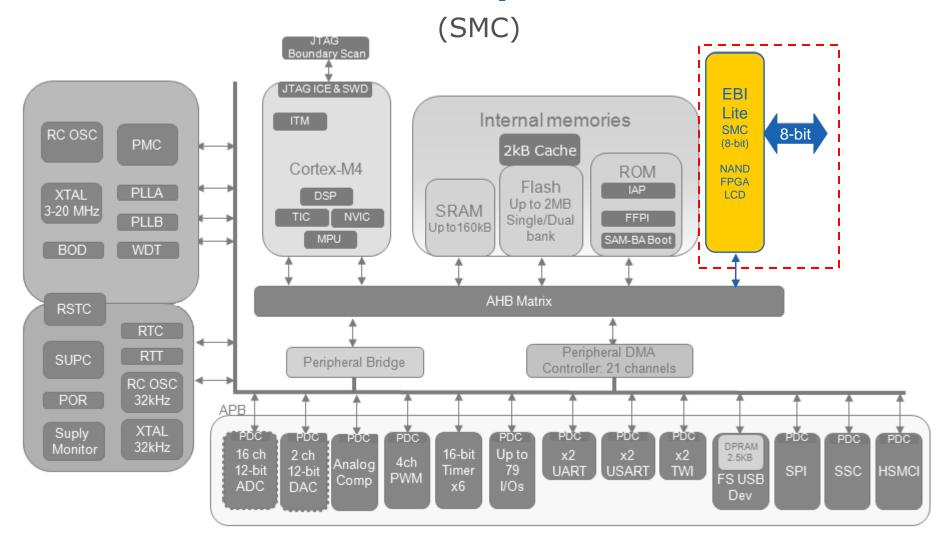
Interfaces the Flash Block with the 32-bit Internal Bus



- Configurable 64/128 bits flash access
- Integrates Code loops optimization
- Integrates Sequential Code Optimization
- Manages :
  - Erases by Plane/Sector/Pages
  - Flash Locking/Unlocking Operations
  - General Purpose NVM bits



## **Static Memory controller**

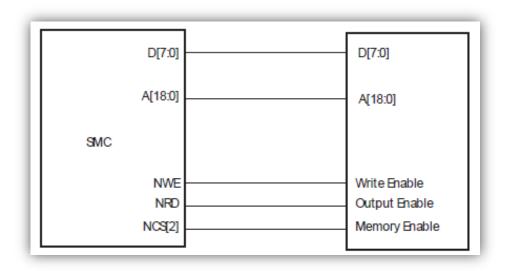




## **Static Memory controller**

#### Overview

 Ensures interfacing between SAM4S and external static memory devices.



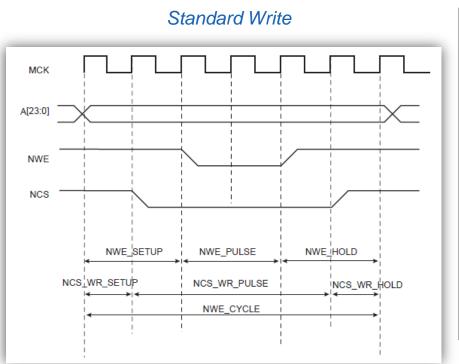
- 8- bit Data Bus
- 4 Configurable chip select
- Scrambling/Unscrambling Functionality
- Programmable wait state
- External Wait Request support
- Asynchronous Read in Page Mode
- Additional NAND Flash logic
- Capable of handling several types of external memories: SRAM,PSRAM, Rom based memories, LCD Module, NOR Flash, NAND Flash, FPGA...

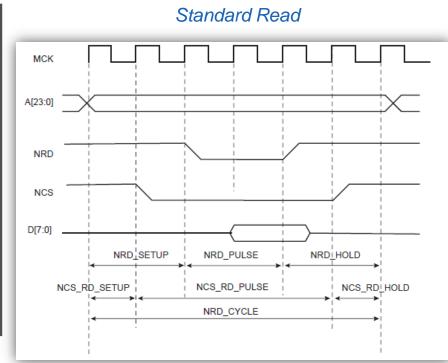


# **Static Memory controller**

### Adjustable Read/Write timings

Adjustable SETUP, HOLD and PULSE timings

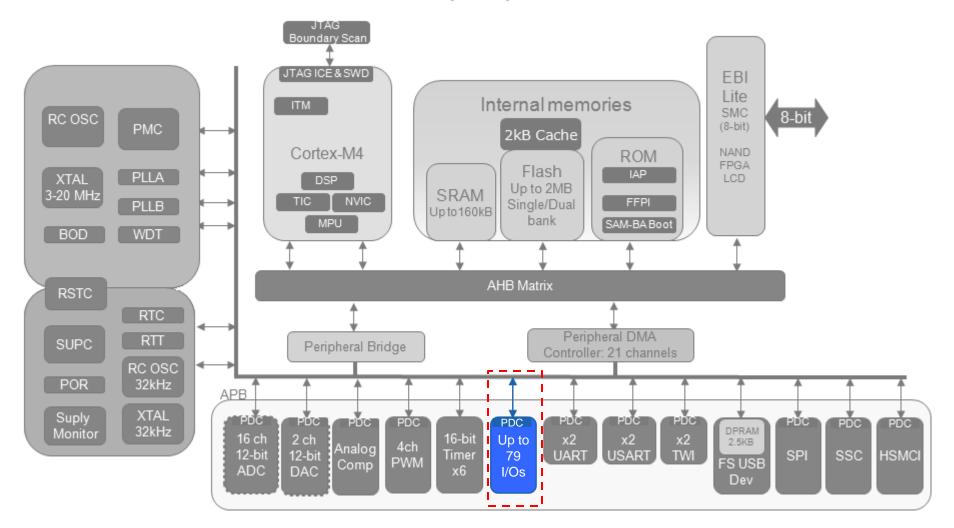




Allows flexibility in communication



(PIO)



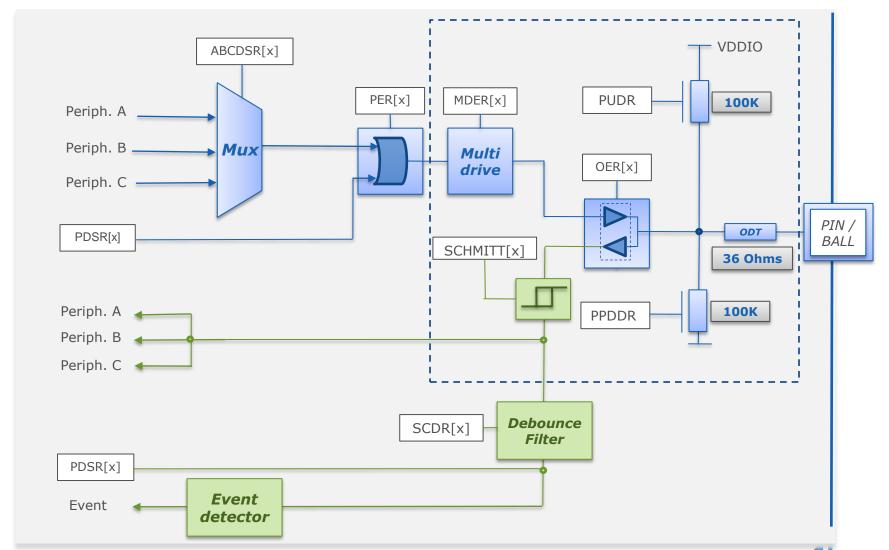


#### Overview

- Each Parallel Input/Output Controller (PIO) manages 32 independently programmable input/output lines.
  - Common Input/output Features :
    - On die termination resistor
    - Programmable Pull-up
    - Programmable Pull-down
  - Output Only Features :
    - Multi drive capability enabling drive in Open Drain
  - Input Only Features :
    - Programmable Schmitt triggers
    - Debounce filter
    - Event detector (Input Change Interrupt)

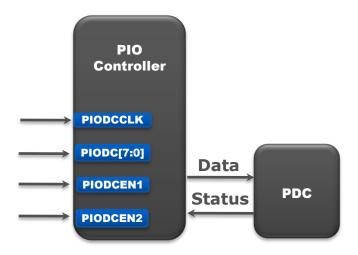


### I/O Line Control Logic



### Parallel Capture Mode

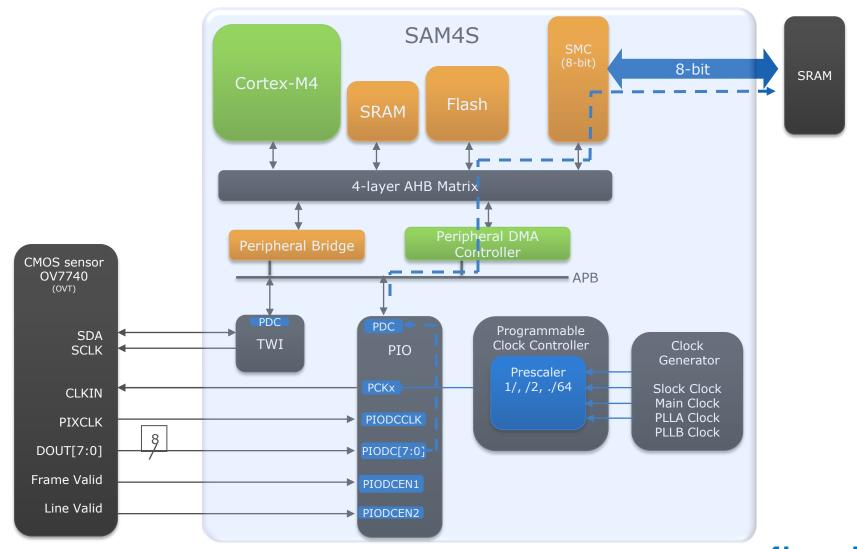
 Allows Capture of parallel data from an external peripheral (CMOS sensor, parallel ADC or a DSP)



- Can be linked to a specific PDC channel to allow data transfer without CPU intervention:
  - Up to MCK/4 data rate in Always sampling mode.
  - Up to MCK/3 data rate in Half sampling mode.



### Parallel Capture Mode - PIR Camera Application





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