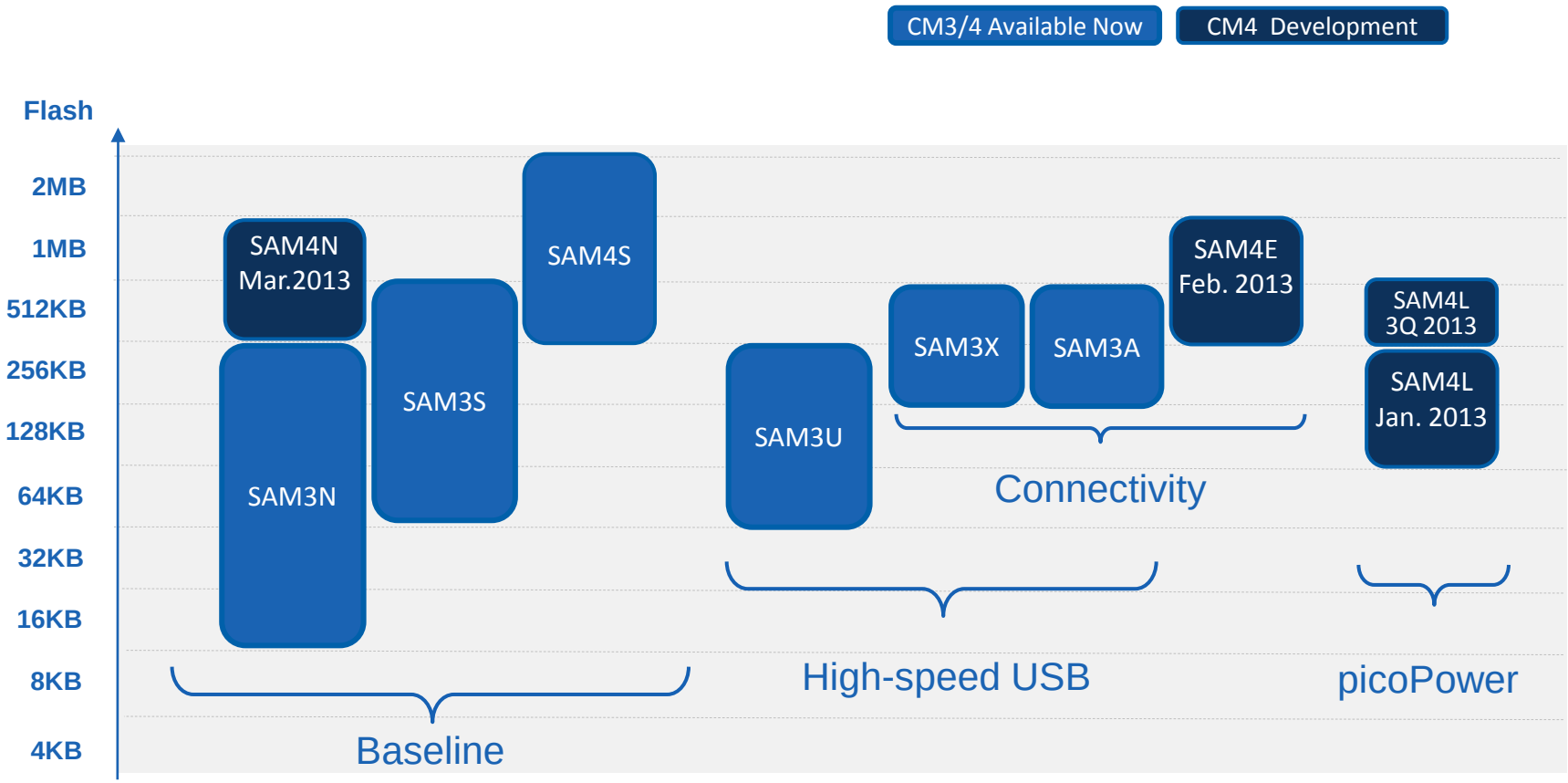
Atmel SAM4S Flash MCU Product Highlights

Atmel Cortex-M Roadmap



Atmel SAM3/4 Family Overview

	SAM3N SAM4N	SAM3S SAM4S	SAM4L	SAM3U	SAM3A	SAM3X	SAM4E
Frequency (max)	80MHz	120MHz	50MHz	96MHz	84MHz	84MHz	120MHz
Flash (KB)	16-1024	64-2048	128-512	64-256	256-512	256-512	512-1024
SRAM (KB)	4-80	16-160	32-64	20-50	64-100	64-100	128
USB (embedded PHY)	—	FS Dev	FS H&D	HS Dev	HS H&D	HS H&D	FS Dev
EMAC	—	—	—	—	—	✓	✓
Dual CAN	—	—	—	—	✓	✓	✓
DAC	✓	✓	✓	✓	✓	✓	✓
QTouch®	✓	✓	✓	✓	✓	✓	—
External Bus	—	✓	—	✓	—	✓	✓

Common Features

- Cortex-M3/4/4F CPU
- Timer, PWM
- QFP/QFN/BGA
- 48 to 144 pins
- Extended supply 1.62-3.6V
- Up to 24 x 16-bit ADC
- Backup mode down to 0.7 µA
- USART, SPI, I2C, I2S

Cortex-M4

Benefits and Advantages vs. Cortex-M3

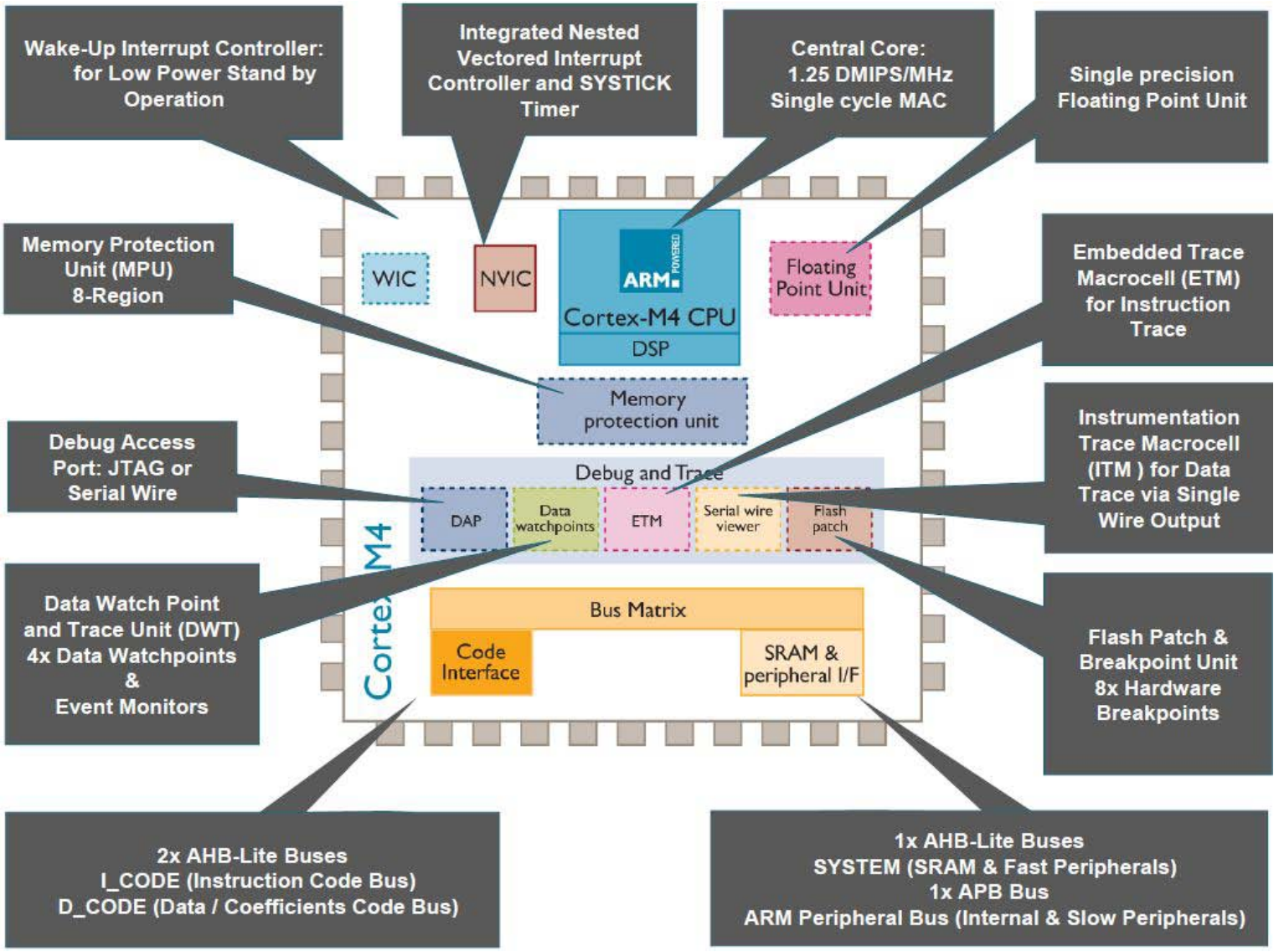
Why Cortex-M4?

- Designed for applications requiring more computational performance
- Cortex-M4 frees CPU resources in case digital signal processing tasks are used (less active cycles are needed)
- Cortex M4 features:
  - A single-cycle multiply-accumulate unit (MAC)
  - Optimized single instruction multiple data (SIMD) instructions, saturating arithmetic instructions
  - Optional single precision Floating-Point Unit (FPU)

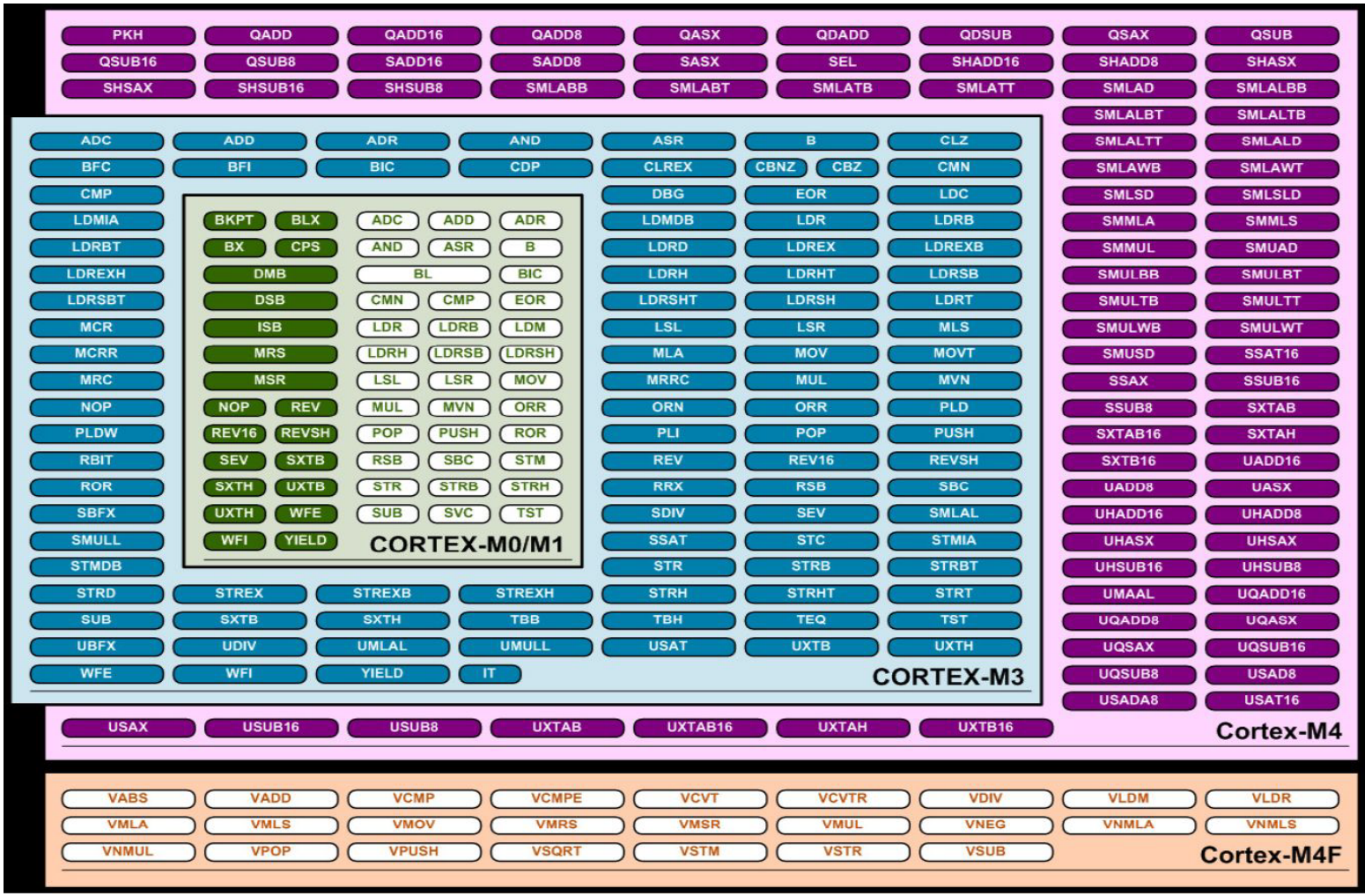
Cortex-M4 vs. Cortex-M3

	Cortex-M3	Cortex-M4
Architecture	ARMv7-M (Harvard)	ARMv7-M (Harvard)
ISA Support	Thumb / Thumb-2	Thumb / Thumb-2
DSP Extensions	NA	Single cycle 16, 32-bit MAC Single cycle dual 16-bit MAC 8, 16-bit SIMD arithmetic Hardware Divide (2-12 cycles)
Optional Floating Point Unit	NA	Single precision floating point unit IEEE 754 compliant
Pipeline	3-stage + branch speculation	3-stage + branch speculation
Interrupts	NMI + 1 to 240 interrupts	NMI + 1 to 240 interrupts
Interrupt Latency	12 cycles (6 when Tail Chaining)	12 cycles (6 when Tail Chaining)
Sleep Modes	Integrated (3)	Integrated (3)
Memory Protection	8 regions MPU	8 regions MPU
Dhrystone	1.25DMIPS/MHz	1.25DMIPS/MHz

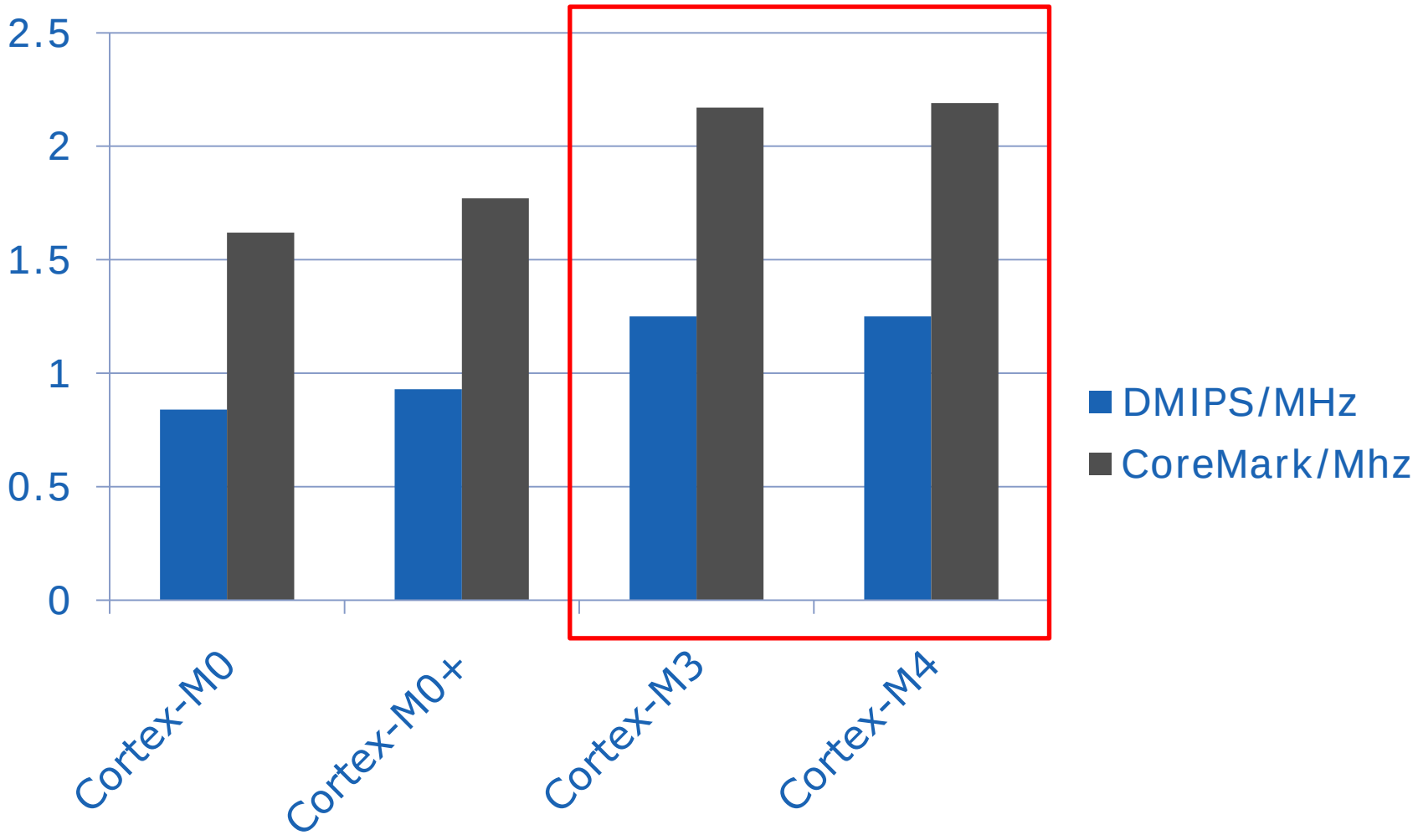
Cortex-M4 Processor Overview



Cortex-M4 Instruction Set



Performance Efficiency



Single Cycle Multiply Accumulate Instructions

- Cortex-M4 features 32-bit hardware multiply-accumulate (MAC) unit
  - Makes digital signal processing more efficient and greatly reduces the consumption of CPU resources
  - Capable of accomplishing an operation of up to *32×32+64->64* or two operations of *16×16* in a single cycle
- Main features:
  - Wide range of multiply-accumulate instructions
  - Choice of 16 or 32 bit multiply and 32 or 64 bit accumulate
  - All instructions execute in a single cycle

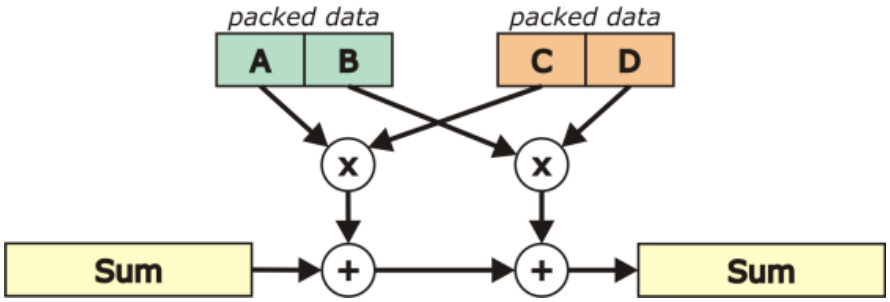
MAC Instructions

OPERATION	INSTRUCTION
16 x 16 = 32	SMULBB, SMULBT, SMULTB, SMULTT
16 x 16 + 32 = 32	SMLABB, SMLABT, SMLATB, SMLATT
16 x 16 + 64 = 64	SMLALBB, SMLALBT, SMLALTB, SMLALTT
16 x 32 = 32	SMULWB, SMULWT
(16 x 32) + 32 = 32	SMLAWB, SMLAWT
(16 x 16) ± (16 x 16) = 32	SMUAD, SMUADX, SMUSD, SMUSDX
(16 x 16) ± (16 x 16) + 32 = 32	SMLAD, SMLADX, SMLSD, SMLSDX
(16 x 16) ± (16 x 16) + 64 = 64	SMLALD, SMLALDX, SMLSLD, SMLSLDX
32 x 32 = 32	MUL
32 ± (32 x 32) = 32	MLA, MLS
32 x 32 = 64	SMULL, UMULL
(32 x 32) + 64 = 64	SMLAL, UMLAL
(32 x 32) + 32 + 32 = 64	UMAAL
32 ± (32 x 32) = 32 (upper)	SMMLA, SMMLAR, SMMLS, SMMLSR
(32 x 32) = 32 (upper)	SMMUL, SMMULR

Single Instruction Multiple Data (SIMD)

- Several instructions operate on “packed” data types
  - Byte or halfword quantities packed into words
  - Allows more efficient access to packed structure types
- SIMD instructions can act on packed data:
  - Quad (4 parallel) 8-bit adds or subtracts
  - Dual (2 parallel) 16-bit adds or subtracts
  - All instructions execute in a single cycle
- SIMD extensions perform multiple operations in one cycle

Sum = Sum + (A x C) + (B x D)



SIMD techniques operate with packed data

- C Compilers won’t automatically generate SIMD instructions
  - Source code/Library must be adapted to execute them (in assembly)

Typical DSP Algorithms

- **DSP operations – MAC is key operation**
  - Most operations are dominated by MACs
  - These can be on 8, 16 or 32 bit operations

- FIR Filters
  - Data communications
  - Echo cancellation (adaptive versions)
  - Smoothing data

$$y[n] = \sum_{k=0}^{N-1} h[k]x[n-k]$$

- IIR filters
  - Audio equalization
  - Motor control

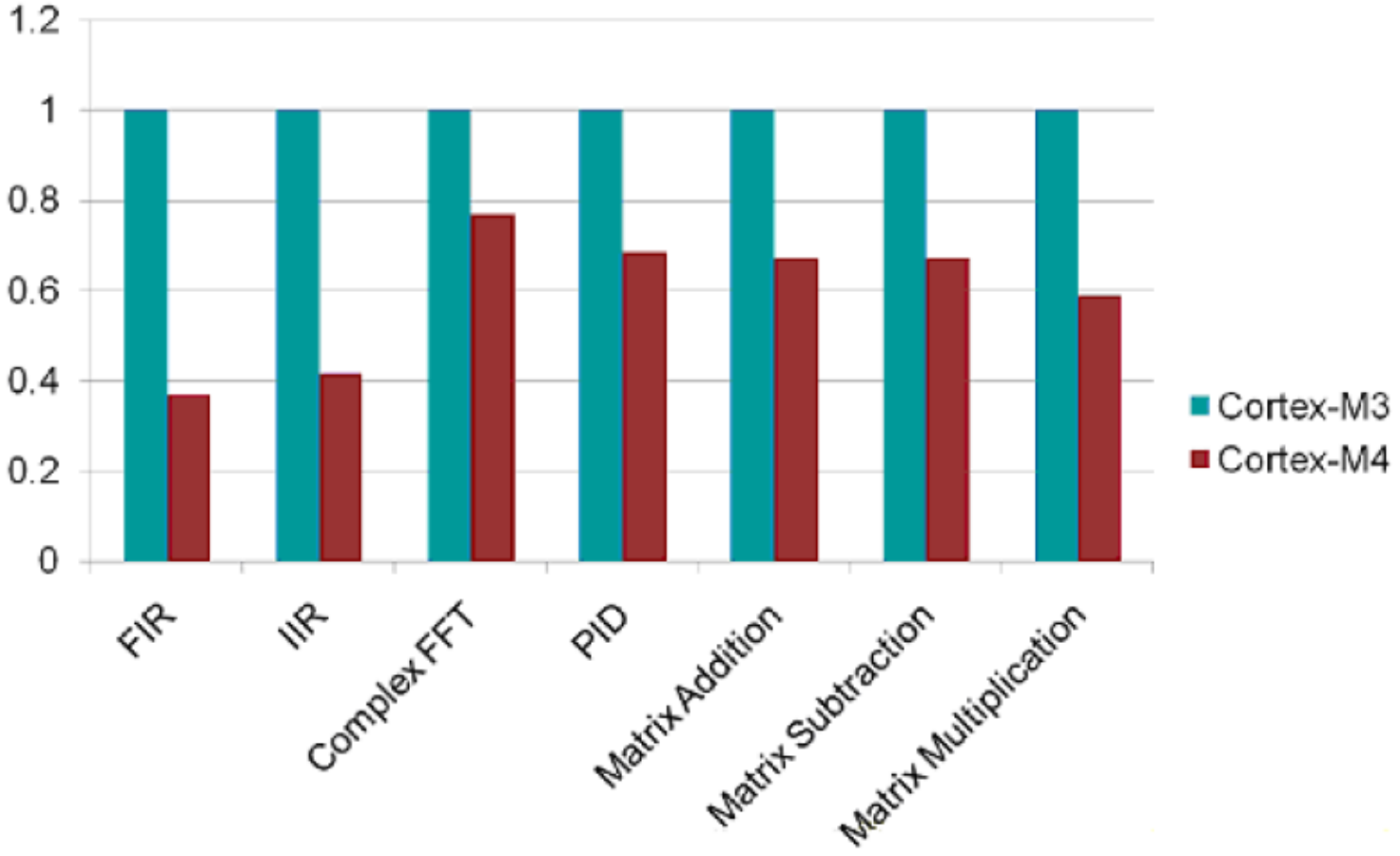
$$y[n] = b_0 x[n] + b_1 x[n-1] + b_2 x[n-2] + a_1 y[n-1] + a_2 y[n-2]$$

- FFT
  - Audio compression
  - Spread spectrum communication
  - Noise removal

$$Y[k_1] = X[k_1] + X[k_2]e^{-j\omega}$$
$$Y[k_2] = X[k_1] - X[k_2]e^{-j\omega}$$

Digital Signal Processing Performance

Relative cycle count

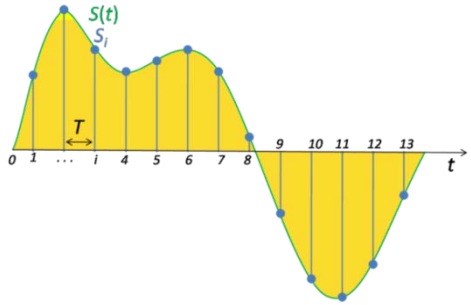


Cortex Microcontroller Software Interface Standard (CMSIS)

- Abstraction layer for all Cortex-M processor based devices
- Developed in conjunction with silicon, tools and middleware partners

- Benefits to the embedded developer
  - Consistent software interfaces for silicon and middleware vendors
  - Simplifies re-use across Cortex-M processor-based devices
  - Reduces software development cost and time-to-market
  - Reduces learning curve for new Cortex microcontroller developers

CMSIS-DSP Library V2.10



- C Source Code optimized for Cortex-M4
- For CMSIS compliant C Compilers (MDK ARM, IAR and GCC)

- Basic Math Functions
  - Vector Absolute Value
  - Vector Addition
  - Vector Dot Product
  - Vector Multiplication
  - Vector Negate
  - Vector Offset
  - Vector Scale
  - Vector Shift
  - Vector Subtraction
- Fast Math Functions
  - Cosine
  - Sine
  - Square Root
- Complex Math Functions
  - Complex Conjugate
  - Complex Dot Product
  - Complex Magnitude
  - Complex Magnitude Squared
  - Complex-by-Complex Multiplication
  - Complex-by-Real Multiplication
- Filtering Functions
  - Biquad Cascade IIR Filters Using Direct Form I Structure
  - Biquad Cascade IIR Filters Using a Direct Form II Transposed Structure
  - High Precision Q31 Biquad Cascade Filter
  - Convolution
  - Partial Convolution
  - Correlation
  - Finite Impulse Response (FIR) Decimator
  - Finite Impulse Response (FIR) Filters
  - Finite Impulse Response (FIR) Lattice Filters
  - Finite Impulse Response (FIR) Sparse Filters
  - Infinite Impulse Response (IIR) Lattice Filters
  - Least Mean Square (LMS) Filters
  - Normalized LMS Filters
  - Finite Impulse Response (FIR) Interpolator
- Matrix Functions
  - Matrix Addition
  - Matrix Initialization
  - Matrix Inverse
  - Matrix Multiplication
  - Matrix Scale
  - Matrix Subtraction
  - Matrix Transpose
- Transform Functions
  - Complex FFT Functions
  - DCT Type IV Functions
  - Real FFT Functions
- Controller Functions
  - Sine Cosine
  - PID Motor Control
  - Vector Clarke Transform
  - Vector Inverse Clarke Transform
  - Vector Park Transform
  - Vector Inverse Park transform
- Statistics Functions
  - Maximum
  - Mean
  - Minimum
  - Power
  - Root mean square (RMS)
  - Standard deviation
  - Variance
- Support Functions
  - Convert 16-bit Integer value
  - Convert 32-bit Integer value
  - Convert 32-bit floating point value
  - Convert 8-bit Integer value
  - Vector Copy
  - Vector Fill
- Interpolation Functions
  - Linear Interpolation
  - Bilinear Interpolation

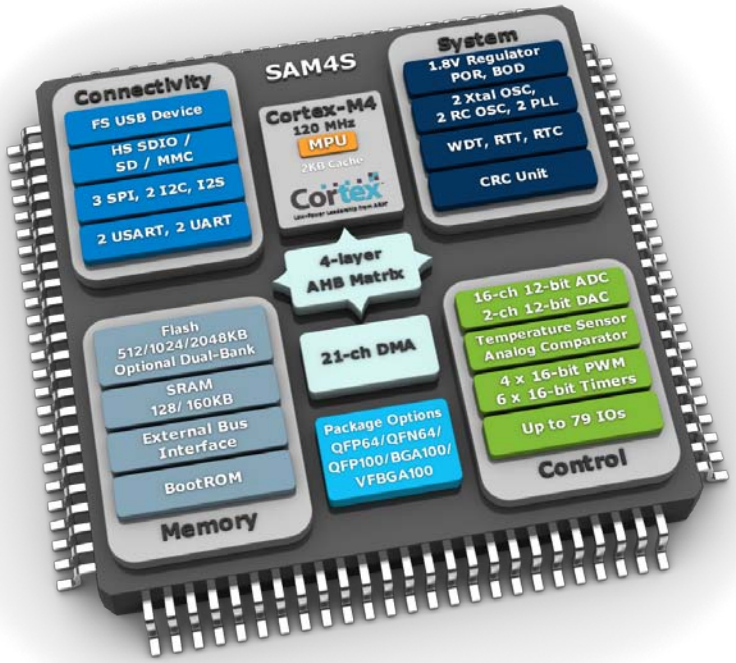
SAM4S Series

Product Highlights

SAM4S Series

SAM4SD, SAM4SA, SAM4S

- ARM Cortex-M4 Processor Running up to 120MHz
- Memory
  - From 512KB to 2MB of Flash
  - Single & Dual bank flash
  - Up to 160KB of SRAM
- 2KB of Cache to Accelerate Flash Execution
  - SAM4SA, SAM4SD
- Dual Boot capability to ease IAP
  - SAM4SD
- Power Consumption
  - 200µA/MHz
  - 30µA in wait mode
- Parallel I/O Capture (CMOS Interface)
- Pin-to-pin Compatible with SAM7S/SAM3S/SAM3N/SAM4N
- High Data Rate Serial Communication Interfaces including:
  - USB 2.0 device, SDIO/SD/MMC, 4 UARTs, 3 SPI, 2 I^2C and I2S

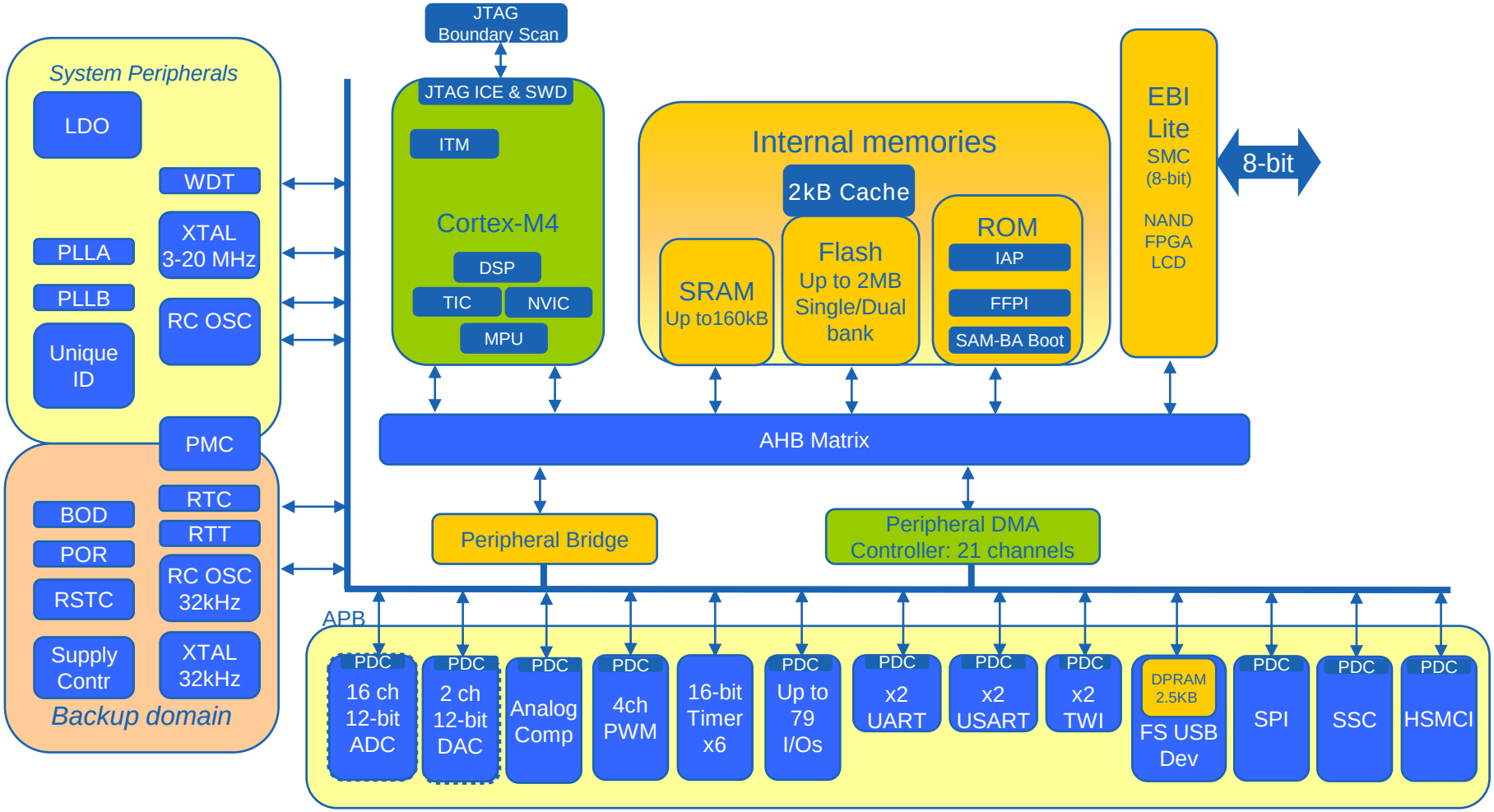


SAM4S Series Comparison Table

	SAM4S8/16	SAM4SA16	SAM4SD16/32
Core	Cortex-M4	Cortex-M4	Cortex-M4
Frequency	120MHz	120MHz	120MHz
Cache	-	2KB	2KB
Flash	512KB/1MB Single bank	1MB Single bank	1MB/2MB Dual bank
SRAM	128K	160K	160K
Package Options	64, 100 QFN, QFP, BGA VFBGA100	64, 100 QFN, QFP, BGA VFBGA100	64, 100 QFN, QFP, BGA VFBGA100

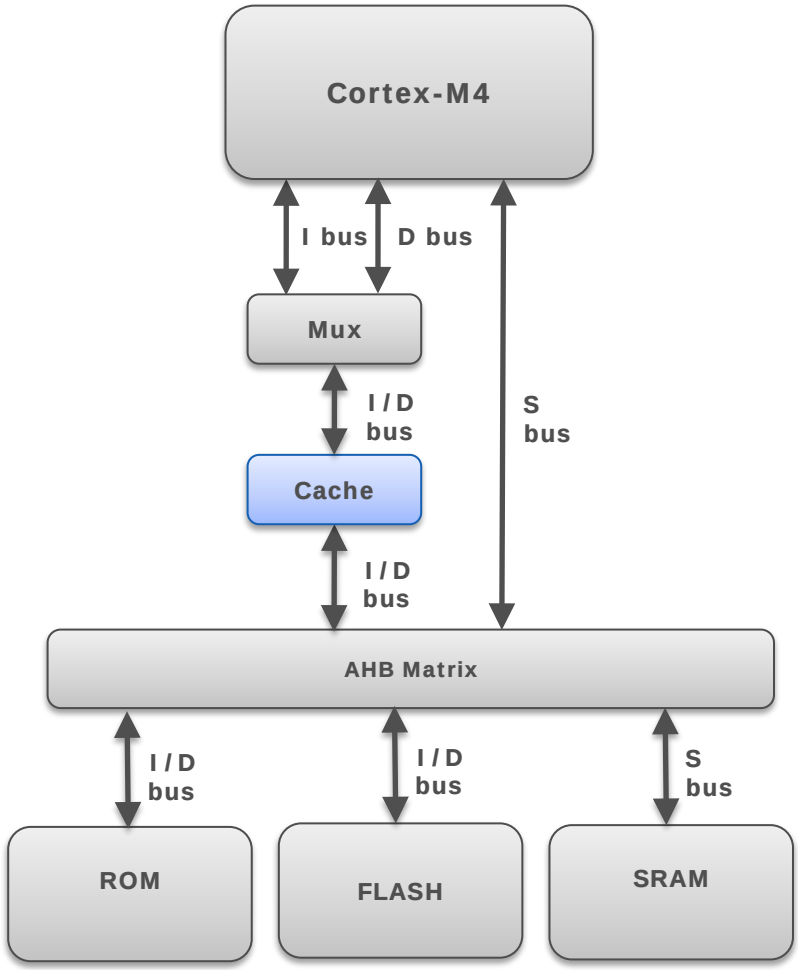
SAM4S Block Diagram

SAM4SD32



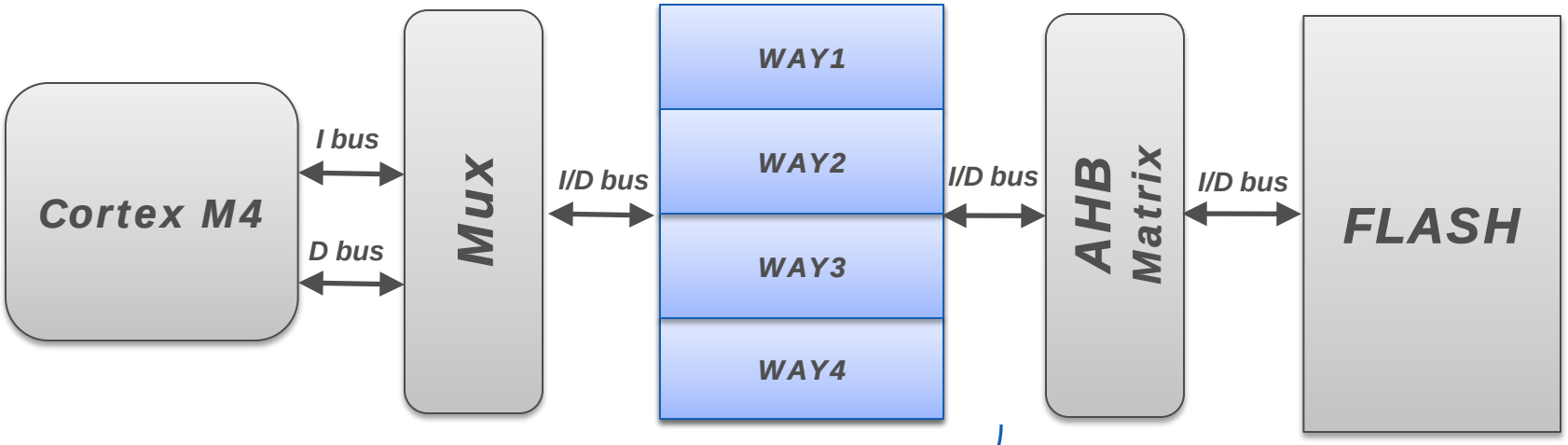
SAM4SA / SAM4SD Cache System

- 2Kbytes of 4-way consecutive cache with monitor system
- Certified Coremark results (IAR 6.50.1):
  - 408.61 coremark @ 120MHz
  - 3.32 Coremark/Mhz
- Advantage
  - Compensate wait state penalty at high frequency
  - Reduce power consumption
- Drawback
  - Not suitable if Deterministic tasks to be executed (i.e. : Real Time Applications)



SAM4SA / SAM4SD Cache System Principle

When cache is full and new instructions / data have to be stored , the ways are erased (round robin) and new instruction are stored



Instructions and data already stored in cache are Accessed at core speed (Cache hit = No wait states needed)

When fetched for the first time , the Instructions and data are copied in cache . (Cache Miss = num Wait state + 1 cycle)

SAM4SD Dual Bank Flash

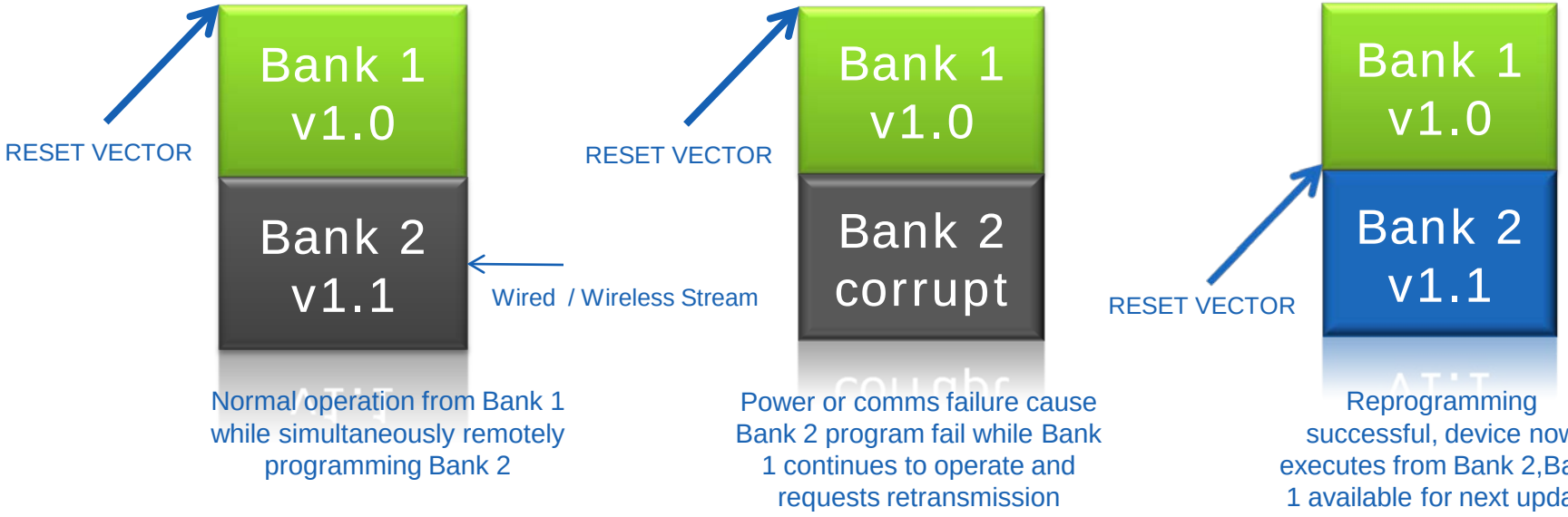
Dual Bank Flash enables Fault Tolerant Self-Programming

What Problem does it Solve?

- Provides a fail-safe method of upgrading firmware on remote networked systems
- Enables background firmware upgrade without halting application execution
- Prevents system corruption while upgrading the system software

How Does it Work?

- Safe and secure remote update:



Normal operation from Bank 1 while simultaneously remotely programming Bank 2

Power or comms failure cause Bank 2 program fail while Bank 1 continues to operate and requests retransmission

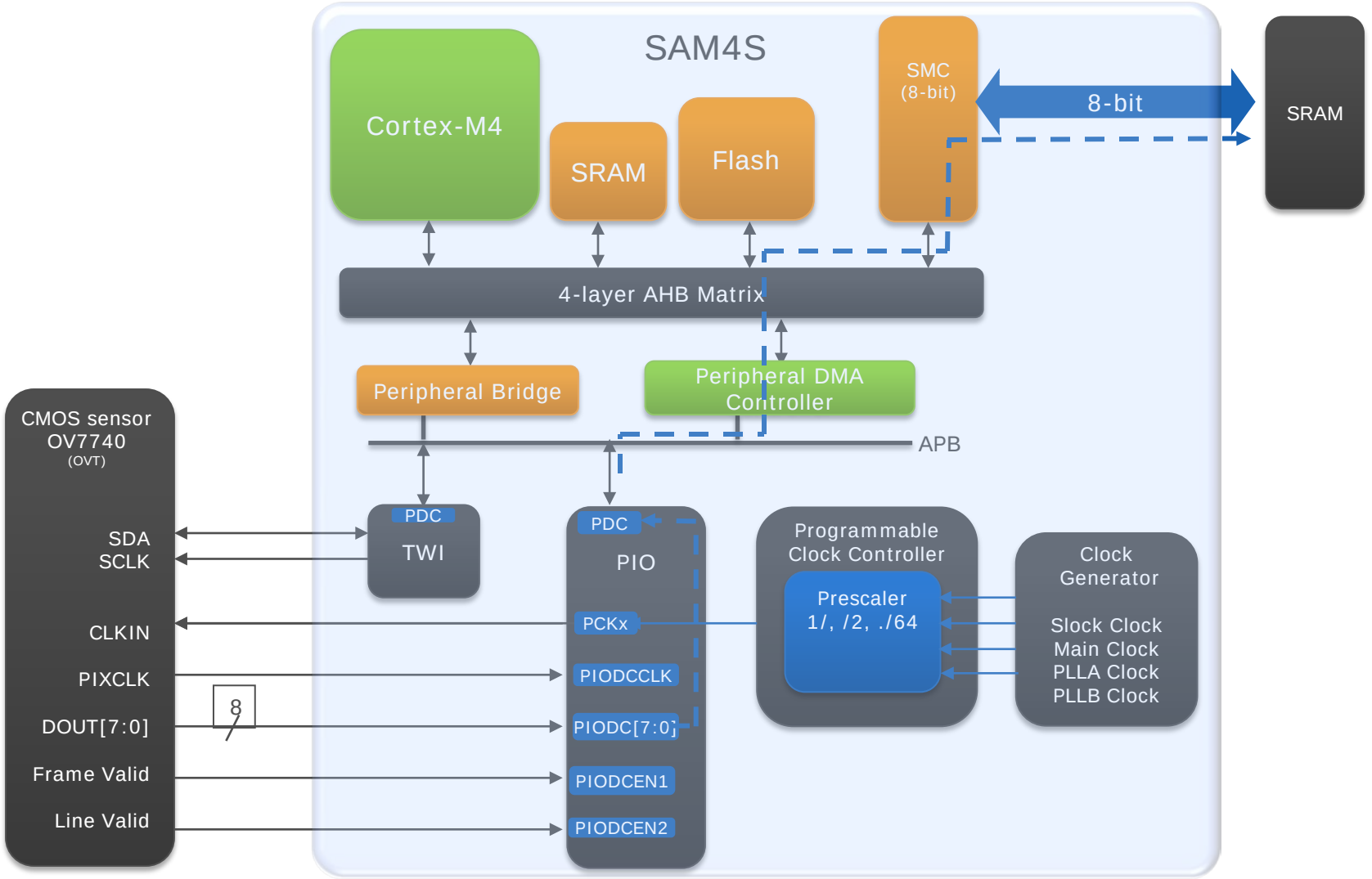
Reprogramming successful, device now executes from Bank 2,Bank 1 available for next update

SAM4S Power Consumption

Power Consumption Mode	Condition	SAM4S16	Unit
Backup (IDDIO)	VDDMain@ 3.3V VDDMain@ 1.8V	2 1	 uA
Sleep Mode Typical @25 Degres @48MHz	IDDCore Total consumption	2.5 3	 mA
Wait Mode VDDCore = 1.2V Regulator int @25Degres	IDDCore Total consumption	20.4 32.2	 uA
Active Mode Periph clock OFF Total consumption	120 MHz, Flash 64 bits 120 MHz, Flash 128 bits 64 MHz, Flash 64 bits 64 MHz, Flash 128bits 1 MHz, Flash 64 bits 1 MHz, Flash 128bits	21.4 28.8 13.9 17.6 1.6 1.3	mA

SAM4S Parallel IO Capture

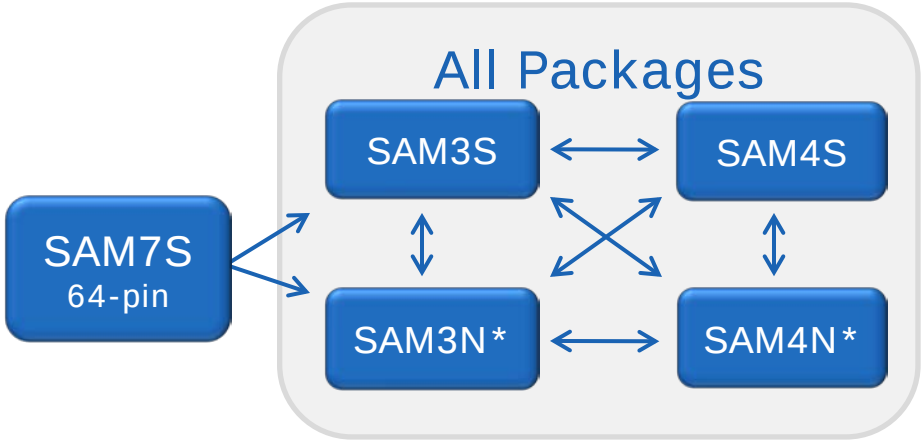
Parallel Capture Mode – PIR Camera Application



Atmel ARM Cortex-M4 Value Proposition

- Seamless Migration Path Between SAM7S, SAM3N, SAM3S, SAM4N and SAM4S Devices
  - HW Pin to pin compatibility for SAM7S 64-pin packages
  - Full HW/SW pin to pin compatibility between SAM3S/N and SAM4S/N

Form, Fit & Function Compatibility



*** Except for USB device**

Enabling Unlimited Possibilities™