Model Question Paper

Subject Code: CS/IT/CM/CD- 213 (R20)

R.V.R. & J.C. College of Engineering, Guntur – 522019

(Autonomous)

B.Tech. Semester-III [Second Year] Degree Examination

Subject Name: Computer Organization

Time: 3 hrs Max. Marks: 70

All Questions carry equal marks.

Answer Question No.1 compulsory (14 x 1 = 14 Marks)

Answer ONE Question from each unit (4 x 14 = 56 Marks)

	Answer ALL Questions		Marks	COs	Blooms Taxonomy Level
1.	(a)	List different types of computers	1	CO1	L1
	(b)	What is called the subroutine linkage method?	1	CO2	L1
	(c)	Illustrate the Rotate Right with carry instruction.	1	CO2	L2
	(d)	Calculate the effective address of Load R1, 10(R2), if the value of R2 is 200.	1	CO2	L3
	(e)	What is called Memory Function Complete (MFC)?	1	CO2	L1
	(f)	What is called data hazard?	1	CO3	L1
	(g)	What is operand forwarding?	1	CO3	L1
	(h)	Define Interrupt latency.	1	CO4	L1
	(i)	Mention any two data transfer signals used in the PCI bus.	1	CO4	L1
	(j)	List various processor controlled registers.	1	CO4	L1
	(k)	Compare EPROM and EEPROM.	1	CO5	L2
	(l)	Define page fault.	1	CO5	L1
	(m)	Find the binary equivalent of $(46.25)_{10}$	1	CO6	L3
	(n)	What is called a biased exponent?	1	CO6	L1

UNIT – I

2.	(a)	Describe the basic operational concepts of a computer.	7	CO1	L2
	(b)	Convert the following pairs of decimal numbers to 5-bit 2's complement numbers then add them. State whether or not overflow occurs in each case. i) 4 and 11 ii) 6 and -14 iii) -13 and 12 iv) -9 and -14	7	CO1	L3
		(OR)			
3.	(a)	Explain different types of addressing modes supported in RISC system with examples.	7	CO2	L2
	(b)	Define subroutine. Explain the use of a stack frame during the execution of the subroutine.	7	CO2	L2

UNIT – II

4.	(a)	Discuss the concept of hardwired control with a neat diagram.	7	CO2	L2
	(b)	List the sequence of actions needed to fetch and execute the following instructions.	7	CO2	L2

		i) Add R3,R4,R5 ii) Load R5, X(R7) iii) Store R6, X(R8)			
		(OR)			
5.	(a)	Explain the five-stage pipeline organization with a diagram. How the memory delays effects the pipelined execution.	7	CO3	L2
	(b)	What is the effect of conditional branching on the pipeline? Explain the concepts of delayed branch & dynamic branch prediction.	7	CO3	L2

UNIT – III

6.	(a)	Explain the concept of the interrupt and how that can be handled when multiple devices are connected to the processor.	7	CO4	L2
	(b)	What is the need of I/O interfaces? Explain how they control the data transfer.	7	CO4	L2
		(OR)			
7.	(a)	Explain the Asynchronous data transfer with hand shaking signals.	7	CO4	L2
	(b)	Discuss in detail about the parallel interface.	7	CO4	L2

UNIT – IV

8.	(a)	What is DMA (Direct Memory Access)? Discuss in detail the role of the DMA controller in detail.	7	CO5	L2
	(b)	What is the set associative mapping of cache memory? A block-set-associative cache consists of a total of 64 blocks, divided into 4-block sets. The main memory contains 4096 blocks, each consisting of 32 words. Assuming a 32-bit byte-addressable address space, how many bits are there in each of the Tag, Set, and Word fields?	7	CO5	L3
		(OR)			
9.	(a)	Explain the Booth's algorithm. Apply the booth's algorithm to multiply the numbers (-13) and (+16).	7	CO6	L3
	(b)	Design the 4-bit carry-lookahead adder with generating and propagate functions. Explain.	7	CO6	L4