2nd Sem CSE/IT R-18 Nov-2020

Hall Ticket Number:

CS/IT221(R18)

B.TECH. DEGREE EXAMINATION, NOVEMBER-2020

Semester IV [Second Year] (Regular)

COMPUTER ORGANIZATION

Time: Three hours | Maximum Marks: 60

Answer Question No.1 compulsorily. (12 x 1 = 12)
Answer One Question from each unit. (4 x 12 = 48)

1. Answer the following:
   (a) How the numbers are represented in computer memory? CO1
   (b) Write any three types of computers. CO1
   (c) What is instruction sequencing? CO1
   (d) Define hard wired control. CO2
   (e) What is the main cause of data hazard? CO2
   (f) Define effective address. CO2
   (g) Define interrupt latency. CO3
   (h) What is the main aim of virtual memory organization? CO3
   (i) Write the function of copy back protocol. CO3
   (j) What is the size of mantissa in double precision number format? CO4
   (k) How will you increase the speed of memory access in pipelining? CO4
   (l) Define branch delays in pipelining. CO4

UNIT – I

2. (a) Explain the instruction cycle with an example. (6M) CO1
   (b) Explain the internal organization of a processor with a neat diagram. (6M) CO1

(OR)

3. (a) What is multiprocessor system? Explain the advantages of multiprocessor over uniprocessor. (6M) CO1
   (b) What do you mean by inter-process arbitration? (6M) CO1

UNIT – II

4. (a) Explain the use of multiple-bus organization for executing a three-operand instruction. Explain how it is implemented in multiprocessor architecture? (6M) CO2
   (b) Explain the issue involved with multiplication operation. (6M) CO2

(OR)

5. (a) Explain the design of hardwired control unit. (6M) CO2
   (b) What are handshaking signals? Explain the handshake control of data transfer during input and output operation. (6M) CO2

UNIT – III

6. (a) Compare and contrast between Asynchronous DRAM and Synchronous DRAM. (6M) CO3
   (b) Design a 64K * 16 memory chip using 16K * 8 memory chips. (6M) CO3

(OR)

7. (a) What is a mapping function? What are the ways the cache can be mapped? Explain in detail. (6M) CO3
   (b) Explain the method of DMA transfer. How does a DMA controller improve the performance of a computer? (6M) CO3

UNIT – IV

8. (a) With a neat sketch explain the working principle of pipeline processor. (6M) CO4
   (b) Give the design of a 4-bit shifter. (6M) CO4

(OR)

9. (a) Apply Booth's algorithm to multiply the numbers (-18) and (-17). (6M) CO4
   (b) Explain the design of a 4-bit Arithmetic unit with two selection variables, which performs the basic arithmetic functions. (6M) CO4

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Hall Ticket Number:

CS/IT221(R18)

B.TECH. DEGREE EXAMINATION, AUGUST-2021

Semester IV [Second Year] (Regular & Supplementary)

COMPUTER ORGANIZATION

Time: Three hours | Maximum Marks: 60

Answer Question No.1 compulsorily. (12 x 1 = 12)
Answer One Question from each unit. (4 x 12 = 48)

1. Answer the following:
   (a) List the operations performed by the computer. CO1
   (b) Distinguish immediate and indirect addressing modes. CO1
   (c) Define byte-addressable memory and give it's diagrammatic representation. CO1
   (d) What is memory-mapped I/O? CO2
   (e) What is called Memory Function Completed (MFC)? CO2
   (f) What is meant by an effective address? CO1
   (g) What is a bus arbitration? CO3
   (h) Distinguish EPROM and EEPROM. CO3
   (i) Define page fault. CO3
   (j) Mention the need of Translation Look-aside-Buffer (TLB). CO3
   (k) How can you represent -32.75 in the IEEE 754 single-precision format? CO4
   (l) What is called a biased exponent? CO4

UNIT – I

2. (a) Explain various functional units of a computer with a neat diagram. (6M) CO1
   (b) Discuss various representations used for the integer and floating-point numbers in detail. (6M) CO1

(OR)

3. (a) Define subroutine. Discuss parameter passing mechanism through stack with suitable example. (6M) CO1
   (b) Explain the following instructions with suitable examples:
   (i) Logic instructions (ii) Shift and Rotate instructions (iii) Multiplications and Division. (6M) CO1

UNIT – II

4. (a) Discuss in detail the program-controlled I/O. (6M) CO2
   (b) How to handle the interrupts when multiple devices are connected to the processor? (6M) CO2

(OR)

5. (a) Explain the five-step sequence of actions for the following instructions Load, Store and add. (6M) CO2
   (b) Discuss the concept of hardwired control with a neat diagram. (6M) CO2

UNIT – III

6. (a) Explain the synchronous data transfer operation of the bus with neat timing diagrams. (6M) CO3
   (b) Discuss the basic structure and operations of the PCI bus in detail. (6M) CO3

(OR)

7. (a) Explain the working of 32MX8 DRAM memory chip. (5M) CO3
   (b) What is cache memory? Explain the different mapping techniques used in the usage of cache memory. (7M) CO3

UNIT – IV

8. (a) Explain the Booth's algorithm. Apply the booth's algorithm to multiply the numbers (-13) and (+16). (6M) CO4
   (b) Illustrate how the multiplication is performed with the summand addition tree using 3-2 reducers. (6M) CO4

(OR)

9. (a) Explain the five-stage pipeline organization with a diagram. (6M) CO4
   (b) Discuss the hardware and software solutions to handle the data dependency issue of pipelining with an example. (6M) CO4

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CS/IT221(R18)

Hall Ticket Number:

CS/IT221(R18)

B.TECH. DEGREE EXAMINATION, JANUARY-2021

Semester IV [Second Year] (Supplementary)

COMPUTER ORGANIZATION

Time: Three hours | Maximum Marks: 60

Answer Question No.1 compulsorily. (12 x 1 = 12)
Answer One Question from each unit. (4 x 12 = 48)

1. Answer the following:
   (a) List different types of computers — CO1
   (b) What is called the subroutine linkage method? — CO1
   (c) Define memory access time. — CO1
   (d) Define Interrupt latency. — CO2
   (e) List various processor controlled registers. — CO2
   (f) How can you define the disk access time? — CO2
   (g) Mention any two data transfer signals used in the PCI bus. — CO3
   (h) Differentiate RAM and ROM. — CO3
   (i) What is the meaning of locality of reference? — CO3
   (j) What is called data hazard? — CO4
   (k) What is the need of guard bits in the arithmetic operations? — CO4
   (l) What is the binary equivalent of $(46.25)_{10}$? — CO4

UNIT – I

2. (a) Describe the basic operational concepts of a computer. (6M) CO1
   (b) Convert the following pairs of decimal numbers to 5-bit 2's complement numbers then add them. State whether or not overflow occurs in each case.
   (i) 4 and 11 (ii) 6 and –14 (iii) –13 and 12
   (iv) –9 and –14. (6M) CO1

(OR)

3. (a) Explain different types of addressing modes supported in RISC a system with examples. (6M) CO1
   (b) Define subroutine. Explain the use of a stack frame during the execution of the subroutine. (6M) CO1

UNIT – II

4. (a) Define Interrupt. How to enable and disable the interrupt? (6M) CO2
   (b) What is the need of I/O interfaces? Explain how they control the data transfer? (6M) CO2

(OR)

5. (a) Discuss how the control signals generated for the data path in a 5-stage execution sequence and instruction address generator with neat diagrams. (6M) CO2
   (b) List the sequence of actions needed to fetch and execute the following instructions.
   (i) Add R3,R4,R5 (ii) Load R5, X(R7)
   (iii) Store R6, X(R8) (6M) CO2

UNIT – III

6. (a) Explain the Asynchronous data transfer with hand shaking signals. (6M) CO3
   (b) Discuss in detail about the parallel interface. (6M) CO3

(OR)

7. (a) What is DMA (Direct Memory Access)? Discuss in detail the role of the DMA controller in detail. (6M) CO3
   (b) Explain the concept of virtual memory in detail. (6M) CO3

UNIT – IV

8. (a) Explain the pipelined execution in the ideal case. Explain how that is effected with memory delays? (6M) CO4
   (b) What is the effect of conditional branching on the pipeline? Explain the concepts of delayed branch and dynamic branch prediction. (6M) CO4

(OR)

9. (a) Write the register configuration of the sequential circuit binary multiplier. Explain the steps of how the multiplication of 1101 and 1011 is performed? (6M) CO4
   (b) Design the 4-bit carry-look ahead adder with generating and propagate functions. Explain. (6M) CO4

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CS/IT

Hall Ticket Number:

CS/IT221(R18)

B.TECH. DEGREE EXAMINATION, DECEMBER-2021

Semester IV [Second Year] (Supplementary)

COMPUTER ORGANIZATION

Time: Three hours | Maximum Marks: 60

Answer Question No.1 compulsorily. (12 x 1 = 12)
Answer One Question from each unit. (4 x 12 = 48)

1. Answer the following:
   (a) List any three data transfer instructions. CO1
   (b) Write any two memory operations. CO1
   (c) What is store operation? CO1
   (d) What is the role of micro programmed control unit? CO2
   (e) Differentiate between SRAM and DRAM. CO2
   (f) Differentiate between maskable and non-maskable interrupt. CO2
   (g) Where the return address from the interrupt-service routine is stored? CO3
   (h) List any two functions of I/O interface. CO3
   (i) How DMA differs from the interrupt mode? CO3
   (j) How many bits the mantissa of a fraction occupy in IEEE 32 bit representation? CO4
   (k) What is structural hazard? CO4
   (l) Define Memory delays in Pipelining. CO4

UNIT – I

2. (a) Draw and explain the block diagram of a complete processor. (6M) CO1
   (b) What do you mean by addressing mode? Discuss about any five addressing modes with suitable examples. (6M) CO1

(OR)

3. (a) List and explain the steps involved in the execution of a complete instruction. (8M) CO1
   (b) Discuss about various functional units of a computer. (4M) CO1

UNIT – II

4. (a) Explain the basic organization of a micro programmed control unit and the generation of control signals during micro program. (6M) CO2
   (b) Compare memory mapped I/O and IO mapped I/O. (6M) CO2

(OR)

5. (a) What are the advantages and disadvantages of hardwired and micro programmed control? (6M) CO2
   (b) Explain how control signals are generated using micro programmed control? (6M) CO2

UNIT – III

6. (a) What is Cache memory? Explain the different mapping functions. (6M) CO3
   (b) What are the different types of bus interfaces? Explain in detail USB bus organization. (6M) CO3

(OR)

7. (a) Explain internal organization of memory chips. (6M) CO3
   (b) Explain the Address Translation in Virtual Memory. (6M) CO3

UNIT – IV

8. (a) Design a 4-bit Adder / Subtractor for floating point numbers. (6M) CO4
   (b) Discuss any three representations of Signed integers with suitable examples. (6M) CO4

(OR)

9. (a) Design a 2x3 array multiplier. (6M) CO4
   (b) Design a basic pipeline. What are the basic pipeline stages? Show the instruction execution in it. (6M) CO4

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