Quad Channel Camera Application for Surround View and CMS Camera Systems

Thorsten Lorenzen, Brian Shaffer, Chaitanya Ghone, Dac Tran, and Albert Fischer

ABSTRACT

This application report discusses in detail a reference design jointly developed between OmniVision Technologies, Inc. and Texas Instruments, Inc. It interconnects Megapixel Image Sensors with the TDA2x ADAS Applications Processor. In order to bridge long distances over coax cables, TI's FPD-Link III technology comes into play. The concept proves a method over which continuous high speed transfers of four fully synchronized independent camera streams over independent coax links is achieved (see Figure 1). Order information can be found at the end of this document.

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1   Introduction

Multi camera systems are common for development of Automotive Vision Surround View Systems used to assist the parking process. Today's systems under development can include up to six cameras to observe and identify the scene around the car. A minimum of four camera streams are stitched together for the best driver experience. However, the systems are capable of providing the driver with more than just a 3D view of what surrounds the car. Object detection algorithms can provide collision warnings for several kinds of obstacles like pillars or measure the size of a possible parking slot. The image data can also be used for back-over prevention to protect pedestrians passing the car as it is reversing.

2   Omnivision Image Sensor Technology

The OV10640 Megapixel color imager is a 1/2.56" optical format, 1280x1080 single-chip for machine vision automotive applications. The sensor's 4.2-micron OmniBSI™ pixel is capable of recording highly detailed full-resolution 1.3-megapixel images and video at 60 frames per second (fps). The sensor uses OmniVision's unique split pixel HDR technology, in which the scene information is sampled simultaneously rather than sequentially, minimizing motion artifacts and delivering superior image quality in RAW output in the most demanding and difficult lighting conditions. It features the OmniHDR-S™ technology to extend pixel precision to 12 bits of dynamic range. Therefore, the sensor reads out up to three exposure values: "long (L)", "short (S)" and "very short (VS)". It will be used to further process high dynamic range images when fed into an image signal processor (ISP). OV10640 integrates an ISP for basic post processing tasks. It calculates statistic data to be applied to automatic exposure control, automatic gain control and automatic dynamic range control. The OV10640 supports output formats such as 12/16/20-bit HDR or 12-bit RAW data through either a parallel digital video port or a standard MIPI/CSI-2 interface. This document discusses the use of an external ISP providing advanced processing capability. Multi camera systems such as those used in surround view systems require all incoming video streams to be in perfect sync, which ensures that all parts of the stitched output are in perfect sync. This prevents visual artifacts and avoids errors on any further algorithm that uses the stitched output. In order to synchronize multiple cameras, OV10640 features frame synchronization mechanism using frame sync input (FSIN) to the camera. The Host processor can apply a common periodic synchronization pulse to all image sensors' FSIN pin. In this mode, a new frame starts automatically whenever a raising edge of FSIN is detected. In case one sensor runs out of synchronization, the periodic pulse enforces the last video rows to skip. Hence, sufficient idle rows need to be provided for the end of each frame to avoid loss of active video data. Registers will be programmed using the serial camera control bus (SCCB).
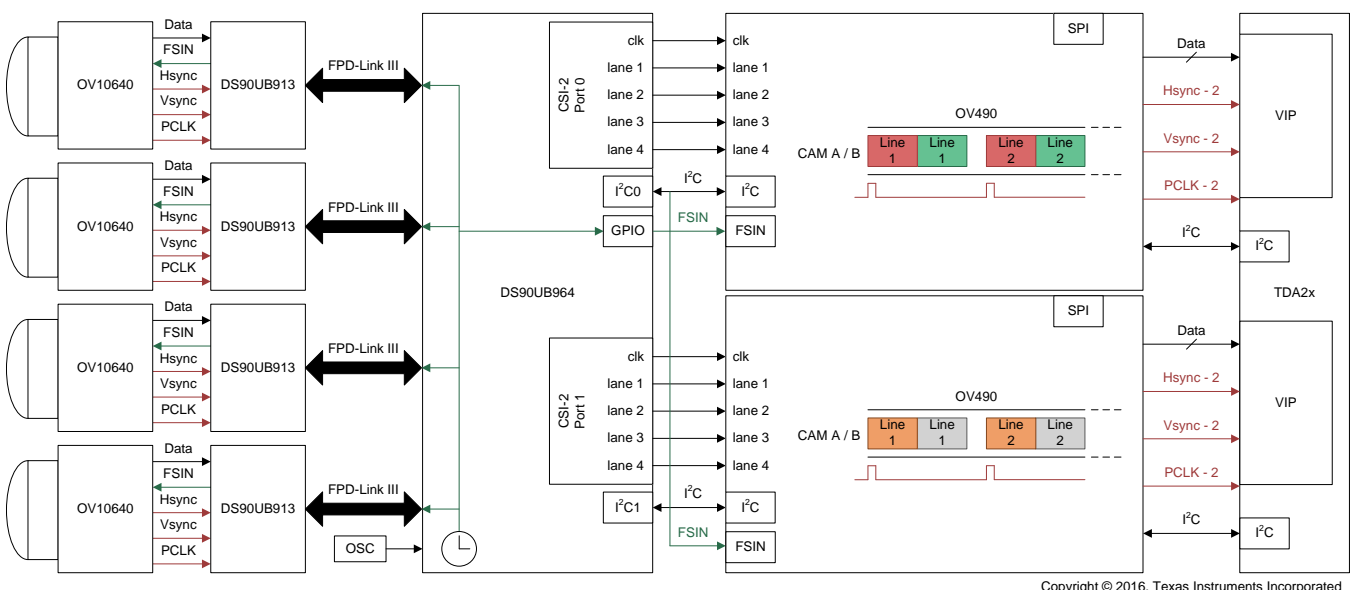
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Figure 1. Design Concept

The SCCB can be serviced from a host controller over a standard inter-integrated circuit (I2C) interface. The sensor's standard device address is 0x60. However, through external pins GPIO[2:0], alternative addresses can be set for the connection of multiple sensors.

> **NOTE:** For more information, see Section 13 and contact your local OmniVision representative (www.ovt.com).

3 Omnivision ISP Companion for HD Image Processing

The OV490 integrates a high performance ISP with advanced HDR capabilities in order to achieve high quality images. In addition, it can output RAW data for machine vision processing and fully processed YUV data for display concurrently. Through its MIPI CSI-2 interfaces, it allows to receive, process and output two independent video streams at the same time. To accomplish this, MIPI standard offers up to four virtual channels to separate the streams within the physical layer of the interface. The streams arrive separated in long (L), short (S) and very short (VS) exposure channels indicated by the MSB of each value. After multiple pre-processing steps such as lens correction, white balancing or defective pixel correction, the ISP combines the channels with different exposures to generate high dynamic range output. Therefore, dark areas of the image will be filled with pixels from L exposure channel while bright areas will be filled with pixels from either S or VS channel. It results in images providing extended dynamic range. The weighted output of the combination feeds back into the blocks automatic gain control (AGC), automatic exposure control (AEC) and HDR block in order to calculate statistics. The statistics including histogram can be transferred to the host as part of idle rows within the video stream. The OV490 features a RISC processor to control the filter blocks and for configuration. Through its 4-wire serial interface the ISP needs to boot up from an external code provider. When configured to (boot mode pins: FSIN0, FSIN1), OV490 allows booting from an external SPI Flash memory device. Doing so, the RISC processor loads the firmware into its on-chip memory and begins to execute. To obtain customized firmware, contact www.ovt.com. There are two sets of SCCB master/slave and one of SCCB slave interfaces on the chip (I2C interface). The master SCCB port configures the image sensors and optimizes its performance during runtime. The slave SCCB port receives configurations for ISP registers from an external master.

> **NOTE:** For more information, contact your local OmniVision representative (www.ovt.com).

4 TI FPD-LINK III LVDS Serializer Technology

The DS90UB913A-Q1 FPD-Link III 1.4 Gbit/s serializer is intended to link with mega-pixel image sensors. It transforms a parallel LVCMOS data bus (video port) along with a bidirectional control bus (I2C port) into a single high-speed differential pair. The DS90UB913A-Q1 can accept up to 12 bits of data + 2 bits (for example, HSYNC/VSYNC) + pixel clock (PCLK) in a range of 25 MHz to 100 MHz. The integrated bi-directional control channel transfers data over the same differential pair. Therefore, it eliminates the need for additional wires to program the image sensors' registers. In addition, the Serializer provides up to four GPO pins. They can act as outputs for the input signals that are fed into the Deserializer general-purpose input/output (GPIO) pins triggering the image sensor's logic (see FSIN in Figure 1). For example, the Deserializer (see Section 5) and the Serializer can be configured in a way so that one GPIO pin on the Deserializer side causes one GPO pin on the Serializer side to toggle. In other words, the Serializer's output pins reflect the assigned input pins from the Deserializer. Alternatively, the GPO 2 pin can be configured to become a clock output pin when set in external oscillator mode (CLKOUT). In turn, the GPO 3 pin acts as input for an external clock source (CLKIN). It allows the Serializer to drive the image sensor's system clock input (XVCLK) (see Figure 2).

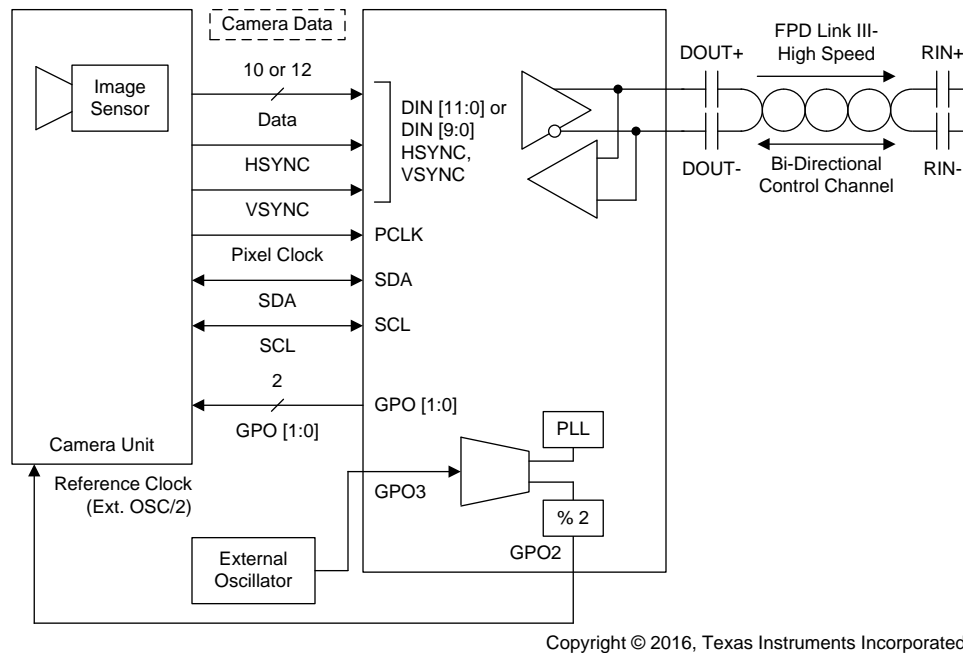Copyright © 2016, Texas Instruments Incorporated

Figure 2. Frame Sync Generation

The DS90UB913A-Q Serializer features one master/slave I2C interface. In I2C slave mode, one host controller can register program the Serializer for extra features or it can control the GPOs directly. When I2C pass-through option is enabled, the I2C interface of the Serializer turns into master mode. For this option, one host programs the I2C slave controller of the Deserializer instead. The I2C programmed sequence bridges the FPD-Link III connection into the Serializer. It outputs through its I2C interface for image sensor configuration. In this fashion, an external device such as image sensors can be programmed remotely (see Figure 3).

> **NOTE:** For more information, see the DS90UB913A-Q1 25-MHz to 100-MHz 10/12-Bit FPD-Link III Serializer Data Sheet.
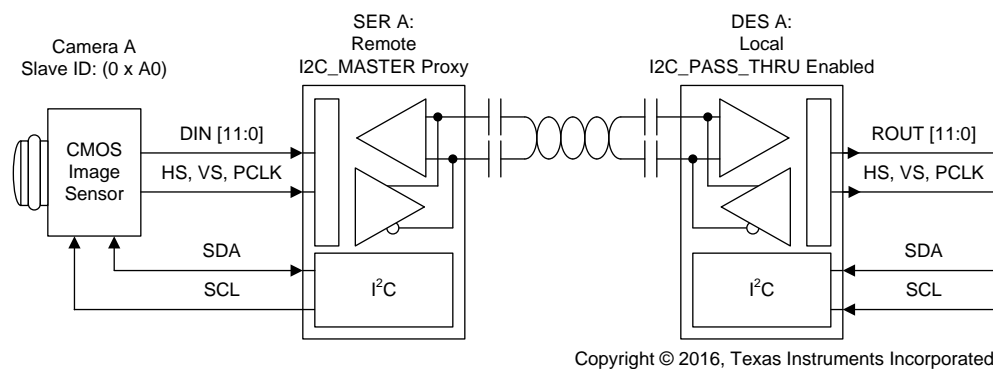

Figure 3. I2C Pass Through Scheme

5   TI FPD-LINK III LVDS Deserializer Technology

The DS90UB964-Q1 FPD-Link III Deserializer hub, when coupled with DS90UB913A-Q1 Serializers, receives FPD-Link III streams from up to four image sensors concurrently. It provides two MIPI CSI-2 output ports consisting of four physical lanes, plus a clock lane. The Deserializer decodes incoming FPD-Link III streams to be multiplexed on one or two of the MIPI CSI-2 output ports. In order to keep incoming video streams separated, both MIPI CSI-2 ports offer up to four virtual channels. Every data stream is combined into packets designated for each virtual channel. A unique channel identification number (VC-ID) in the packet header identifies the virtual channel. This way streams will be interleaved into the CSI-2 ports for transmission (see Figure 4).
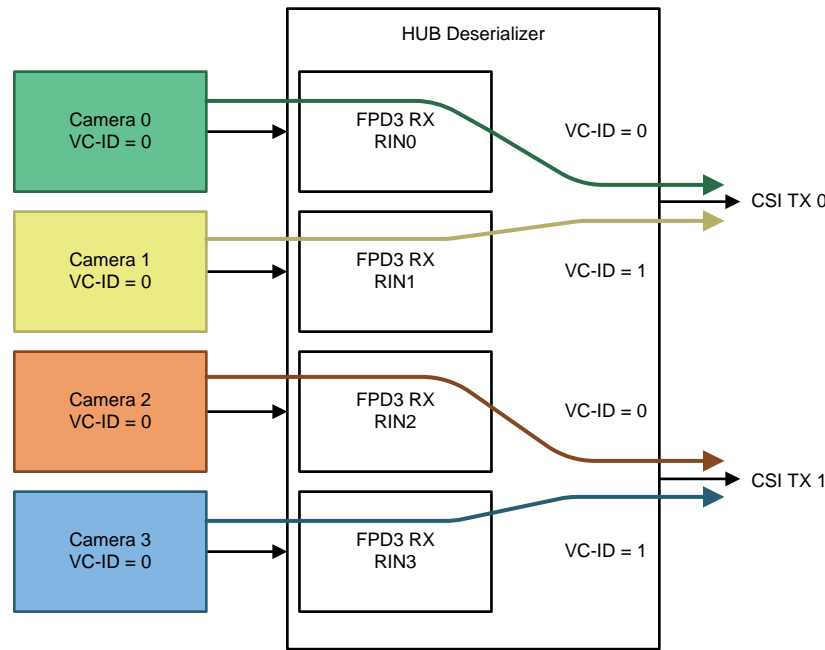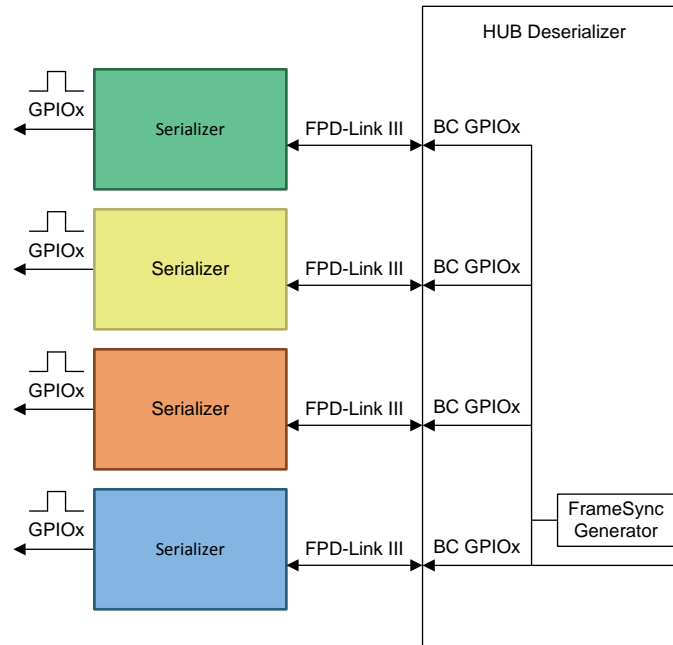

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Figure 4. Virtual Channel Scheme

In addition to forwarding video streams, the DS90UB964-Q1 Deserializer offers a back channel on the same FPD-Link III lane. As part of the bi-directional control channel (BCC), it allows the De/Serializers to send signals back and forth. The Deserializer offers up to 8 GPIOs. Each GPIO pin can be mapped to one of the Serializers' GPO pin. It reflects the current state of a GPIO pin for general-purpose use. Alternatively, device status information such as "data lock indication" or "Frame Sync signal" can be mapped to one of the GPIOs. Frame sync signals can be generated in two different methods:

*   The first option offers sending the Frame Sync signal using one of the Deserializer's GPIO pin as input and mapping it to one GPO of all the DS90UB913A-Q Serializers.
*   The second option is to have the Deserializer to internally generate a periodic frame sync signal to send over the back channel of BCC to one Serializer's GPO pin.

Frame sync signaling on all back channels is synchronous, which ensures all cameras to operate fully synchronized (see Figure 5).

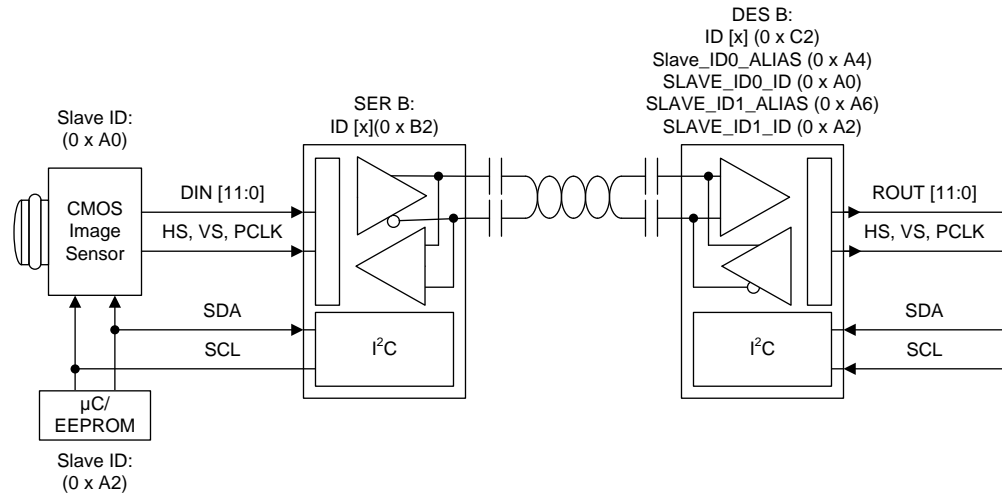Copyright © 2016, Texas Instruments Incorporated

Figure 5. Frame Sync Scheme

The DS90UB964-Q1 Deserializer features two slave mode I2C interfaces:

- The first I2C port is for local register configuration on the Deserializer side. Additionally, the bi-directional control channel (BCC) allows I2C communication with remote Serializers as well as remote I2C slave devices (for example, image sensors).
- The second I2C port uses the same I2C address as the primary I2C port. In addition, RX Port I2C IDs are also available for the second I2C port.

It is common to connect with multiple I2C slave devices holding the same Slave ID. For this reason an aliasing scheme had to be introduced to avoid conflicts. For instance, each Serializer connects with its own image sensor of the same type. Therefore, all of the image sensors' device IDs will be equal (physical address). In order to pass over I2C information to one sensor the I2C slave device address (Slave ID) needs to be assigned to one unique alias address (Slave Alias ID). If so, one external host will use unique alias addresses to access the slave devices' registers. In turn, the Deserializer re-maps the Slave Alias ID with the physical Slave ID and passes the stream over to the assigned BCC (see Figure 6).

> **NOTE:** For more information, see the DS90UB964-Q1 product page.

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Figure 6. I2C Slave Alias Translation

6 TI TDA2X Multi-Core Single Chip Processor

TI's TDAxx system-on-chip (SoC) family offers scalable and open solutions and a common hardware and software architecture for Advanced Driver Assistance Systems (ADAS) applications. Due to its rich set of interfaces, the TDA2x processor fits well into a wide range of camera-based applications. For instances, it offers video ports (VIP) to connect with more than six HDR video cameras providing up to 16 bits of dynamic range per pixel. Because of the heterogeneous architecture, it offers best in class ratio between the computational performance versus power consumption. The SoC incorporates the TI Vision Acceleration Pac with up to 4x Embedded Vision Engine (EVE) cores mainly for vector based low-level processing tasks. Two TI C66x DSP cores for intermediate-level processing: one dual core ARM Cortex A15 for high-level post-processing and two dual ARM Cortex M4 modules for host side application control (Control Logic).
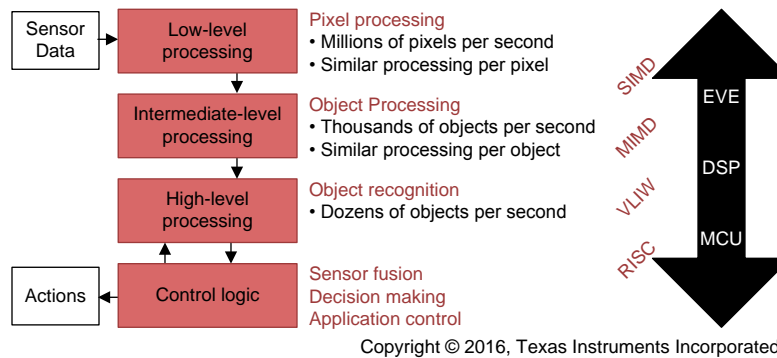
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Figure 7. Application Processing Levels

The TI VisionSDK is a multi-processor software development platform for TI's family of ADAS SoCs. The software framework allows you to create different ADAS application data flows involving video capture, video pre-processing, video analytics algorithms and video display. The SDK has sample ADAS data flows that exercise different CPUs and hardware accelerators in the ADAS SoC, and show customers how to effectively use different SoC sub-systems.

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NOTE: For more information, see the *TDA2x ADAS Applications Processor 23mm Package (ABC Package) Silicon Revision 1.1 Data Manual* (SPRS859) and the *TDA2x SoC for Advanced Driver Assistance Systems (ADAS) Silicon Revision 2.0, 1.x Technical Reference Manual* (SPRUHK5) or please contact your local TI representative.

7 System Data Flow

7.1 Forward Channel Stream

As illustrated in Figure 8, video streams from the imagers feed into four independent FPD-Link III LVDS Serializers (DS90UB913A-Q1). The Serializer's output streams travel over four long-distance coax cables to feed into a single FPD-Link III LVDS Deserializer hub (DS90UB964-Q1). The Deserializer hub merges two input streams into one MIPI CSI-2 output stream using virtual channel mode. The hub outputs four video streams in two CSI-2 channels, each containing two video streams. Each MIPI CSI-2 stream feeds into one OmniVision ISP (OV490). Each of the ISPs process two incoming camera streams. For each HDR picture to be computed, two incoming images are required. Depending on the current environmental brightness level, the images are either exposed "Long and Short" or "Short and Very Short". Each ISP processes two independent camera streams concurrently. However, it forms up one single video output stream consisting of lines in double length. One stream of computed HDR images in double width outputs through one parallel video port each (DVP). Finally, the TDA2x processor received the two streams over two independent video ports (VIP) and begins to process and display.

7.2 Back Channel Stream

Surround view systems require keeping all camera streams synchronized in order to stitch and render the streams together correctly. Frames of each camera will drift out of sync due to the variation of individual input clocks and other system tolerances. To keep the cameras synchronized, this design utilizes the GPIO feature of the FPD-LINK III back channel. Each image sensor (OV10640) supports frame sync control input on a dedicated FSIN pin. One FSIN trigger generated from the Deserializer is routed to all cameras ensuring the frames of each camera will start at the same time. Using this method, the cameras remain synchronized within ± one video row. Hence, the worst case delay will be about two lines. The Deserializer is programmed in sync mode and recognizes the start of the frame from the first FPD-Link channel. However, it waits even for the start of frame from the second FPD-Link channel prior to the output the combined stream on the CSI-2 bus. This ensures the interleaved dual camera stream on each MIPI port is NOT shifted by one or two lines. Designated packets from each virtual channel will be of same time slot. Alternately, in Round Robin mode, incoming rows of all cameras are streamed out across the chain in a first-come first-send fashion. However, this delay may not be acceptable. Additionally, the FSIN signal is sent out to the ISPs (OV490) via GPIO pins as well.
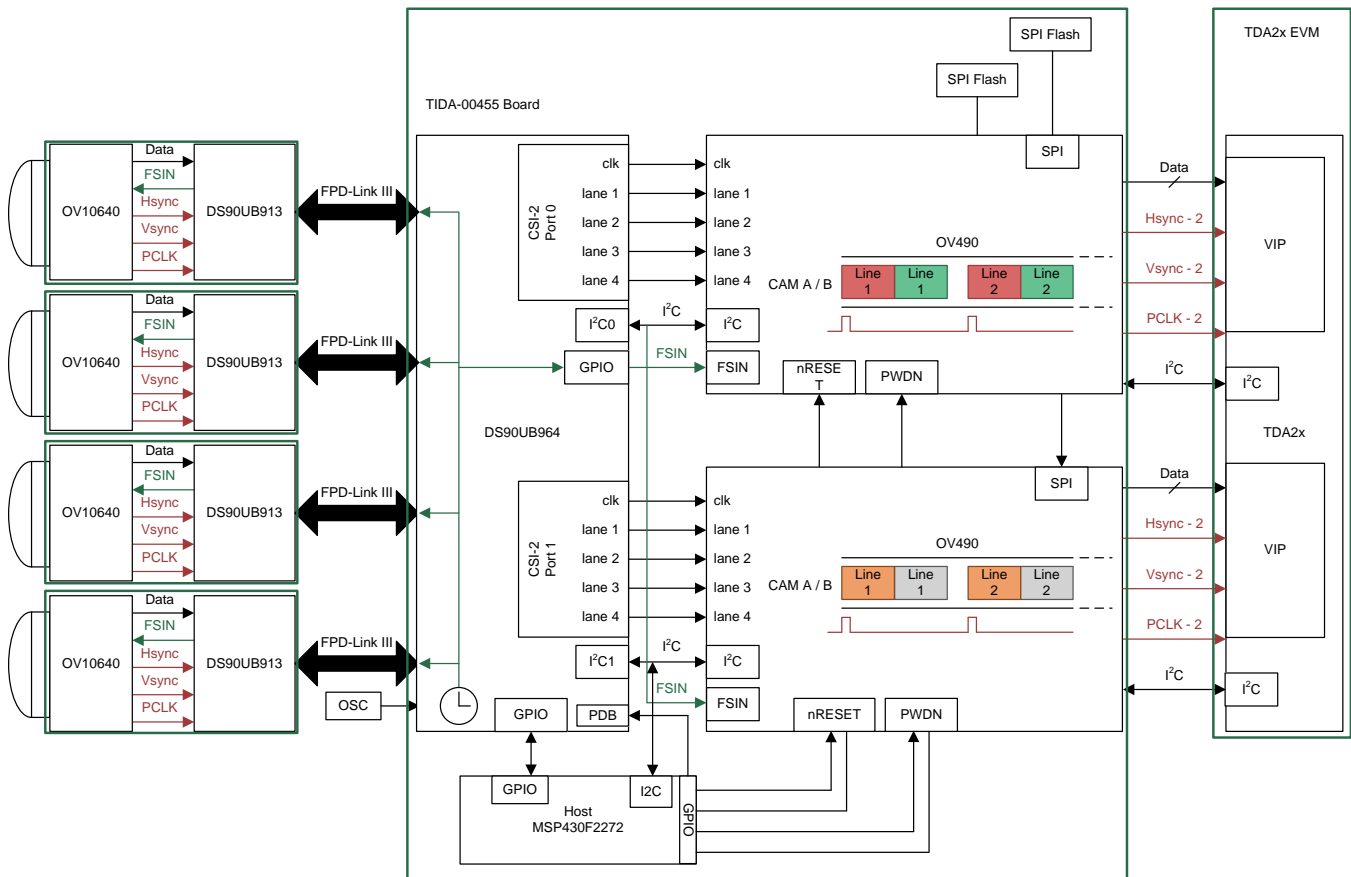
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Figure 8. TIDA-00455 Reference Design

8 TIDA-00455 System Configuration (or Setup)

Figure 8 shows the system stack up in the form of multiple modules encapsulated in green rectangles. The reference design includes one TIDA-00455 board consisting of 4x Rosenberger/FAKRA coaxial connectors, one DS90UB964-Q1 FPD-Link III Deserializer, two OmniVision OV490 ISPs, two SPI Flash memory devices and one MSP430 uController for system start up. In addition, four TIDA-00421 camera modules plug into the TIDA-00455 board using the FAKRA Jack coaxial cable. The TIDA-00421 combines the OV10640 1.3 Megapixel imager with the DS90UB913A-Q1 1.4 Gbit/s Serializer and providing the necessary power supply for both. All of this functionality is contained on a 20mm x 20 mm circuit card. The only connection required by the system is a single 50 Ω coaxial cable. For more information, see the TI Designs – TIDA-00421 Automotive 1.3M Camera Module Design with OV10640, DS90UB913A and Power Over Coax Design Guide. The TIDA-0455 board is connected to the TDA2x using the expansion connector (referenced as EXP-P2 in the schematic). For system order information, see Section 13.

9 TIDA-00455 System Start Up

This section discusses the sequence applied to the system in order for configuration and start up. When the system configuration is completed (see Section 10), power can be applied. The MSP430 host controller starts up turning the Deserializer and the two ISPs into reset/power down state. As a second step, it wakes up the Deserializer and begins to program its register set utilizing the I2C port.

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The host maps the FPD link control channel 0 and 1 to be linked with I2C port 0. In turn, it maps the FPD link control channel 2 and 3 to be linked with I2C port 1. From now on, the Deserializer passes incoming configurations over the I2C port 0 onto camera module 0 and 1. Likewise, it passes incoming configurations on I2C port 1 onto camera modules 2 and 3. As a next step, the CSI port transmitter speed is set to 800 mbps to ensure sufficient bandwidth. The frame sync generator's period is programmed to reflect the image sensor's frame interval. As follows, the generated frame sync signal is routed to GPIO0 of the Deserializer, but to the GPO0 of all the Serializes as well. It causes the frame sync signal to feed into the FSIN pin of all image sensors. Instead, GPIOs 1 to 4 are programmed to indicate FPD-Link RX ports to be locked. Finally, the frame sync generator will be enabled.

As a next programming sequence, all FPD-Link RX ports will be configured. RX ports are set for read and write transactions, BCC speed set to 2.5 Mbit and I2C commands to pass through. At this state, all I2C physical slave IDs are programmed to 0x60 because all image sensors respond on the same I2C device address. However, all I2C alias slave IDs are set to 0x60 for RX port 0, 0x62 for RX port 1, 0x64 for RX port 2 and 0x66 for RX port 3.

The following actions program the CSI ports. Per default, the incoming FPD-Link streams of all RX ports are assigned to a unique virtual channel number (VC). For instance, the stream received on RX port 0 from camera module zero will be assigned to VC-0. Whereas, the stream received on RX port 1 from camera module one will be assigned to VC-1 and so forth. The corresponding map registers assign VC-0 and VC-1 to CSI-2 port 0 while VC-2 and VC-3 are assigned to CSI-2 port 1. As presented in Figure 4, two camera modules are routed to one CSI-2 port. Finally, CSI-2 ports are set for normal operation in 4-lane mode. When the programming sequence to the Deserializer is completed, the host (MSP430) releases the ISPs (OV490) from reset. In turn, the ISPs load the firmware from two SPI Flash memory devices and begin to execute. As soon as base configuration is done, the ISPs take ownership of the image sensor configuration. The firmware design is left to OmniVision Technologies, Inc. To obtain customized firmware, contact www.ovt.com. Data flow kicks off and two video streams reach the expansion connector J29 for TDA2x VIPs to consume. The complete programming sequence including the register listing can be found in the file "init.c" of the MSP430 project.

10   TIDA-00455 System Board Bring Up

Several steps need to be gone through prior to the system being used. The following instructions need to be completed in order to prepare the system for startup. Please exercise carefully. Install jumper J6 on pins 2-3 to power the camera modules. Power over coax (PoC) voltage is 12 V by default and can be reduced to 5 V by installing jumper J13. Review board configuration in Figure 9.
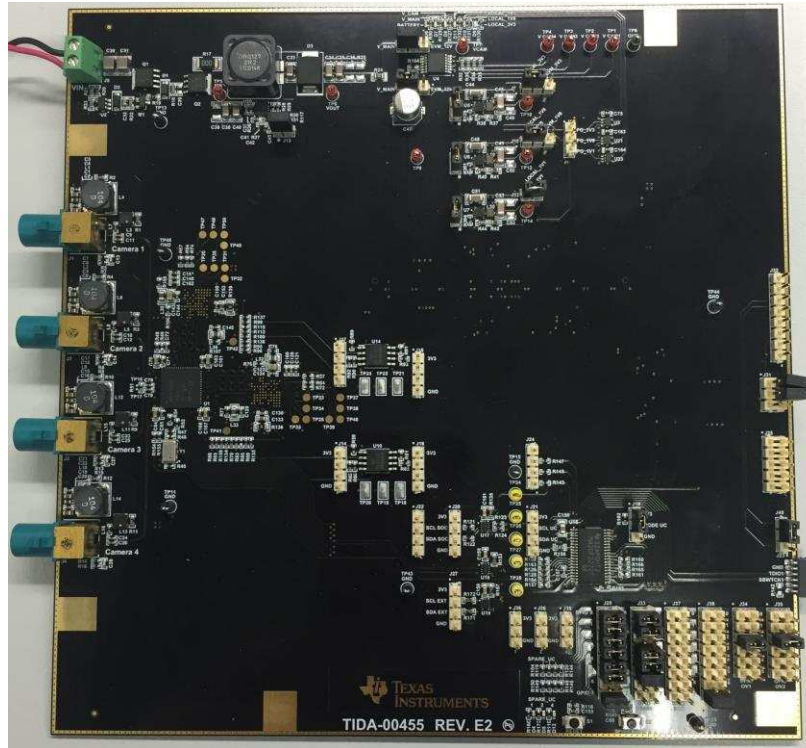

Figure 9. Board Review

10.1   MSP430 Software Setup

For board start up, the MSP430 uController acts as the base level host in the system. It needs to be programmed with control software to execute. The installation of TI's Code Composer Studio™ (CCS) development environment is required in order to upload the program onto on-chip Flash memory. Code Composer Studio even allows editing code source or debugging the configuration sequence. It requires the EZ430 debugger to upload the program. For more details, see Section 12.

10.2   OmniVision Software Setup

OmniVision Technologies Inc. provides the firmware for the ISPs to work. The firmware needs to be uploaded to the external SPI Flash memory devices. Using a SPI flash writer, hardware programming can be achieved. For more details, see Section 12.

10.3   TDA2x Software Setup

VisionSDK offers example "use cases" to help customers begin. It includes one use case supporting the -00455 system. One option to run VisionSDK on TDA2x is to copy a full VisionSDK image MLO file on a mirco SD Card in order to put the card into the card slot of the TDA2x EVM and to configure the EVM to boot from SD Card. With help of the terminal program, like TeraTerm or HyperTerminal, access to the program can be established using the universal asynchronous receiver/transmitter (UART) terminal on the TDA2x EVM.

- EVM switch settings:
  - Set SD boot mode using SYSBOOT [0-15] (SW2 and SW3) = 'b111000001000001
- Settings for UART:
  - Baud rate: 115200
  - Flow-control: none
  - Data: 8 bit
  - Parity: none
  - Stop: 1 bit

For basic board bring up, a pre-built test binary is shared at the TIDA-00455 landing page (see Section 13). The binary loads up a VisionSDK configuration supporting only TIDA-00455 board. Output is displayed on the HDMI port of TDA2x EVM. It displays a 2x2 mosaic of the videos from four camera inputs.

It also provides two UART based controls:

- '0' Exit and restart the use-case
- '1' Cycle the display on every '1' input as follows: Mosaic → Cam1 → Cam2 → Cam3 → Cam4 → Mosiac

Option '1' is useful to view individual camera outputs at full resolution. Mosaic output works only if all four camera links are active. Thus, this option also helps to identify the failed camera links by displaying individual outputs. After system power up, a menu will be listed in the terminal window with a selection of use cases. The use-case for TIDA-00455 system is listed under the "Multi-camera use-cases" menu. VisionSDK use-case expects all camera links to be working and will not display any video if any of the camera links fail. An introduction to VisionSDK can be found in the TI Vision SDK, Optimized Vision Libraries for ADAS Systems. For access to VisionsSDK sources, contact your local TI representative.

10.4 TIDA-00455 Board Level Programming

- Apply 12 V power
- Connect EZ430 debugger to J23
- Upload the program to MSP430 using CCS

10.5 TIDA-00455 SPI Flash Programming

- Apply 12 V power to TIDA-00455 board
- Jumper J40 selects the SPI flash chip (for memory 1 "Jumper pin 1-2"for memory 2 "Jumper pin 2-3")
- Jumper 3x of J31 (for SPI programming only)
- Put board into SPI Programming Mode:
  - Hold "spare_UC 3" S2 button and press S1 (reset)
- Release S1
- Connect Aardvark I2C/SPI Programmer to J25; ensure pin #1 to pin #1
- Connect Aardvark I2C/SPI Programmer with PC USB port
- Run flash center exe.
- Press "Add Adapters" button. You should find the Programmer in the list if the driver is installed correctly.
- Add w25q128 support using "winbond-spi-flash_w25q128.xml".
- Menu "Operations": "Choose Target" → press "load part file" → browse and select "winbond-spi-flash_w25q128.xml".
- It will add w25q128 support to the flash center.
- Select the w25q128 and press OK.
- Menu "File": Load file → select file to program "Erase" part. "Program" part.
- Move J40 jumper from 1-2 to 2-3, and repeat for the second SPI flash.

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- Remove J31 Jumpers before starting the application.
- Press reset (S1).

The functional demonstration can be found in Figure 10, which includes all of the components discussed. Four cameras are attached to the tripod on the left.

Figure 10. Demonstration

11   Power Supply Management Including POC

System power supply requirements and their concepts for camera-based ADAS systems can vary quite a lot from each other. Power management component selections depends on the system's automotive safety integrity level (ASIL) requirements needed for the end application (safety relevant or not), and if the surround view system is based either on a centralized or decentralized system concept. The impact of centralized/decentralized topology from a power supply perspective means, that the camera imagers are either supplied directly from the car battery each (with a local supply connector) or are supplied by a pre-regulated voltage rail coming from the surround view camera system's ECU within the video cable link.

To keep the TIDA-00455 reference design flexible, particularly during the evaluation phase of the system, the board includes a complete power supply concept to provide all required voltage rails. The main power to the board can either be supplied through connector J5 or directly from the TDA2x EVM by setting J6 correctly. In order to allow an evaluation of the system under real car battery load conditions, using test pulses for load dump, cranking, jump start, reverse battery, and so forth. The PCB might need some modification in order to fully meet all automotive test requirements (for example, it may not operate during cold crank). Even though, the TIDA-00455 reference design has a very wide voltage input range 'Vin' covering car battery input requirements from 4 V to 60 V and should withstand load dump and jump conditions.

The main supply input, labeled with 'car battery input' in the schematic (see Figure 11), includes a protection circuitry for over voltage and reverse battery protection. The component values for over voltage protection circuit have been chosen such that the switch-off trip point is at about 15.9 V, using the TLVH431-Q1 shunt regulator. If the input voltage exceeds the trip point, the shunt comparator causes the n-channel MOSFET M1 to switch off. This pulls up the p-channel MOSFET (Q2) gate and causes the transistor to switch off the main rail. Whereas, the body diode in Q1 remains forward biased. In addition, transistor Q1 is there to provide the reverse polarity protection. With this, the input to the first pre-stage DCDC regulator will have an input voltage protection, limited to about 16 V. 'Vin_Protect' is the input to the pre-regulating Wide-Vin voltage range DC-DC Converter TPS55340-Q1.

It is configured in a single ended primary inductance converter (SEPIC) topology. This switch mode power supply is adjusting the main system rail 'V_MAIN' to 12 V (or 5 V) depending on the configuration of J13. Any voltage from about 3 V to 16 V can be created by changing the feedback resistors R29, R30/31 The SEPIC topology has the advantage to work as a buck and boost regulator simultaneously, allowing to either increase or decrease the output voltage with regards to the input. This allows the system to operate from an input voltage as low as 4 V.

The setting of the output voltage is done by selection of the appropriate feedback resistor ratio of R30/R31. Here, the standard formula for setting the output voltage is used: Vout= Vref*(R30/R31+1). Resistor R29 must be added to R30 unless J13 is installed. The switching frequency of the regulator is selected by using resistor R28 within the following formula: fsw (KHz)=41600*R(freq)^-0.97(KΩ). It set's the switching frequency to about 2.5 MHz. All other adjustments for control loop compensation, selection of the SEPIC components (inductors, capacitor), and so forth are referred to the respective application section within the device-specific data sheet.
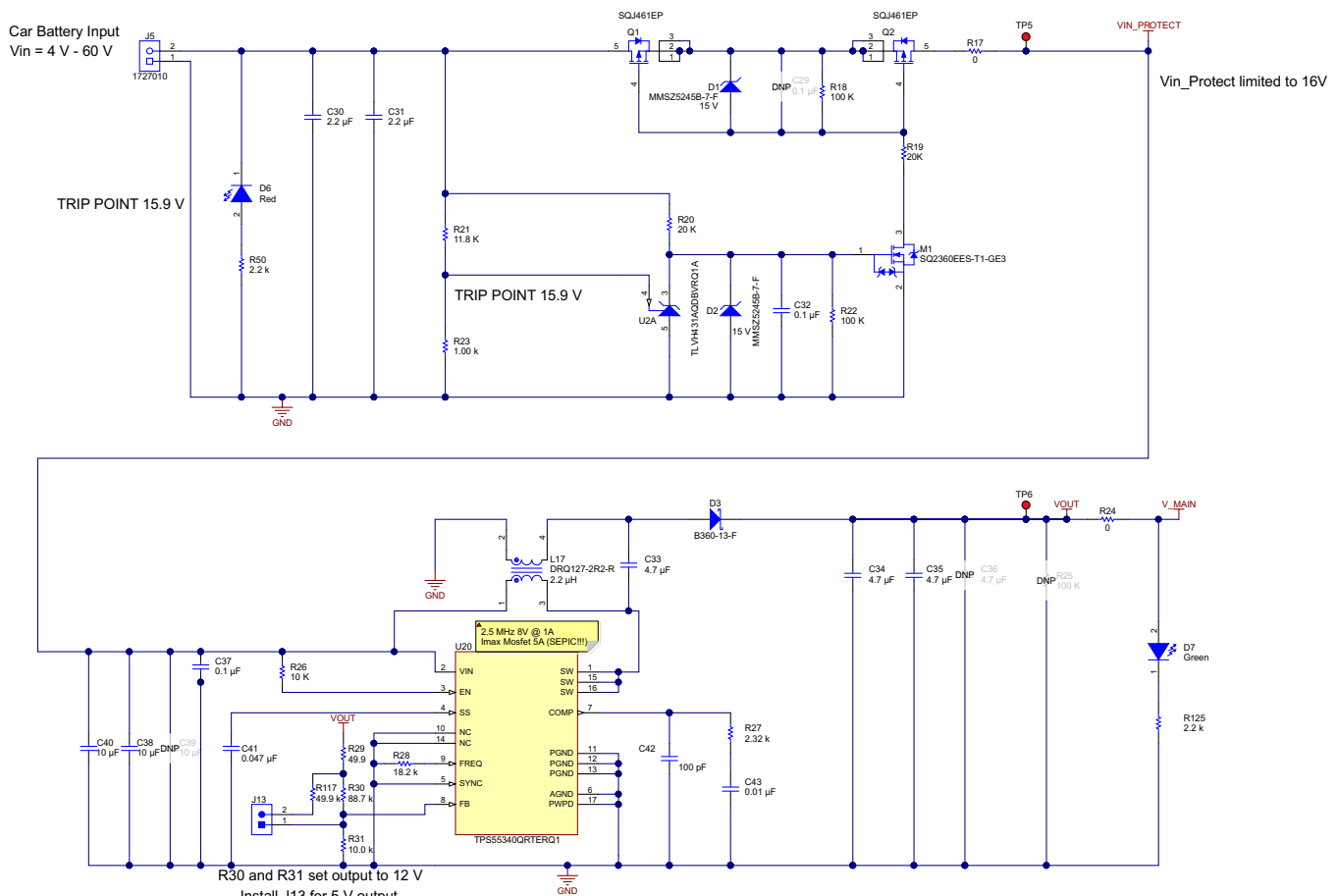
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**Figure 11. Input Circuitry and Pre-Stage Converter**

Subsequently to the TPS55340-Q1, a single smart high side switch TPS1H100-Q1 is used as a second stage line control for all four cameras as depicted in Figure 12. This switch enables the imagers, providing them with a low ripple voltage supply that is current limited. The total current limit (CL) for all camera heads is set to 500 mA imager (adjusted with R140). The switch is controlled by the onboard microcontroller and also includes diagnostic capabilities for short to GND/battery, open load, reverse polarity and thermal conditions.
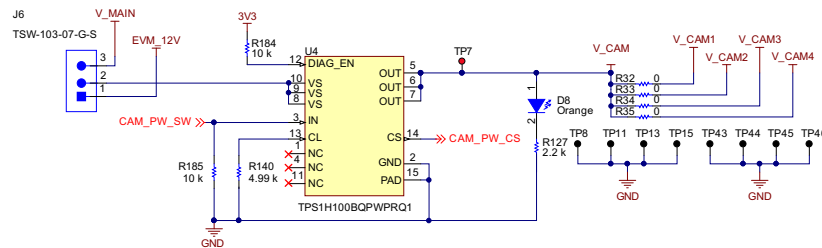
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Figure 12. Second Stage Line Control

Each of the four cameras is supplied from the reference design using PoC technology. The supply voltage/current is combined with the FPD-Link III high-speed data video line. It uses the single ended coax cable wire as the current forward path to the imager and the cable shield as the return current path to the system ground. Filters are used at each end to either combine or separate the signals of interest. Figure 13 illustrates the concept.
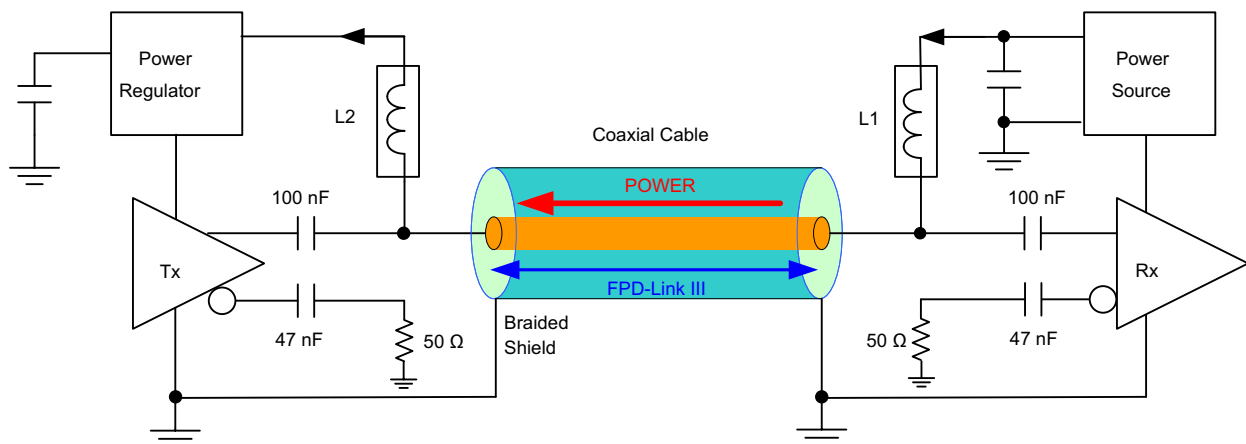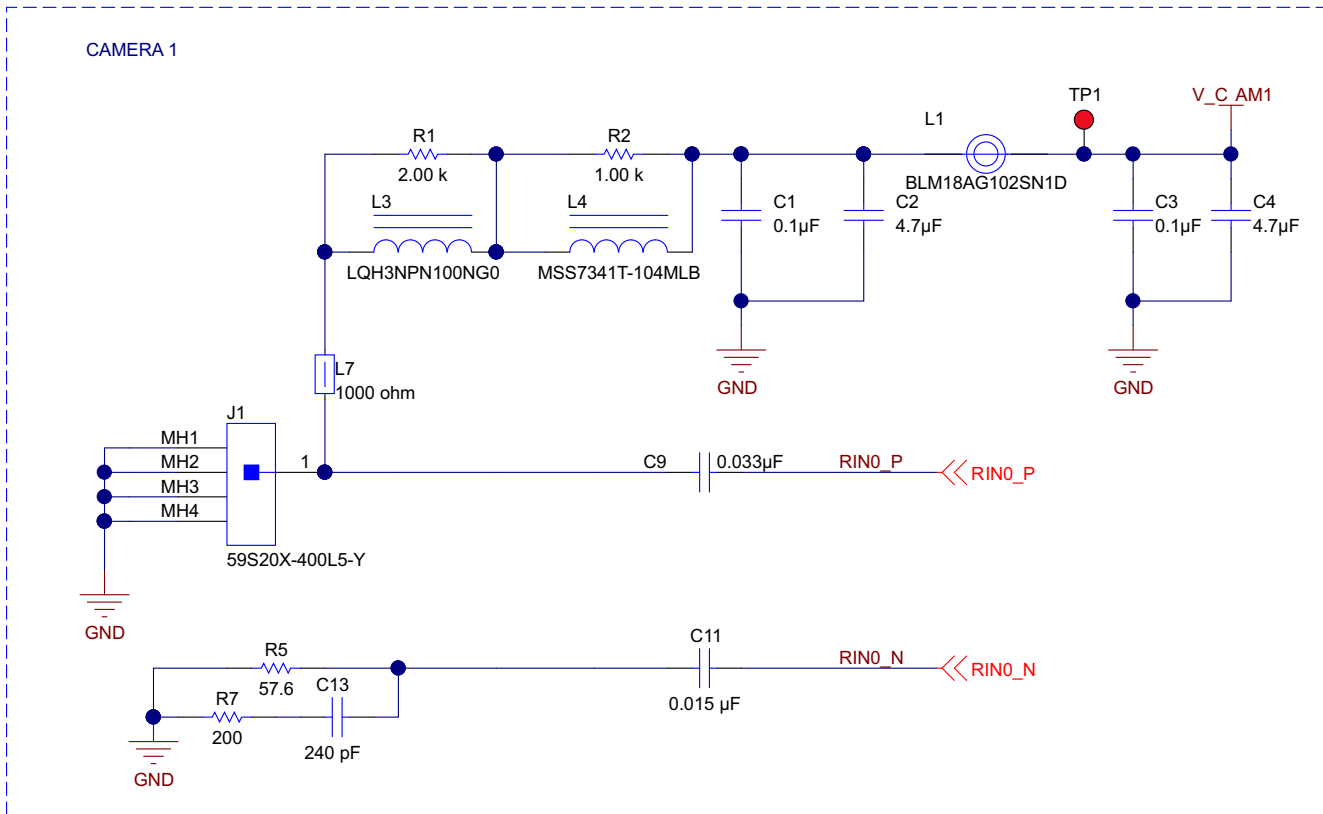

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Figure 13. PoC Concept

The most critical aspect to this is the correct power insertion filter design, which has to be implemented four times on the PCB. One filter section for camera 1 is representatively depicted in Figure 14.

The main filter components are two inductors in series (in this design 4.7uH + 100uH) that are required to provide high impedance characteristic at the frequency band of interest. This frequency range will be particularly defined by the FPD-Link III forward video data throughput rate (or pixel clock rate) and the back channel communication frequency. The filter impedance characteristic has to be 1KΩ or larger over the complete frequency range of interest to not affect the signal integrity of the video data. Since the DS90UB913A Serializer is capable to support a maximum pixel clock of 75 MHz in the 12-bit high frequency mode, the maximum line rate can be up to 1.4Gbps. This results into an analog bandwidth of 700 MHz. Since the back channel band requires 1-4MHz, the resulting frequency band to be covered is from 1-700 MHz (>1KΩ impedance).

An additional 1KΩ resistor in parallel to the inductors prevents the filter from spiking too high and allowing a total impedance of 1KΩ for higher frequencies. An additional pi/EMI-filter is added to allow the limiting of high frequency noise (for example, common mode noise) and to improve the EMI performance of the design. The ferrite bead (FB) has to be selected for best suppressor performance, so that the noise frequency falls into the resistive area of the FB's 'frequency vs. impedance' plot. For more detailed information, see Sending Power Over Coax in DS90UB913A Designs.

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Figure 14. PoC Filter Design

Remaining supply rails (3.3 V, 1.8 V and 1.1 V) are generated by three Second Stage BUCK converters acting synchronously (TPS62160-Q1). The converters generate the supply rails for components such as the Deserializer HUB (DS90UB960-Q1), two ISPs (OmniVision OV490), SPI Flash, micro controller (MSP430) and some I2C switches. Since frequency compensation is included, only a few external components are required to act stable, see Figure 15.

## 11.1 Various Power Supply Options and Levels of Integration

Designing a single board surround view system, the level of power management complexity increases. System includes even the Processor, external memory and other additional components that need to be supplied. Nevertheless, advanced power management concepts will allow achieving higher levels of functional safety. Therefore, the next sections discuss extended considerations in order to support several levels of automotive ASIL requirements.

11.1.1 Support of ASIL-A Requirements

The way the TIDA-00455 system is built it will most likely achieve ASIL-A requirements only.

NOTE: To meet any ASIL level is not the focus for this design approach. In any case of system disruptions, the application will not have control of defecting itself.

None of the voltage rails are monitored from an independent source. If for example the main rail 'V_MAIN' would drop out, the system wouldn't have evidence to react. Therefore, an additional comparator and an independent voltage reference would have to be implemented in order to control one rail (vise versa comparators for every rail). Another option is to sample each rail by an ADC (or an 8/16 channel MUX ADC) along with one uController for analysis. Often, uControllers provide such feature on-chip. Alternatively, supervisory devices can tie the open drain outputs together. Doing so, only one uController input pin is required. However, it avoids visibility of which rail is dropping. For certain levels of safety, this still might be acceptable and more cost effective.
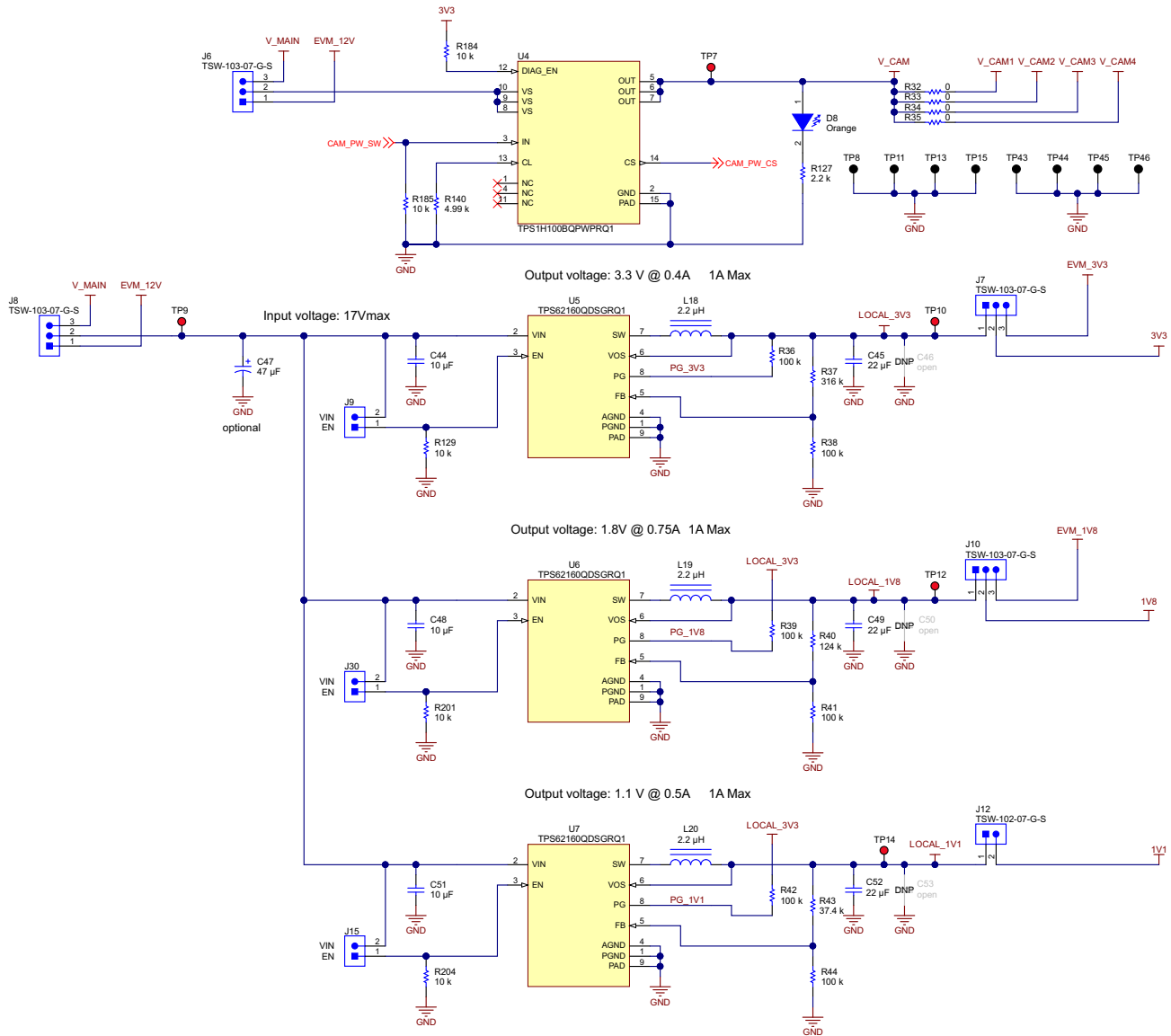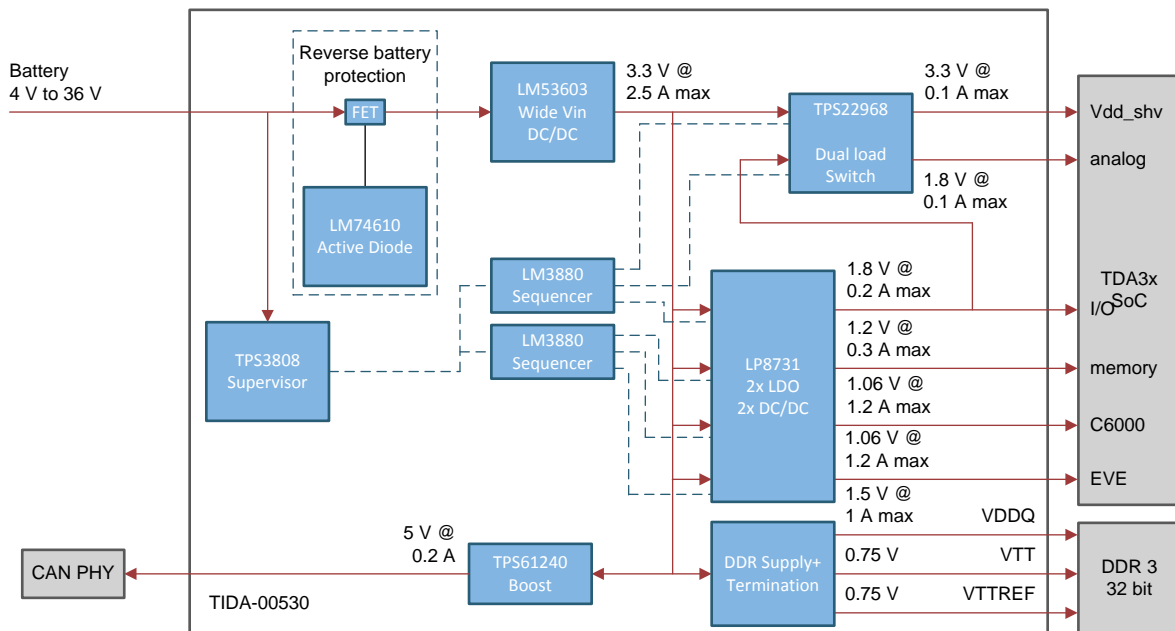

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Figure 15. Power Management

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11.1.2 Support of ASIL-A and ASIL-B Requirements

In comparison to the TIDA-00455 design, the TIDA-00530 reference design demonstrates an advanced approach. Multiple blocks have been added to increase the level of integration (see Figure 16). At main battery input (4 V to 36 V), the TIDA-00455 design uses a pair of TVS diodes to protect against positive and negative transitions. On TI Designs – TIDA-00530 Automotive Power Reference Design for Low Power TDA3x Based Systems, an LM74610-Q1 is used as an active diode for reverse battery protection. It addresses the automotive requirement to not drive significant backward current into the car board net. Even though this has no relevance for ASIL itself, the active diode reduces the power consumption of the system quite significantly (typ. 600-700 mV times the load current). The first block more relevant to safety is the LM3808-Q1.

As a supervisory, it detects rising or falling battery voltage levels and enforces power-up and power down sequences, if required. The trip point is set to 4 V, ensuring a voltage level above initiates a controlled power up sequence only. The opposite would shut the system down in a controlled manner. The supervisor should monitor the battery voltage at a point prior to the reverse polarity protection stage. It avoids the LM74610-Q1 "hiccup" behavior impact. The LM3880-Q1, supports multiple sequences to power-up and power-down rails. In addition, respective delays can be selected and factory programmed. It ensures all TDA3x supply rails to ramp in accordance with its specification. The LP8731-Q1 multi-rail PMIC (power management integrated circuit) even implements a power up/down sequence. However, the LP8731 PMIC might not support all possible application use cases. Optionally, a second LP8731-Q1 device or one of the PMIC family members as such as the LP8732-Q1 or the LP8733-Q1 could be used. The LM53603-Q1 is a 3A wide-Vin synchronous Buck converter, ideal to work as an automotive pre-stage regulator (2.1 MHz switching frequency, up to 42 V transients, and so forth). The LM5360x-Q1 series step-down converters provide a 'RESET' function that differentiates from 'power good' flag. It implements a glitch filter, which prevents false flag operation for short excursions in the output voltage during line and load transients. uController or some logic can process it to monitor the 3V3 rail.

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Figure 16. TDA3x Based Power Solution

11.1.3 Support of ASIL-B and –C Requirements

The TPS65310A-Q1 safety PMIC can be used as one option at these levels. It includes one DC/DC controller, two integrated BUCK converters, one BOOST converter and one LDO. It allows direct connection to the car battery supporting input voltage levels from 4.8 V to 40 V (up to 60 V absolute maximum). Along with an external PMOS protection feature (gate drive FET pin), the device is able to withstand even voltage transients up to 80 V. For meeting higher ASIL levels (B and C), it is mandatory to provide independent voltage monitoring capabilities for each rail. The TPS65310 device enables monitoring by providing independent bandgap references.

Independent bandgap references are used for monitoring each output rail of the PMIC and for the switch mode power supply topologies. In addition, the chip includes an integrated watchdog circuit, independent reference voltage output (with separate bandgap) for an external ADC or uController and under/overvoltage protection and detection. With TPS65310A-Q1, the switching frequency of the BUCK controller is 490 KHz, and the BUCK/BOOST converters run at 1 MHz.

If one requires, the switching converter frequency to be above the 2 MHz band for EMI reasons, the TPS65311-Q1 feature and functional equivalent device could be used. It switches all converter blocks at 2.45 MHz. A spread-spectrum clocking feature is implemented in both devices and can be enabled, if required.

The TPS65310A-Q1 can be used as a pre-stage safety PMIC, providing all main rail supplies into the system (such as 1V8, 3V3, 5V0, and so forth). As a secondary power management IC, the TPS65917 or LP8732/33 can be used to support multiple processors of the TDAxx family (TDA2x, TDA3x).

Since the TPS65917-Q1 is a complementary power management device for TI's TDA2x processor, it provides dedicated one-time programming (OTP) capability to meet the processor sequencing specification. It includes the configuration of all five SMPS outputs (including integrated monitoring) and five LDO outputs (one low noise LDO). In addition, it controls power up/down sequencing for TDA2x, manages interrupt handling, offers a watchdog timer, supports adaptive voltage scaling (AVS) capability for multiple rails and the clocking scheme (and more). A complete block diagram is depicted in Figure 17.
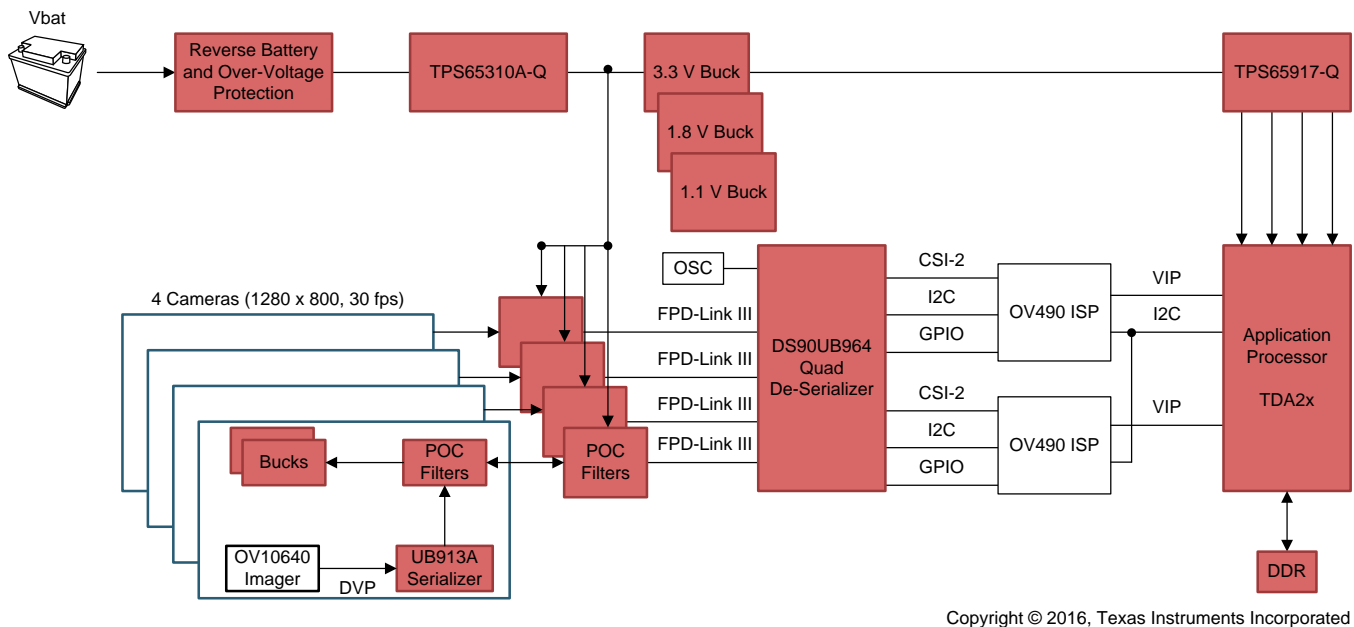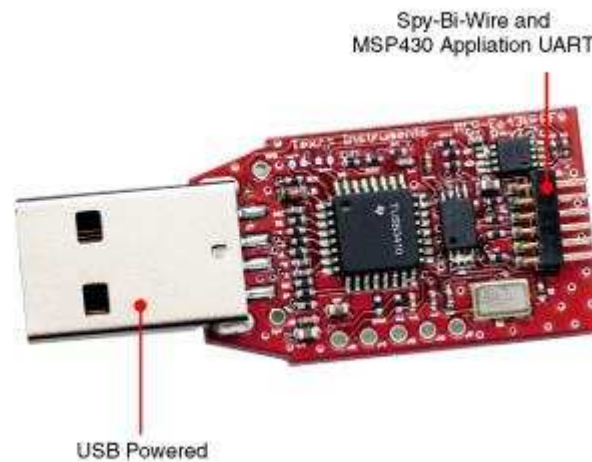

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Figure 17. TPS65310/TPS65917 Block Diagram

12 System Tools

- Code Composer Studio Development Environment
- VisionSDK
    - Contact your local TI representative.
- MSP430 Programmer with Code Composer
    - EZ430-F2013 Development Tool to program MSP430
      Order at: http://www.ti.com/tool/eZ430-f2013

- Aardvark I2C/SPI Host Adapter, or similar to program SPI FLASH
-
    - http://www.totalphase.com/products/aardvark-i2cspi/
- Download Totalphase USB drivers for the Aardvark I2C/SPI Host Adapter:
    - http://www.totalphase.com/products/usb-drivers-windows
- Install first. After completed, plug in Aardvark I2C/SPI Host Adapter.
    - Download Totalphase "flash center" http://www.totalphase.com/products/flash-center/.

13 References

- 4x Camera modules:
  - 4x TIDA-00421
    - http://www.ti.com/tool/tida-00421
- Fakra Coaxial Cables:
  - 4x FAKRA Jack to FAKRA Jack cables using RG174 Coax:
    - PE38746Z-60 Cable, 60 in Rosenberger HSD connectors and cables
    - http://www.pasternack.com/fakra-jack-fakra-jack-rg174au-cable-assembly-pe38750z-p.aspx
- TIDA-00455 board:
  - http://processors.wiki.ti.com/index.php/TIDA-00455_-_Automotive_ADAS_4_Camera_Hub_with_integrated_ISP_and_DVP_outputs
  - Order at: http://www.krypton-solutions.com/ Krypton Solutions LLC, 3060 Summit Avenue, Plano, Texas 75074, Cell: 469-685-8260
- Power over coax (PoC):
  - Sending Power Over Coax in DS90UB913A Designs
- TDA2x EVM:
  - TDA2x EVM:
    - Part number: 703761-1021: Vayu CPU Board ES 1.1/ES 2.0 GP
  - Sales email: http://www.spectrumdigital.com/
    - Sales telephone: 1,281.494.4500 x-113
  - Alternatively, order in Germany at lilotronik
    - http://www.lilotronik.com/
- Monitor:
  - Standard HDMI 1080p60 Monitor
- Literature:
  - TIDA-00455 system landing page
- OV10640 Data Sheet
- OV490 Data Sheet
  - Contact your local OVT representative.
- DS90UB913A-Q1 product folder: http://www.ti.com/product/ds90ub913a-q1
- DS90UB964-Q1 product folder: http://www.ti.com/product/ds90ub964-q1
- TIDA-00421 camera module description
- *TDA2x ADAS Applications Processor 23mm Package (ABC Package) Silicon Revision 1.1 Data Manual* (SPRS859)
- *TDA2x SoC for Advanced Driver Assistance Systems (ADAS) Silicon Revision 2.0, 1.x Technical Reference Manual* (SPRUHK5)
- TI Designs – TIDA-00421 Automotive 1.3M Camera Module Design with OV10640, DS90UB913A and Power Over Coax
- TI Vision SDK, Optimized Vision Libraries for ADAS Systems
- Sending Power Over Coax in DS90UB913A Designs
- TI Designs – TIDA-00530 Automotive Power Reference Design for Low Power TDA3x Based Systems

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (August 2016) to A Revision   **Page**

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