



1. Description

1.1. Project

Project Name	CubeIDE-TPC-Test-Bench-703885-01
Board Name	NUCLEO-L011K4
Generated with:	STM32CubeMX 6.2.1
Date	06/16/2021

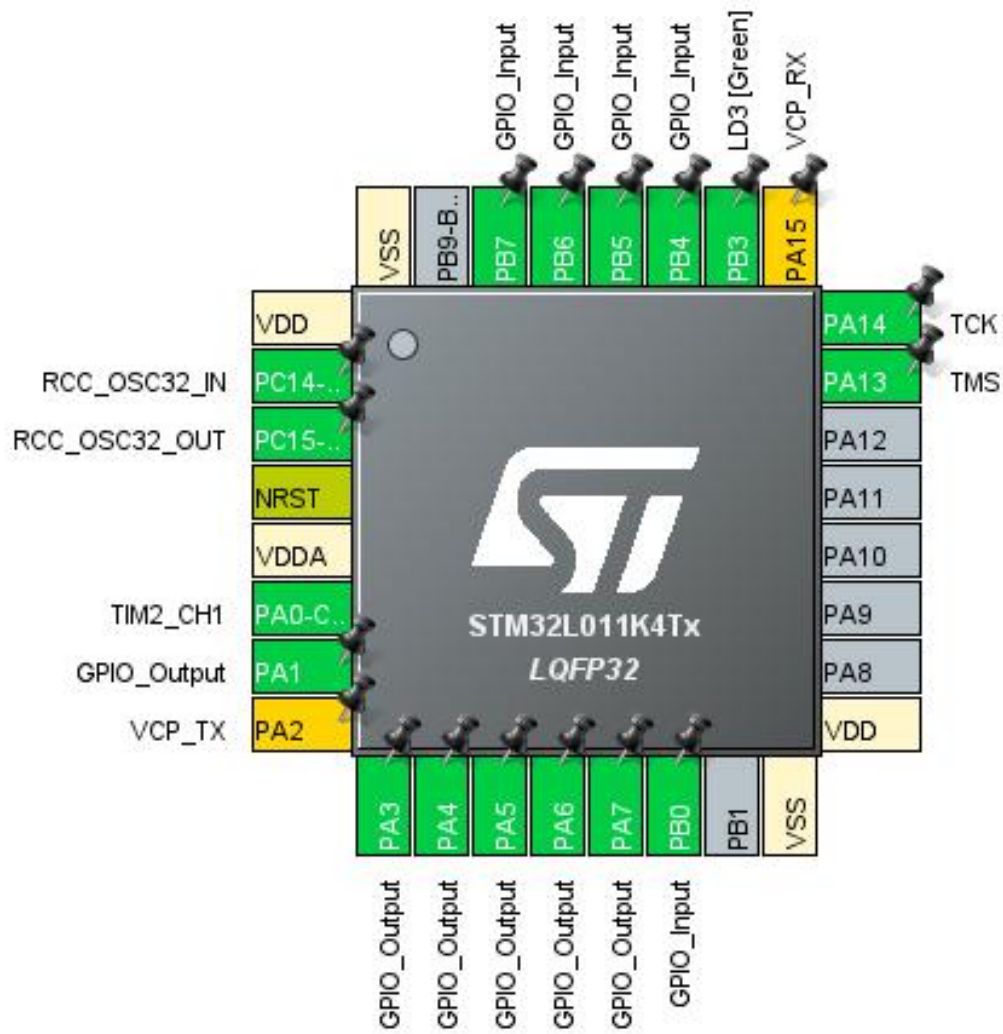
1.2. MCU

MCU Series	STM32L0
MCU Line	STM32L0x1
MCU name	STM32L011K4Tx
MCU Package	LQFP32
MCU Pin number	32

1.3. Core(s) information

Core(s)	Arm Cortex-M0+
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2. Pinout Configuration



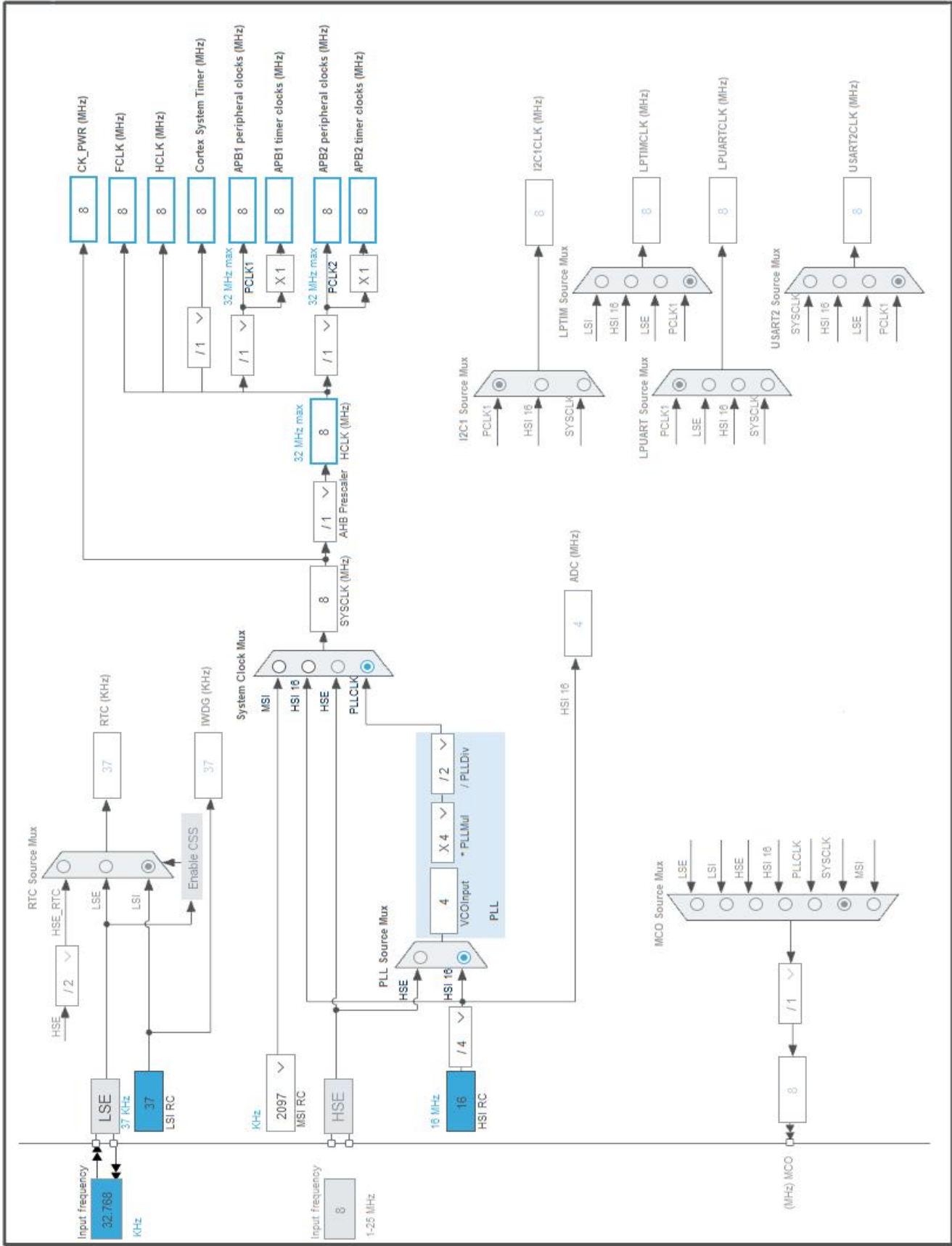
3. Pins Configuration

Pin Number LQFP32	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VDD	Power		
2	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
3	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
4	NRST	Reset		
5	VDDA	Power		
6	PA0-CK_IN	I/O	TIM2_CH1	
7	PA1 *	I/O	GPIO_Output	
8	PA2 **	I/O	USART2_TX	VCP_TX
9	PA3 *	I/O	GPIO_Output	
10	PA4 *	I/O	GPIO_Output	
11	PA5 *	I/O	GPIO_Output	
12	PA6 *	I/O	GPIO_Output	
13	PA7 *	I/O	GPIO_Output	
14	PB0 *	I/O	GPIO_Input	
16	VSS	Power		
17	VDD	Power		
23	PA13	I/O	SYS_SWDIO	TMS
24	PA14	I/O	SYS_SWCLK	TCK
25	PA15 **	I/O	USART2_RX	VCP_RX
26	PB3 *	I/O	GPIO_Output	LD3 [Green]
27	PB4 *	I/O	GPIO_Input	
28	PB5 *	I/O	GPIO_Input	
29	PB6 *	I/O	GPIO_Input	
30	PB7 *	I/O	GPIO_Input	
32	VSS	Power		

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	CubeIDE-TPC-Test-Bench-703885-01
Project Folder	D:_limbo\Synov-groupe\test-jigs\tpc\new\CubeIDE-TPC-Test-Bench-703885-01
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_L0 V1.12.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x080
Minimum Stack Size	0x200

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_TIM2_Init	TIM2
4	MX_TIM21_Init	TIM21

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32L0
Line	STM32L0x1
MCU	STM32L011K4Tx
Datasheet	DS11100_Rev4

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Li-SOCL2(AAA700)
Capacity	700.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	10.0 mA
Max Pulse Current	30.0 mA
Cells in series	1
Cells in parallel	1

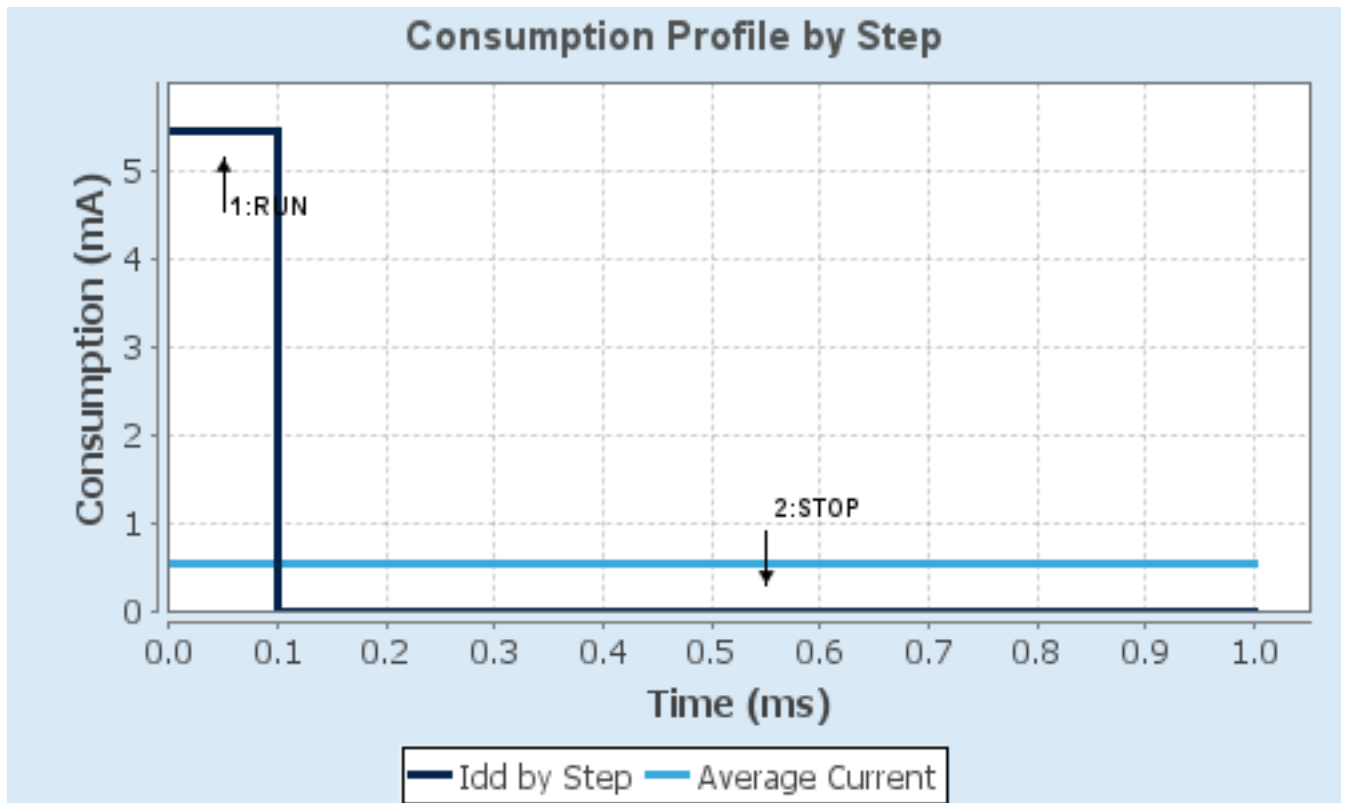
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-High	NoRange
Fetch Type	FLASH/PREFETCH	FLASH
CPU Frequency	32 MHz	0 Hz
Clock Configuration	HSI PLL2 Flash-ON	ALL CLOCKS OFF
Clock Source Frequency	16 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	5.45 mA	344 nA
Duration	0.1 ms	0.9 ms
DMIPS	30.0	0.0
Ta Max	104.02	105
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	545.31 μ A
Battery Life	1 month, 22 days, 23 hours	Average DMIPS	3.04 DMIPS

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. RCC

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.1.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Buffer Cache	Enabled
Prefetch	Disabled
Preread	Enabled
Flash Latency(WS)	0 WS (1 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
MSI Calibration Value	0
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
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7.2. SYS

mode: Debug Serial Wire

Timebase Source: SysTick

7.3. TIM2

Clock Source : Internal Clock

Channel1: PWM Generation CH1

7.3.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	1600 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	400 *
Output compare preload	Disable *
Fast Mode	Disable
CH Polarity	High

7.4. TIM21

Clock Source : Internal Clock

7.4.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	26667 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

* User modified value

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_SWDIO	n/a	n/a	n/a	TMS
	PA14	SYS_SWCLK	n/a	n/a	n/a	TCK
TIM2	PA0-CK_IN	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
Single Mapped Signals	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	VCP_TX
	PA15	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	VCP_RX
GPIO	PA1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB0	GPIO_Input	Input mode	Pull-up *	n/a	
	PB3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD3 [Green]
	PB4	GPIO_Input	Input mode	Pull-up *	n/a	
	PB5	GPIO_Input	Input mode	Pull-up *	n/a	
	PB6	GPIO_Input	Input mode	Pull-up *	n/a	
	PB7	GPIO_Input	Input mode	Pull-up *	n/a	

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
System service call via SWI instruction	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
TIM21 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash and EEPROM global interrupt	unused		
RCC global interrupt	unused		
TIM2 global interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
System service call via SWI instruction	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
TIM21 global interrupt	false	true	true

* User modified value

9. System Views

9.1. Category view

9.1.1. Current

Middleware				
System Core	Analog	Timers	Connectivity	Computing
DMA		TIM2 ✓		
GPIO ⚠		TIM21 ✓		
I2C ✓				
RCC ✓				
SYS ✓				

10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00206508.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00108282.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00104451.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00237371.pdf
Application note	http://www.st.com/resource/en/application_note/CD00160362.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00081379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00085385.pdf
Application note	http://www.st.com/resource/en/application_note/DM00087593.pdf
Application note	http://www.st.com/resource/en/application_note/DM00108286.pdf
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Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00145318.pdf
Application note	http://www.st.com/resource/en/application_note/DM00151811.pdf
Application note	http://www.st.com/resource/en/application_note/DM00158601.pdf
Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf
Application note	http://www.st.com/resource/en/application_note/DM00150423.pdf

Application note http://www.st.com/resource/en/application_note/DM00209725.pdf

Application note http://www.st.com/resource/en/application_note/DM00209768.pdf

Application note http://www.st.com/resource/en/application_note/DM00220769.pdf

Application note http://www.st.com/resource/en/application_note/DM00206898.pdf

Application note http://www.st.com/resource/en/application_note/DM00257177.pdf

Application note http://www.st.com/resource/en/application_note/DM00272912.pdf

Application note http://www.st.com/resource/en/application_note/DM00226326.pdf

Application note http://www.st.com/resource/en/application_note/DM00236305.pdf

Application note http://www.st.com/resource/en/application_note/DM00260952.pdf

Application note http://www.st.com/resource/en/application_note/DM00327191.pdf

Application note http://www.st.com/resource/en/application_note/DM00355687.pdf

Application note http://www.st.com/resource/en/application_note/DM00354244.pdf

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