# Department of Computer Science & Engineering

## University of Asia Pacific (UAP)

**Program: B.Sc. in Computer Science and Engineering**

**Final Examination** **Spring 2020** **3rd Year 2nd Semester**

**Course Code: CSE 317** **Course Title: Computer Architecture** **Credits: 3**

**Full Marks: 120* (Written)** **Duration: 2 Hours**

* Total Marks of Final Examination: 150 (Written: 120 + Viva: 30)

**Instructions:**

1. There are **Four (4)** Questions. Answer all of them. All questions are of equal value. Part marks are shown in the margins.
2. Non-programmable calculators are allowed.

**1.** Design and Implement the single cycle data path for the following instructions and write down the procedure of data path for following MIPS instructions: (consider all the functional units of Data path according to MIPS architecture)

* Where X= last two digits of your ID.

i) lw $s4, x($s0) ; **5**

ii) sw $to, X($s0) ; **5**

iii) Add $to, $s1, $s2; **5**

iv) A [x] =Y + A [x+8]; **15**

**2.** **a)** CPU request the following Block addresses (x+20), (x+16) and (x+25). **20**
There are 16 one-word blocks in cache. Design and Show the memory mapping for the following cache configurations.

I. Direct mapped.

II. 2-Way, 4-way ,8-way and 16- way set associative mapped. (use LRU replacement policy)
* Where X= last two digits of your ID.

**b)** **10**

For the following configuration Determine the number of bits required for physical address, tag, index and block offset.

i) Consider 32 words cache and 512 words main memory. Block size 4 words. Determine the number of memory blocks and cache lines.
ii) Consider 16 words cache and 64 words main memory. Block size 4 words.
iii) Consider 16 words cache and 128 words main memory. Block size 4 words.
iv) Consider 32 words cache and 1024 words main memory. Block size 4 words.

v) Consider 8 words cache and 16 words main memory. Block size 4 words
Also draw the required block for direct mapping cache.

**3.** **a)** Compare between pipeline machine and non-pipeline machine. suppose there are (x+7) instructions in a program. Draw the page table and compute the following: (where X is the last digit of you ID number) * consider there are 5 stages and each takes one clock cycle. **10**

- Total time for pipeline and non-pipeline.
- Speedup
- Efficiency or utilization

**b)** Consider a non-pipelined machine with 5 execution stages of lengths 12 ns, 15 ns, 8 ns, 18 ns, and 20 ns. **10**

- Find the instruction latency on this machine.
- How much time does it take to execute (**i**+1000) instructions?

Suppose we introduce pipelining on this machine. Assume that when introducing pipelining.

- What is the instruction latency on the pipelined machine?
- How much time does it take to execute (**i**+1000) instructions?

Also calculate the speedup.

(where **i** is the last two digits of you ID number)

**c)** This question considers the basic MIPS, 5-stage pipeline (IF, ID, EXE, MEM, WB). **10**

Assume that you have the following sequence of instructions:

lw $s2, 0($s1) (instr1)
add $s3, $s4, $s2 (instr2)
Sub $s6, $s2, $s3. (instr3)

Show the implementation through 5 stages and explain the implementation for both pipelined and non-pipelined design. (explain if there is any pipeline hazards)

**4.** **a)** What is the objective of memory hierarchy? According to cost, size, distance and speed compare among the levels of memory. **5**

**b)** Solve the following using 3rd or final version of multiplication algorithm. **20**
m*(-mx) using 5-bit multiplier.
Where m = multiplicand = {(last digit of your registration) mod 5} + 4.
Mx = multiplier = 5

**c)** Also draw the required hardware for the solution of question 4. b. **5**

**OR**

**a)** What are the four questions about cache design? Show and explain the hardware implementation of block identification. (data may be Hit OR miss). **5**

**b)** For the following high-level statement write the MIPS machine Code. **20**

X[**i**] = Z + X[i+11] - W; Where i = last two digits of your registration number.

| Instruction | Opcode/Function |
|---|---|
| lw | 100011 |
| sw | 101011 |
| sub | 100010 |
| add | 100000 |

**c)** What is the objective of memory hierarchy? According to cost, size, distance and speed compare among the levels of memory. **5**