

University of Asia Pacific
Department of CSE
Mid-Semester Examination Spring 2020
Program: B.sc in CSE

Course Title: Computer Architecture

Course No. CSE 317

Credit: 3.00

Time: 1.30 Hour.

Full Mark: 60

There are **four** Questions. **Answer three questions including Q-2 and Q-3.**

1. a. Draw the basic components of computer and Layer of a computer. Show the relationship among Instruction Set, Software and Hardware that define computer architecture. [5]
 - b. Suppose we have two implementation of same instruction set architecture. [15]
Computer A has a clock cycle time of 300 ns and a CPI of 1.8 for some program, and computer B has a clock cycle time of 550 ns and a CPI of 1.4 for the same program. Which computer is faster and how much?

or
 - a. Define the following terms: [5]
 - Response time/ execution time
 - Bandwidth/ throughput
 - Relative performance
 - Measuring performance
 - Clock cycle
 - b. Compiler designer is trying to decide between two code sequences for a [15]
particular machine. Based on the hardware implementation, there are three different classes of instructions: Class A, Class B, and Class C, and they require three, two, and four cycles (respectively).
The first code sequence has 9 instructions: 4 of A, 2 of B, and 3 of C.
The second sequence has 11 instructions: 6 of A, 3 of B, and 2 of C.

Which sequence will be faster? How much?
2. a. How many instruction classes are in MIPS architecture? Why R-type class [5]
instructions are faster than I- type instruction class.

- b. For the following high-level statement write the MIPS machine Code. [15]

$X[i] = Z + X[i+5] - W$; Where i = last two digits of your registration number.

3. a. Solve the following using **Booth's** logic. [15]

$m * (-mx)$ using 5-bit multiplier.

Where m = multiplicand = $\{(\text{last digit of your registration}) \bmod 5\} + 4$.

Mx = multiplier = -4 .

- b. Also draw the required hardware for the solution of question 4. a.

[5]

Instruction	Opcode/Function
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lw	100011
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sw	101011
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sub	100010
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add	100000
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