## Department Of Computer Science and Engineering

**Course Title:** VLSI Lab

**Course Code:** CSE 458

**Lab Report:** 06

**Experiment Name:** Directed Testing or Digital Sub-System

| | |
|---|---|
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## Objective:

Most digital ICs are developed using semi-custom IC design methodologies, which rely on HDL-based design and EDA tools for synthesis, placement, and routing.
Semi-custom methods include:

1)Standard Cell-based ASIC Design

2)Gate Arrays

3)FPGA

In ASIC design, pre-designed library cells are used, giving flexibility in cell placement and routing. The top-down design flow starts from system-level specifications, then proceeds to behavioral and RTL models for functional verification through simulation.

This experiment aims to:

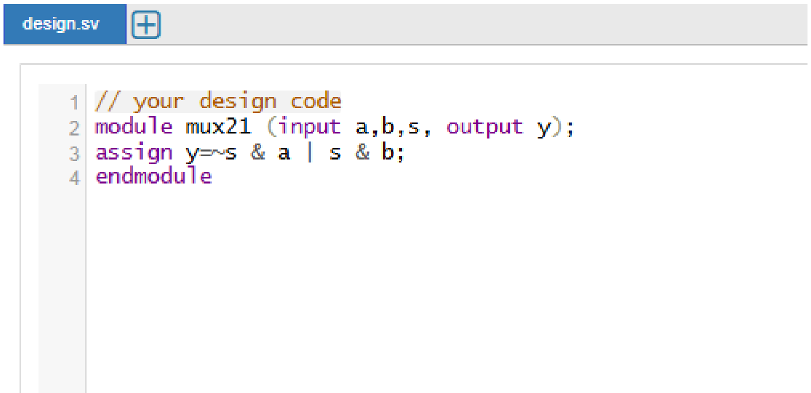
1)Explore EDA Playground for RTL design.

2)Understand Verilog testbenches using directed testing.

## Task 1:

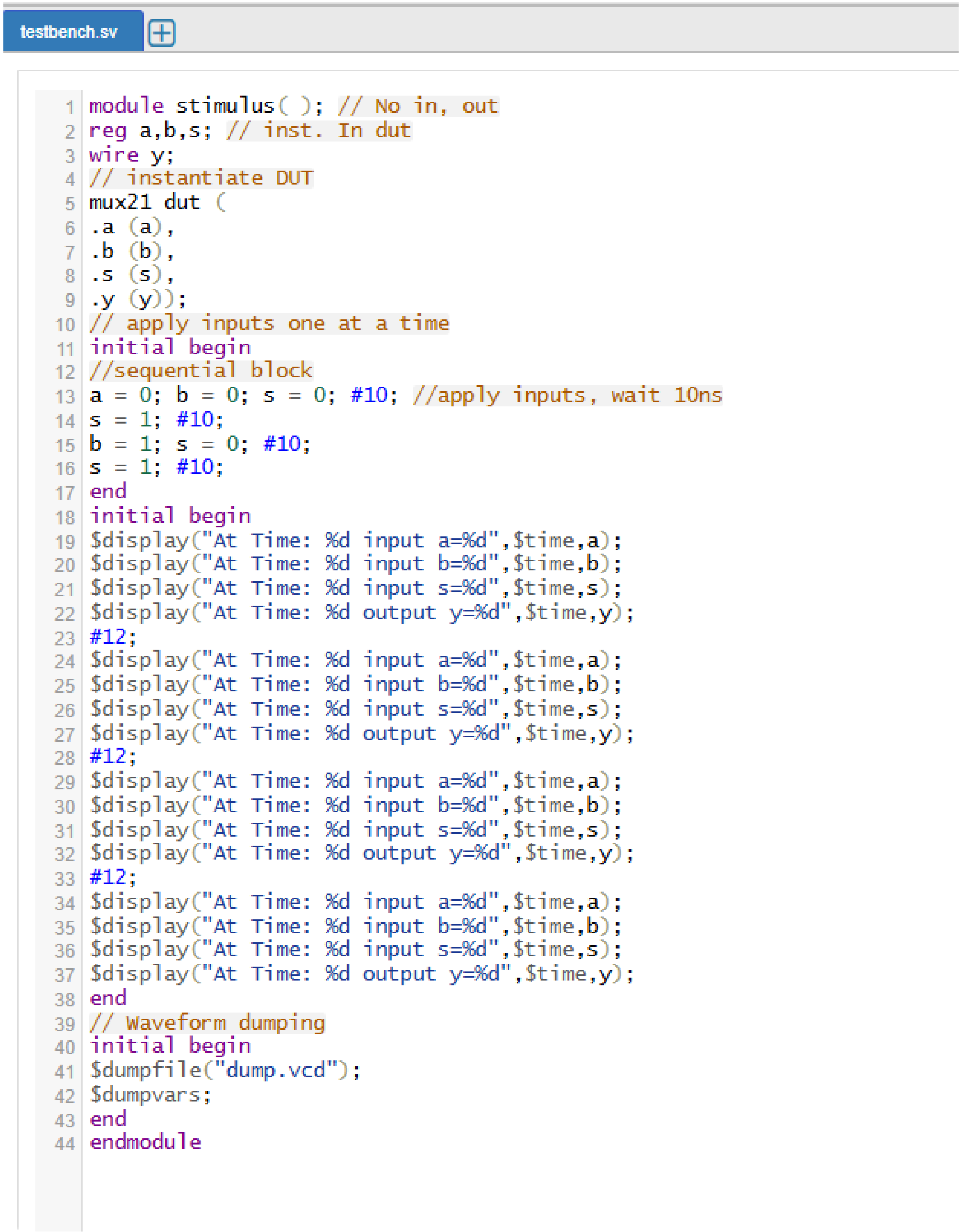
Write the verilog code of a 2/1 mux. Test your code with a direct testbench. Show the code of the circuit, its testbench, and the output obtained from the simulator. Also, show the waveform of the signals.

Design Code:



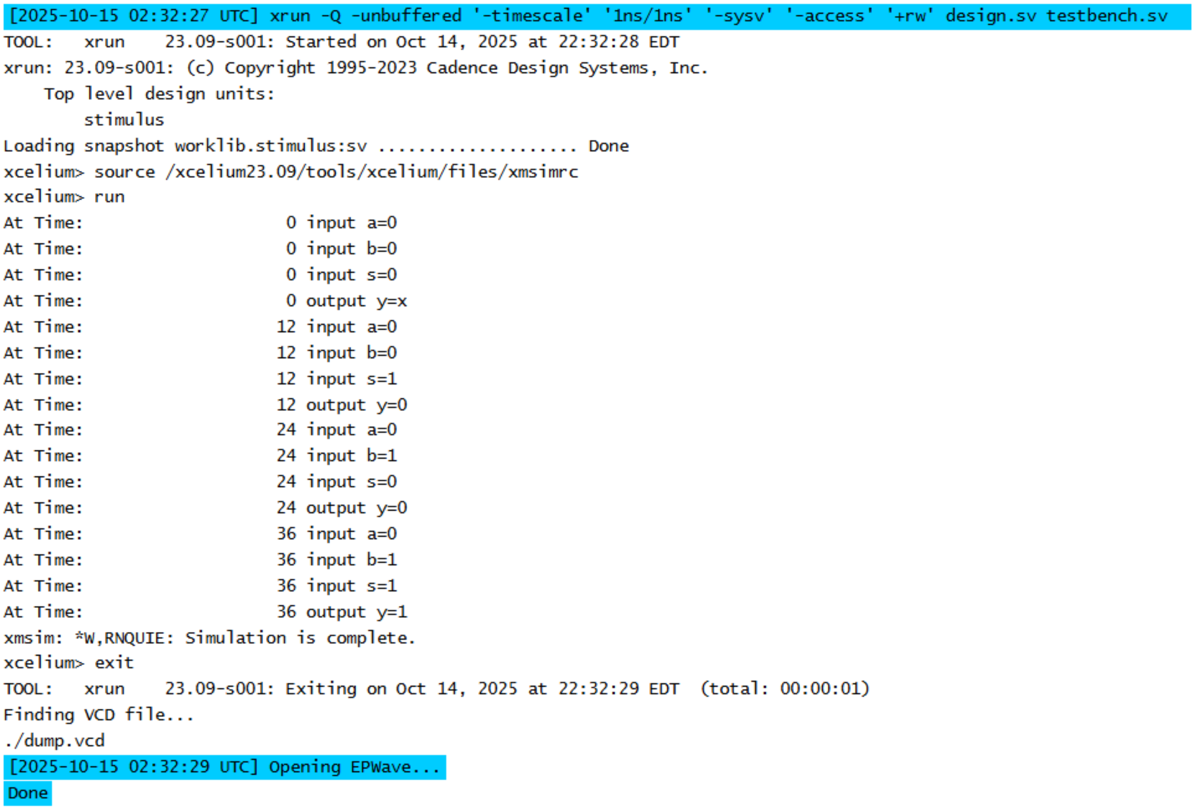
```
// your design code
module mux21 (input a,b,s, output y);
assign y=~s & a | s & b;
endmodule
```

**Test Bench Code:**



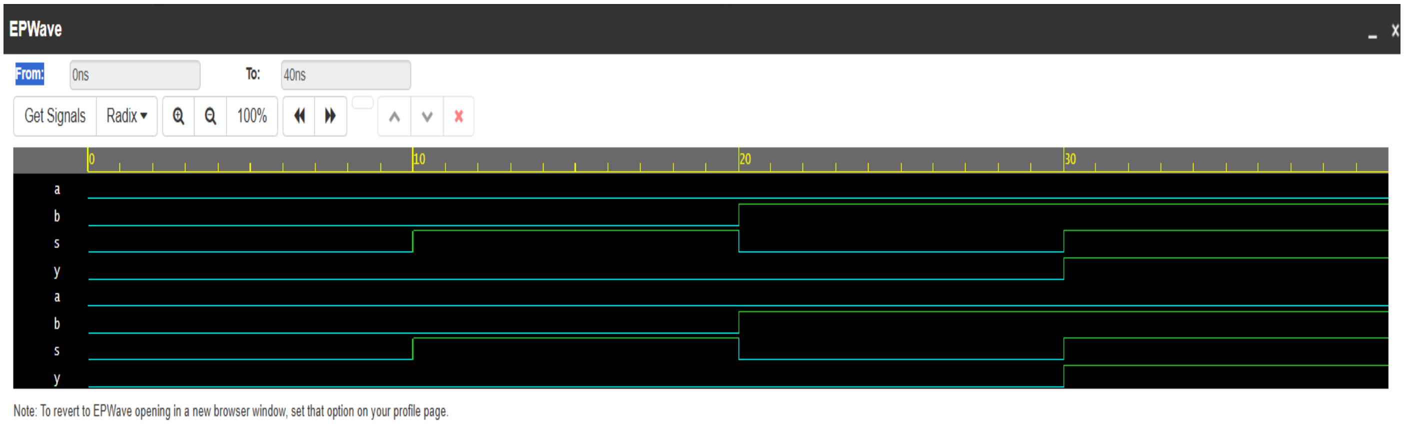
```
module stimulus( ); // No in, out
reg a,b,s; // inst. In dut
wire y;
// instantiate DUT
mux21 dut (
.a (a),
.b (b),
.s (s),
.y (y));
// apply inputs one at a time
initial begin
//sequential block
a = 0; b = 0; s = 0; #10; //apply inputs, wait 10ns
s = 1; #10;
b = 1; s = 0; #10;
s = 1; #10;
end
initial begin
$display("At Time: %d input a=%d",$time,a);
$display("At Time: %d input b=%d",$time,b);
$display("At Time: %d input s=%d",$time,s);
$display("At Time: %d output y=%d",$time,y);
#12;
$display("At Time: %d input a=%d",$time,a);
$display("At Time: %d input b=%d",$time,b);
$display("At Time: %d input s=%d",$time,s);
$display("At Time: %d output y=%d",$time,y);
#12;
$display("At Time: %d input a=%d",$time,a);
$display("At Time: %d input b=%d",$time,b);
$display("At Time: %d input s=%d",$time,s);
$display("At Time: %d output y=%d",$time,y);
#12;
$display("At Time: %d input a=%d",$time,a);
$display("At Time: %d input b=%d",$time,b);
$display("At Time: %d input s=%d",$time,s);
$display("At Time: %d output y=%d",$time,y);
end
// Waveform dumping
initial begin
$dumpfile("dump.vcd");
$dumpvars;
end
endmodule
```

## Output:



```
[2025-10-15 02:32:27 UTC] xrun -Q -unbuffered '-timescale' '1ns/1ns' '-sysv' '-access' '+rw' design.sv testbench.sv
TOOL:    xrun    23.09-s001: Started on Oct 14, 2025 at 22:32:28 EDT
xrun: 23.09-s001: (c) Copyright 1995-2023 Cadence Design Systems, Inc.
    Top level design units:
        stimulus
Loading snapshot worklib.stimulus:sv .................... Done
xcelium> source /xcelium23.09/tools/xcelium/files/xmsimrc
xcelium> run
At Time:                    0 input a=0
At Time:                    0 input b=0
At Time:                    0 input s=0
At Time:                    0 output y=x
At Time:                   12 input a=0
At Time:                   12 input b=0
At Time:                   12 input s=1
At Time:                   12 output y=0
At Time:                   24 input a=0
At Time:                   24 input b=1
At Time:                   24 input s=0
At Time:                   24 output y=0
At Time:                   36 input a=0
At Time:                   36 input b=1
At Time:                   36 input s=1
At Time:                   36 output y=1
xmsim: *W,RNQUIE: Simulation is complete.
xcelium> exit
TOOL:    xrun    23.09-s001: Exiting on Oct 14, 2025 at 22:32:29 EDT  (total: 00:00:01)
Finding VCD file...
./dump.vcd
[2025-10-15 02:32:29 UTC] Opening EPWave...
Done
```

Waveform:



From: 0ns To: 40ns

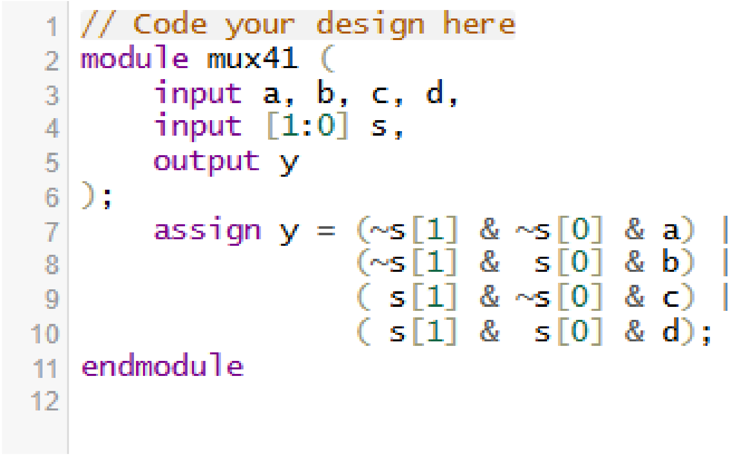
Note: To revert to EPWave opening in a new browser window, set that option on your profile page.

## Task 2:

Write the verilog code of a 4/1 mux. Test your code with a direct testbench. Show the code of the circuit, its testbench, and the output obtained from the simulator. Also, show the waveform of the signals.

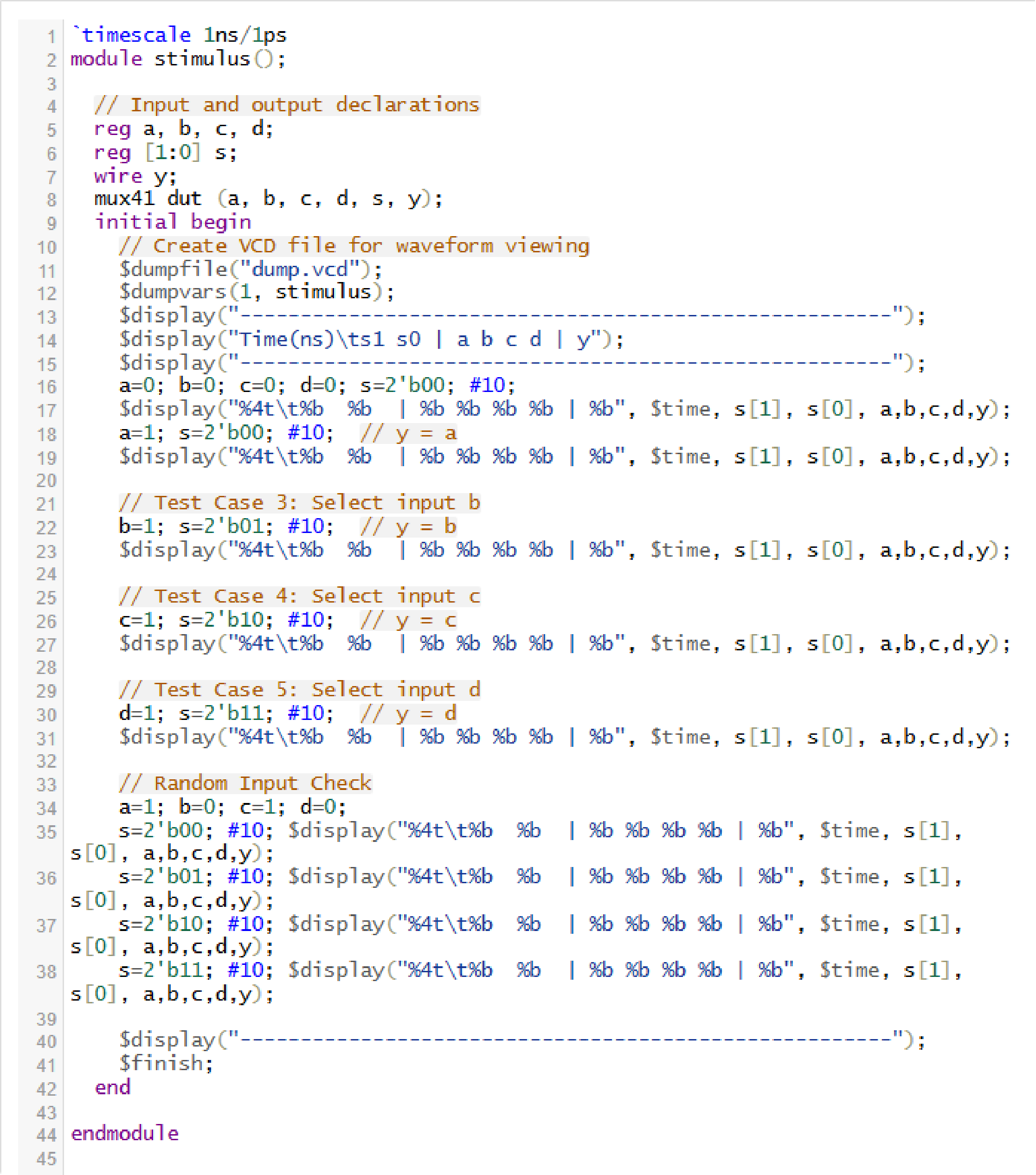
### 4:1 Mux Verilog Code

### Design Code:



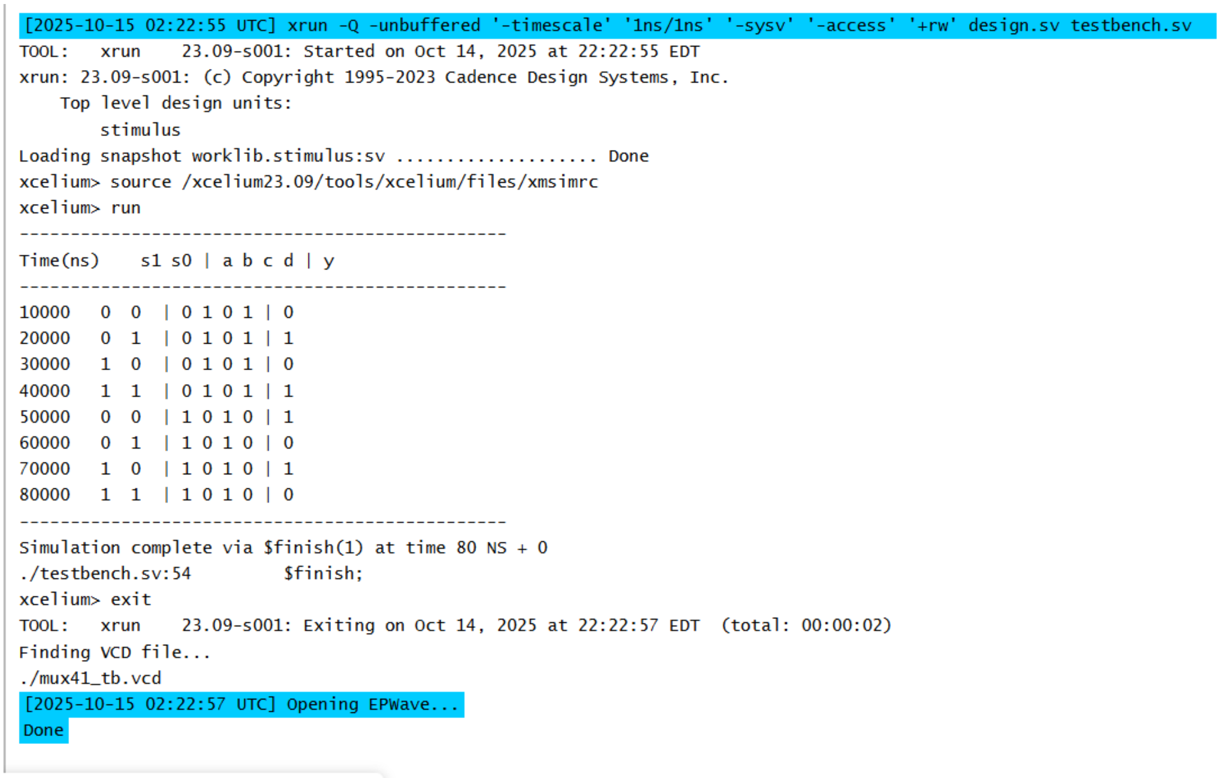
```verilog
// Code your design here
module mux41 (
    input a, b, c, d,
    input [1:0] s,
    output y
);
    assign y = (~s[1] & ~s[0] & a) |
               (~s[1] &  s[0] & b) |
               ( s[1] & ~s[0] & c) |
               ( s[1] &  s[0] & d);
endmodule

```

### Test Bench Code:



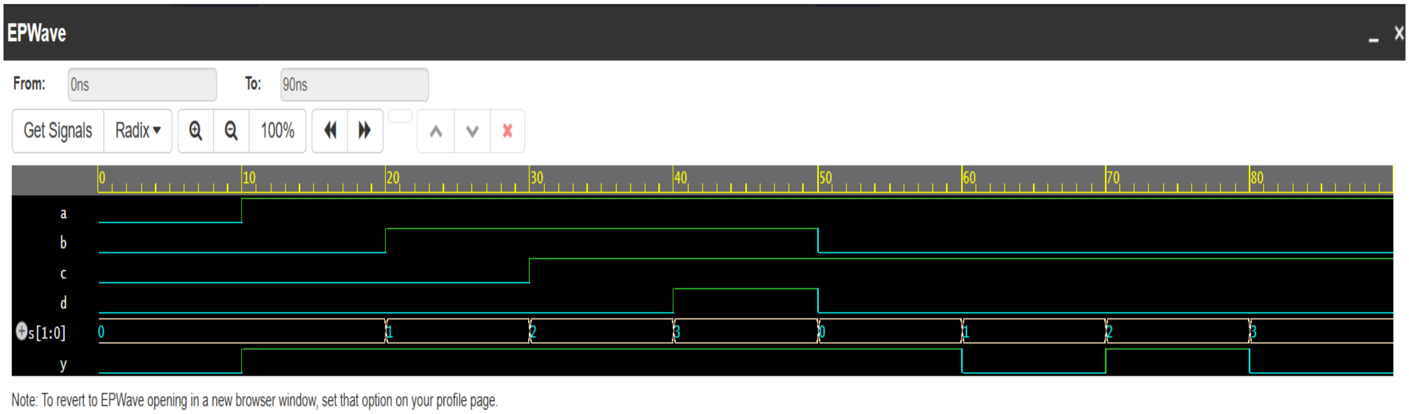
```verilog
`timescale 1ns/1ps
module stimulus();

  // Input and output declarations
  reg a, b, c, d;
  reg [1:0] s;
  wire y;
  mux41 dut (a, b, c, d, s, y);
  initial begin
    // Create VCD file for waveform viewing
    $dumpfile("dump.vcd");
    $dumpvars(1, stimulus);
    $display("-----------------------------------------------------");
    $display("Time(ns)\ts1 s0 | a b c d | y");
    $display("-----------------------------------------------------");
    a=0; b=0; c=0; d=0; s=2'b00; #10;
    $display("%4t\t%b  %b  | %b %b %b %b | %b", $time, s[1], s[0], a,b,c,d,y);
    a=1; s=2'b00; #10;  // y = a
    $display("%4t\t%b  %b  | %b %b %b %b | %b", $time, s[1], s[0], a,b,c,d,y);

    // Test Case 3: Select input b
    b=1; s=2'b01; #10;  // y = b
    $display("%4t\t%b  %b  | %b %b %b %b | %b", $time, s[1], s[0], a,b,c,d,y);

    // Test Case 4: Select input c
    c=1; s=2'b10; #10;  // y = c
    $display("%4t\t%b  %b  | %b %b %b %b | %b", $time, s[1], s[0], a,b,c,d,y);

    // Test Case 5: Select input d
    d=1; s=2'b11; #10;  // y = d
    $display("%4t\t%b  %b  | %b %b %b %b | %b", $time, s[1], s[0], a,b,c,d,y);

    // Random Input Check
    a=1; b=0; c=1; d=0;
    s=2'b00; #10; $display("%4t\t%b  %b  | %b %b %b %b | %b", $time, s[1], s[0], a,b,c,d,y);
    s=2'b01; #10; $display("%4t\t%b  %b  | %b %b %b %b | %b", $time, s[1], s[0], a,b,c,d,y);
    s=2'b10; #10; $display("%4t\t%b  %b  | %b %b %b %b | %b", $time, s[1], s[0], a,b,c,d,y);
    s=2'b11; #10; $display("%4t\t%b  %b  | %b %b %b %b | %b", $time, s[1], s[0], a,b,c,d,y);

    $display("-----------------------------------------------------");
    $finish;
  end

endmodule
```

## Output:

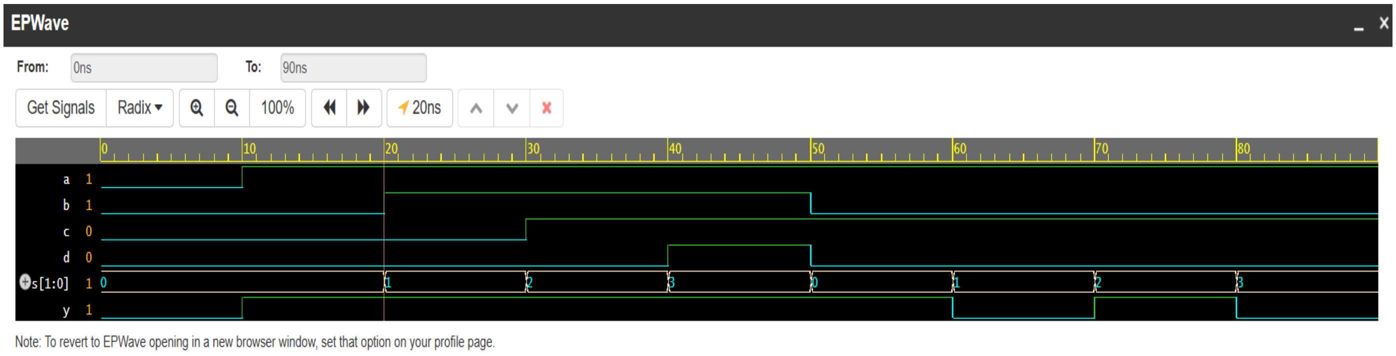


```
[2025-10-15 02:22:55 UTC] xrun -Q -unbuffered '-timescale' '1ns/1ns' '-sysv' '-access' '+rw' design.sv testbench.sv
TOOL:	xrun	23.09-s001: Started on Oct 14, 2025 at 22:22:55 EDT
xrun: 23.09-s001: (c) Copyright 1995-2023 Cadence Design Systems, Inc.
    Top level design units:
        stimulus
Loading snapshot worklib.stimulus:sv .................... Done
xcelium> source /xcelium23.09/tools/xcelium/files/xmsimrc
xcelium> run
------------------------------------------------
Time(ns)    s1 s0 | a b c d | y
------------------------------------------------
10000   0  0  | 0 1 0 1 | 0
20000   0  1  | 0 1 0 1 | 1
30000   1  0  | 0 1 0 1 | 0
40000   1  1  | 0 1 0 1 | 1
50000   0  0  | 1 0 1 0 | 1
60000   0  1  | 1 0 1 0 | 0
70000   1  0  | 1 0 1 0 | 1
80000   1  1  | 1 0 1 0 | 0
------------------------------------------------
Simulation complete via $finish(1) at time 80 NS + 0
./testbench.sv:54         $finish;
xcelium> exit
TOOL:	xrun	23.09-s001: Exiting on Oct 14, 2025 at 22:22:57 EDT  (total: 00:00:02)
Finding VCD file...
./mux41_tb.vcd
[2025-10-15 02:22:57 UTC] Opening EPWave...
Done
```

## Waveform:



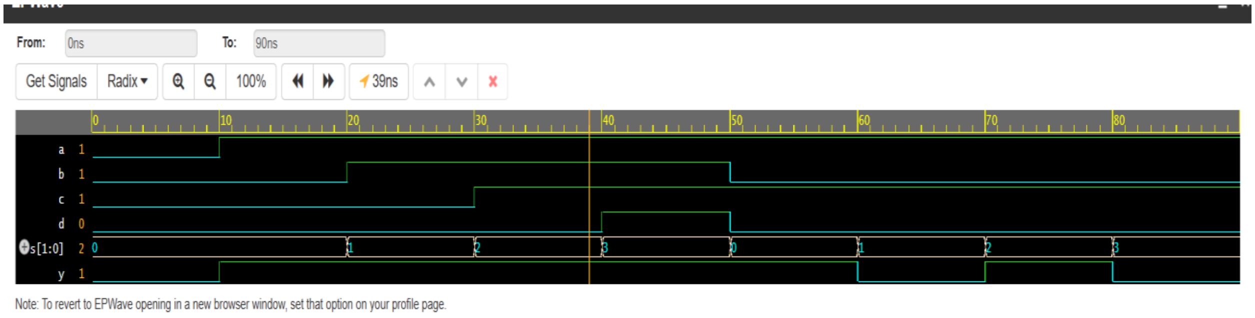
Note: To revert to EPWave opening in a new browser window, set that option on your profile page.


EPWave

From: 0ns To: 90ns

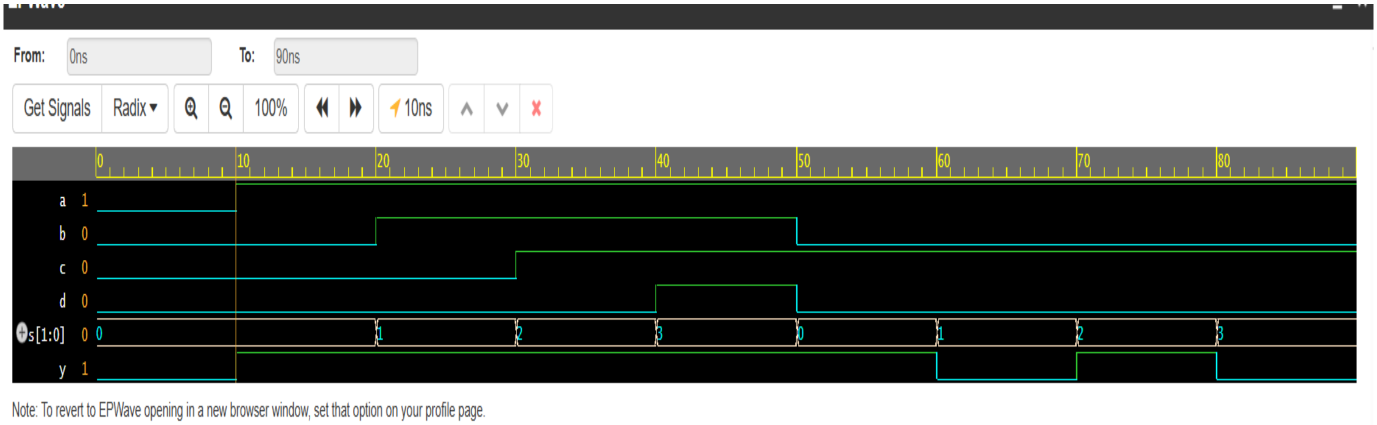
```
a      1
b      1
c      0
d      0
s[1:0] 1
y      1
```

Note: To revert to EPWave opening in a new browser window, set that option on your profile page.


From: 0ns To: 90ns

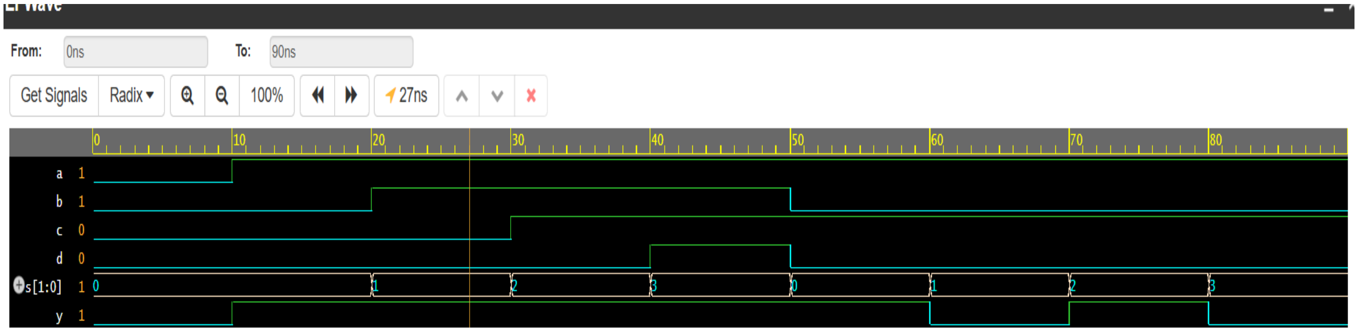
```
a      1
b      1
c      1
d      0
s[1:0] 2
y      1
```

Note: To revert to EPWave opening in a new browser window, set that option on your profile page.


From: 0ns To: 90ns

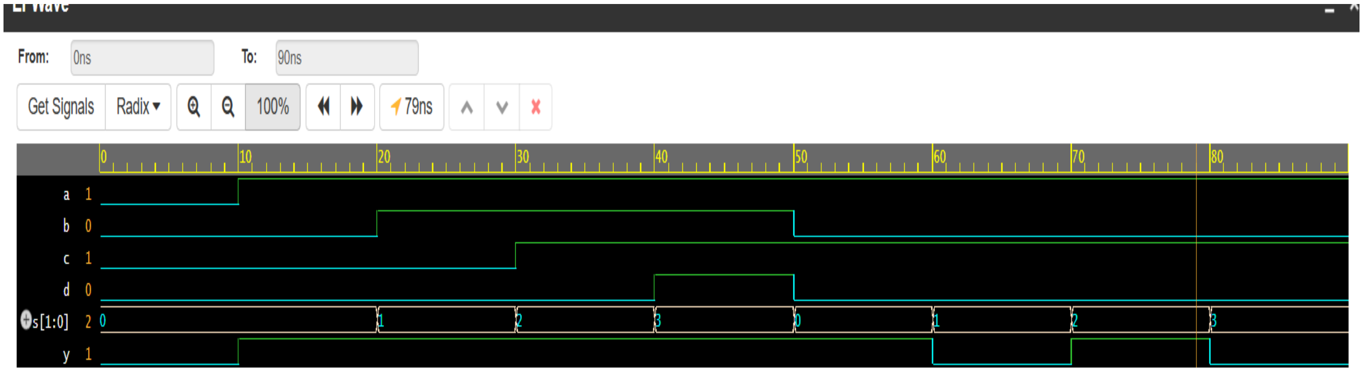
```
a      1
b      0
c      0
d      0
s[1:0] 0
y      1
```

Note: To revert to EPWave opening in a new browser window, set that option on your profile page.



From: 0ns To: 90ns

Note: To revert to EPWave opening in a new browser window, set that option on your profile page.



From: 0ns To: 90ns

Note: To revert to EPWave opening in a new browser window, set that option on your profile page.