Department Of Computer Science and Engineering

Course Title: VLSI Lab

Course Code: CSE 458

Title: Design and Verification of 2-input NAND Gate.

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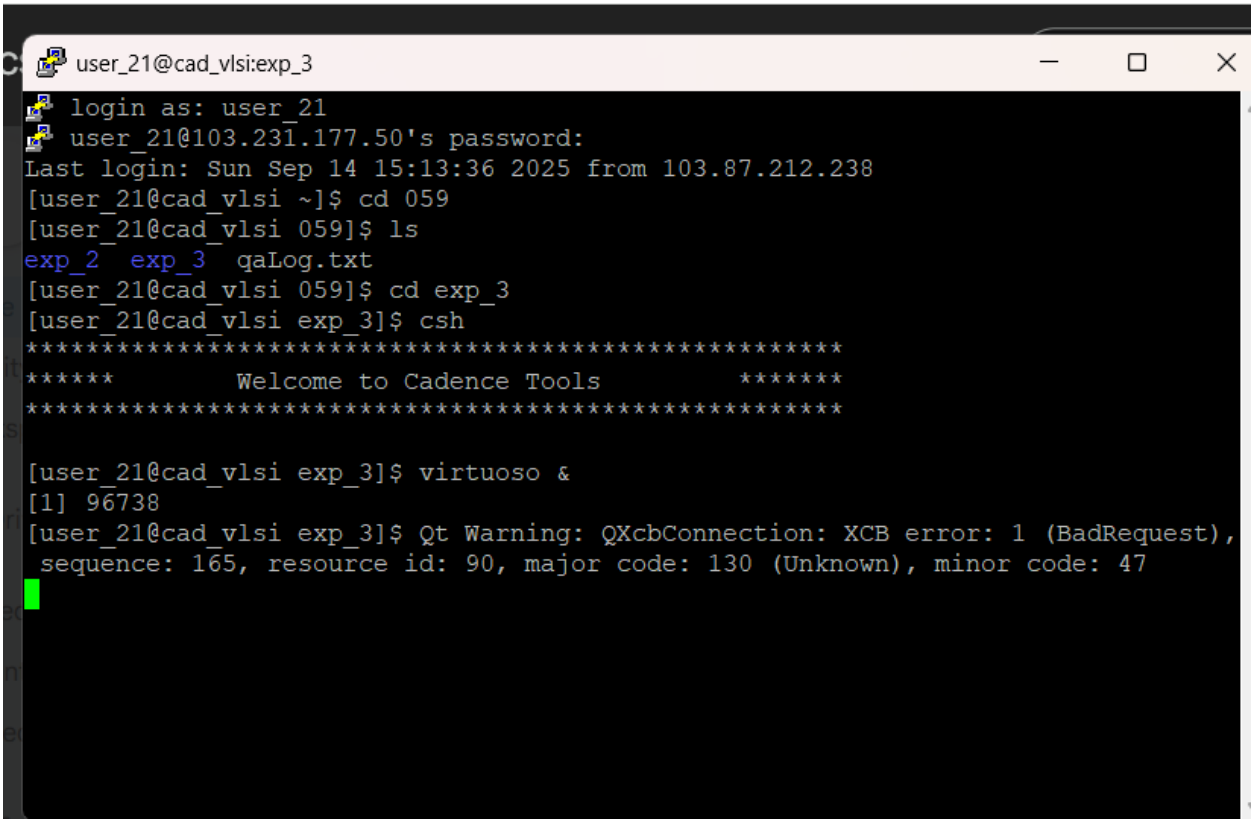

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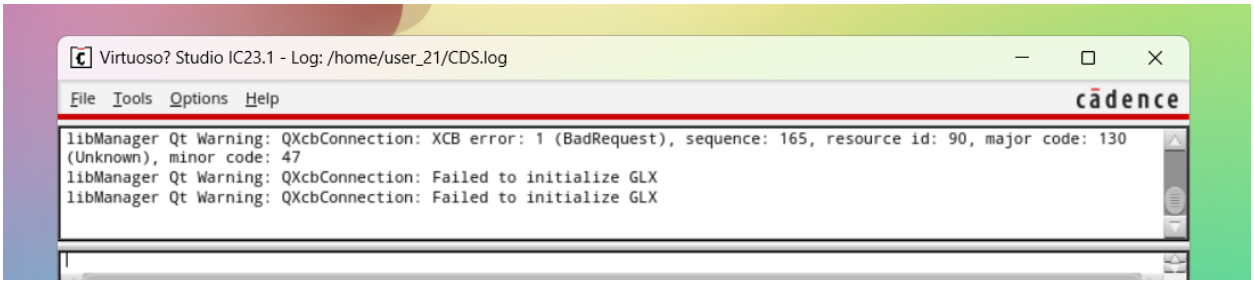
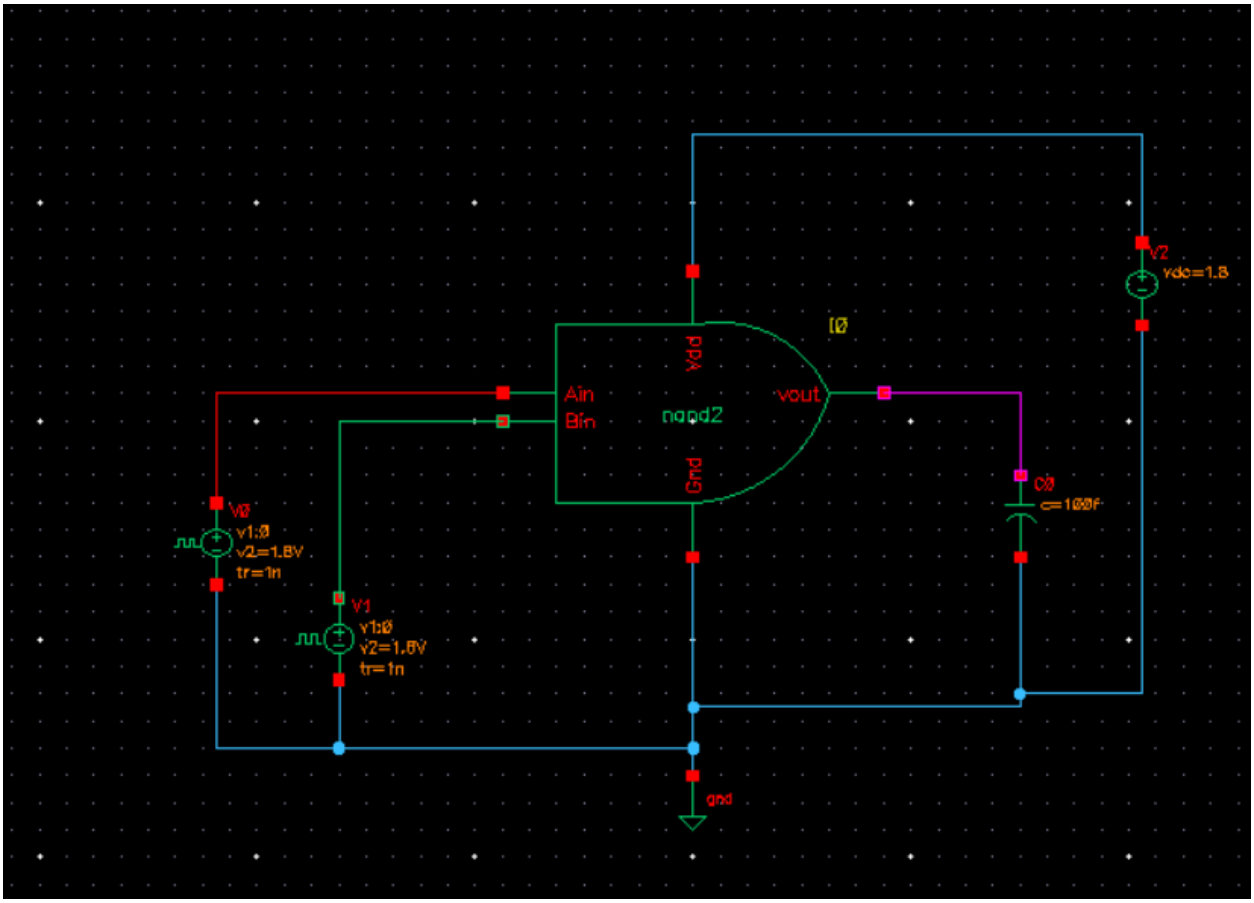


Circuit Diagram:



Circuit Description

1. **Logic Gate:**
    - The block in the middle labeled “nand2” is a 2-input NAND gate.
    - Inputs: Ain and Bin.
    - Output: vout.
2. **Power Supply:**
    - V2 = 1.8 V (DC) is providing VDD (the supply voltage) to the NAND gate.
    - Gnd is the reference ground**.**
3. **Input Sources:**
    - **V1: A pulse voltage source connected to input Bin.**

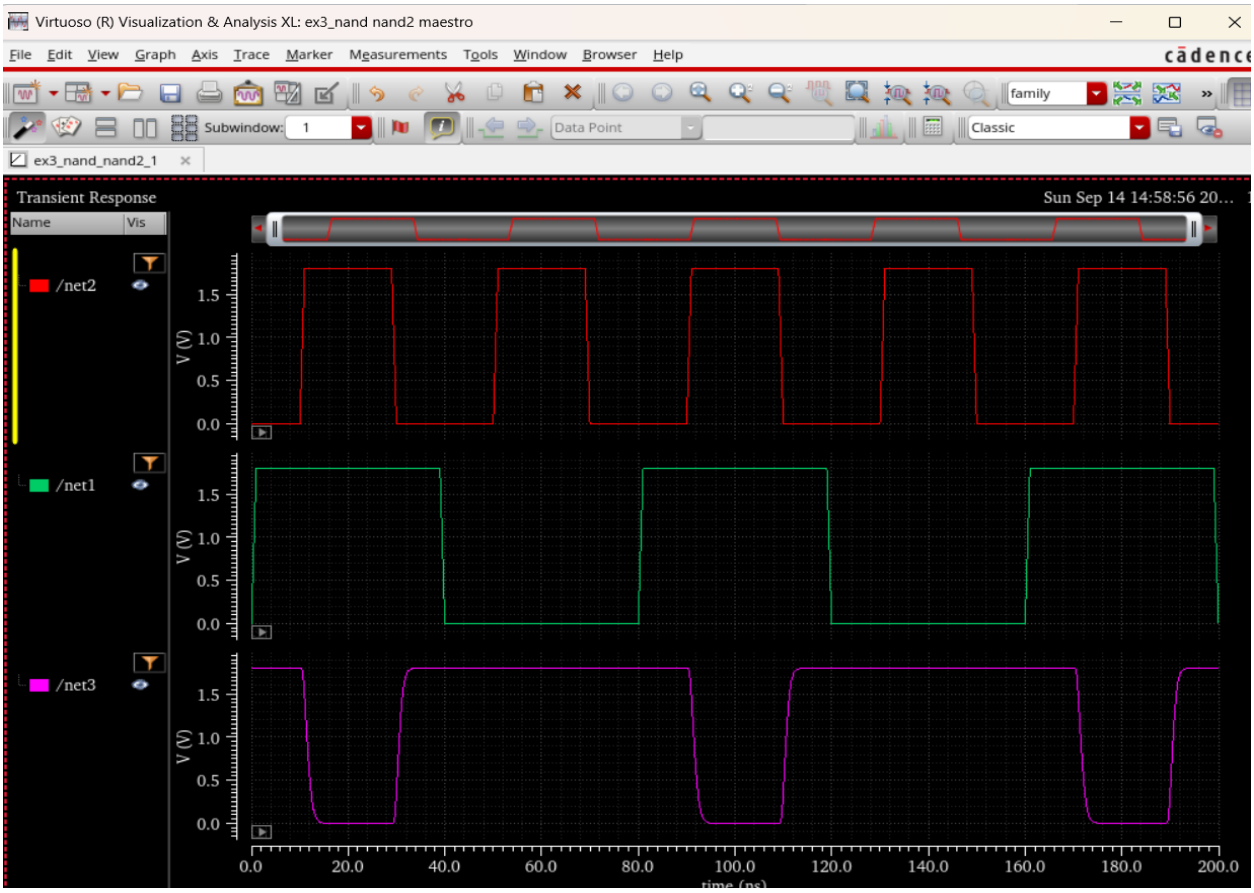
- Alternates between 0 V and 1.8 V.
- Transition time = 1 ns.

- **V3: Another pulse voltage source connected to input Ain.**
  - Also alternates between 0 V and 1.8 V.
  - Transition time = 1 ns.

4. **Output Load:**
   - A capacitor C0 = 100 fF is connected at the NAND output node (vout).
   - This represents the load capacitance .

Output

Trans



Key Observations

The transient waveforms display three signals:

Input Voltages (A and B):

- Two digital pulse sources (shown in green and red) drive the inputs.
- Each alternates between 0 V and 1.8 V with a configured rise time of about 1 ns, ensuring fast logic-level switching**.**

Output Voltage (Vout):

- The purple trace represents the output, which varies between 0 V and 1.8 V.
- Unlike the sharp transitions at the inputs, the output edges appear smoother and slightly delayed.
- This effect arises from the output capacitance (C = 100 fF) and the finite drive strength of the MOS transistors, introducing an RC charging/discharging characteristic**.**

Logic Behavior:
The circuit functions as a two-input NAND gate. The output matches the expected NAND truth table, remaining HIGH unless both inputs are HIGH simultaneously. Short pulses and rounded edges are observed due to the capacitive loading.

Purpose of Analysis:
The transient analysis was performed to confirm logic functionality, edge characteristics, and dynamic timing parameters (rise and fall times) under capacitive load conditions.

Measured Timing:

- **Rise time (t_r):**
  33.78104 ns−29.245094 ns=4.535946 ns
- **Fall time (t_f):**
  94.04953 ns−90.50824 ns=3.54129ns

Conclusion

The simulation verifies correct operation of the CMOS NAND gate. The output switches cleanly between 0 V and 1.8 V according to the NAND truth table, confirming logical accuracy. The presence of the load capacitor slows down transitions compared to the inputs, producing rounded rising and falling edges that reflect realistic circuit behavior. Thus, the analysis demonstrates both the functional correctness and the dynamic switching response of the design.