Department Of Computer Science and Engineering

Course Title: VLSI Lab

Course Code: CSE 458

Lab Report: 05

Experiment Name: Inverter Layout Design

Submitted To:

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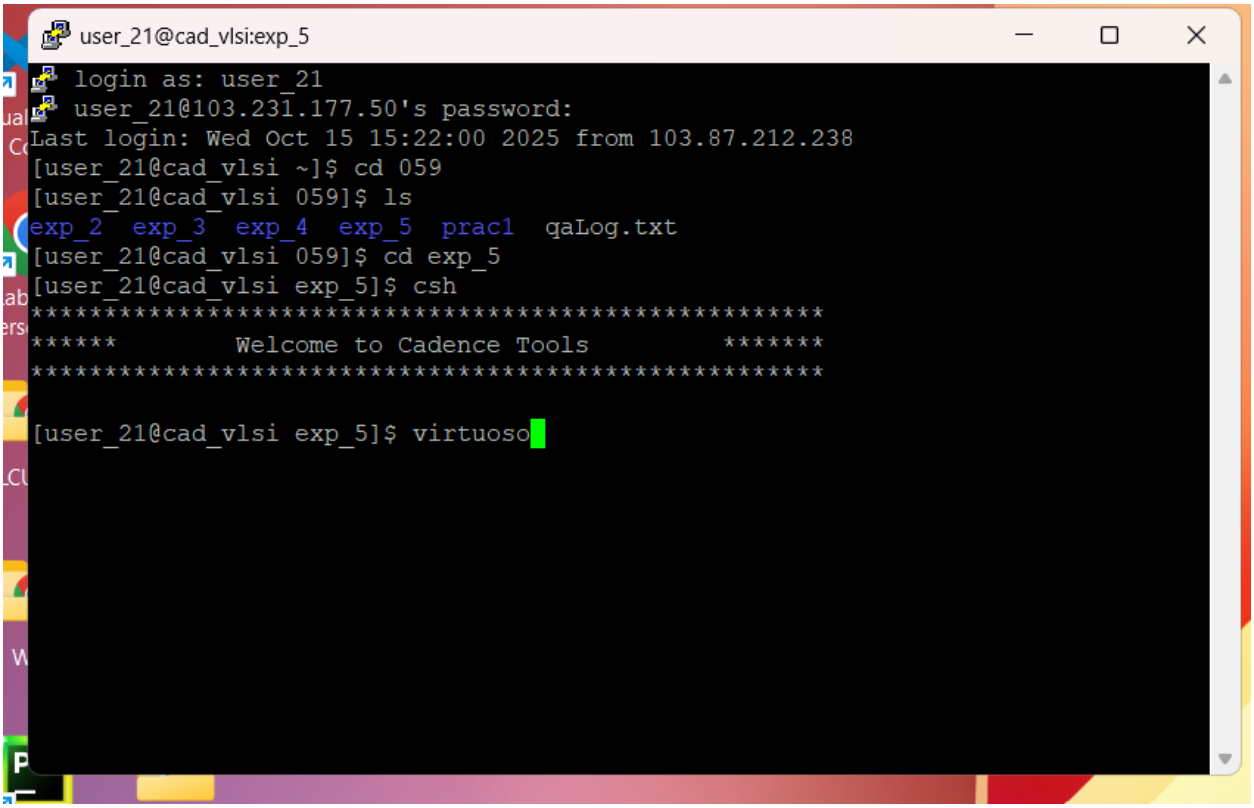
Experiment Date:06.09.2025

Submission Date: 15.10.2025

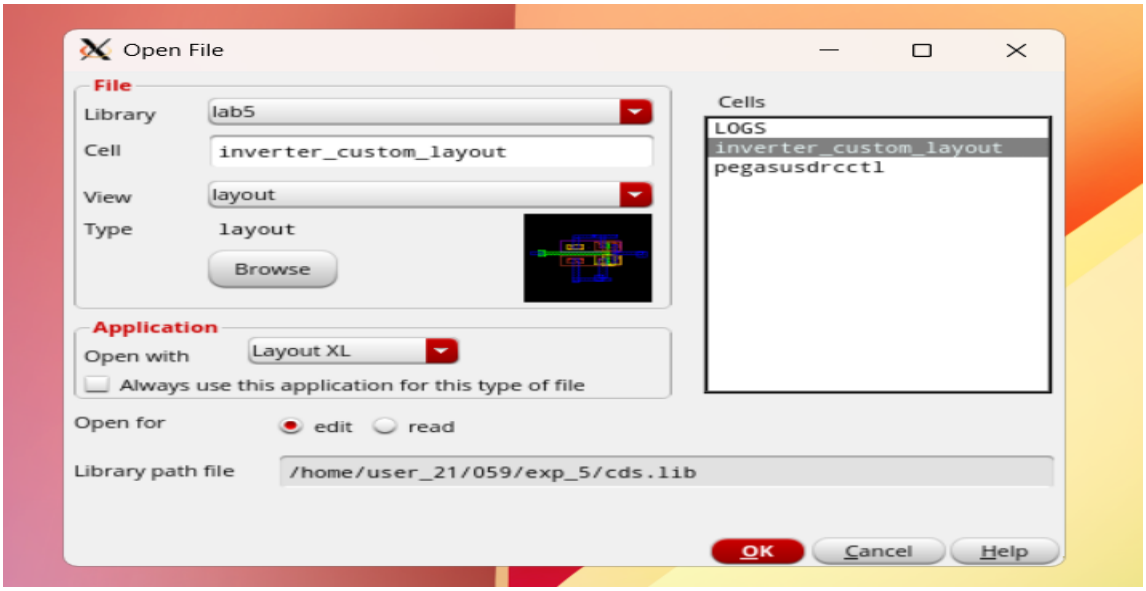
Objective:

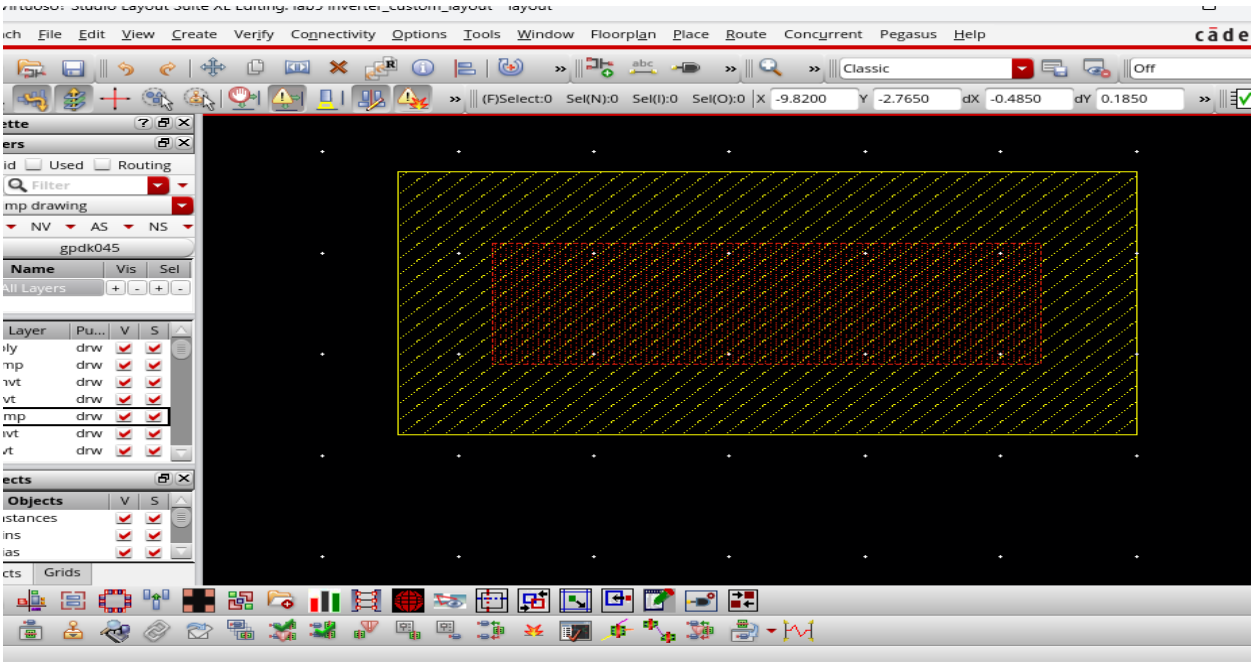
The objective of this experiment is to design the layout of a CMOS inverter using the Cadence Virtuoso Layout Editor as part of the VLSI design process. The layout is created by accurately placing various layers such as oxide, diffusion (N-type and P-type implants), polysilicon, metal, and contact layers in compliance with CMOS fabrication rules. Furthermore, a Design Rule Check (DRC) is performed using the Pegasus verification tool to ensure that the layout adheres to all design constraints and fabrication requirements. This process verifies the correctness and manufacturability of the inverter layout before proceeding to the next stages of the VLSI design flow.

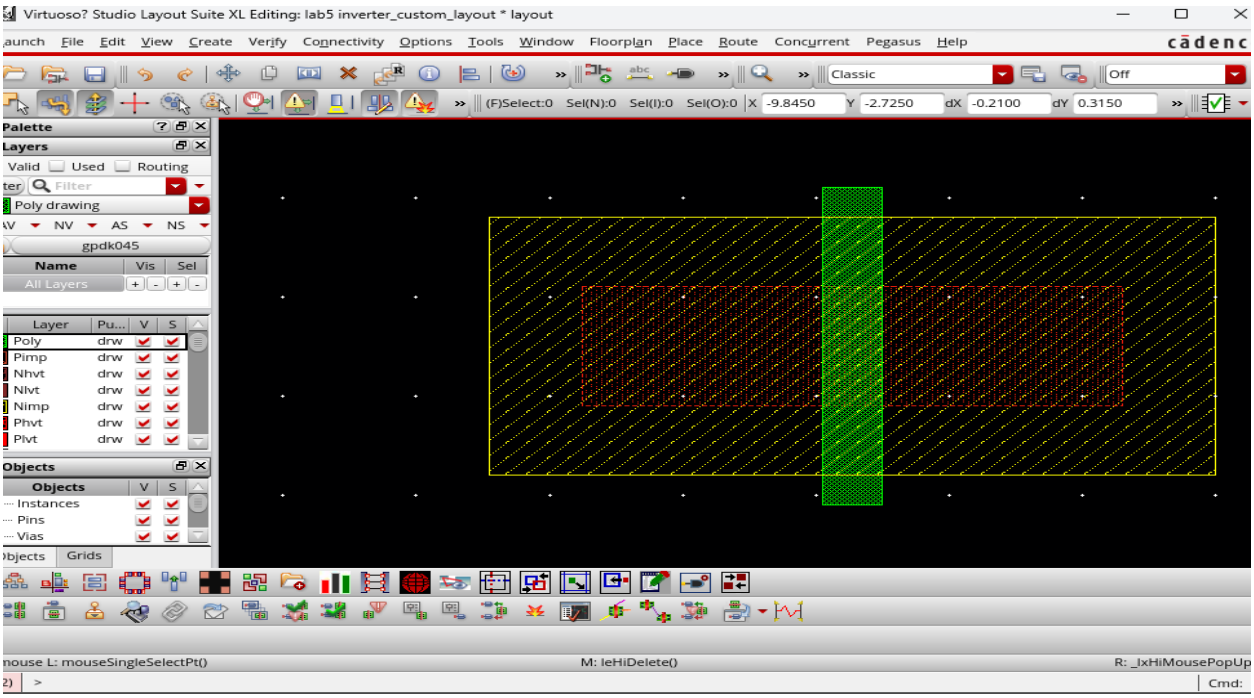
Steps Inverter Layout Design:

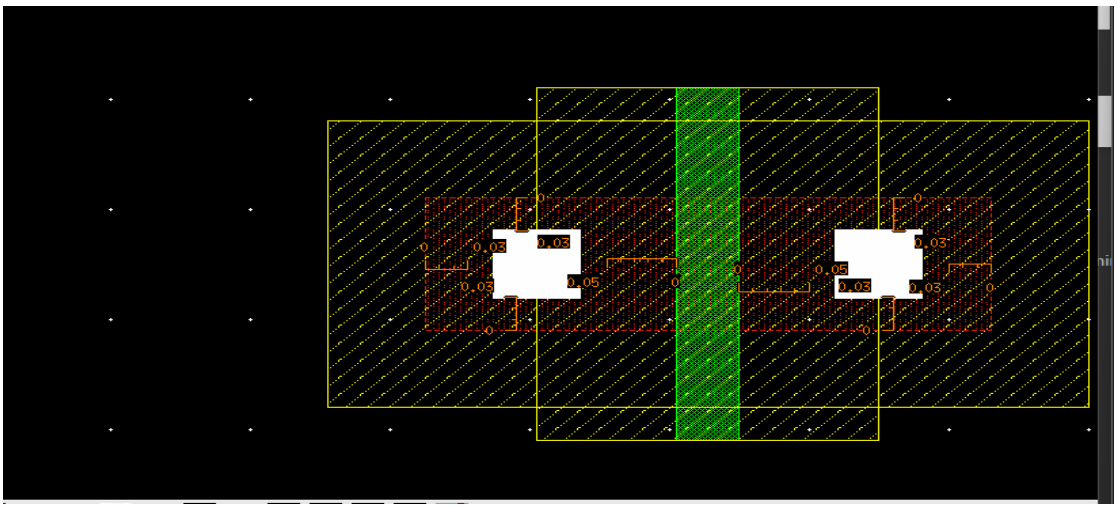


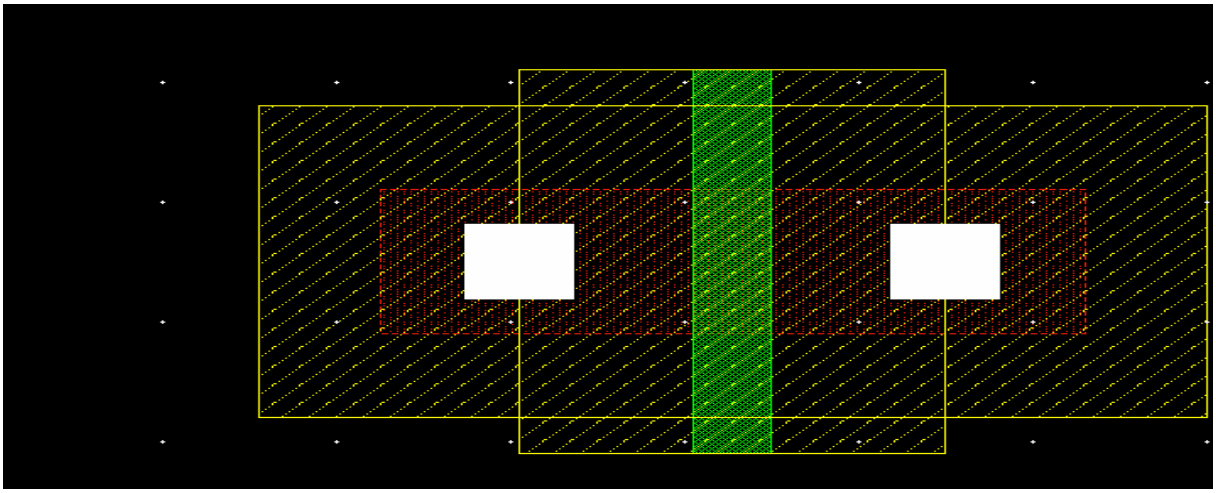
Cell View Setup:

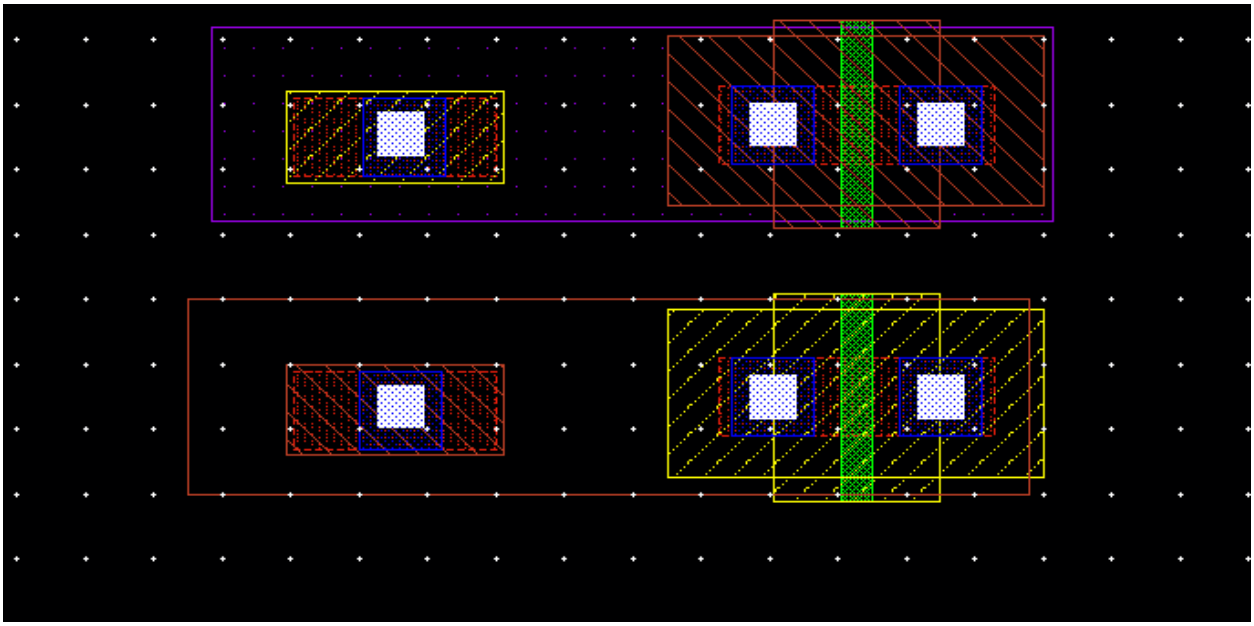


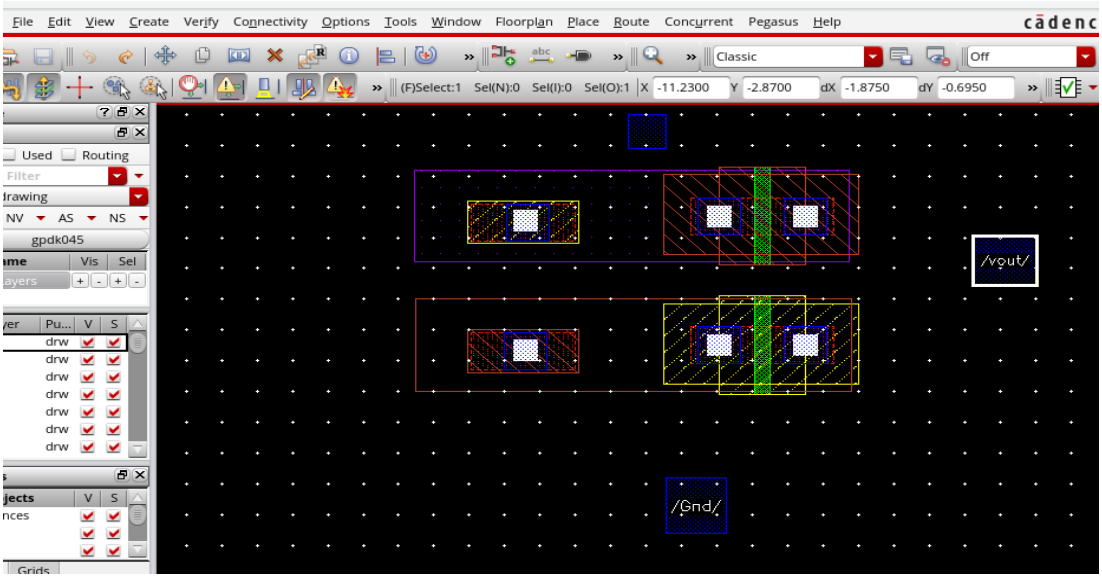


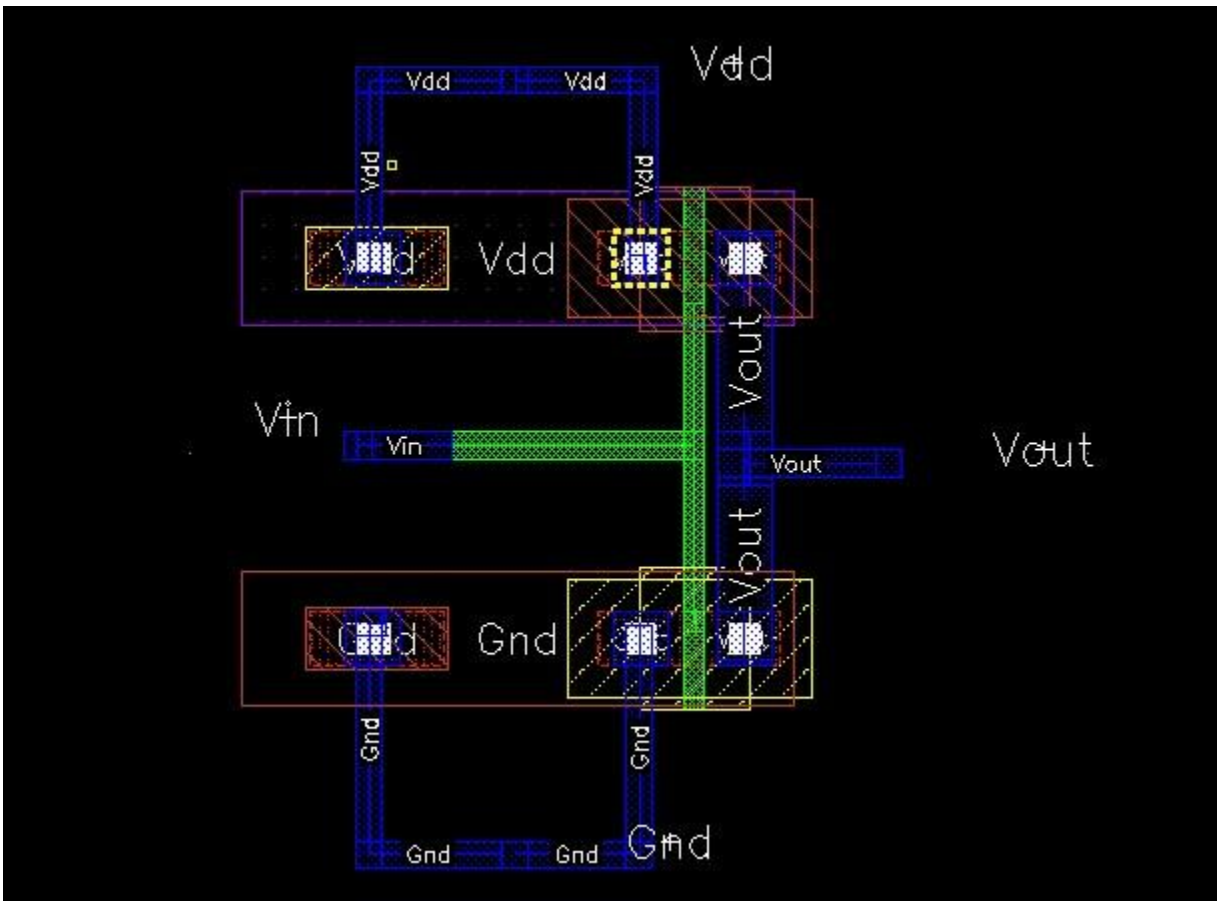

Virtuoso® Studio Layout Suite XL Editing: lab5 inverter_custom_layout * layout
File Edit View Create Verify Connectivity Options Tools Window Floorplan Place Route Concurrent Pegasus Help
Palette
Layers
Valid Used Routing
Poly drawing
gpdk045
Name Vis Sel
All Layers
Layer Pu... V S
Poly drw
Pimp drw
Nhvt drw
Nlvt drw
Nimp drw
Phvt drw
Plvt drw
Objects
Objects V S
Instances
Pins
Vias
Grids
Classic
Off
(F)Select:0 Sel(N):0 Sel(I):0 Sel(O):0 X -9.8450 Y -2.7250 dX -0.2100 dY 0.3150
M: leHiDelete()
Cmd:








File Edit View Create Verify Connectivity Options Tools Window Floorplan Place Route Concurrent Pegasus Help
cadenc
Classic
Off
(F)Select:1 Sel(N):0 Sel(I):0 Sel(O):1 X -11.2300 Y -2.8700 dX -1.8750 dY -0.6950
Used Routing
Filter
drawing
NV AS NS
gpdk045
/vout/
/Gnd/


Vdd
Vdd
Vdd
Vdd
Vdd
Vdd
Vin
Vin
Vout
Vout
Vout
Vout
Gnd
Gnd
Gnd
Gnd
Gnd
Gnd

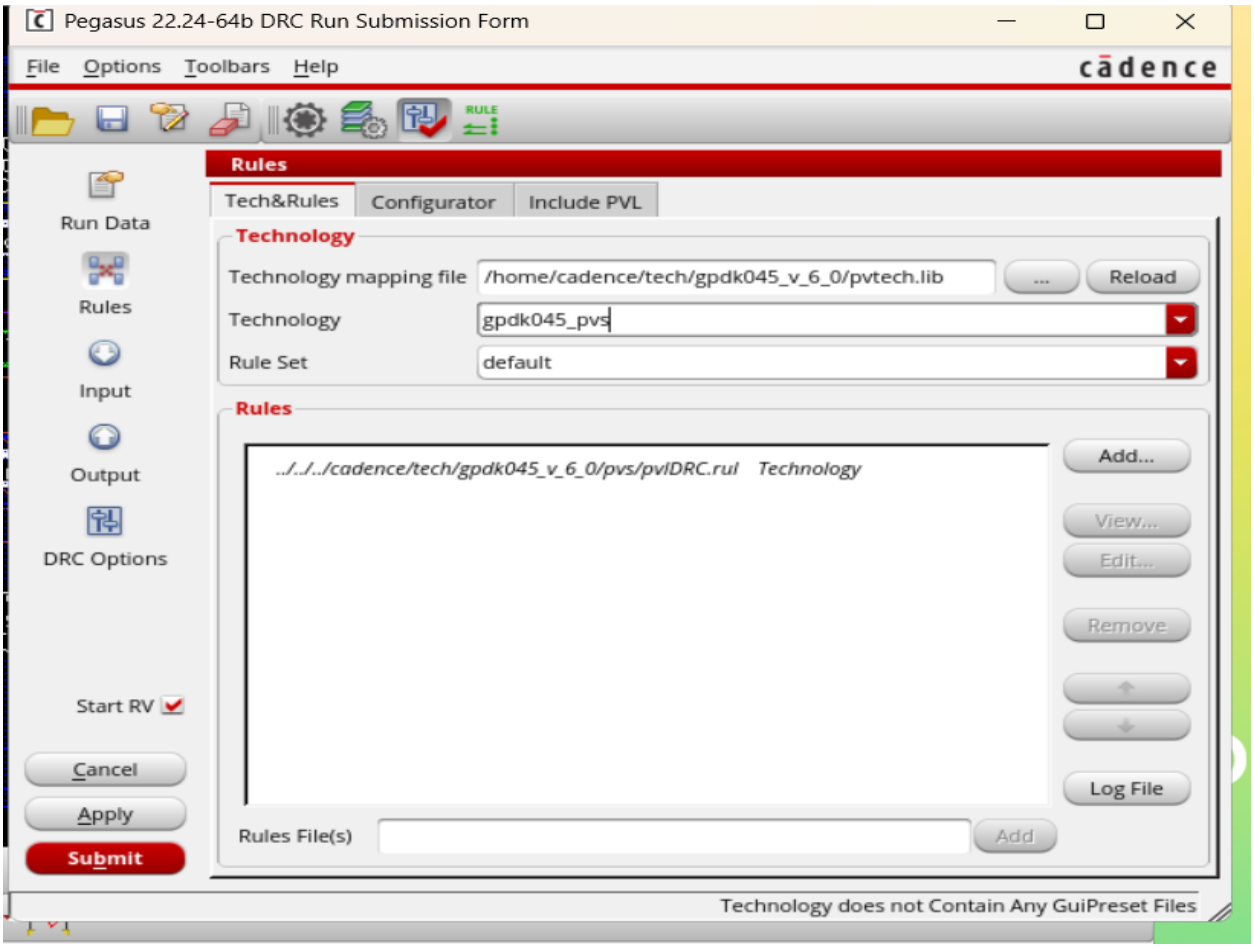
The necessary value we used:

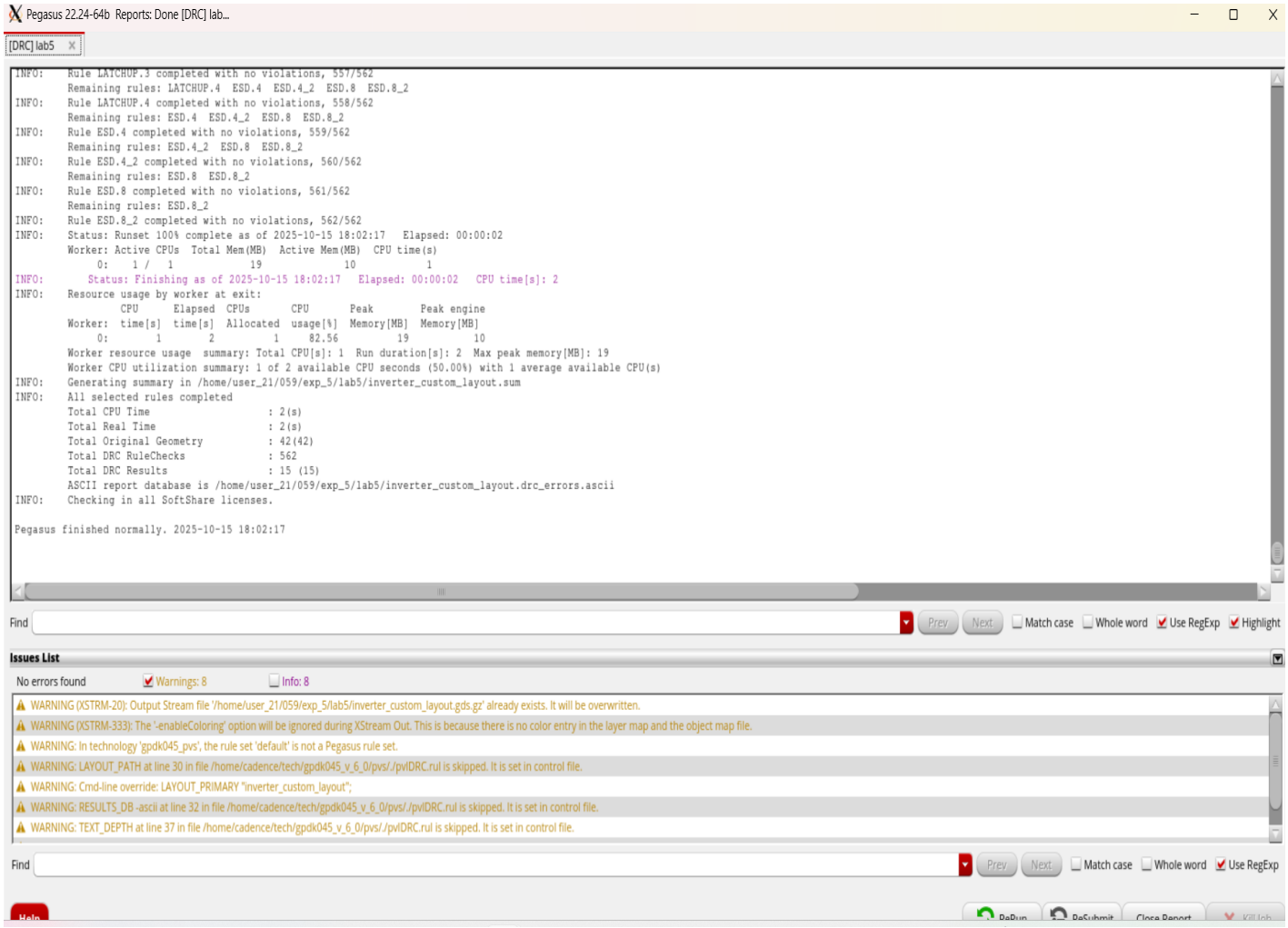
	Region name	Length (um)	Width (um)	Remarks	
2	Oxide	0.405	0.12		
3	Nimp	0.545	.26	Nimp overlapping oxide (Min) : 0.07 um	
4	Poly	.045	.32	Poly extending to oxide (Min) : 0.1 um	Poly width Min: 0.045 um (Fixed MOS gate length)
5	Nimp around gate	0.245	.32		
6	Cont	.06	.06	Contact to oxide spacing (Min) : 0.03 um	Contact to poly spacing (Min) : 0.05 um
7	Metal 1	0.12	0.12	Min Metal 1 to Contact enclosure: 0.03 um	Minimum Metal 1 width : 0.06 um
8	Body tap a.Oxide b. Pimp	 a. .295 b. .315	 a. .12 b. .14		
9	PWdummy	1.23 5	0.3 8		

17. In the LSW window select the NWELL layer and draw the NWELL rectangle.

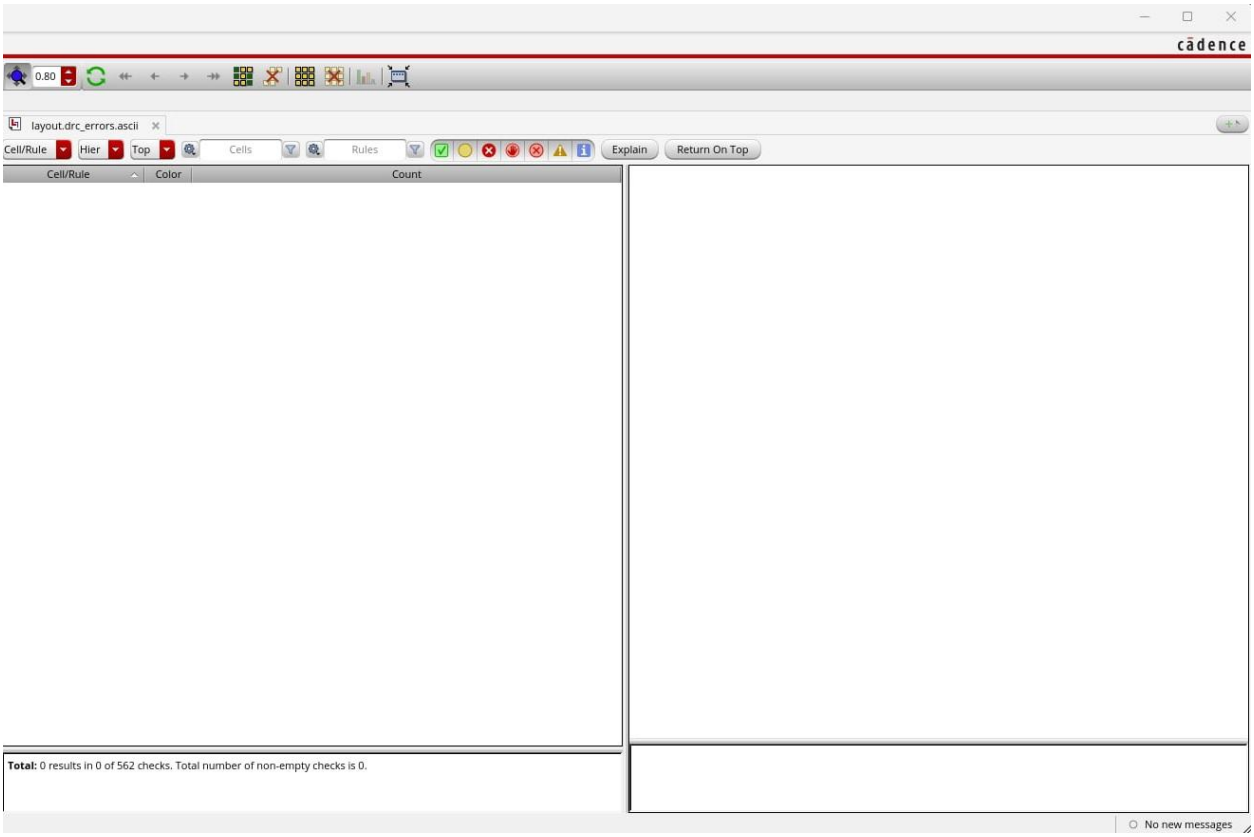
	Region name	Length (um)	Width (um)	Remarks	
11	Pimp	0.545	.26	Pimp overlapping oxide (Min) : 0.07 um	
13	Pimp around gate	0.245	.32		
16	Body tap a.Oxide b. Nimp	 a. .295 b. .315	 a. .12 b. .14		
17	Nwell	1.235	0.3 8	Min Nwell width : 0.3 um	

DRC Output Check Steps:




Pegasus 22.24-64b Reports: Done [DRC] lab...
[DRC] lab5
INFO: Rule LATCHUP.3 completed with no violations, 557/562
Remaining rules: LATCHUP.4 ESD.4 ESD.4_2 ESD.8 ESD.8_2
INFO: Rule LATCHUP.4 completed with no violations, 558/562
Remaining rules: ESD.4 ESD.4_2 ESD.8 ESD.8_2
INFO: Rule ESD.4 completed with no violations, 559/562
Remaining rules: ESD.4_2 ESD.8 ESD.8_2
INFO: Rule ESD.4_2 completed with no violations, 560/562
Remaining rules: ESD.8 ESD.8_2
INFO: Rule ESD.8 completed with no violations, 561/562
Remaining rules: ESD.8_2
INFO: Rule ESD.8_2 completed with no violations, 562/562
INFO: Status: Runset 100% complete as of 2025-10-15 18:02:17 Elapsed: 00:00:02
Worker: Active CPUs Total Mem(MB) Active Mem(MB) CPU time(s)
0: 1 / 1 19 10 1
INFO: Status: Finishing as of 2025-10-15 18:02:17 Elapsed: 00:00:02 CPU time[s]: 2
INFO: Resource usage by worker at exit:
Worker: CPU time[s] Elapsed time[s] CPUs Allocated CPU usage[%] Peak Memory[MB] Peak engine Memory[MB]
0: 1 2 1 82.56 19 10
Worker resource usage summary: Total CPU[s]: 1 Run duration[s]: 2 Max peak memory[MB]: 19
Worker CPU utilization summary: 1 of 2 available CPU seconds (50.00%) with 1 average available CPU(s)
INFO: Generating summary in /home/user_21/059/exp_5/lab5/inverter_custom_layout.sum
INFO: All selected rules completed
Total CPU Time : 2(s)
Total Real Time : 2(s)
Total Original Geometry : 42(42)
Total DRC RuleChecks : 562
Total DRC Results : 15 (15)
ASCII report database is /home/user_21/059/exp_5/lab5/inverter_custom_layout.drc_errors.ascii
INFO: Checking in all SoftShare licenses.
Pegasus finished normally. 2025-10-15 18:02:17
Find
Prev
Next
Match case
Whole word
Use RegExp
Highlight
Issues List
No errors found
Warnings: 8
Info: 8
WARNING (XSTRM-20): Output Stream file '/home/user_21/059/exp_5/lab5/inverter_custom_layout.gds.gz' already exists. It will be overwritten.
WARNING (XSTRM-333): The '-enableColoring' option will be ignored during XStream Out. This is because there is no color entry in the layer map and the object map file.
WARNING: In technology 'gpdk045_pvs', the rule set 'default' is not a Pegasus rule set.
WARNING: LAYOUT_PATH at line 30 in file /home/cadence/tech/gpdk045_v_6_0/pvs/./pvlDRC.rul is skipped. It is set in control file.
WARNING: Cmd-line override: LAYOUT_PRIMARY "inverter_custom_layout";
WARNING: RESULTS_DB -ascii at line 32 in file /home/cadence/tech/gpdk045_v_6_0/pvs/./pvlDRC.rul is skipped. It is set in control file.
WARNING: TEXT_DEPTH at line 37 in file /home/cadence/tech/gpdk045_v_6_0/pvs/./pvlDRC.rul is skipped. It is set in control file.
Find
Prev
Next
Match case
Whole word
Use RegExp
Help
ReRun
ReSubmit
Close Report
Kill Job

The Output:



Result and Discussion

The layout of a CMOS inverter was designed in Cadence Virtuoso Layout Editor using various layers such as oxide, Nimp, Pimp, polysilicon, metal, and contact layers. After completing the layout, a Design Rule Check (DRC) was performed using Pegasus, and the design passed without any errors.
The final three screenshots show the completed inverter layout and the successful DRC verification results.