Department Of Computer Science and Engineering

Course Title: VLSI Lab

Course Code: CSE 458

Lab Report: 04

Experiment Name: Characterization of a MOSEFT

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Objective:

1) To construct the schematic of an NMOS transistor using the Cadence Virtuoso tool.

2) To simulate the device and evaluate its electrical characteristics under different biasing conditions.

3) To perform DC sweeps in order to generate:

i) Ids vs Vds plots for a range of gate voltages (Vgs).

ii)Ids vs Vgs plots for varying drain voltages (Vds).

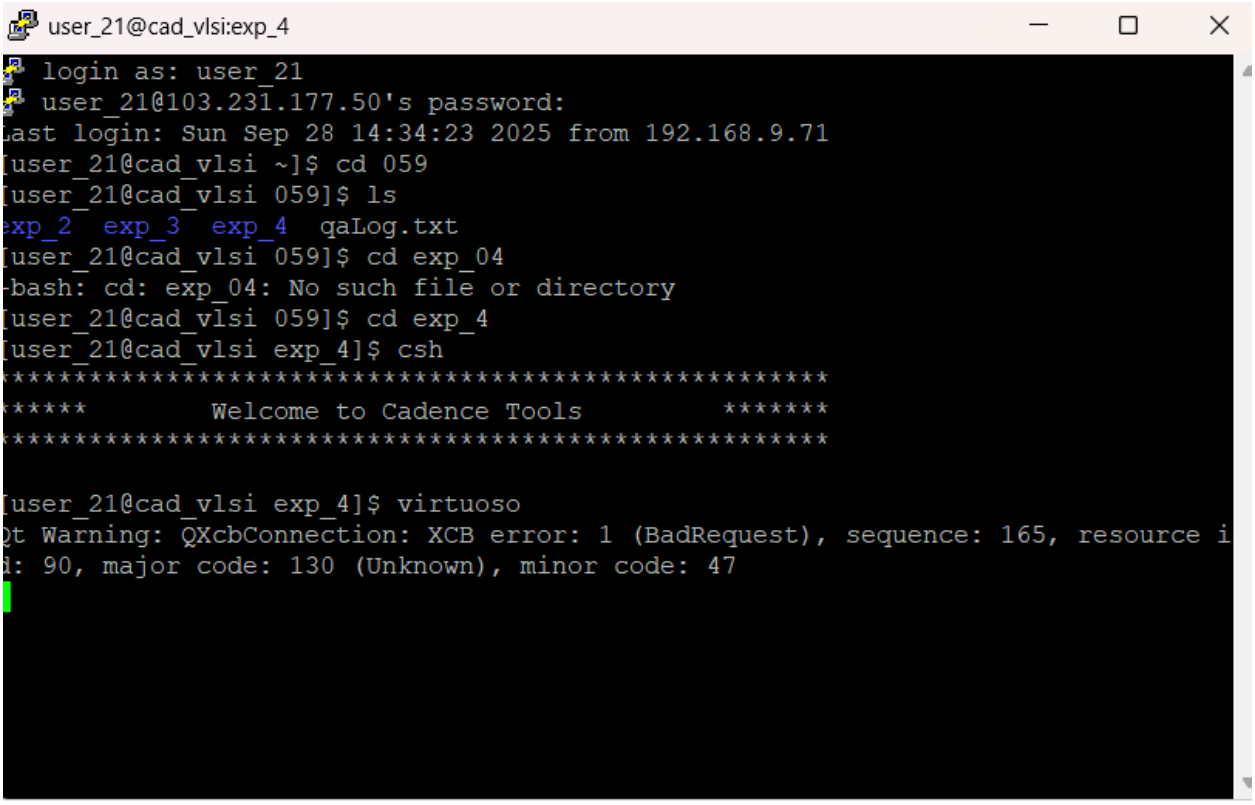
4) To execute parametric analysis of the drain current with respect to drain-to-source voltage and study its variation with gate bias.

Introduction:

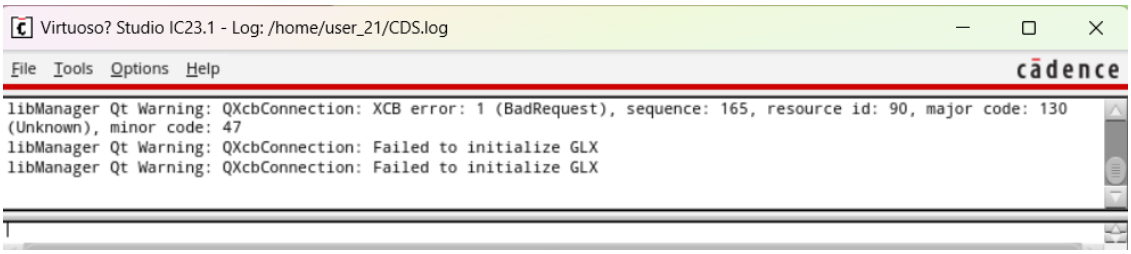
The MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor) is a fundamental device in modern electronics, widely used in both analog and digital circuits. Its operation is based on controlling the flow of carriers in a semiconductor channel by applying voltage at the gate terminal.

Characterizing a MOSFET involves analyzing its I–V behavior under different biasing conditions. From Ids–Vds and Ids–Vgs plots, important parameters such as threshold voltage (Vth), transconductance (gm), and operating regions (cut-off, linear, and saturation) can be identified. Using Cadence simulations, these characteristics can be observed and studied, which is essential for circuit design and performance analysis.

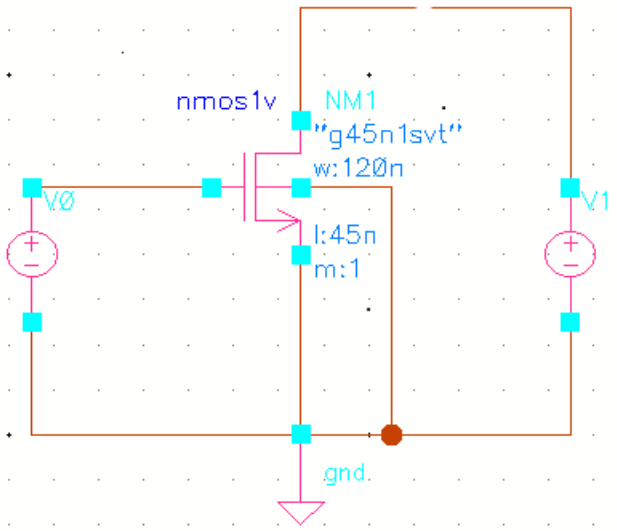
Cadence:



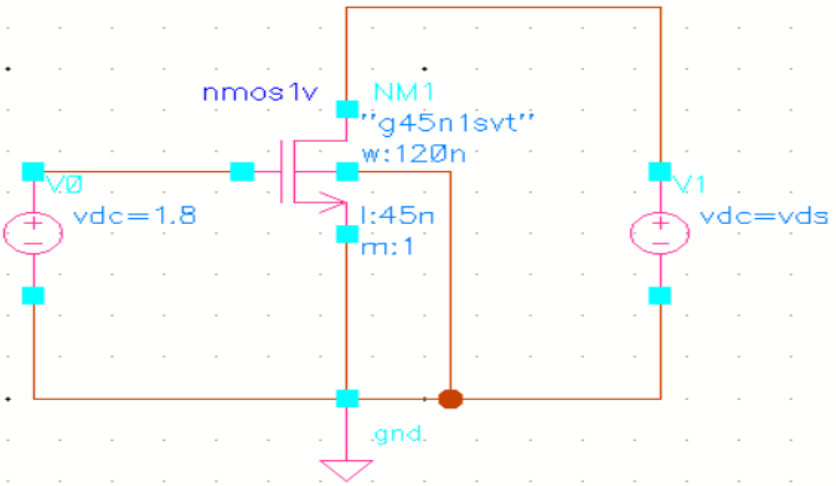
Virtuoso:



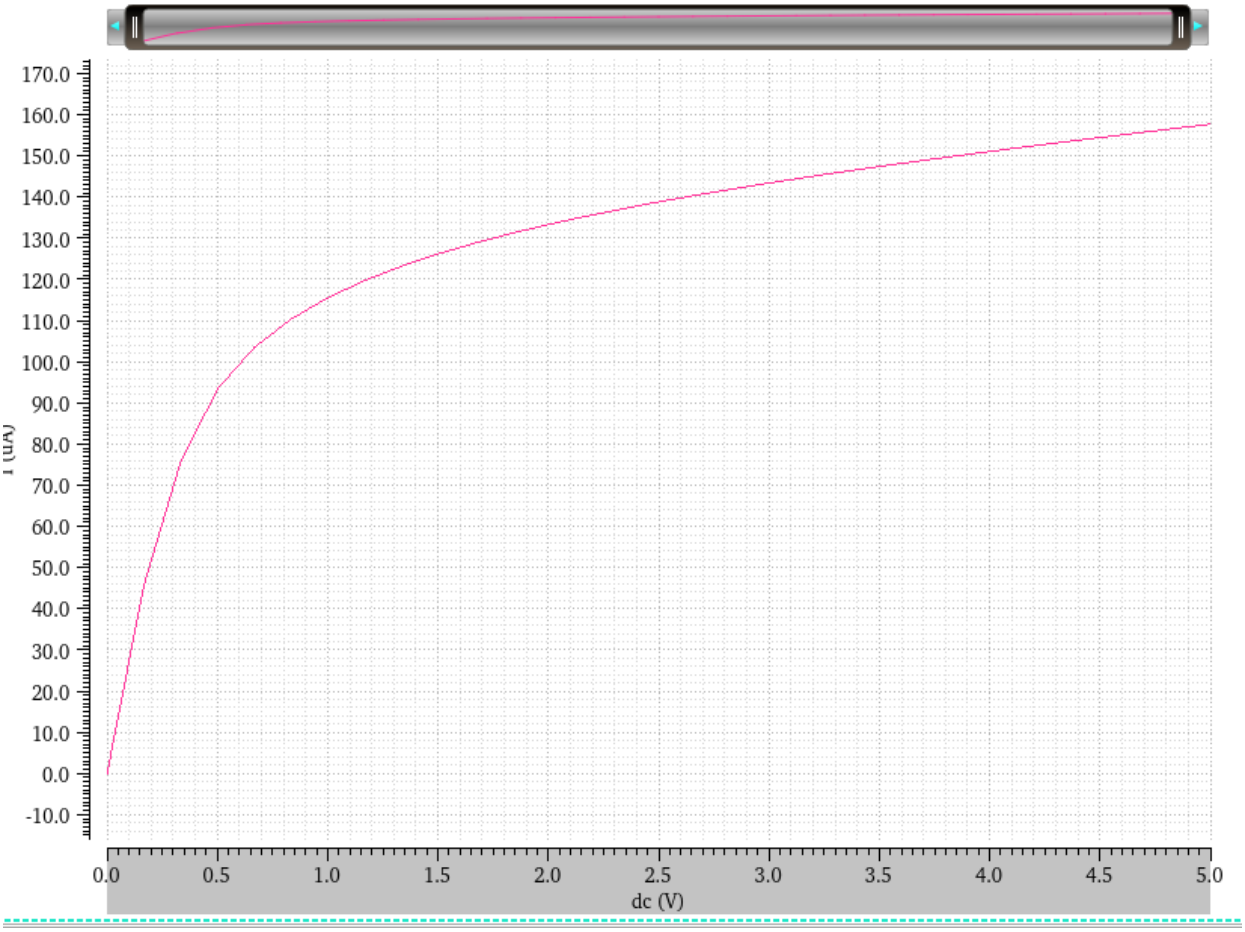
Schematic Design of NMOS:



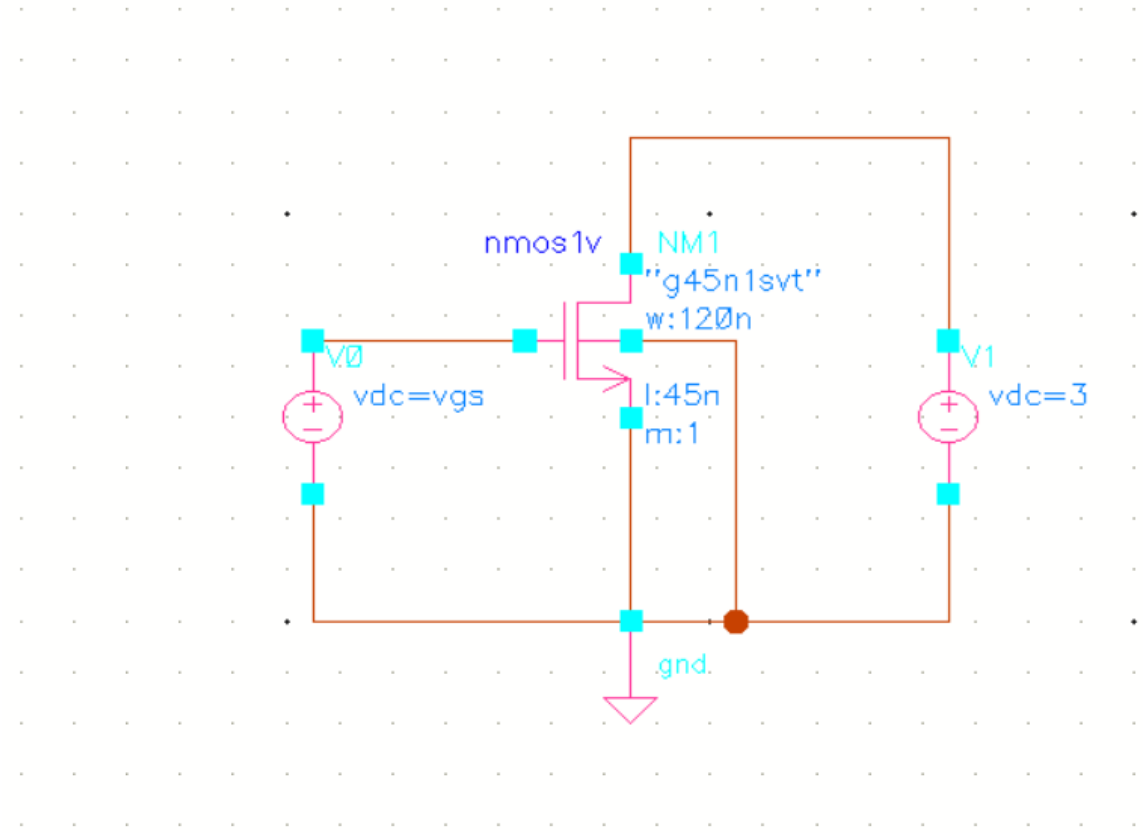
Schematic Design of NMOS (Ids vs Vds)



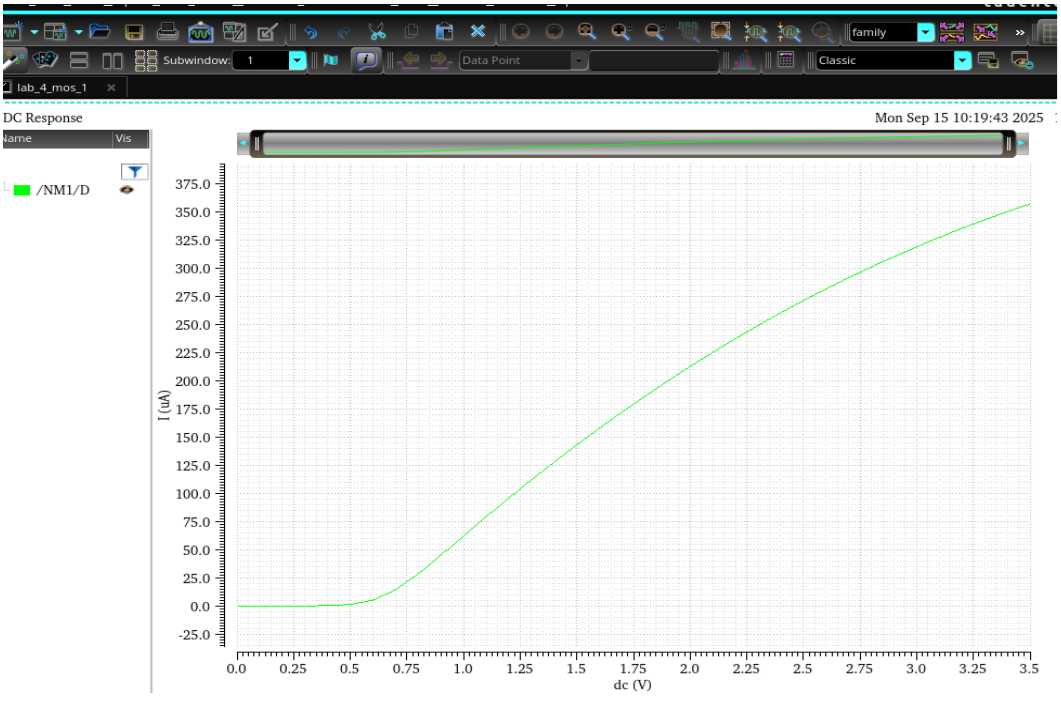
Graph of Ids vs Vds:



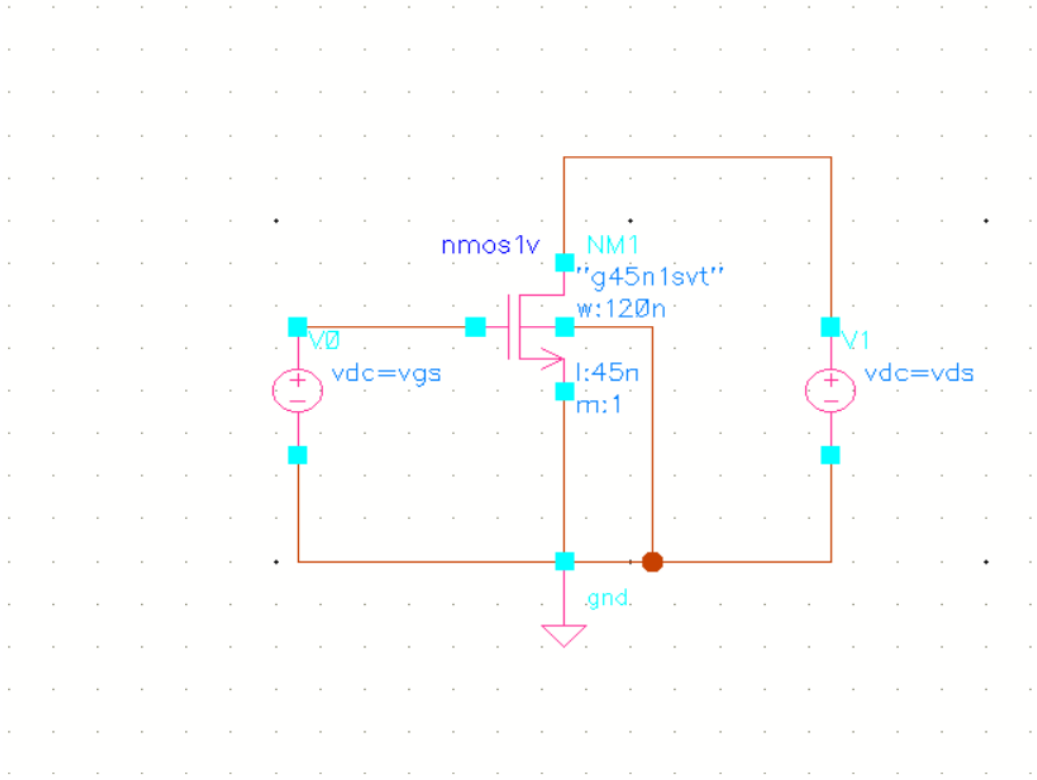
Schematic Design of NMOS (Ids vs Vgs):



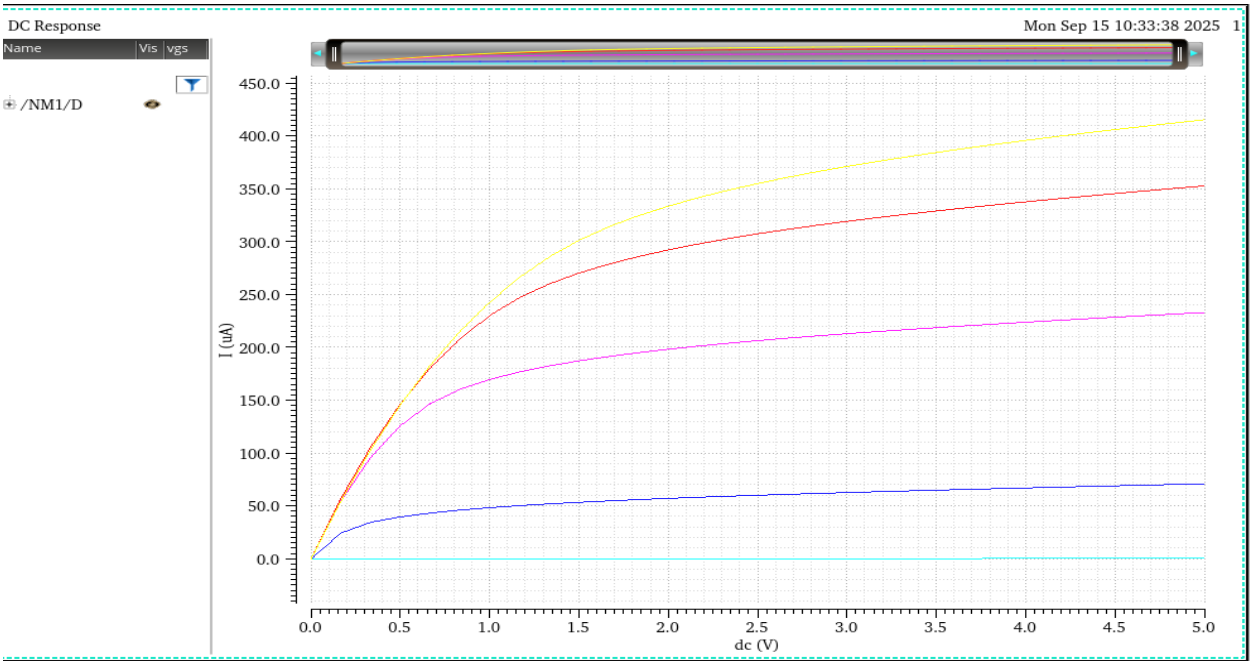
Graph of Ids vs Vgs:



Parametric analysis for Ids vs Vds:



Graph of Ids vs Vds:



Conclusion:

The NMOS transistor was successfully characterized through Cadence simulations. From the Ids Vds and Ids Vgs curves, the distinct operating modes of the MOSFET cut off, linear, and saturation were clearly observed. The Ids Vds plots showed that current rises linearly at first and then levels off, indicating the transition from the triode to the saturation region. Similarly, the Ids Vgs plots confirmed that the device remains OFF until the threshold voltage (around 0.6–0.7 V) is reached, after which the drain current increases rapidly, verifying the voltage-controlled nature of the MOSFET. The parametric sweep further demonstrated that larger gate voltages yield higher drain currents. Overall, the results highlight the MOSFET's high input impedance, controllable conduction, and well-defined regions of operation, making it suitable for applications in logic circuits, amplification, and switching systems