Department Of Computer Science and Engineering

Course Title: VLSI Lab

Course Code: CSE 458

Title: CMOS circuit in Virtuoso

Submitted To:

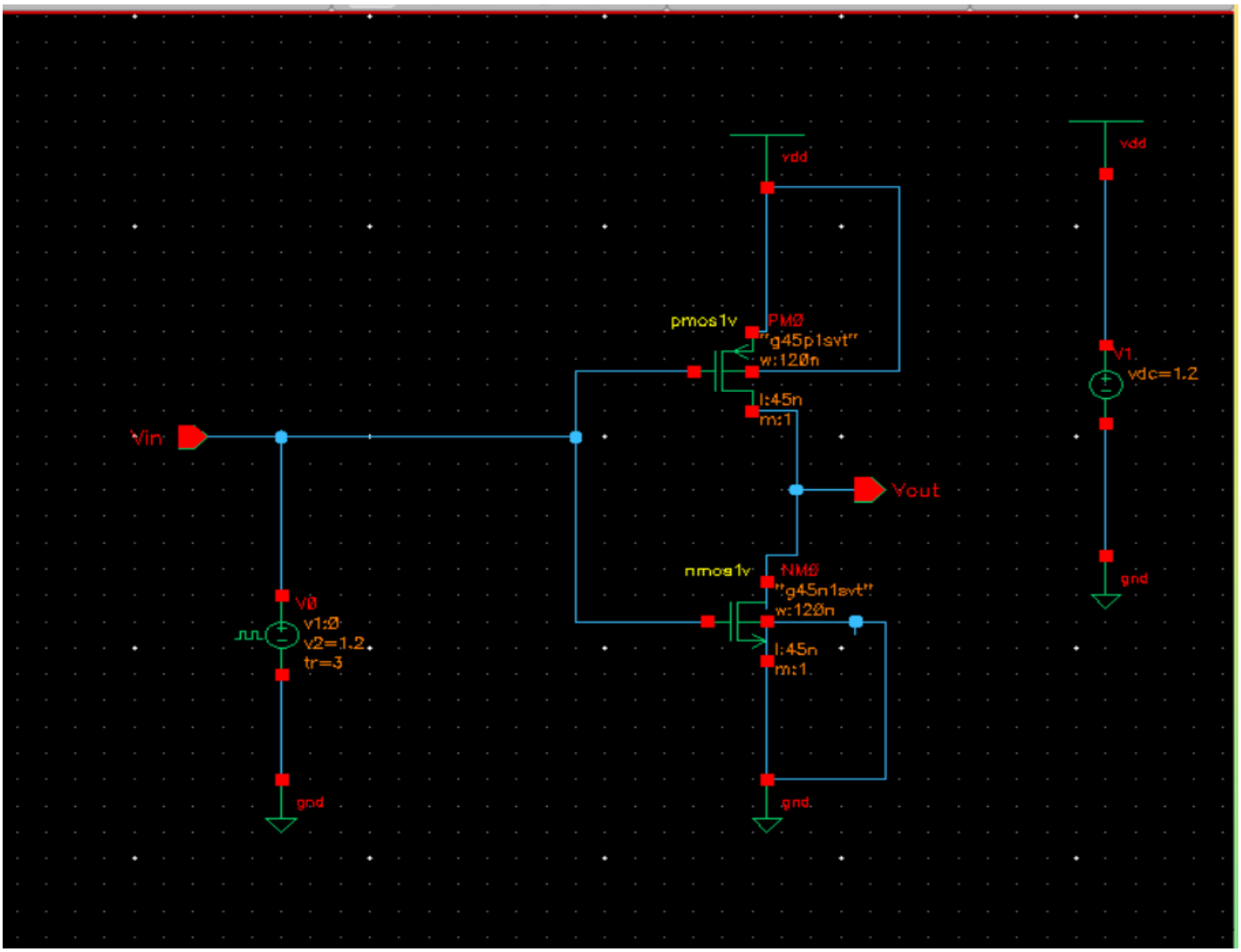
Md Sabbir Ahmed
Lecturer
Department Electrical & Electronic Engineering

Submitted By:

Labanya Saha
Reg No:21201059
Roll:59
Sec:B1

Submission Date: 10.08.2025

The construction of CMOS circuit in Virtuoso:



CMOS Inverter Schematic Description

The above schematic represents a CMOS inverter implemented using one PMOS and one NMOS transistor. The PMOS transistor (PM0) is connected at the top, with its source tied to the positive supply voltage (Vdd = 1.2 V), while the NMOS transistor (NM0) is connected at the bottom, with its source tied to ground. Both transistors share a common gate connection, which serves as the input (Vin), and a common drain connection, which forms the output (Vout).

Key Components:

1. **Transistors:**

   PMOS: Model g45p1svt, width 120 nm, length 45 nm.

   NMOS: Model g45n1svt, width 120 nm, length 45 nm.

2. **Input Source (V0):**

   A pulse voltage source generating a digital-like waveform.

   Parameters:

   - Low voltage = 0 V
   - High voltage = 1.2 V
   - Rise time = 3 ns (tr = 3).

3. **Power Supply (V1):**

   DC voltage source providing Vdd = 1.2 V.

4. **Connections:**

   The input (Vin) drives the gates of both NMOS and PMOS transistors.

   The output (Vout) is taken from the common drain connection.

   The PMOS source is connected to Vdd, while the NMOS source is connected to ground.

Conclusion:

The circuit is a CMOS inverter powered at 1.2 V, using matched PMOS and NMOS transistors (W=120 nm, L=45 nm). A pulse input (0–1.2 V, 3 ns rise time) controls both gates, producing an inverted output at Vout through complementary switching of the transistors**.**