Department Of Computer Science and Engineering

Course Title: VLSI Lab

Course Code: CSE 458

Title: Design of CMOS inverter circuit in Cadence Virtuoso Schematic Editor and Performing Transient Simulation with Spectre and DC Analysis.

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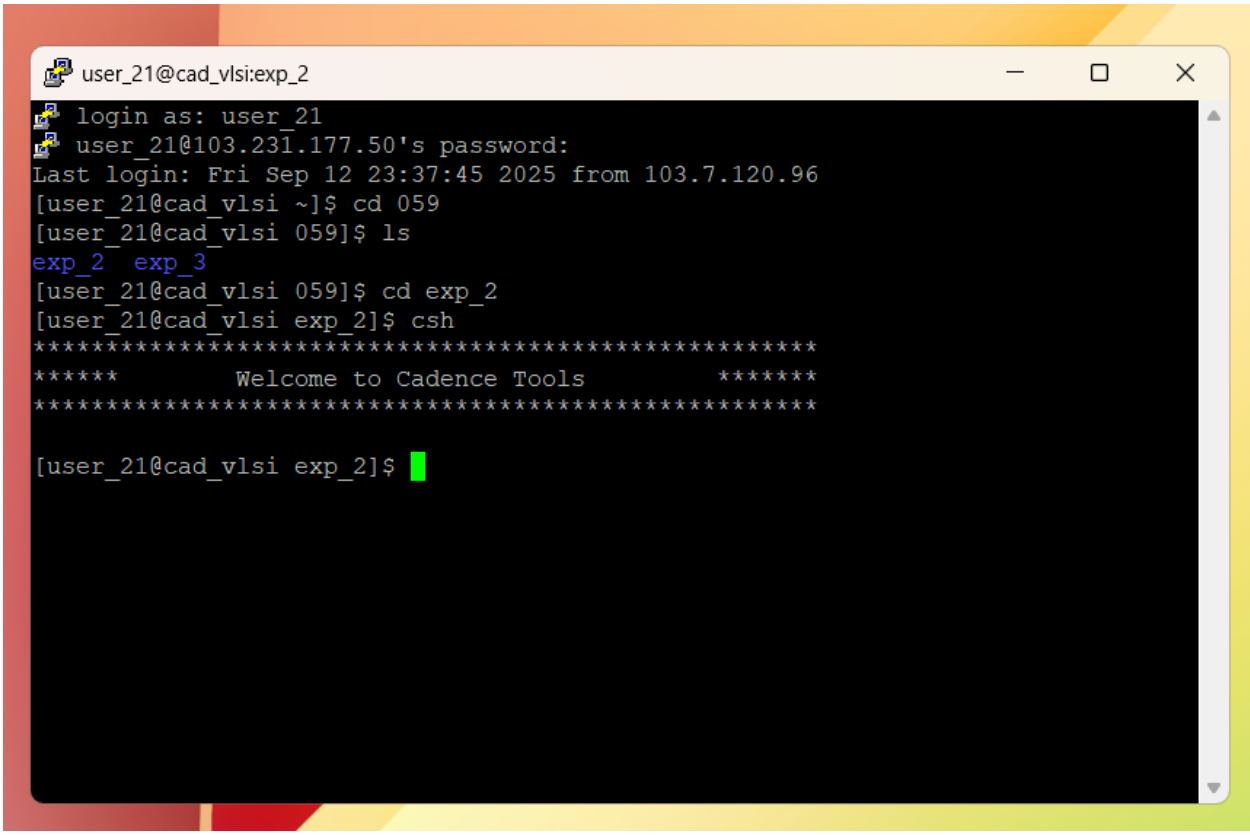
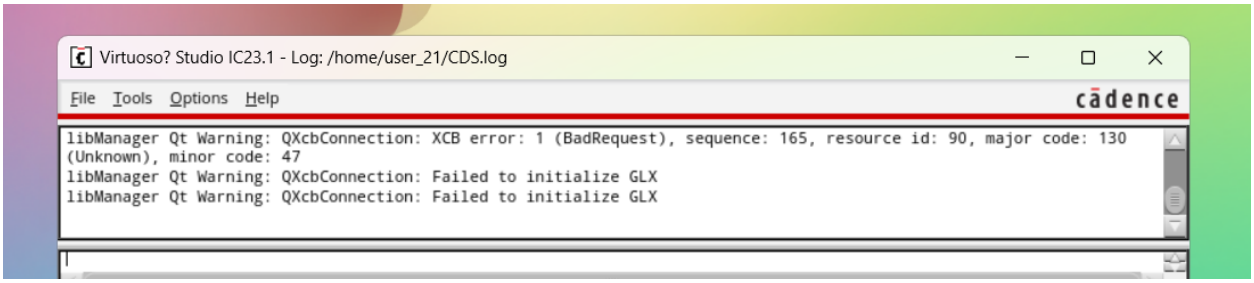
Cadence:



Virtuoso:



Circuit Diagram:

CMOS Inverter Schematic Description

The above schematic represents a CMOS inverter implemented using one PMOS and one NMOS transistor. The PMOS transistor (PM0) is connected at the top, with its source tied to the positive supply voltage (Vdd = 1.2 V), while the NMOS transistor (NM0) is

connected at the bottom, with its source tied to ground. Both transistors share a common gate connection, which serves as the input (Vin), and a common drain connection, which forms the output (Vout).

Key Components:

1. **Transistors:**

   PMOS: Model g45p1svt, width 120 nm, length 45 nm.

   NMOS: Model g45n1svt, width 120 nm, length 45 nm.

2. **Input Source (V0):**

   A pulse voltage source generating a digital-like waveform.

   Parameters:

   - Low voltage = 0 V
   - High voltage = 1.2 V
   - Rise time = 3 ns (tr = 3).

3. **Power Supply (V1):**

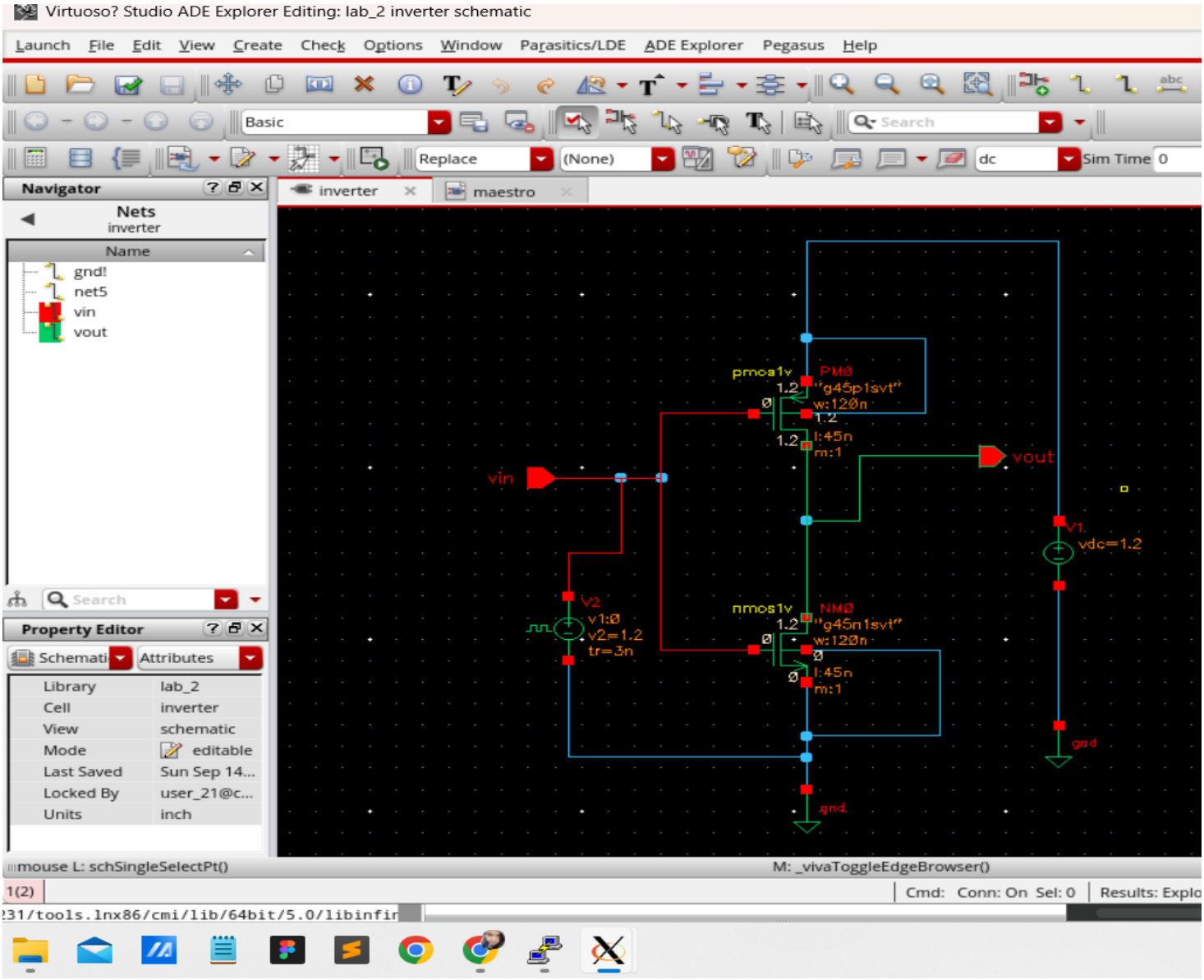
   DC voltage source providing Vdd = 1.2 V.

4. **Connections:**

   The input (Vin) drives the gates of both NMOS and PMOS transistors.

   The output (Vout) is taken from the common drain connection.

   The PMOS source is connected to Vdd, while the NMOS source is connected to ground.



Transient Analysis Setup:

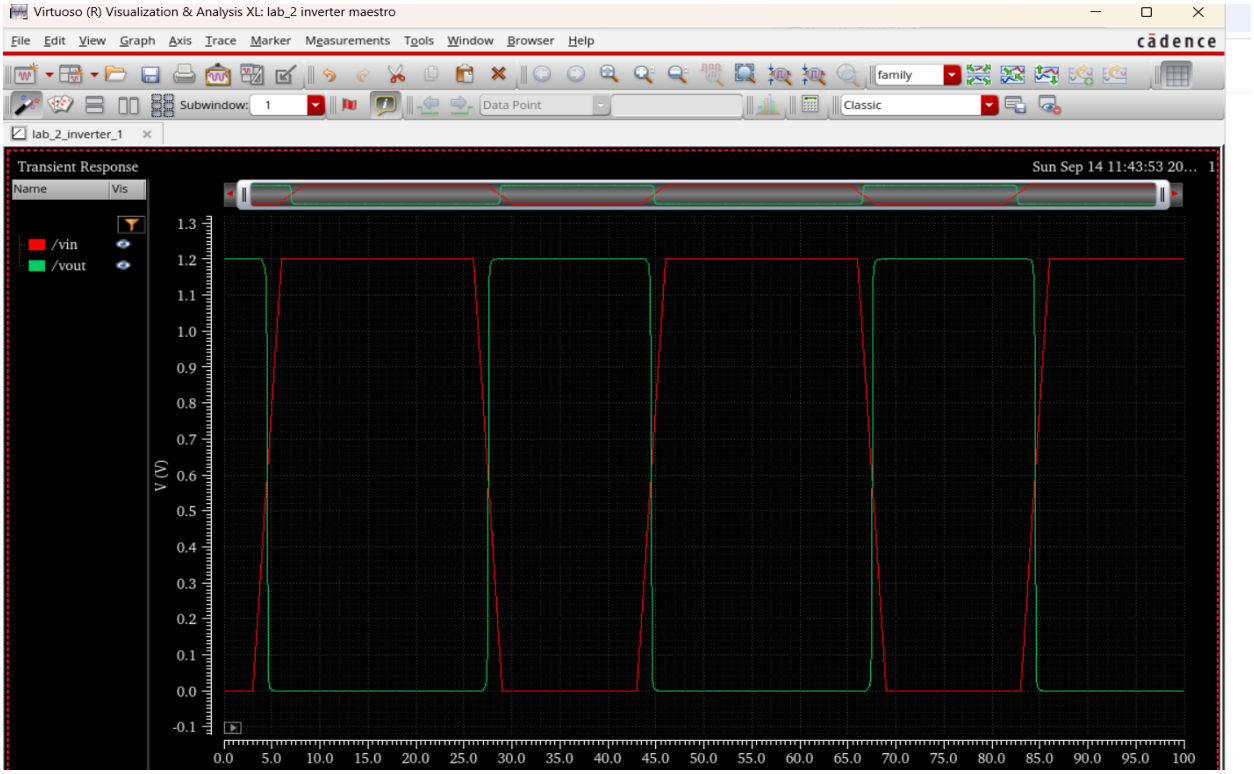
In Cadence Virtuoso ADE Explorer, the Transient (tran) analysis was selected. The stop time was set to 100n to capture several input cycles, with moderate accuracy. Input (Vin) and output (Vout) . Finally, the simulation was run to observe the inverter's time-domain behavior.

DC Analysis Setup:

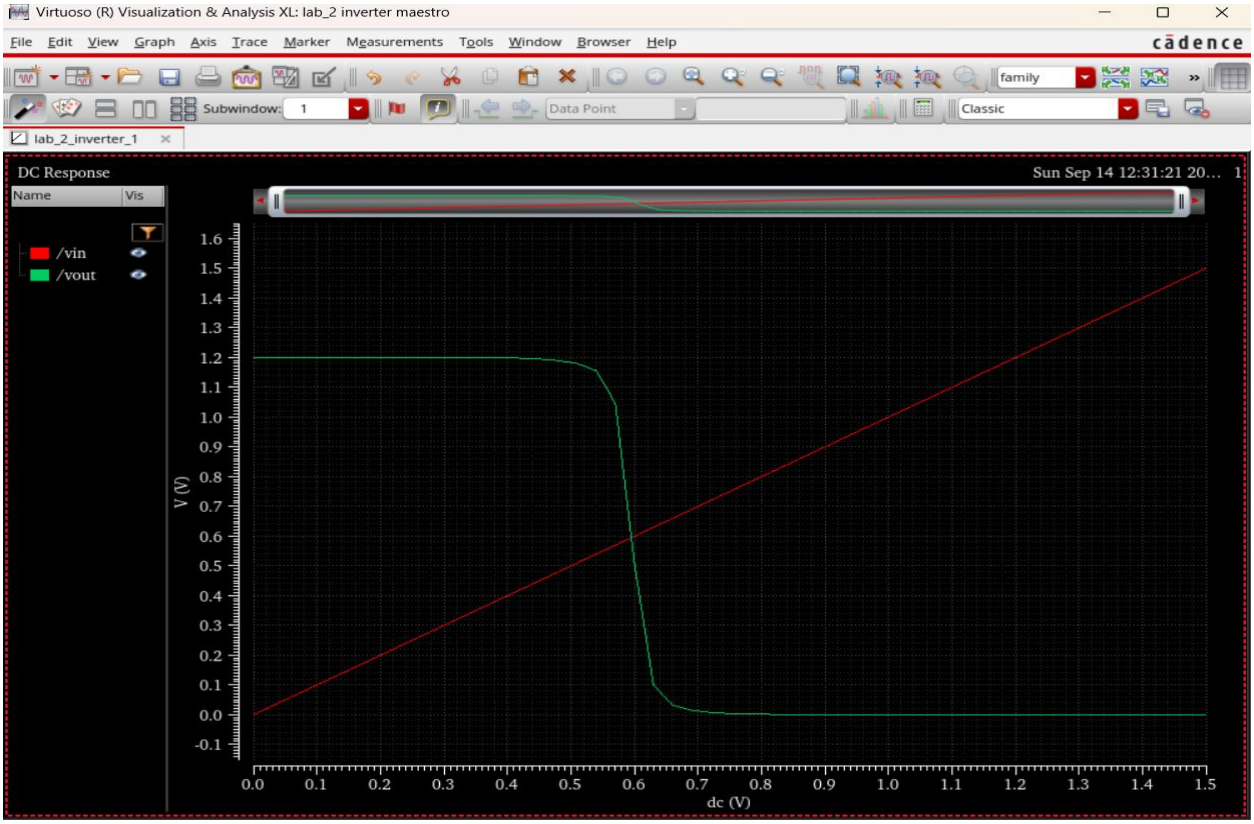
For DC analysis in Cadence Virtuoso ADE Explorer, the DC analysis was selected. The input source was defined using a vpulse component. The DC parameter sweep was applied to the input voltage, with start = 0 V and end = 1.5 V. This setup allowed plotting of the DC transfer characteristics (Vin vs. Vout) of the CMOS inverter.

Output:

Trans:



DC:



Key Observations

The wavefrom simulation produced two primary signals:

Input Voltage (Vin):

- The red waveform represents the input.
- It is a square wave toggling between 0 V (LOW) and 1.2 V (HIGH).

Output Voltage (Vout):

- The green waveform represents the output.
- It toggles between 0 V and 1.2 V, and is the inverse of Vin.
- When Vin = HIGH, Vout = LOW, confirming inverter operation**.**

Circuit Function:
The circuit behaves as a CMOS inverter (NOT gate). The waveform confirms correct inversion with clean rail-to-rail switching.

Purpose of Analysis:
The transient analysis verifies switching behavior, timing performance, and logic functionality of the CMOS inverter. It ensures that the output correctly follows the inverse of the input.

Timing Parameters:

- **Rise Time (t_r):**
  $t\_r = 27.6168\ ns - 27.4784\ ns = 0.1384\ ns$
- **Fall Time (t_f):**
  t_f= 44.5811 ns-44.4643 ns =0.4577 ns

Conclusion

The transient results verify that the designed circuit operates as a CMOS inverter (NOT gate). The output shows a clear and full-swing inversion of the input, with short rise and fall times, demonstrating correct digital switching and stable logic performance.