

VLSI _01_Introduction

Integrated Circuit Trends:

Integrated Circuits (known as Chips), where an entire circuit is manufactured in a single piece of Silicon, first appeared in 1960.

-at that time, the chip size and transistor dimensions were such- that only a few simple gates offering primitive logic functions such as NOT, NAND, NOR etc. could be accommodated; this level of integration is called small scale Integration (SSI).

-Improvements in the processing techniques in subsequent years have resulted in a steadily increasing chip area and a progressively reducing size. In 1970, Medium Scale Integrated (MSI) circuits with about a thousand transistors appeared.

-In 1980 Large Scale Integrated (LSI) circuits of approximately one hundred thousand devices were possible.

-In 1990, chips capable of containing around ten million components. This projection of several million transistors per chip is realistic. This level of integration is called Very Large Scale Integration (VLSI).

-Ultra large-scale integration (ULSI) is the process of integrating or embedding millions of transistors on a single silicon semiconductor microchip. ULSI technology was conceived during the late 1980s when superior computer processor microchips, specifically for the Intel 8086 series, were under development. ULSI is a successor to large-scale integration (LSI) and very large-scale integration (VLSI) technologies but is in the same category as VLSI.

Limitations: The capability of integrated circuits has reached the point where an entire system can be integrated. As the chip content becomes more complex, the problem of producing a correct design at the first attempt within an acceptable time scale becomes increasingly difficult.

-Barron's Corollary to Moore's second law suggests that the design of a million transistors will take thirty men ten years!

VLSI _01_Introduction

-with such integrated systems, the complexity and management of the design is dominating all other problem areas.

Choice of Technology:

-Materials are available for manufacturing integrated circuits, such as Silicon, Gallium arsenide etc. there is a considerable cost of penalty involved in their use.

-Thus Silicon remains and is likely to stay as the most economically effective way of implementing VLSI.

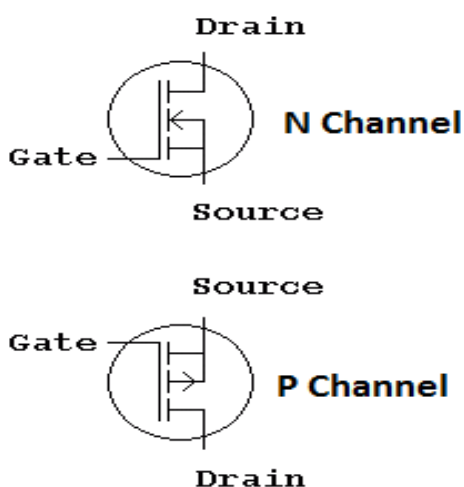
Two distinct types of technology are fabricated in Silicon based upon the Bipolar Junction Transistor

and

the Metal Oxide Semiconductor (MOS) Transistor.

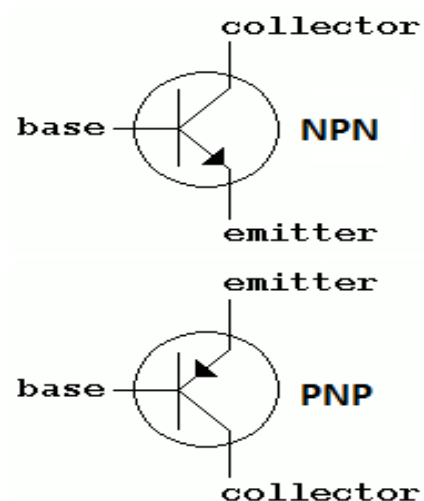
MOS Vs Bipolar Junction:

MOSFET



Metal Oxide Semiconductor Field Effect Transistor

BIPOLAR



Bipolar Junction Transistor

VLSI _01_Introduction

Difference between BJT and MOSFET

- The BJT is a bipolar junction transistor whereas MOSFET is a metal oxide semiconductor field effect transistor.
- A BJT has three terminals namely base, emitter and collector, while a MOSFET has three terminals namely source, drain and gate.
- MOS logic circuits requires appreciably less current and hence less power than its bipolar counter part.
- The working of BJT depends on the current at the base terminal and the working of the MOSFET depends on the voltage at the oxide insulated gate electrode.
- The BJT is a current controlled device and MOSFET is a voltage controlled device.
- The structure of an MOS transistor is much simpler than that for bipolar devices.
- MOS technology able to implement dynamic logic which leads to further reductions in area and power and such circuits are obviously important in the context of VLSI. It is not possible to implement dynamic logic in bipolar technology.
- In terms of area, power dissipated, yield and flexibility, MOS technology is superior (capable of realizing VLSI) to Bipolar technology.

MOS Vs Bipolar Junction (which one faster?):

This depends on application.

-For current mode signal processing, BJT will be faster since its current amplification doesn't involve large changes in junction potential.

-For switching applications where the collector/drain voltage has to go close to zero and back up, MOSFET will be faster, since in case of a BJT there will be minority carrier storage in the base in saturation which will take time to flush out.

-For typical circuits in modern processes MOSFETs will be faster since they can be much smaller than BJT and therefore have smaller junction capacitances.

VLSI _01_Introduction

NMOS Vs CMOS (Complementary metal oxide semiconductor):

- NMOS logic family is based upon n-channel MOS transistors while CMOS requires both n-channel and p-channel MOS transistors.
- NMOS process is simpler than that for CMOS since only one transistor type is involved.
- NMOS logic structures require fewer devices and occupy (about 60 per cent) less area than the equivalent CMOS. The additional area required by CMOS is not thought to be a limitation of VLSI realization because it is likely that most of chip area will be required for interconnections and therefore circuits will occupy a relatively small area.
- CMOS is likely to be eventually the design medium for VLSI as it requires much less power than NMOS.
- CMOS circuit speed is superior to NMOS.

Design Approaches:

There are three approaches to implementing digital design.

1. The first is to design with chips which are available 'off the shelf' from manufacturers.
 - although there is a wide range of SSI, MSI and LSI devices available in silicon and other technologies, the designer is limited to the integrated circuits on offer.
2. Second design approach is referred to as full custom design and for LSI/VLSI designs, MOS technology is used.
 - Implementation of a design from the viewpoint of functionality, space and power is to integrate it. Here, the designer has total control over the chip function including the specification of the content of each layer manufactured in Silicon (is the designer's imagination).

VLSI _01_Introduction

3. Semi-custom design in the form of the uncommitted Logic Array (ULA).

-Here the silicon is performed as a set of uncommitted logic cells, each of which can be configured to perform a variety of simple logic functions.

The designer only needs to specify the cell inter-connections and the cell configuration to provide a user-specified function.

Out of above three approaches Full Custom Design offers the potential to realize a VLSI circuit that is totally defined by the designer.

Design Process:

The design methodologies adopted for all digital design is that of a top-down, hierarchical approach.

System Specification	
System Design	<p>-System design is performed at the highest level. This takes the System Specification and translates it in to a block diagram of the architecture.</p> <p>-Like, functional blocks, such as cache memory, register arithmetic blocks, logic blocks etc. and their interconnecting data paths.</p>
Logic Design	<p>The architectural blocks we expanded into logic diagrams. Here each item drawn represents a particular logic function, such as gate.</p> <p>Control and timing logic is also included in this level.</p> <p>Logic simulation can be used to verify that the logic functions correctly and performs the tasks required by the system specification.</p>

VLSI _01_Introduction

Circuit Design	<p>The logic is translated into circuits with dimensions assigned to the transistors.</p> <p>The circuit diagrams are often drawn as stick diagram rather than with conventional transistor symbols.</p> <p>The stick diagram is a pictorial representation of the circuit in terms of the lines and connections required at each layer of the Silicon.</p> <p>Circuit simulation can verify the design at this level and provide an indication of the power dissipation and speed.</p>
Geometric Layout	<p>Combining the Stick Diagram with the fabrication rules for the Geometric layout, the size of each circuit can be estimated.</p> <p>This allows the designer to check that the design can be accommodated on the chip and that there is sufficient area left for circuit interconnections.</p> <p>If stick diagram is used then a Geometric layout can be derived against the circuit design to confirm that circuit details have been correctly translated to the lower level.</p>
Fabrication	<p>After the layout stage, the design normally passes out of the designer's hands. The data representation of the Geometric layout is normally used to produce a (photographic) mask of each silicon layer.</p> <p>The masks are then used at the different production stage of the Fabrication process to produce the specified Chip.</p>
Chip	