Northern University Bangladesh

Clearance for Assessment

Student ID.: 04180301280 **Semester:** Fall 2021

Student Name: Md Labib Arefin **Enrolled Semester:** 10

Program: Bachelor of Science in Computer Science and Engineering (CSE)

Course Code	Course Title	Credit Hour	Section	Remarks
CSE 3124	Microprocessor and Assembly Language Programming	3.0	A	
CSE 3171	Microprocessor and Assembly Language Programming Lab Work	1.0	A	
CSE 4278	Computer Graphics and Multimedia System Design	3.0	B	
CSE 4288	Computer Graphics Lab work	1.0	C	
CSE 4351	Image Processing and Computer Vision	3.0	A	
CSE 4355	Artificial Intelligence and Expert System	3.0	B	
CSE 4383	Image Processing and Computer Vision Lab Work	1.0	A	
CSE 4385	Artificial Intelligence and Expert System Lab Work	1.0	B	

Valid for Mid Term Assessment, Fall 2021

Answer according to Question no. 1

ID: 1803012280
Md Labib Arafin
CSE: 3124

Ans. So the question says is that 'Assembly language is a low level language' so the answer is false because this an assembly language is a type of programming language that translates high-level languages into machine language.

In 8086 micro.p

b

b) CF - It means carry flag. It is a set bit in a system status register / flag register used to indicate when an arithmetic carry or borrow has been generated out of most significant arithmetic logic unit (ALU) bit position

29 H
4C H
---
75 H

PF - The It means parity flag. The flag is set 1 when there is even no, of the one bits in result, and to 0 where is odd number of one bits.

ZF.- It means zero flag. The flag bits are changed to 0 and 1 depending upon the value of result after the arithmetic or logical operations.

Answer according to Question no. 1

ID: 1803012800
Md Labib Arafin

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SF - It means ~~fl~~ sign flag

1. c) i. 0Bh x (200-225) + 127

```
MOV AX 0Bh
MOV BX, 200 h
SUB BX, 225 h
MUL BX
ADD BX, 127
```

ii. FFFh x 10h + 1111b

```
MOV AX, 0FFFh
MOV BX, 10h
MUL BX
ADD AX, 1111b
```

Answer according to Question no. 3

a) NMI is a non-maskable interrupt pin having higher priority than than maskable interrupt pin (INTR)

when an interrupt is activated, those are the actions,

- Completes the current instruction that is in process
- Pushes the flag register values on to stack
- pushes cs (code segment) value and IP (instruction pointer) value of return address on the stack
- IP is loaded from the contents of word location 00008H
- cs is loaded from the contents of next word location 0000AH
- Interrupt and trap flag are reset to 0.

INTR

It is a maskable interrupt because the micro processor will be interrupted only if interrupts are enabled using set interrupt flag instruction. It should not be enabled using clear interrupt flag instruction.

It is activated by an I/O port

b)

i. 2460 E

⇒ The BX register is an offset of data segment (DS) register. So the location of

2460 E x 10 + 2450 E H

= 24600 E + 2450 E

= 27050 E H

ii. 2450 A

The 2450 A $\$$ x 10 H + 2450 H

= 26950 H

c) The Fetching next instruction is fetched from memory address that is currently stored in program counter and stored into instruction register. At end of fetch operation, the Program counter points the next instruction to be that will read at next cycle.

ex: This could include taking one value, putting it into ALU, then execution: taking a different value from a register and adding the two together.

Execution: The control unit of CPU passes the decoded information as a sequence of control signals to relevant functional units of CPU to perform the required by an instructions such as registers.