22.99 - Laboratorio de Microprocesadores

Instituto Tecnológico de Buenos Aires

GUÍA Nº2

Introducción a Kinetis

Grupo II

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Septiembre 2020

Contenido

1. Ejercicio 1

1.1. 1.1

Numero de pin del MCU en el que se encuentra el puerto PTA12: 42.(PAG 71 fila 7 y PAG 79. archivo: Kinetis K64F Sub-Family Data Sheet. en campus: Kinetis K64 - Datasheet - rev 7 - 11-2016.pdf)

1.2. 1.2

Pines que pueden funcionar como entradas analogicas:

5.2 Unused analog interfaces

Table 57. Unused analog interfaces

Module name	Pins	Recommendation if unused
ADC	ADC0_DP1, ADC0_DM1, ADC1_DP1, ADC1_DM1, ADC0_DP0/ADC1_DP3, ADC0_DM0/ADC1_DM3, ADC1_DP0/ ADC0_DP3, ADC1_DM0/ADC0_DM3, ADC1_SE16/ADC0_SE22, ADC0_SE16/ADC0_SE21, ADC1_SE18	Ground
DAC [1]	DAC0_OUT, DAC1_OUT	Float
USB	VREGIN, USB0_GND, VOUT33[2]	Connect VREGIN and VOUT33 together and tie to ground through a 10 kΩ resistor. Do not tie directly to ground, as this causes a latch-up risk.
	USB0_DM, USB0_DP	Float

1. Unused DAC signals do not apply to all parts. See the Pinout section for details.
2. USB0_VBUS and USB0_GND are board level signals

FIGURA 1: Unused analog

1.3. 1.3

Pines del puerto PTE disponibles en el MCU de 100 pines:

- PTE0
- PTE1
- PTE2
- PTE3
- PTE4 ¿¿¿¿Disabled????
- PTE5 ¿¿¿¿Disabled????
- PTE6 ¿¿¿¿Disabled????
- PTE24
- PTE25

- PTE26 ¿¿¿¿Disabled????

Esto sale de:

144 LQFP	144 MAP BGA	121 XFB GA	100 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
—	L5	L7	—	RTC_ WAKEUP_ B	RTC_ WAKEUP_ B	RTC_ WAKEUP_ B								
—	—	B11	—	PTB12	DISABLED		PTB12	UART3_ RTS_b	FTM1_CH0	FTM0_CH4		FTM1_QD_ PHA		
—	—	C11	—	PTB13	DISABLED		PTB13	UART3_ CTS_b	FTM1_CH1	FTM0_CH5		FTM1_QD_ PHB		
—	—	A11	—	NC	NC	NC								
—	M5	—	—	NC	NC	NC								
—	A10	—	—	NC	NC	NC								
—	B10	K3	—	NC	NC	NC								
—	C10	H4	—	NC	NC	NC								
1	D3	E4	1	PTE0	ADC1_ SE4a	ADC1_ SE4a	PTE0	SPI1_PCS1	UART1_TX	SDHC0_D1	TRACE_ CLKOUT	I2C1_SDA	RTC_ CLKOUT	
2	D2	E3	2	PTE1/ LLWU_P0	ADC1_ SE5a	ADC1_ SE5a	PTE1/ LLWU_P0	SPI1_ SOUT	UART1_RX	SDHC0_D0	TRACE_D3	I2C1_SCL	SPI1_SIN	
3	D1	E2	3	PTE2/ LLWU_P1	ADC0_DP2/ ADC1_ SE6a	ADC0_DP2/ ADC1_ SE6a	PTE2/ LLWU_P1	SPI1_SCK	UART1_ CTS_b	SDHC0_ DCLK	TRACE_D2			
4	E4	F4	4	PTE3	ADC0_ DM2/ ADC1_ SE7a	ADC0_ DM2/ ADC1_ SE7a	PTE3	SPI1_SIN	UART1_ RTS_b	SDHC0_ CMD	TRACE_D1		SPI1_ SOUT	
5	E5	E7	—	VDD	VDD	VDD								
6	F6	F7	—	VSS	VSS	VSS								
7	E3	H7	5	PTE4/ LLWU_P2	DISABLED		PTE4/ LLWU_P2	SPI1_PCS0	UART3_TX	SDHC0_D3	TRACE_D0			
8	E2	G4	6	PTE5	DISABLED		PTE5	SPI1_PCS2	UART3_RX	SDHC0_D2		FTM3_CH0		
9	E1	F3	7	PTE6	DISABLED		PTE6	SPI1_PCS3	UART3_ CTS_b	I2S0_MCLK		FTM3_CH1	USB_SOF_ OUT	
10	F4	—	—	PTE7	DISABLED		PTE7		UART3_ RTS_b	I2S0_RXD0		FTM3_CH2		
11	F3	—	—	PTE8	DISABLED		PTE8	I2S0_RXD1	UART5_TX	I2S0_RX_ FS		FTM3_CH3		
12	F2	—	—	PTE9	DISABLED		PTE9	I2S0_TXD1	UART5_RX	I2S0_RX_ BCLK		FTM3_CH4		
13	F1	—	—	PTE10	DISABLED		PTE10		UART5_ CTS_b	I2S0_TXD0		FTM3_CH5		

144 LQFP	144 MAP BGA	121 XFB GA	100 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
14	G4	—	—	PTE11	DISABLED		PTE11		UART5_ RTS_b	I2S0_TX_ FS		FTM3_CH6		
15	G3	—	—	PTE12	DISABLED		PTE12			I2S0_TX_ BCLK		FTM3_CH7		

FIGURA 2: PTE

Pinout

144 LQFP	144 MAP BGA	121 XFB GA	100 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
38	L3	K5	27	DAC0_ OUT/ CMP1_IN3/ ADC0_ SE23	DAC0_ OUT/ CMP1_IN3/ ADC0_ SE23	DAC0_ OUT/ CMP1_IN3/ ADC0_ SE23								
39	L4	K4	—	DAC1_ OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_ SE23	DAC1_ OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_ SE23	DAC1_ OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_ SE23								
40	M7	L4	28	XTAL32	XTAL32	XTAL32								
41	M6	L5	29	EXTAL32	EXTAL32	EXTAL32								
42	L6	K6	30	VBAT	VBAT	VBAT								
43	—	—	—	VDD	VDD	VDD								
44	—	—	—	VSS	VSS	VSS								
45	M4	H5	31	PTE24	ADC0_ SE17	ADC0_ SE17	PTE24		UART4_TX		I2C0_SCL	EWM_ OUT_b		
46	K5	J5	32	PTE25	ADC0_ SE18	ADC0_ SE18	PTE25		UART4_RX		I2C0_SDA	EWM_IN		
47	K4	H6	33	PTE26	DISABLED		PTE26	ENET_ 1588_ CLKIN	UART4_ CTS_b			RTC_ CLKOUT	USB_ CLKIN	
48	J4	—	—	PTE27	DISABLED		PTE27		UART4_ RTS_b					
49	H4	—	—	PTE28	DISABLED		PTE28							
50	J5	J6	34	PTA0	JTAG_		PTA0	UART0_	FTM0_CH5				JTAG_	EZP_CLK

FIGURA 3: PTE

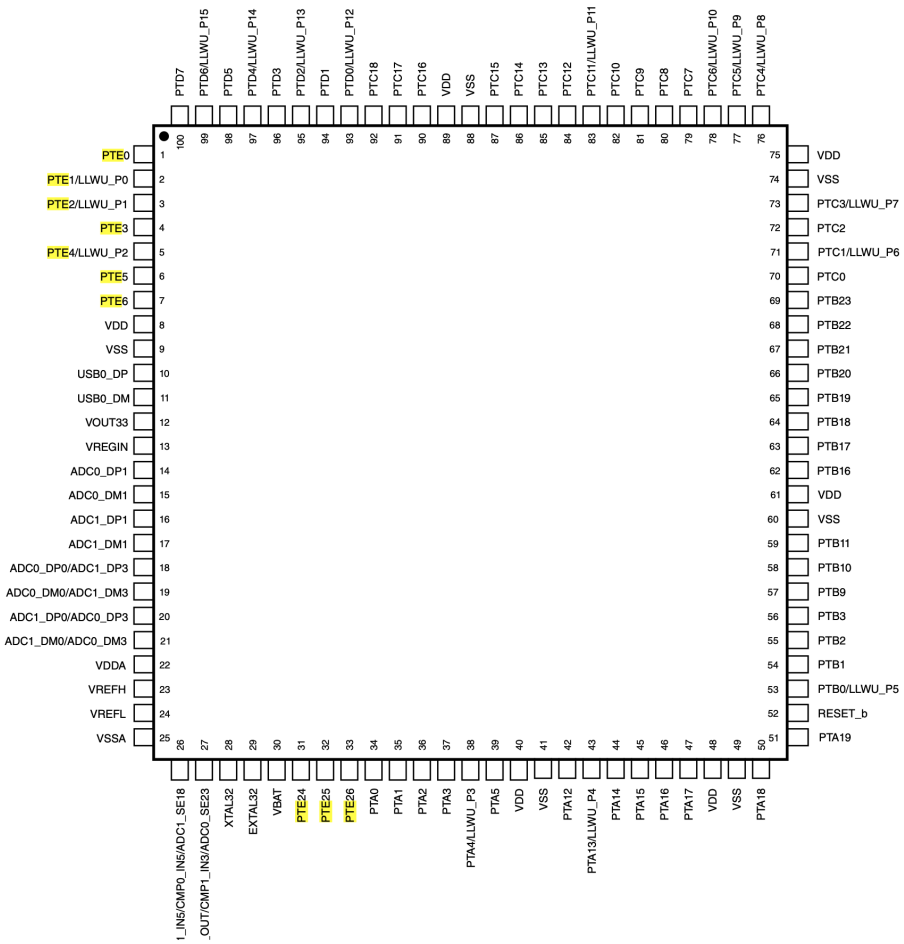

FIGURA 4: PTE

1.4. 1.4

V_{IH}	Input high voltage				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V	0.7 × V_{DD}	—	V	
	• 1.7 V ≤ V_{DD} ≤ 2.7 V	0.75 × V_{DD}	—	V	
V_{IL}	Input low voltage				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V	—	0.35 × V_{DD}	V	
	• 1.7 V ≤ V_{DD} ≤ 2.7 V	—	0.3 × V_{DD}	V	

FIGURA 5: magic

V_{DIO}	Digital input voltage (except RESET, EXTAL, and XTAL)	–0.3	5.5	V

FIGURA 6: more magic

1.5. 1.5

Máxima corriente pin: 25mA (PAG 6 - tabla 1 - fila 6. Archivo: Kinetis K64F Sub-Family Data Sheet. en campus: Kinetis K64 - Datasheet - rev 7 - 11-2016.pdf)

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	3.8	V
I_{DD}	Digital supply current	—	185	mA
V_{DIO}	Digital input voltage (except RESET, EXTAL, and XTAL)	–0.3	5.5	V
V_{DRTC_WAKEUP}	RTC Wakeup input voltage	–0.3	V_{BAT} + 0.3	V
V_{AIO}	Analog[1], RESET, EXTAL, and XTAL input voltage	–0.3	V_{DD} + 0.3	V
I_D	Maximum current single pin limit (applies to all digital pins)	–25	25	mA

FIGURA 7: Idmax

2. Ejercicio 2

2.1. optimize

https://community.nxp.com/thread/388981
https://en.wikipedia.org/wiki/Volatile$_{(computer_programming)}$
VOLATILE

2.2. blink green led

- ***volatile object*** - an object whose type is *volatile-qualified*, or a subobject of a volatile object, or a mutable subobject of a const-volatile object. Every access (read or write operation, member function call, etc.) made through a glvalue expression of volatile-qualified type is treated as a visible side-effect for the purposes of optimization (that is, within a single thread of execution, volatile accesses cannot be optimized out or reordered with another visible side effect that is sequenced-before or sequenced-after the volatile access. This makes volatile objects suitable for communication with a signal handler, but not with another thread of execution, see `std::memory_order`). Any attempt to refer to a volatile object through a non-volatile glvalue (e.g. through a reference or pointer to non-volatile type) results in undefined behavior.

FIGURA 8: Volatile