ELEC6236 Digital System Design Assignment 2025/26

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1-Objective

The objective of this assignment is to design and implement a system for calculating non-linear energy operator (NEO) of a signal and its mathematical representation. Your design should be written in SystemVerilog, and must simulate and synthesise correctly.

This assignment is designed to test your ability to write correct SystemVerilog code and to use the design tools. The assignment is worth 20% of the module marks and should therefore take you about 30 hours to complete. You must complete a short report, describing what you have done.

You may discuss the assignment with other students, but the report that you submit for assessment must be your own work. Please ensure you are familiar with the rules on academic integrity and the penalties for violating those rules.

2-Design Specification

2.1- Nonlinear Energy Operator (NEO)

The Nonlinear Energy Operator (NEO), also known as the Teager Energy Operator (TEO), is a signal processing tool used to estimate the energy of a signal by considering both its amplitude and frequency variations. It is particularly useful for analyzing nonlinear and non-stationary signals. NEO is used in speech and audio signal processing, biomedical signal processing, vibration and mechanical fault detection, radar and sonar signal processing and communications and modulation analysis. NEO is defined as:

$$\psi(n) = x(n) - x(n+1) \cdot x(n-1)$$

where x(n) is the input digitized signal and $\psi(n)$ is the NEO value at sampling point n. This operator highlights the large variations in power and frequency. The NEO operator emphasizes the amplitude-energy variation of the spikes and improves the signal to noise ration (SNR) of the signal.

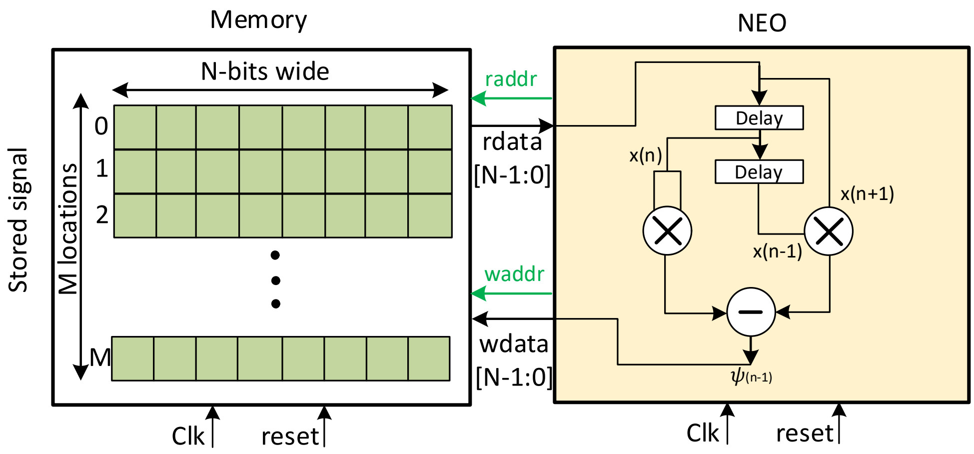

Figure 1. Interfacing the memory to the NEO unit.

2.2- System Design

A signal energy operator is a computational block that calculates the energy of a signal stored in memory shown in Figure 1. Here are the main steps in Figure 1:

- Data is stored in memory during the reset phase.
- Memory has M locations each consisting N bits.
- The stored data in memory $x(n)$ is sent to the NEO unit first. Reading process form memory requires generating reading address rdata.
- NEO performs energy calculations on the stored data.
- The calculated energy $\psi(n)$ is written back to the memory by writing address wdata.
- n-1 denotes the sample that precedes the current sample n in the dataset.

2.3- Timing

Your design must be synchronous. The system must be sensitive to the positive edge of the clock (only). You should include an active low asynchronous reset that will set the contents of memory to the generated data and the NEO registers to 0.

Your energy operator must have a 'ready' output. This should be asserted for one clock cycle only. When the 'ready' signal is asserted, the calculation of $\psi(n)$ for all data is completed.

3-Assessment

Consider a continuous sine wave, $x(t) = A \cdot \sin(\omega t + \varphi)$, where A is the amplitude $\omega = 2\pi f$ is the angular frequency and φ is the phase. The theoretical energy output of the NEO for this signal is: $\Psi[x(t)] = (A\omega)^2$. This means the operator's output is proportional to the square of both the amplitude *and* the frequency. It is a constant value, reflecting the constant energy of a pure sine wave.

Testing NEO with varying amplitude and frequency: generate a sine wave in MATLAB with A = 1.0 and f = 100 Hz, then change the values to A = 2.0 and f = 500 Hz and finally to A = 3.0 and f = 1000 Hz. **Hint: the length of the generated signal should be equal with the number of locations (M) shown in Figure 1. Please also use the following sequence:**

- $x(t) = A \cdot \sin(\omega t + \varphi)$, *A = 1.0, f = 100 Hz:* testing the NEO and report the analysis.
- $x(t) = A \cdot \sin(\omega t + \varphi)$, *A = 2.0, f = 500 Hz:* testing the NEO and report the analysis.
- $x(t) = A \cdot \sin(\omega t + \varphi)$, *A = 3.0, f = 1000 Hz:* testing the NEO and report the analysis.
    - **You can generate sine wave in MATLAB.**

4-Submission

You must also submit your Design Report.pdf in Blackboard. You can create this PDF file using either the Word or Latex templates provided. Please check that the PDF file opens correctly in Acrobat.

The deadline for submission is **16:00 on Tuesday 20th of November 2025**. Late submissions will be penalised in line with ECS regulations. Please ensure that your report file is included with your final submission.