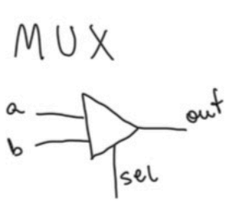
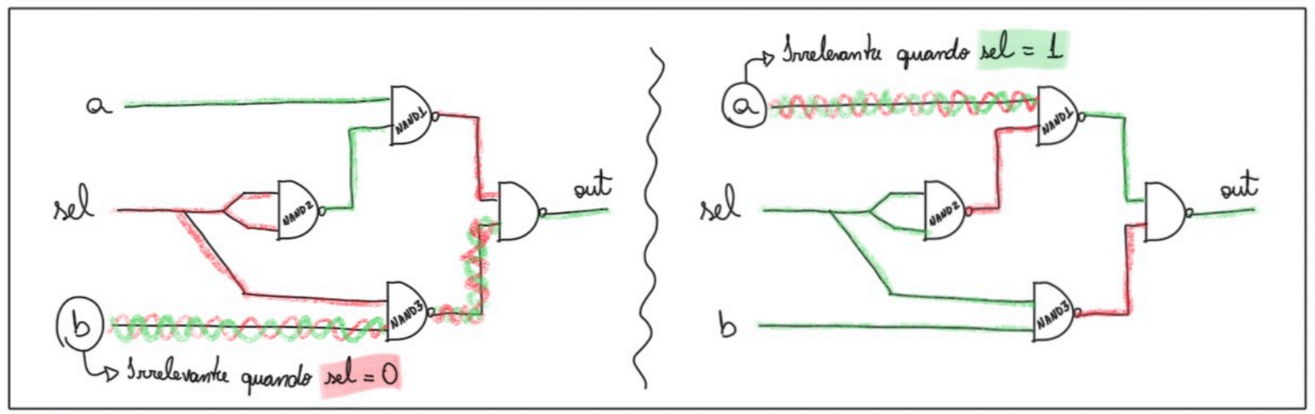
MUX



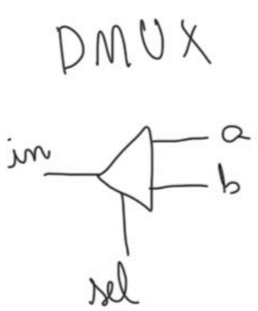
a	b	sel	out
0	0	0	0
0	1	0	0
1	0	0	1
1	1	0	1
0	0	1	0
0	1	1	1
1	0	1	0
1	1	1	1

sel	out
0	a
1	b

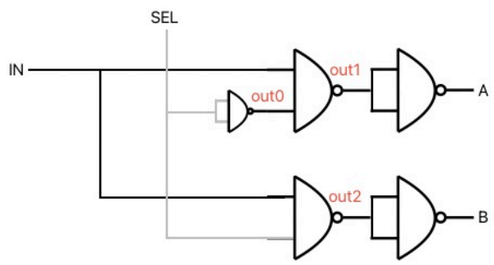


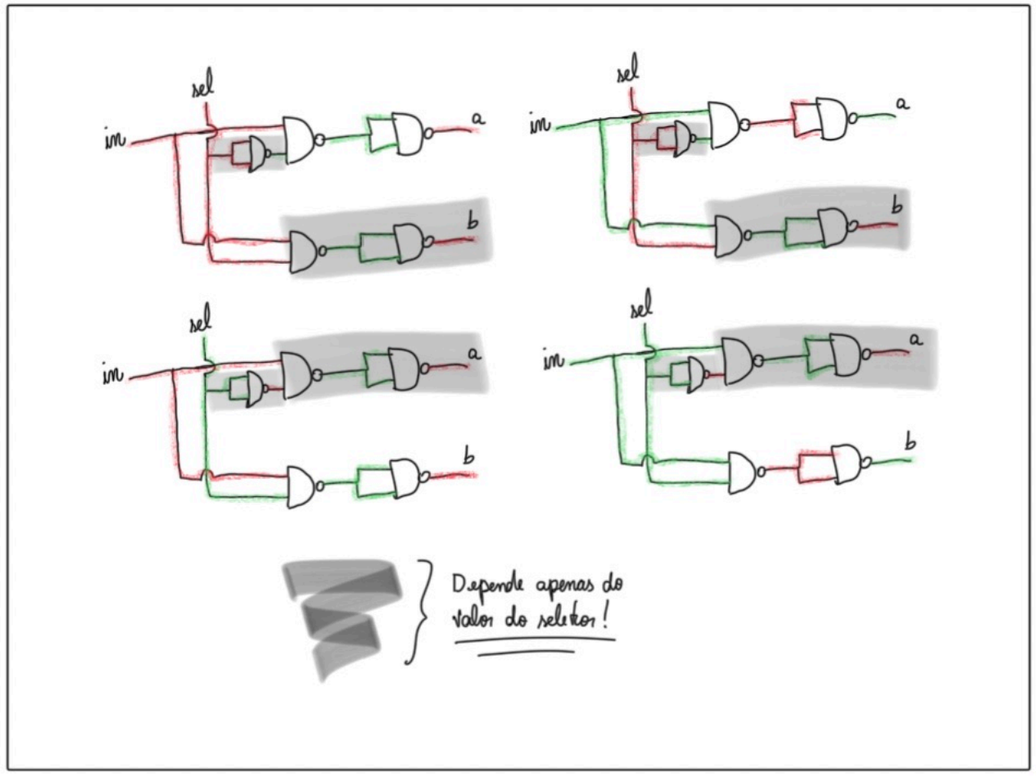

```
CHIP Mux {
    IN a, b, sel;
    OUT out;

    PARTS:
    Nand(a= sel, b= sel, out= out0);
    Nand(a= a, b= out0, out= out1);
    Nand(a= sel, b= b, out= out2);
    Nand(a= out1, b= out2, out= out);
}
```

DMUX



sel	a	b
0	in	0
1	0	in






```
CHIP DMux {
    IN in, sel;
    OUT a, b;

    PARTS:
    Nand(a= sel, b= sel, out= out0);
    Nand(a= in, b= out0, out= out1);
    Nand(a= in, b= sel, out= out2);
    Nand(a= out1, b= out1, out= a);
    Nand(a= out2, b= out2, out= b);
}
```


SEL[0]

SEL[2]

SEL = 00