unsigned and signed

- Closely related to std_logic_vector.
- Used for maths on vectors of std_logic.
- Useful for *counters*
- Two types allow choice of signed or unsigned arithmetic.
- Roll-over at usual boundaries.
- Required libraries:

```
library ieee;
use ieee.std_logic_1164.ALL;
use ieee.numeric_std.all;
```

Conversions

- un/signed <=> std_logic_vector

```
slv      <= std_logic_vector(signd)
slv      <= std_logic_vector(unsignd)
unsignd  <= unsigned(slv)
signd    <= signed(slv)
```

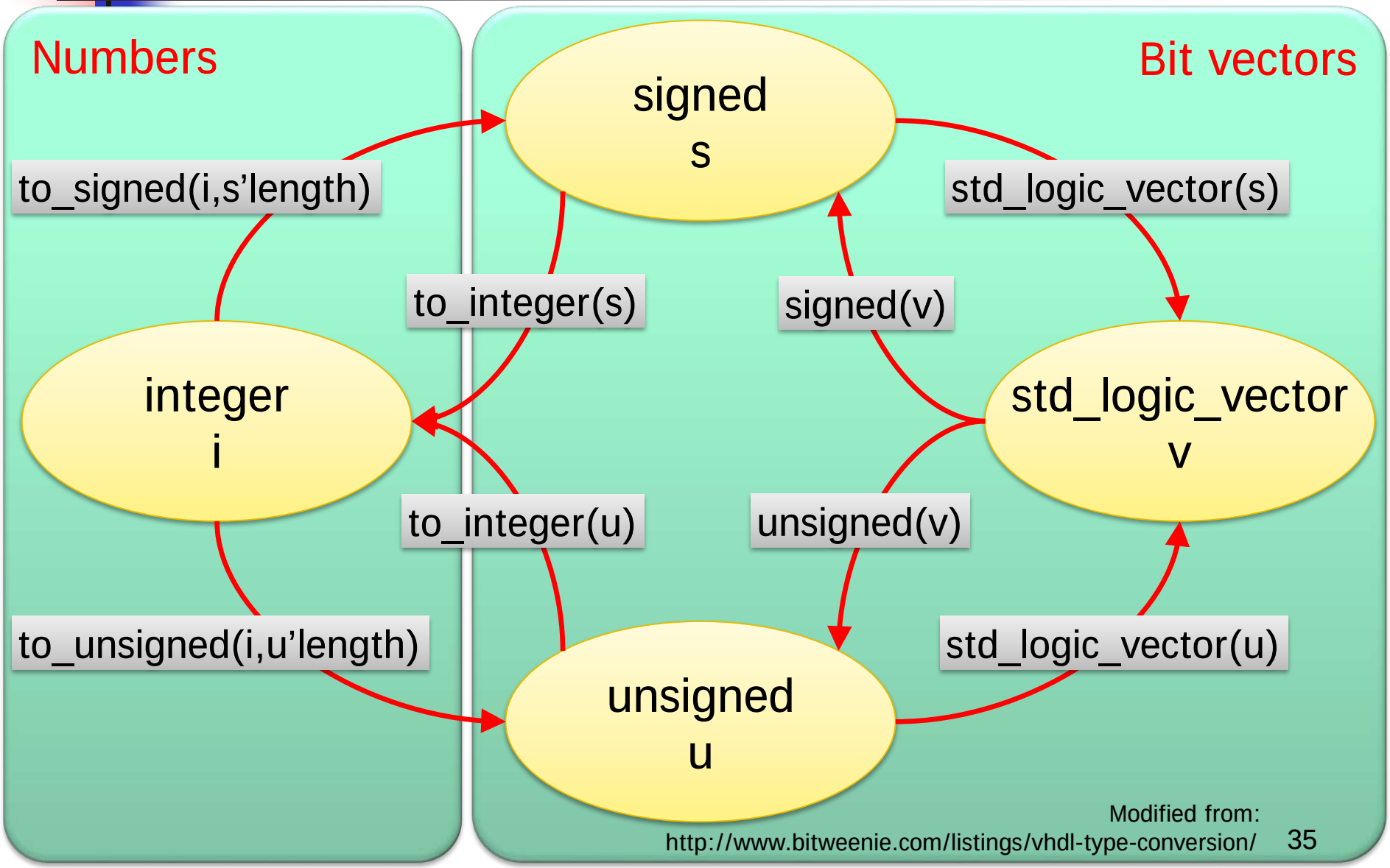
- un/signed <=> integer

```
unsignd <= to_unsigned(int, unsignd'length)
signd   <= to_signed(int,   signd'length)
```

Need width for conversion

```
int     <= to_integer(unsignd)
int     <= to_integer(signd)
```

Conversions



Modified from:
http://www.bitweenie.com/listings/vhdl-type-conversion/