ECE231: Introductory Electronics

Lab #5

MOSFET & BJT Characteristics

Version: 1.4

The Edward S. Rogers Sr.

Department of Electrical and Computer Engineering

University of Toronto

INTRODUCTION

The objective of this experiment is to explore basic MOSFET & Bipolar Junction Transistor (BJT) properties and applications, including I-V characteristics, amplifiers and other practical circuits.

Goals of this experiment

1. Measure the I-V characteristics of the MOSFET & BJT.
2. Compare and contrast the I-V characteristics of MOSFET vs. BJT.
3. Correlate measured results with those produced using SPICE simulation.
4. Analyze a basic MOSFET circuit implementing digital logic.

Lab Preparations

The ALD1101 NMOS and ALD1102 PMOS transistors are not included as part of the Multisim standard component libraries. In order to run simulations for the circuits in the preparation exercises, custom Multisim components that accurately model these transistors are required. A custom component for each transistor has been prepared based on SPICE models provided by the component manufacturer. Follow the steps below in order to use these custom components in your simulations:

1. Download the correct file for your version of Multisim (either .ms12 or .ms13). These files should be provided by your course instructor.
2. Open this file, select the required component, and copy it (take note of the pin names).
3. Paste the component into the desired Multisim file. Be sure to wire the pins correctly.

Preparation Exercises (9 pts)

PE1. Using the ALD1101 NMOS transistor obtained using the above steps, create a circuit with two DC power supplies for evaluating the transistor I-V characteristics. Connect one DC supply between the MOSFET's drain and source to set v_{DS}, connect the second DC supply between the MOSFET's gate and source to set v_{GS}, and connect the MOSFET's source terminal to ground. In order to observe the drain current, i_D, you need to add a "measurement probe" (look on the right-side tool bar for the little yellow bubble symbol or go to Place→Probe→Current) on the wire connected to the drain, making sure it points into the drain.

Use 'Simulate→Analyses→DC sweep', set v_{DS} as Source 1 and v_{GS} as Source 2. Set v_{DS} to sweep from 0-5 V in increments of 0.01 V and set v_{GS} to sweep from 0-5 V in increments of 1 V. For the output, select the current probe that you placed at the drain. This simulation allows you to construct the i_D versus v_{DS} curve for various values of v_{GS}. Identify the regions of operation (i.e. cut-off, triode, saturation). What is the approximate threshold voltage? Do your results match with the component datasheet? You need to list the simulation values and datasheet values to make comparison.

PE2. Using the ALD1101 NMOS and ALD1102 PMOS transistors, construct the circuit in Fig. 13 with only V_{in}, Q_2, and R_{P2_Load}. Ignore the other components for now. Set R_{P2_Load} = 0.5 kΩ and use a 10V DC power supply for V_{DD1}.

a) First, use a DC power supply for V_{in}. Use 'Simulate→Analyses→DC Sweep' and set V_{in} as Source 1 to sweep from 0-10 V in increments of 0.01 V. Display the voltage at the drain of the transistor. This enables you to plot the voltage transfer characteristic of this simple amplifier circuit. Is this amplifier inverting or non-inverting?

b) Remove R_{P2_Load} and add Q_3 and C_3 as shown in Fig. 13 (as if SW_{P2_1} and SW_{P2_4} are closed and all other switches are open). Note, R_7 is not needed since it is strictly just a pull-up resistor that turns off Q_3 when SW_{P2_1} is open. Use a pulse voltage for V_{in}. Set the pulse voltage from 0 to 10 V at a frequency of 2 kHz (you cannot set frequency directly, but you can set "Pulse width" and "Period"). Use 'Simulate→Analyses→Parameter sweep' and set up the simulation to sweep the capacitance of C_3. Set "Sweep variation type" as "List" and enter the following list of values: 1e-8, 5e-8, 1e-7, 2e-7, 5e-7, 1e-6. Set "Analysis to sweep" as "Transient Analysis". Click 'Edit Analysis' and change the settings to run the simulation for 3 ms with a maximum time step of 1e-005. (Increase maximum time step if your computer is running too slowly). Output the same voltage as part (i) and produce a graph showing the effect of added capacitive load. What is the largest capacitance this circuit can handle, before the output no longer reaches 10 V during each period of the output signal?

Background

The MOSFET is a versatile four terminal non-linear device that can be used either as a voltage-controlled resistor in the triode region, or as a voltage-controlled current source in the saturation region. The MOSFET is mainly responsible for the microelectronics revolution that has facilitated the rapid progress in the electronic devices that we use every day. The schematic symbol and physical structure of an n-channel MOSFET are shown in Fig. 1.

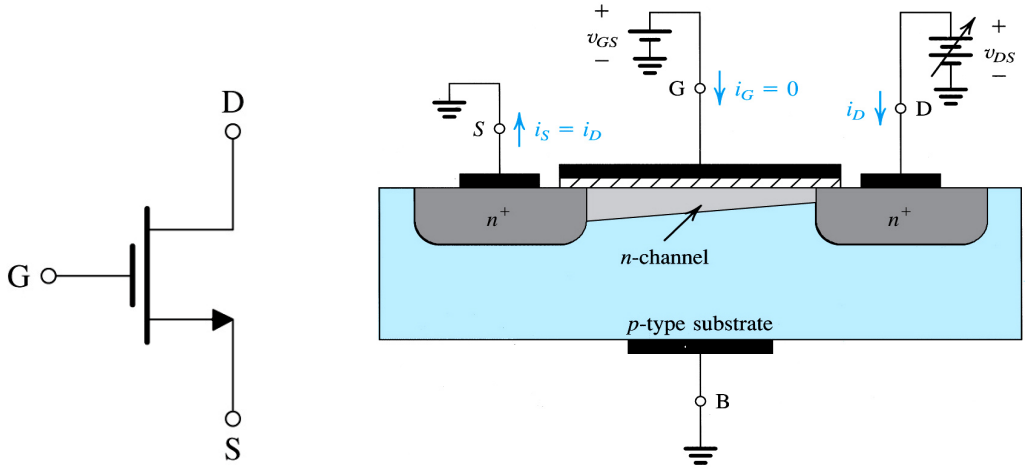


Fig. 1: (a) N-channel MOSFET symbol; (b) Physical structure of an n-channel MOSFET.

The MOSFETs used in this lab are the ALD1101 (NMOS) and ALD1102 (PMOS) parts from Advanced Linear Devices. The datasheets for these two components will be provided to you by your course instructor. The most important MOSFET parameters are listed in Table 1 and Table 2. Note that the parameters W/L and k'n, k'p are not provided, however kn and kp can be derived from the datasheet. When implementing circuits with discrete transistors (i.e.: where the chips are already fabricated), the W/L cannot be changed, however an integer number of identical transistors, say M, can be connected in parallel. This has the same effect as multiplying W/L by the factor M.

Table 1: Important parameters of the ALD1101 N-Channel MOSFET

Parameter	Min	Typ.	Max	Unit	Condition
Threshold voltage, V_{tn}	0.4	0.7	1	V	I_{DS} = 10 µA, $V_{GS} = V_{DS}$
Drain current	25	40		mA	$V_{GS} = V_{DS}$ =5 V
Transconductance, g_m	5	10		mA/V	V_{DS} = 5 V, I_{DS} = 10 mA
Drain-to-source On-resistance (triode), $R_{ds,on}$		50	75	Ω	V_{DS} = 0.1 V, V_{GS} =5 V
Drain-to-source Breakdown Voltage, BV_{DSS}	12			V	I_{DS} = 10 µA, V_{GS} =0 V
Gate leakage current		1	50	pA	V_{DS} = 0, V_{GS} = 12 V

Table 2: Important parameters of the ALD1102 P-Channel MOSFET

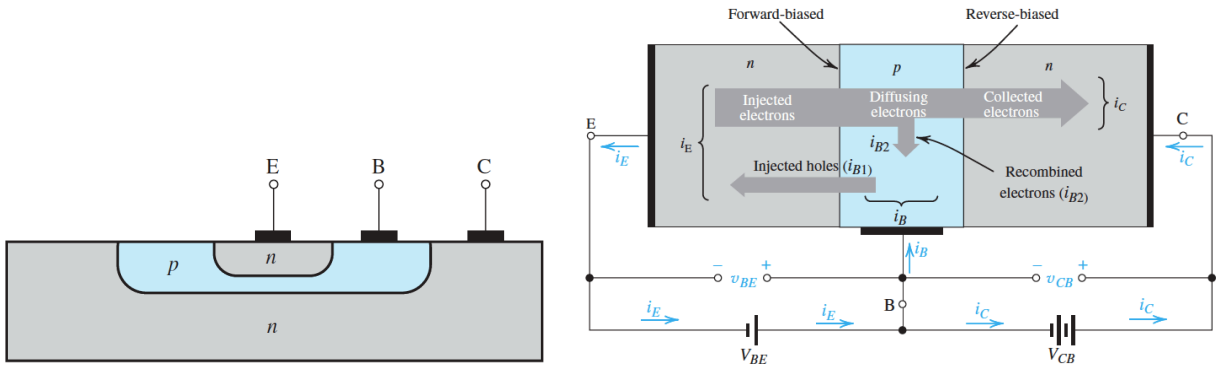
Parameter	Min	Typ.	Max	Unit	Condition
Threshold voltage, Vtp	-0.4	-0.7	-1.2	V	ISD = 10 µA, VSG = VSD
Drain current	-8	-16		mA	VSG =VSD = 5 V
Transconductance, gm	2	4		mA/V	VSD = 5 V, ISD = 10 mA
Drain-to-source On-resistance (triode), Rds,on		180	270	Ω	VSD = 0.1 V, VSG = 5 V
Drain-to-source Breakdown Voltage, BVDSS	-12			V	ISD = 10 µA, VSG = 0 V
Gate leakage current		1	50	pA	VSD = 0, VSG = 12 V

The bipolar junction transistor (BJT), as shown in Fig. 2, is a versatile three-terminal semiconductor device widely used in high precision analog signal processing circuits.

The BJTs used in this experiment are the BC337 (NPN) transistors from ON Semiconductor. The datasheets for these components will be provided by your course instructor. The most relevant properties of the BC337 are listed in Table 3. Notice that β is specified as DC Current Gain, h_{FE}.

While the operation of MOSFETs and BJTs has many similarities, the two transistors also have important differences. The key characteristics of MOSFETs and BJTs are listed in Table 4.

The MOSFET and BJT small-signal models are very similar, as shown in Fig. 3, with the important distinction that the BJT has a non-zero base current and thus a finite input resistance looking into the base, rπ. Note that the relationship between the small-signal parameters and the DC bias conditions is different for the two transistor types.



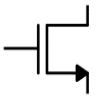
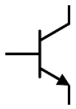
(a) (b)

Fig. 2: (a) Cross-section and (b) current flow in an NPN transistor operating in the active mode.

Table 3: Important parameters the BC337 NPN BJT

Parameter	Min	Typ	Max	Unit	Condition
DC Current Gain, h_{FE}	100	-	250	-	V_{CE} = 1.0 V, I_C = 100 mA
Collector-Emitter Saturation Voltage, $V_{CE(SAT)}$	-	-	0.7	V	I_C = 500 mA, I_B = 50 mA
Base-Emitter Voltage, V_{BE}	-	-	1.2	V	V_{CE} = 1.0 V, I_C = 300 mA
Collector-Base Breakdown Voltage, BV_{CBO}	50	-	-	V	I_C = 100 µA
Collector-Emitter Breakdown Voltage, BV_{CEO}	45	-	-	V	I_C = 10 mA
Emitter-Base Breakdown Voltage, BV_{EBO}	5	-	-	V	I_C = 100 µA

Table 4: Comparison of MOSFET and BJT

Characteristic	MOSFET 	BJT 
Carriers	Unipolar (electrons in NMOS, holes in PMOS)	Bipolar (holes + electrons)
Number of terminals	4	3
Symmetric fabrication	Yes	No
Dominant I-V characteristic	$i_D = \frac{1}{2}k'_n \frac{W}{L}(v_{GS} - V_t)^2$	$i_C = I_S e^{v_{BE}/V_T}$
Relative minimum size	Small (easily scalable)	Large
Most common device	NMOS	NPN
Complimentary device	PMOS	PNP
g_m	Proportional to $\sqrt{I_D}$	Proportional to I_C
Region for operating as a switch	Triode	Saturation
Region for operating as an amplifier	Saturation	Active
Relative matching of two transistors	Poor	Excellent
Input resistance	Infinite	r_π (proportional to β)
Cause of finite output resistance	Channel length modulation	Base width modulation
Voltage drop when used as a switch	$i_D \times r_{DS}$ (in triode)	$V_{CEoff} + i_C \times R_{CEsat}$ or V_{CEsat}

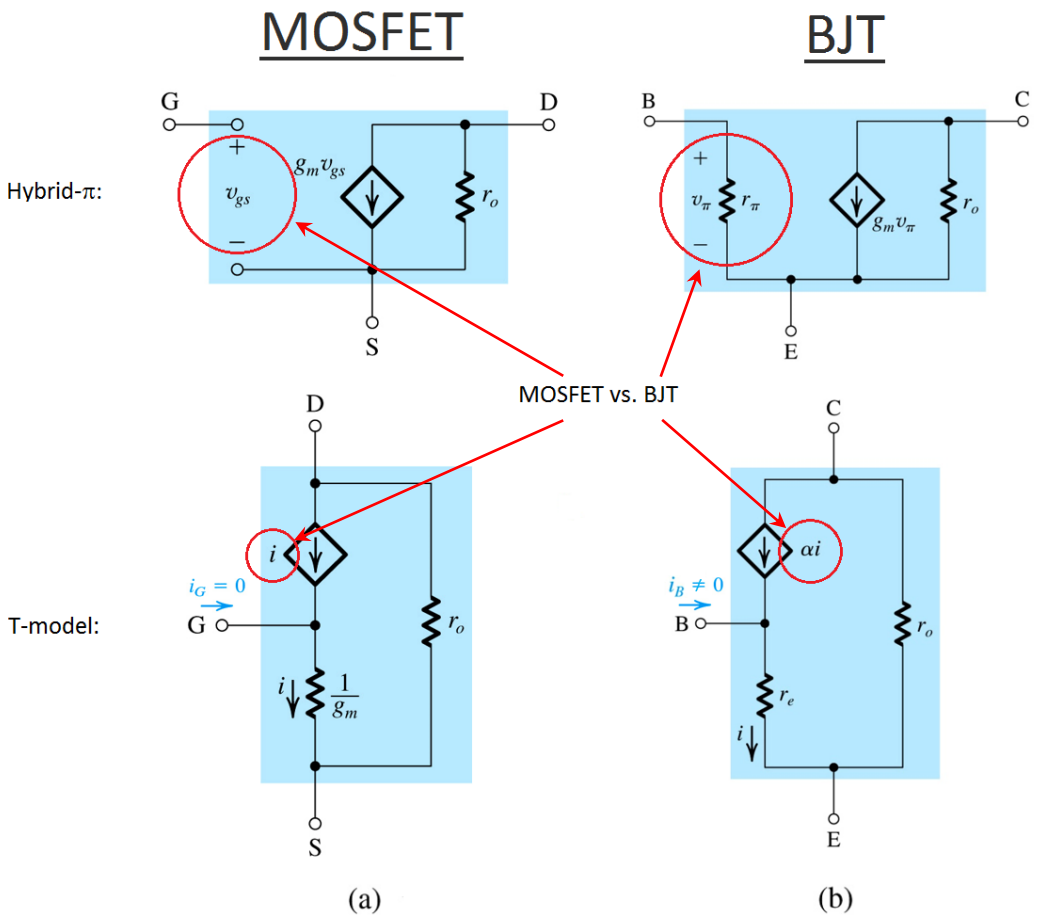


Fig. 3: (a) MOSFET and (b) BJT small-signal models.

Part 1 – MOSFET & BJT I-V Characteristics

A differential amplifier circuit is shown in Fig. 4. The configurable circuit shown in Fig. 5 is used to measure the I-V characteristics of a single NMOS transistor, Q_1. A difference amplifier with a gain, A, of 2 V/V is used to measure the current in the MOSFET by measuring the current through a resistor, $R_{current}$. The output of the difference amplifier, $V_{current}$, is proportional to the drain-to-source current, i_{DS}, according to the relationship:

$$V_{current} = AR_{current} i_{DS} \tag{1}$$

With $A = 2$ and $R_{current} = 100\ \Omega$, this relationship can be simplified to:

$$V_{current} = Ki_{DS} \tag{2}$$

Where $K = 200$. When measuring i_D versus v_{GS}, SW_{P1_1} is OFF while the complimentary switch is ON. In this configuration, the transistor is diode-connected and $v_{DS} = v_{GS}$. The ideal and measured i_D versus v_{GS} characteristics of the NMOS are shown in Fig. 6. When measuring i_{DS} versus v_{DS}, switch SW_{P1_1} is ON and subsequently the complimentary switch will be turned **OFF**. In this case the gate-to-source voltage, v_{GS}, is set using *ANALOG*, while the drain-to-source voltage, v_{DS}, is indirectly set using the input, V_{in}. The ideal and measured i_D versus v_{GS} characteristics of the NMOS are shown in Fig. 7. Note that on the breadboard, the switches will be implemented with wires.

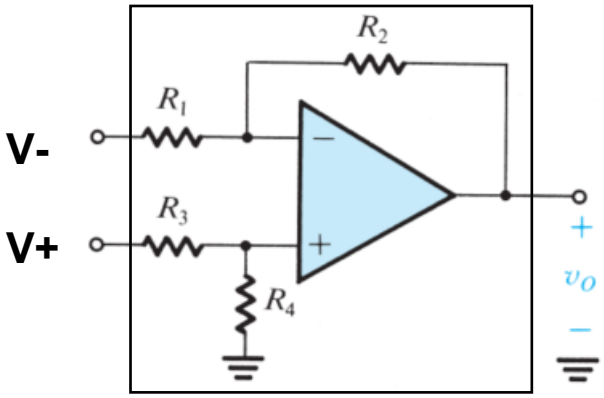


Fig. 4: Differential Amplifier.

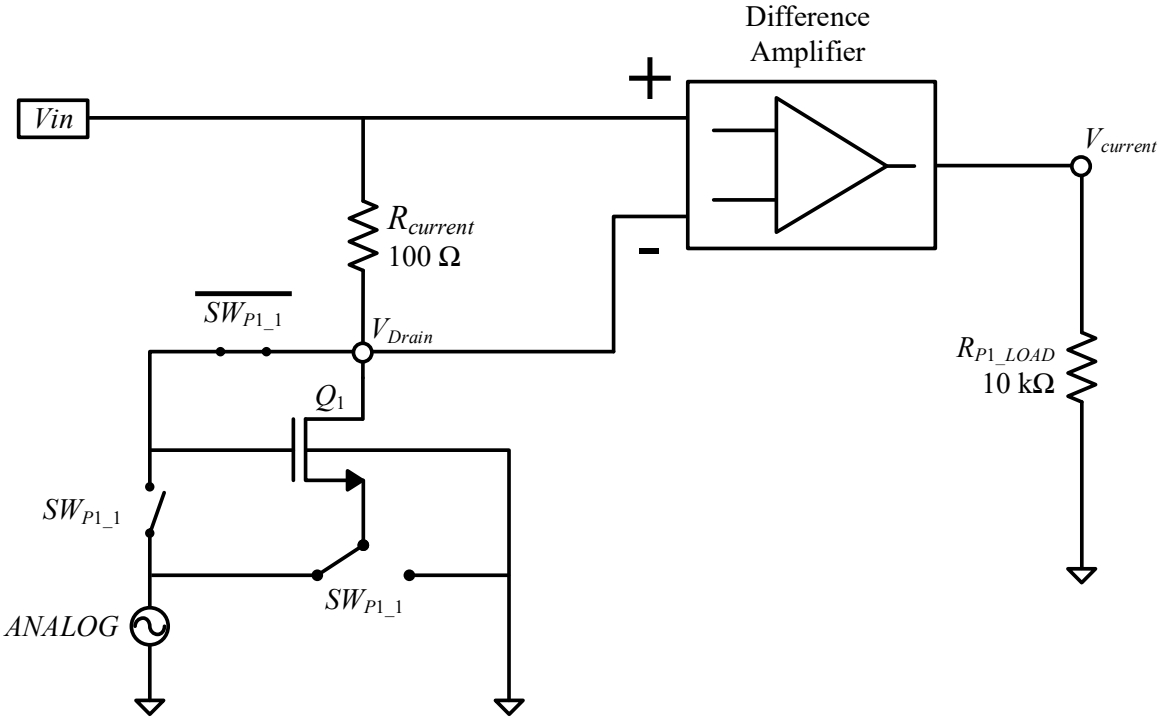
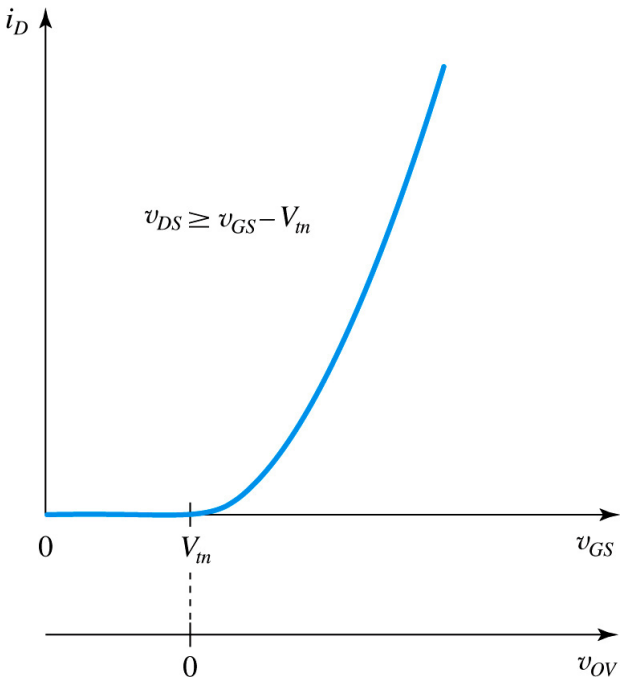
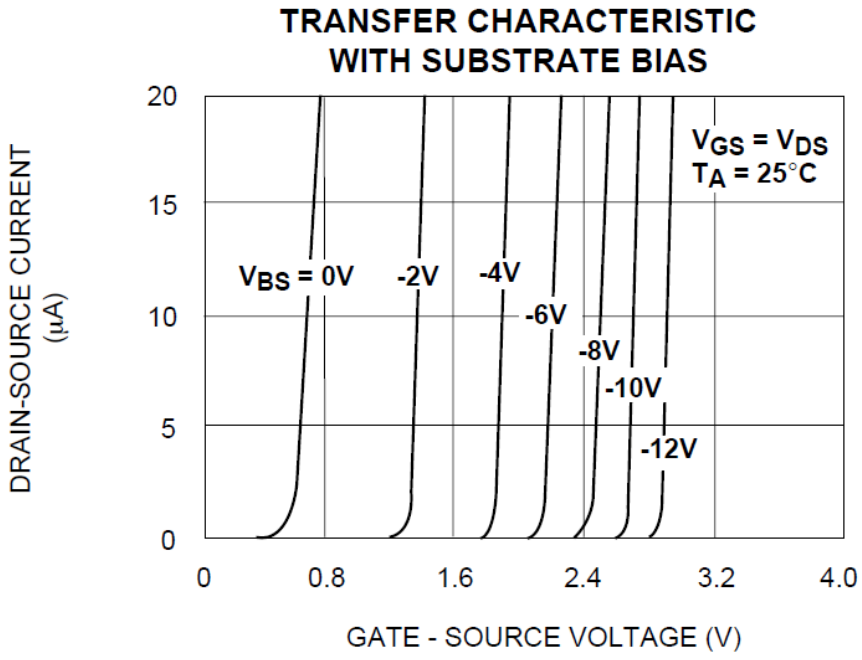


Fig. 5: I-V characteristic measurement circuit.

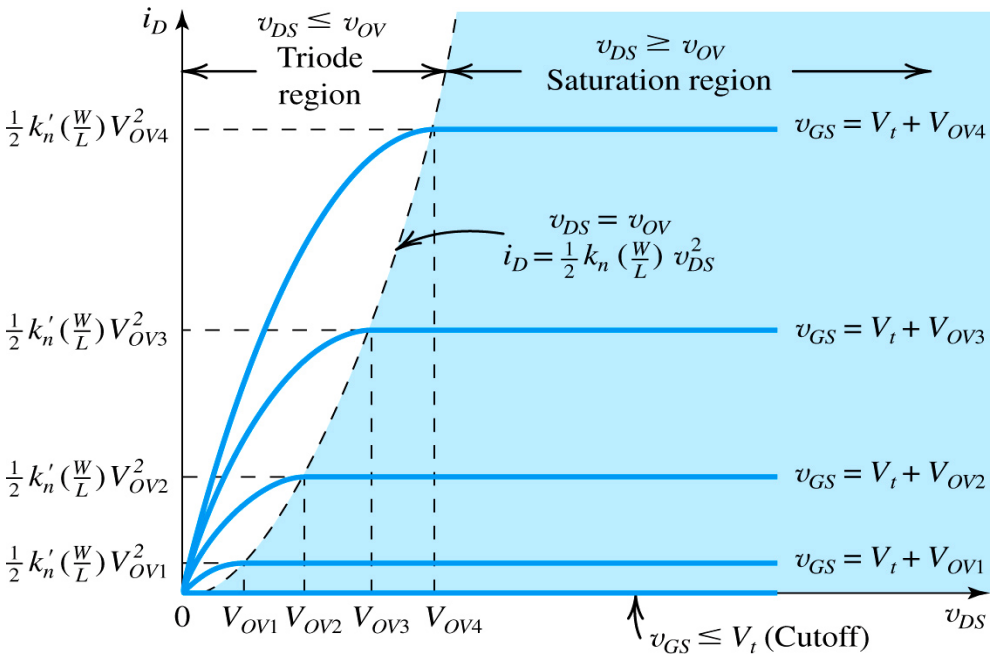


(a)

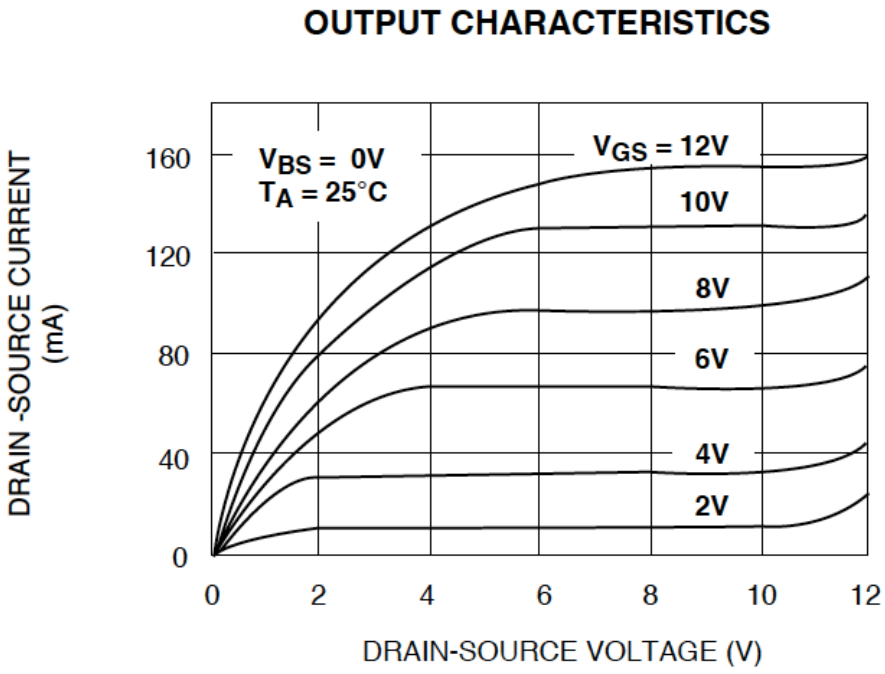


(b)

Fig. 6: (a) Ideal and (b) measured i_{DS} versus v_{GS} characteristic of an NMOS ALD1101 transistor. Notice that the threshold voltage is a function of the body-to-source voltage, V_{BS}, which is known as the "body effect".



(a)



(b)

Fig. 7: (a) Ideal and (b) measured i_D versus v_{DS} characteristics of an NMOS ALD1101 transistor.

The I-V characteristics of a BJT have many similarities to those of a MOSFET, but there are several important differences to note. The ideal BJT i_C *vs.* v_{BE} characteristics are compared to the ideal MOSFET i_D *vs.* v_{GS} characteristics in Fig. 8. A comparison between the ideal BJT i_C *vs.* v_{CE} characteristics and the ideal MOSFET i_D *vs.* v_{DS} characteristics is shown in Fig. 9. The measured BJT i_C *vs.* v_{CE} characteristic from the datasheet is shown in Fig. 10.

One particularly desirable feature of BJTs for amplifier design is that the signal-signal transconductance, g_m, is proportional to the collector current, I_C, while the MOSFET's transconductance is proportional to $\sqrt{I_D}$. Unlike MOSFETs, which ideally have zero gate current due to the oxide capacitance, BJTs have a finite base current, $I_B = I_C/\beta$, which makes solving both DC and small-signal BJT circuits considerably more complex than MOSFET circuits. When used as a switch in saturation mode, BJTs have a voltage offset of approximately 0.2 V, as shown in Fig. 8(b), while MOSFETs have a purely linear characteristic in the triode region, as shown in Fig. 8(a).

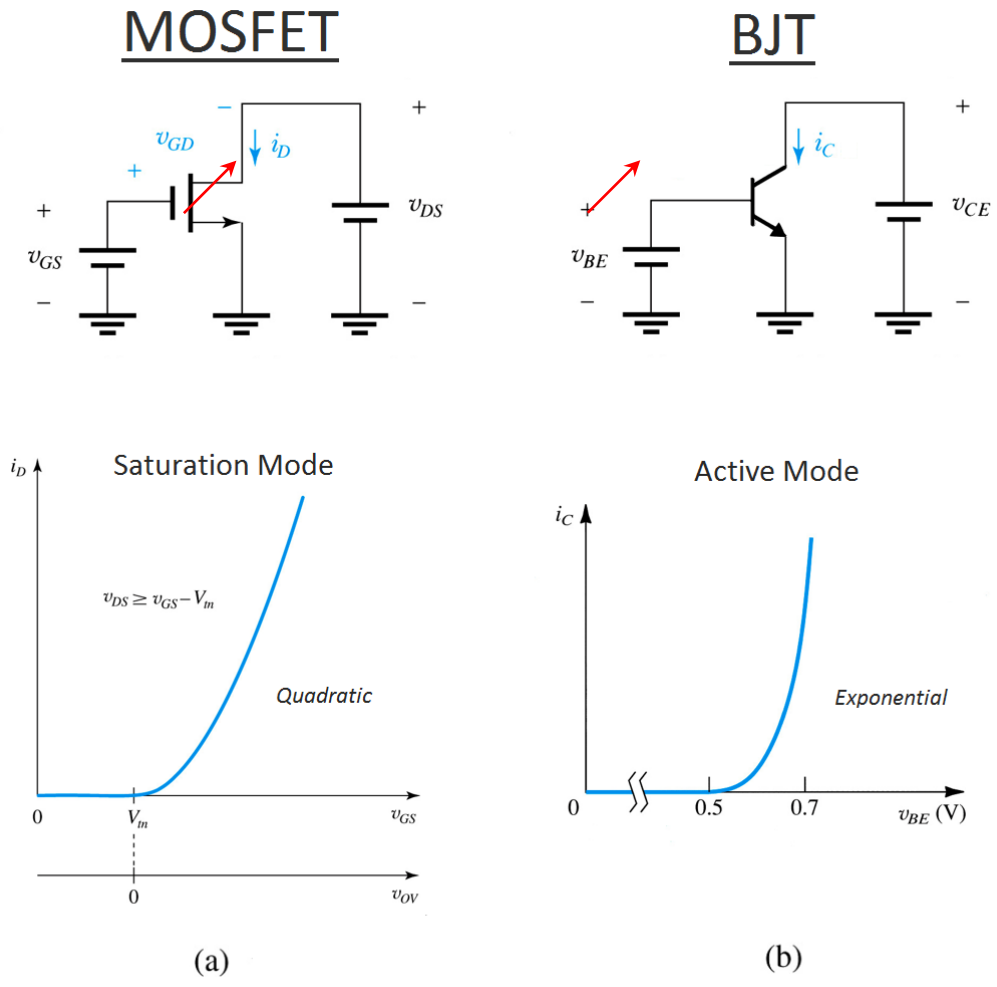


Fig. 8: (a) MOSFET i_D versus v_{GS} characteristic. (b) BJT i_C versus v_{BE} characteristic.

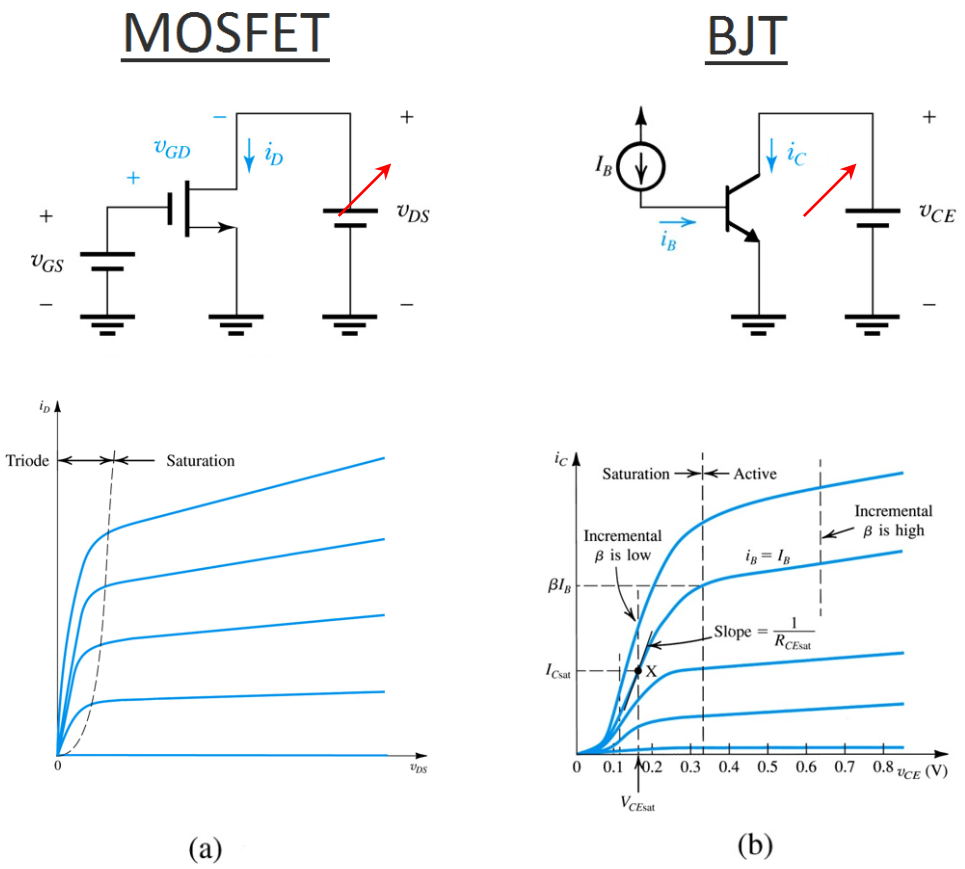


Fig. 9: (a) MOSFET i_D versus v_{DS} characteristic. (b) BJT i_C versus v_{CE} characteristic. Note the distinctly different shape of the curves in the triode (MOSFET) and saturation region (BJT), where the transistors are used as a switch.

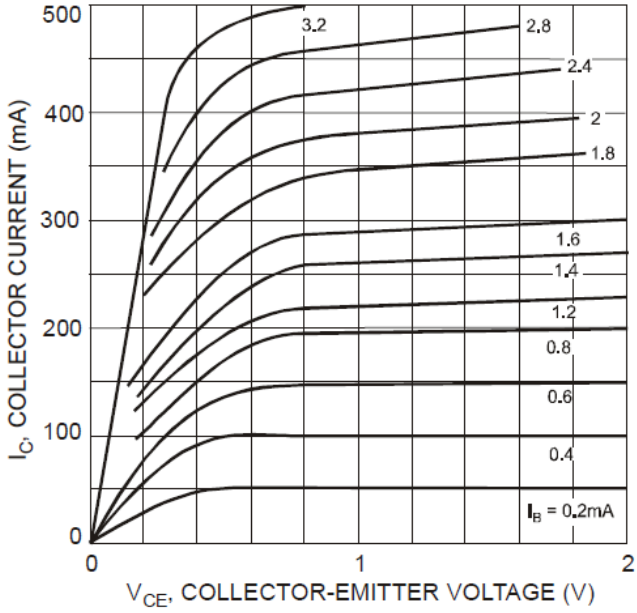


Fig. 10: Measured i_C vs v_{CE} characteristic for the BC817-16

The circuit shown in Fig. 11 is used to measure and compare the I-V characteristics of a BJT. The difference amplifier with a gain, A, are used to measure the transistor currents:

$$V_{CURRENT\_BJT} = AR_{current}i_{C1} = Ki_{C1}, \tag{3}$$

where A = 2 V/V, $R_{current}$ = 100 Ω, K = 200, and i_{C1} is the collector current of the BJT, Q_1. The voltage V_{ANALOG} is used to set the base current of Q_1:

$$i_{B1} = \frac{V_{ANALOG} - v_{BE}}{R_b}, \tag{4}$$

where $v_{BE} \approx 0.7$ V.

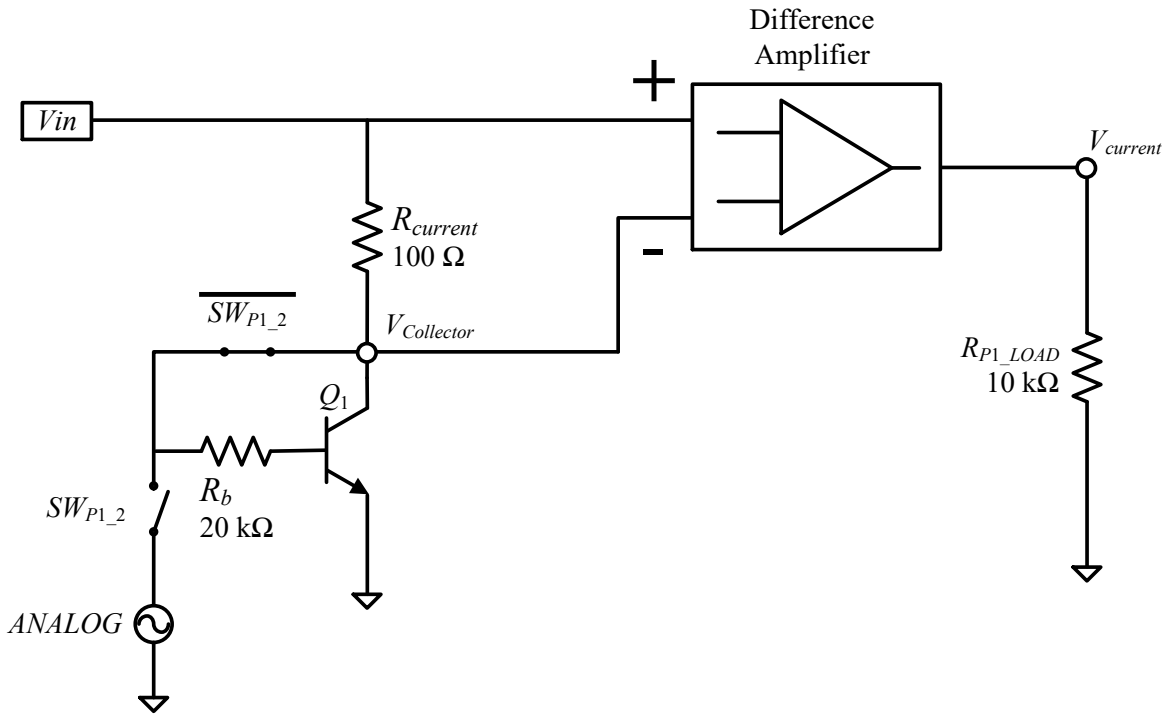


Fig. 11: I-V characteristic measurement circuit.

Part 2 – MOSFET Voltage Transfer Characteristic

Consider the simple circuit shown in Fig. 12(a), whose Voltage Transfer Characteristic (VTC) is shown in Fig. 12(b). The VTC can be explained as follows:

- **Cut-off:** For $v_{GS} < V_t$, the transistor is off and $v_O = V_{DD}$.
- **Saturation**: As v_{GS} is increased beyond the threshold voltage, the MOSFET is in the saturation region and behaves like a voltage-controlled-current-source and $v_O = V_{DD} - R_D \cdot i_D$.
- **Triode:** As v_{GS} is further increased, v_{DS} is reduces below V_{GS}-V_t, the MOSFET enters the triode region and behaves as a voltage-controlled-resistance, or equivalently, as a non-ideal

switch that is ON. In this region $v_O = V_{DD}\, r_{DS}/(r_{DS}+R_D)$, where r_{DS} is the MOSFET drain-to-source resistance and depends on v_{GS}.

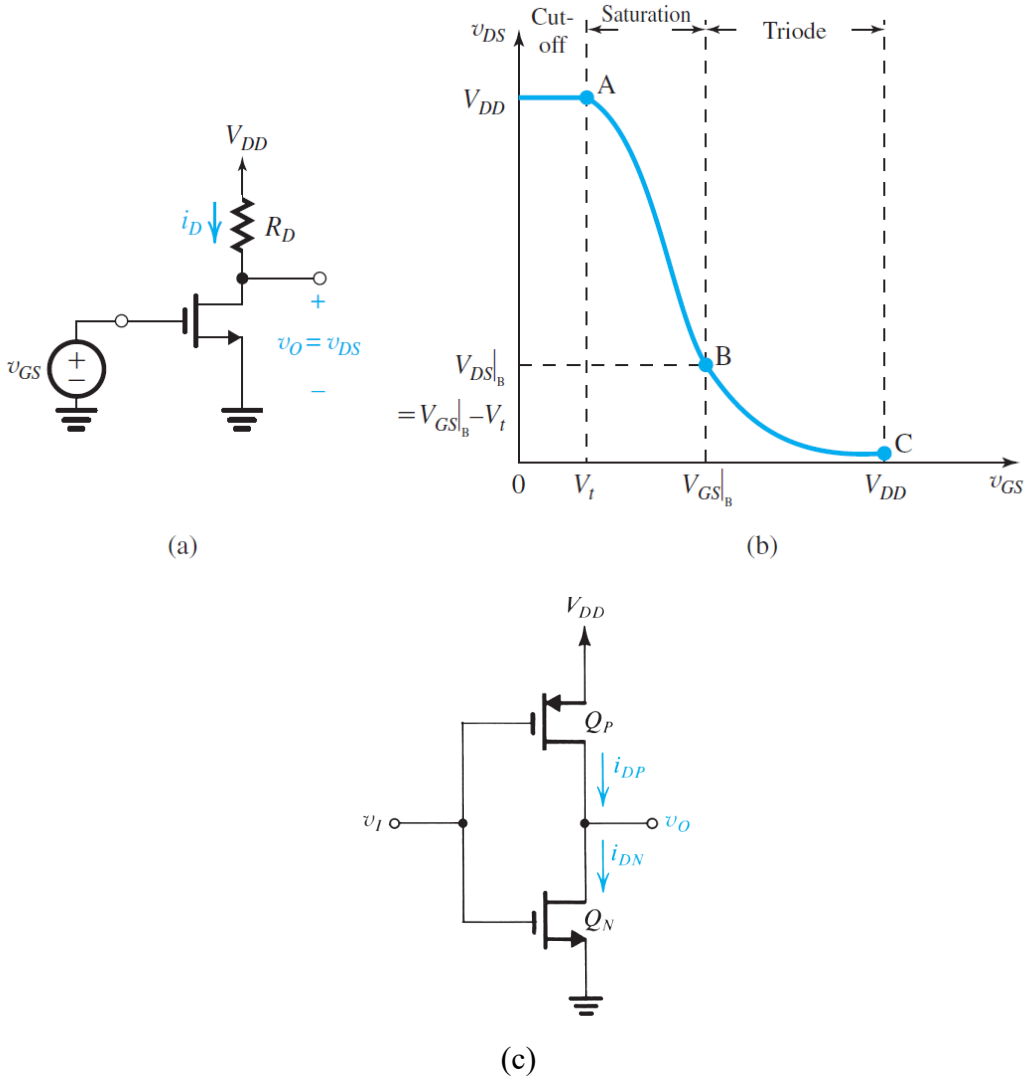


Fig. 12: (a) A simple MOSFET amplifier and (b) the corresponding voltage transfer characteristic. (c) CMOS inverter.

Notice that depending on the application, the circuit in Fig. 12(a) can either be used as an amplifier, or a logic inverter as explained below.

▸ Operation as a Common-Source Amplifier

If biased in the saturation region (between points A and B on the VTC) where the small-signal gain, $dv_O/dv_{GS} = v_o/v_{gs}$, is large then the circuit can be used as an amplifier, as long as the input is constrained such that the MOSFET stays in saturation.

▸ Operation as a Logic Inverter

The VTC shown in Fig. 12(b) can also be used to implement an inverter. A '0' at the input ($v_{GS} = 0$) causes the output voltage to be a '1' (i.e.: $v_O = V_{DD}$), while a '1' at the input ($v_{GS} = V_{DD}$) causes the output to be a logical '0' ($v_O = V_{DD}\, r_{DS}/(r_{DS}+R_D) \cong 0$ for $r_{DS} << R_D$). The voltage corresponding to a '0' therefore depends on the circuit parameters. Historically the first logic inverters were created in this way, since the complimentary PMOS transistor was not available. Note that if R_D in Fig. 12(a) is replaced by a PMOS transistor to create a CMOS inverter, as shown in Fig. 12(c), the VTC is modified such that the output voltage at point C is zero, since Q_P is in cut-off when the input is V_{DD}. The main advantage of a CMOS inverter is that, unlike the circuit in Fig. 12(a) it draws zero current from the power supply in either the '1' or '0' output states.

The circuit shown in Fig. 13 is used in the lab and can be configured to create the circuits in Figs. 12(a) and 12(c) with different load capacitance (C_3 and C_4) and a programmable effective PMOS *W/L* ratio. Note that closing SW_{P2_2} puts Q_3 and Q_4 in parallel, effectively doubling the *W/L* ratio of Q_P in Fig. 12(c).

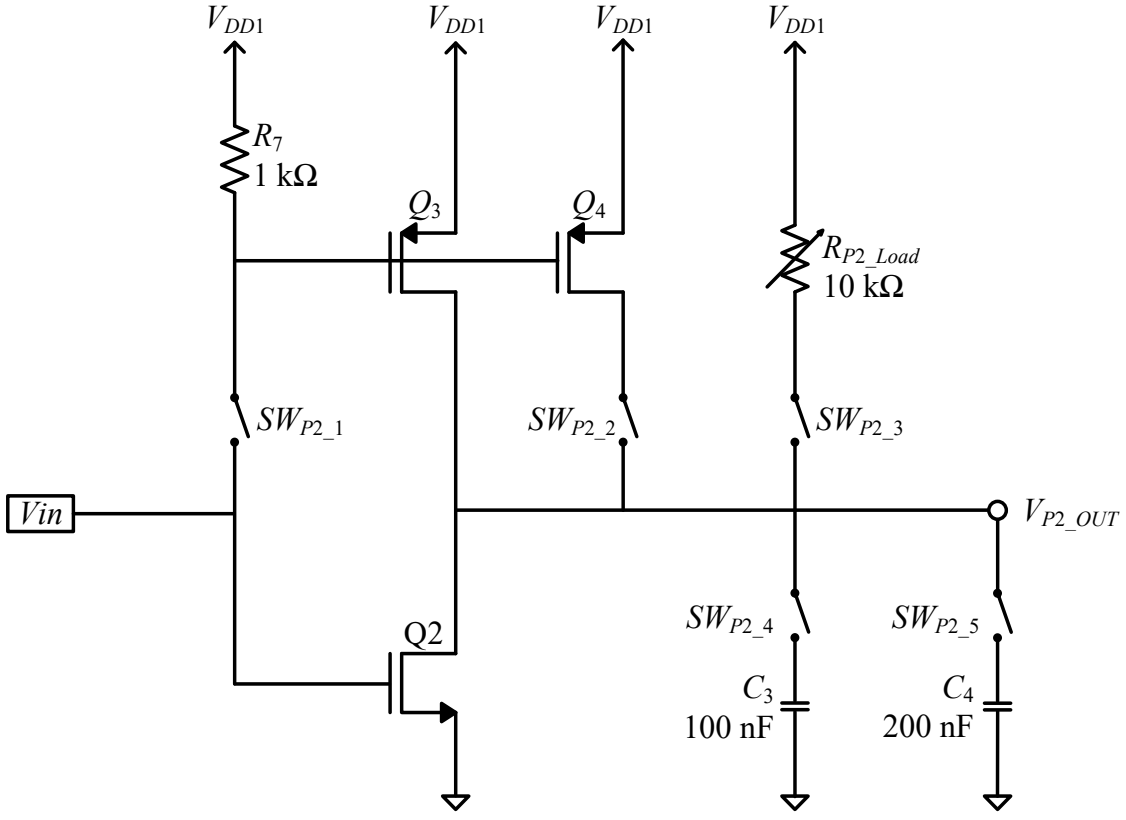


Fig. 13: Voltage transfer characteristic circuit.

Lab Experiments

MOSFET & BJT I-V Characteristics

E1 As shown in Fig. 4, you should set up the Difference Amplifier with a **gain of 5** using MCP6002 op-amp. (Use V_{DD} **= 5 V,** V_{SS} **= 0 V, 1 kΩ and 5.1 kΩ resistors** to build the circuits.)

We will test the functionality of the difference amplifier. Ground the negative terminal of the difference amplifier. Setup the function generator to output V_{in} **as a 0.5** $V_{p\text{-}p}$**, +0.25 V offset, 100 Hz, triangular wave**. Check the signal on scope before connecting it to the positive terminal of the difference amplifier. **Set the DC power supply to 5 V, 0.3 A before turning it on. When you turn on VDD, the current draw should be less than 0.01 A. If you see a large current, please turn off the power supply and check the circuit connection.** The triangular wave at the output should have a gain of 5.

Show your TA before proceeding to the next step!

In this portion of the lab we will use the circuit shown in Fig. 14 to observe the I-V curves of an NMOS transistor by using the oscilloscope in XY mode.

Please follow the following procedures to avoid damaging the components.

E2 You will first perform the I_D *vs*. V_{GS} characterization. Config the circuit as shown in Fig. 14. Setup the function generator to output V_{in} **as a 8** $V_{p\text{-}p}$**, +4 V offset, 100 Hz, triangular wave**. Do not connect V_{in} until you finish the circuit connection and supply 5V to the amplifiers. Use CH1 to probe the voltage V_{drain} at the drain of Q1 ($V_{DS} = V_{GS}$ in this mode). Use CH2 to probe the voltage $V_{current}$ at the output of the difference amplifier ($V_{current} = 100 \cdot i_{DS}$). Set up the oscilloscope in XY mode with CH1 on the x-axis and CH2 on the y-axis; this should resemble Fig. 8(a). Measure the approximate threshold voltage and compare it to the datasheet value. Measure the current in saturation for $V_{GS} = V_{DS} = 5$ V and compare to the value in Table 1. Measure the approximate ΔV_{GS} for I_D increasing from 10 mA to 30 mA (refer to eq. (2)) and calculate $g_m = \frac{\Delta I_D}{\Delta V_{GS}}$.

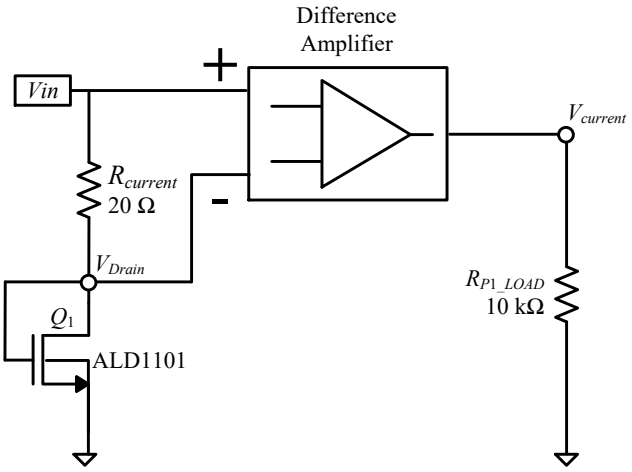


Fig. 14: MOSFET I_D *vs.* V_{GS} characteristic measurement circuit.

E3 Now adjust the circuit as shown in Fig. 15 to characterize I_D versus V_{DS}. Set *ANALOG* to a DC power supply. This connects the DC power supply to the gate of Q_1 in order to independently control V_{GS}. **Set the DC power supply (*ANALOG*) to 0 V before connecting to the MOSFET to prevent damaging the MOSFET.**

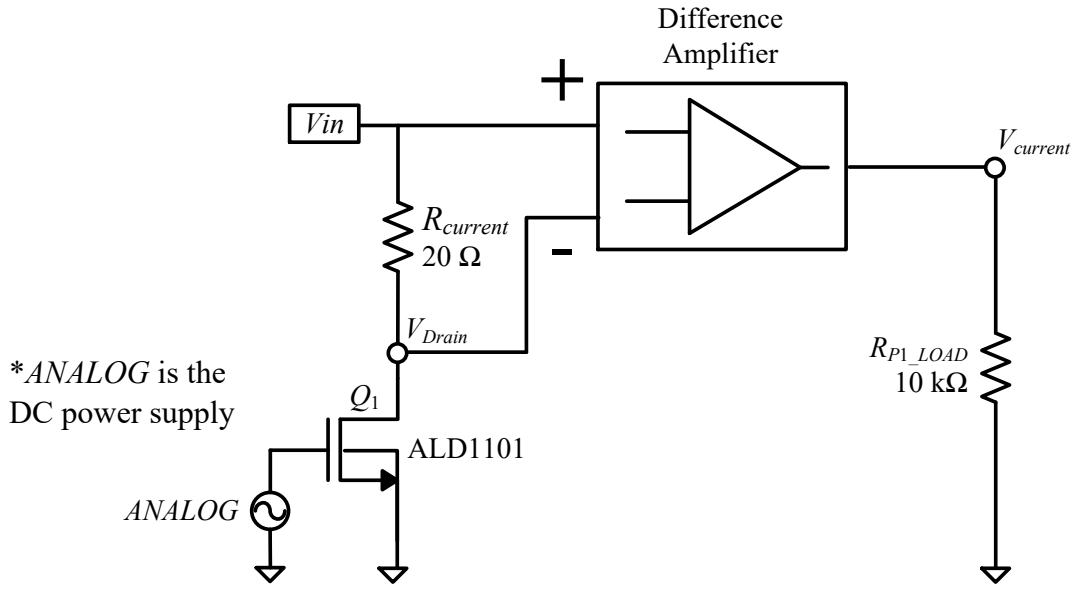


Fig. 15: MOSFET I_D *vs.* V_{DS} characteristic measurement circuit.

E4 Keep the oscilloscope in XY mode, with CH1 and CH2 probing the same nodes as part E2. With 0 V at the gate, the transistor is in cutoff and you will see zero current for all values of V_{DS}. **Slowly** increase the *ANALOG* (DC power supply) voltage gradually until you pass the threshold voltage that you measured in previous steps; the resulting curve should resemble one of the lower curves in Fig. 7. **Keep increasing the *ANALOG* up to 5 V**. Is there any observable channel length modulation?

E5 Set the *ANALOG* to 0 V and increase the *ANALOG* in increments of 1 V, until you reach 5 V. Sketch the family of curves in your lab book and label the three regions of operation.

E6 Set the circuit to as shown in Fig. 16 to characterize 'I_C vs. V_{BE}'. Setup the function generator to output $\boldsymbol{V_{in}}$ **as a 5** $\boldsymbol{V_{p\text{-}p}}$**, +2.5 V offset, 100 Hz, triangular wave**. Set up the unity gain input butter using the second amplifier on MCP6002 first. Since the BJT is diode-connected, $V_{BE} = V_{CE}$. Use CH1 on the oscilloscope to measure V_{BE} by measuring $V_{Collector}$. Use CH2 to measure I_C by using the node $V_{CURRENT}$. Set the oscilloscope in XY mode and compare the curve to Fig. 8(b). Measure the approximate ΔV_{BE} for I_C increasing from 10 mA to ~25 mA (refer to eq. (1)) and calculate $g_m = \Delta I_C/\Delta V_{BE}$. Estimate I_S by using the "Dominant I-V characteristic" equation for a BJT listed in Table 4. Compare the calculated values of g_m for the BJT and the MOSFET.

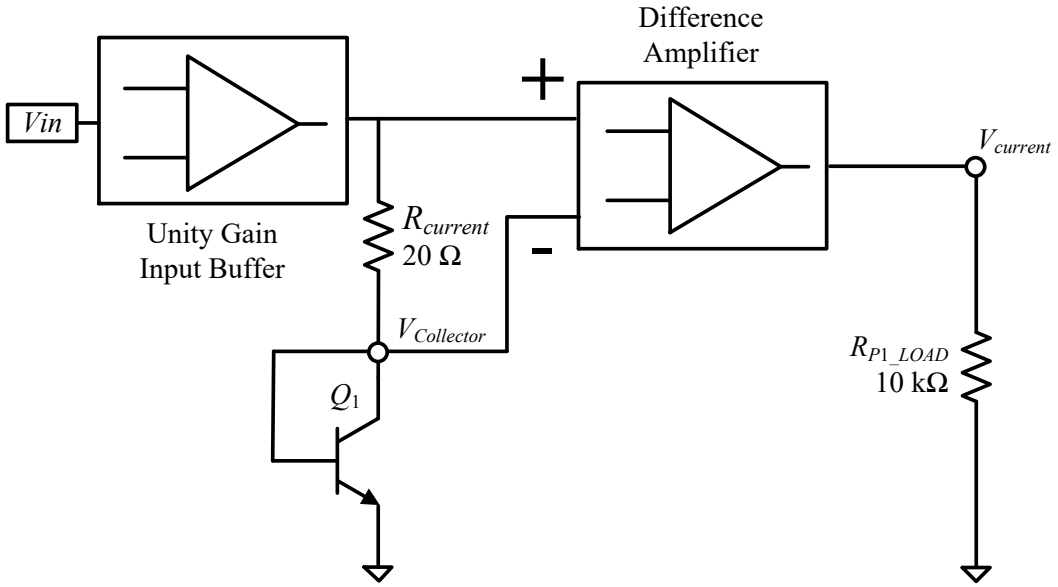


Fig. 16: BJT I_C *vs.* V_{BE} characteristic measurement circuit.

E7 Setup circuit as below**, set the** $\boldsymbol{V_{in}}$ **to 0 V before power on**. Now the V_{in} can be used to control I_B for the BJT. **Increase the *ANALOG* by 0.5 V increments up to 2.5 V.** Compare the family of curves to Fig. 10. Set the *ANALOG* to 0 V and increase the *ANALOG* in 0.5 V increments up to 2.5 V. How is the boundary between the saturation and active regions of a BJT different from the boundary between the triode and saturation regions of a MOSFET?

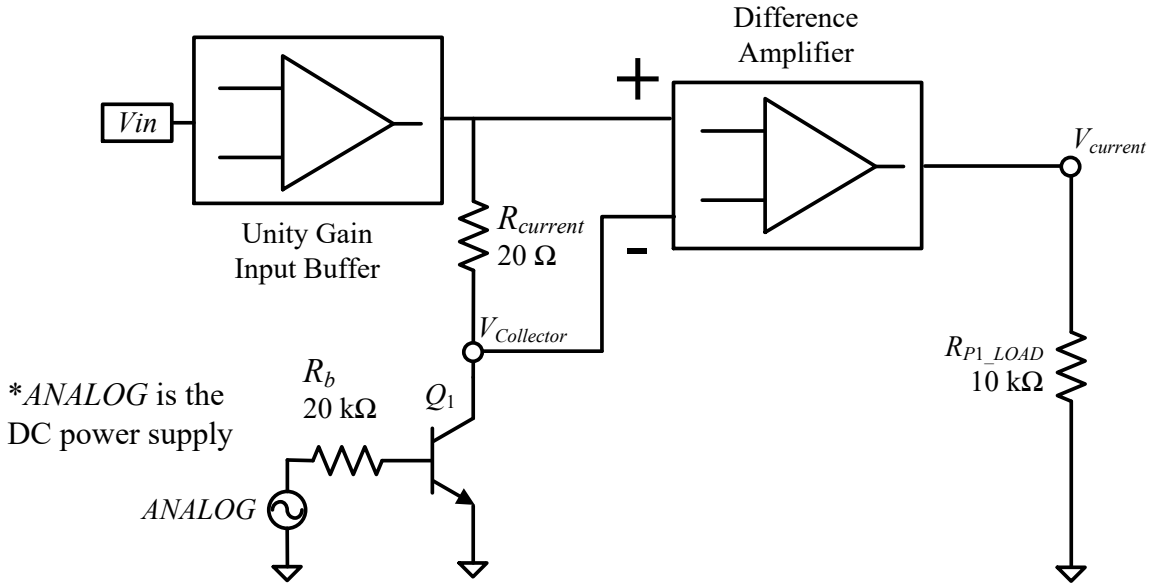


Fig. 17: BJT I_C *vs.* V_{CE} characteristic measurement circuit.

E8 Use the scaling/positioning knobs for CH1 to zoom in horizontally so that the saturation region 0 V ≤ V_{CE} ≤ 0.5 V is clearly visible (i.e. it should occupy the majority of the oscilloscope screen). Set the *ANALOG* to 3 V. How does this compare to the MOSFET triode region?

Bonus – MOSFET Voltage Transfer Characteristic

In this portion of the lab we will investigate the concept of a voltage transfer characteristic and the properties of two types of inverters.

E9 Setup the circuit as shown in Fig. 18. Set R_{load_2} to 0 Ω. Adjust the function generator and send 0-5 V, 100 Hz triangle wave with 2.5 V DC bias to V_{in}.

E10 Use CH1 to measure V_{in} and use CH2 to measure V_{P2_OUT}. Configure the oscilloscope in XY mode and sketch the observed voltage transfer characteristic in your lab book. On the curve, label the regions of operation of the NMOS transistor. Compare your sketch to Fig. 12. (b) and note the voltage at point 'C'. Increase the value of R_{load_2} gradually up to 10 kΩ. How does increased drain resistance affect the small-signal gain of the circuit while the transistor is in saturation? Use the scale (volts per division) on the oscilloscope to determine the approximate maximum gain of this circuit.

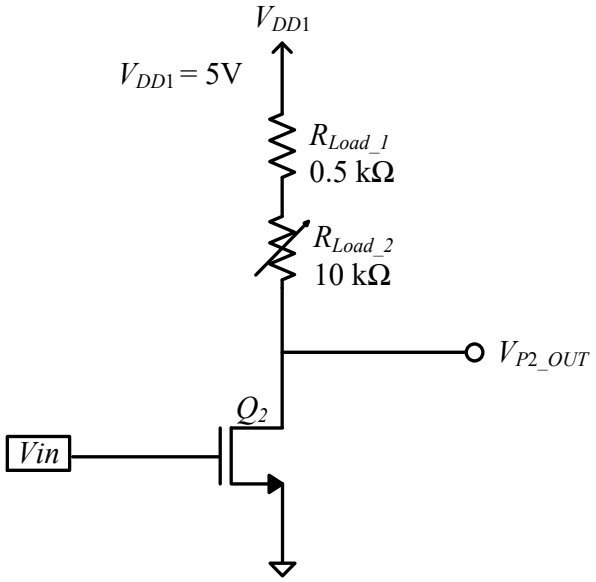


Fig. 18:

E11 Setup new circuit as below in Fig. 19 without load capacitors. This will configure a basic CMOS inverter circuit shown in Fig. 12(c). Keep the function generator amplitude the same but change the waveform from a triangle to square wave and increase the frequency to 2 kHz. Set the oscilloscope back to YT mode (regular time mode). Sketch the input and output waveforms and verify that this circuit is behaving as an inverter. Add C_3 and note the effect on the output. Add C_4 then note the effect on the output. What is the approximate rise time of the output now?

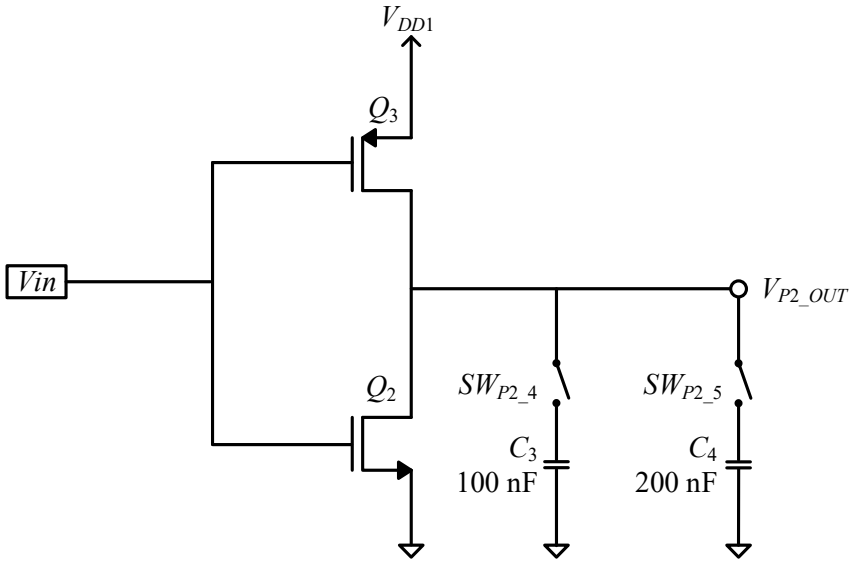


Fig. 19:

E12 Setup new circuit as shown in Fig 20. Notice that a second PMOS, Q_4, is in parallel with the original PMOS, Q_3. This is equivalent to having a single PMOS with twice the W/L ratio, allowing two times the current to flow from V_{DD1} to the capacitive load, $C_{load} = C_3 + C_4$. Observe the output on the oscilloscope. What is the approximate rise time now? Does adding Q_4 affect the fall time at the output?

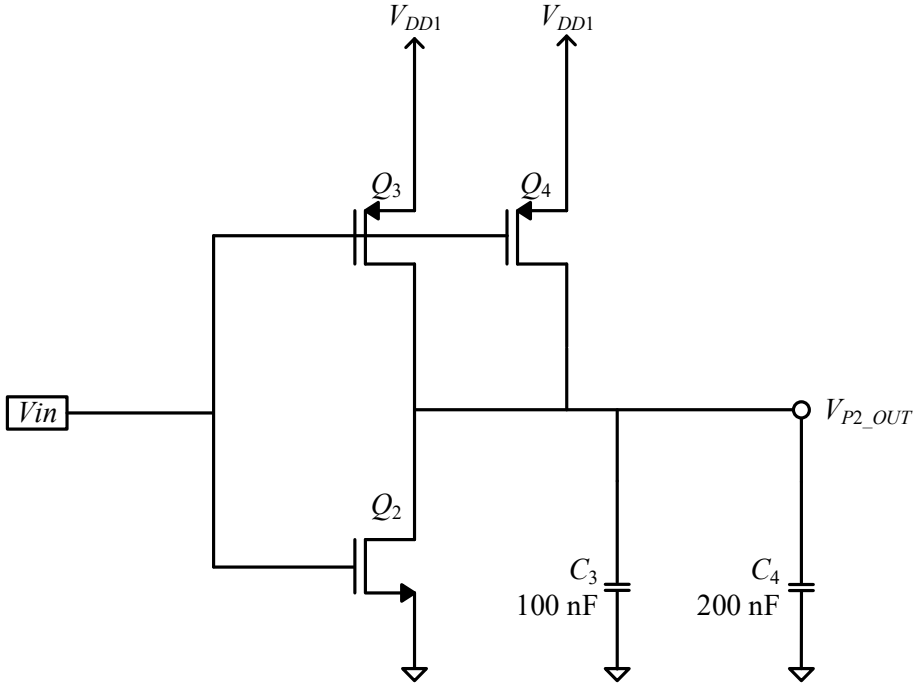
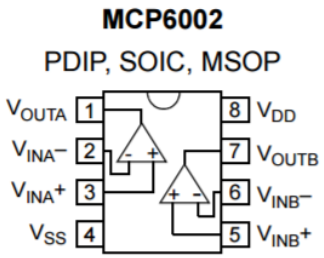
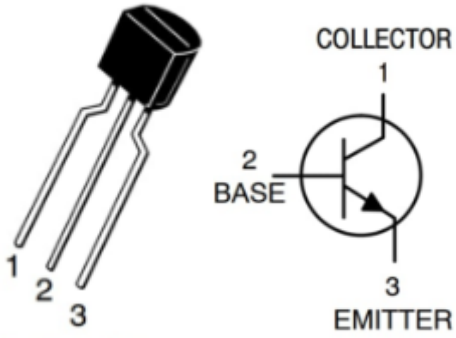


Fig. 20:

Appendix



MCP6002



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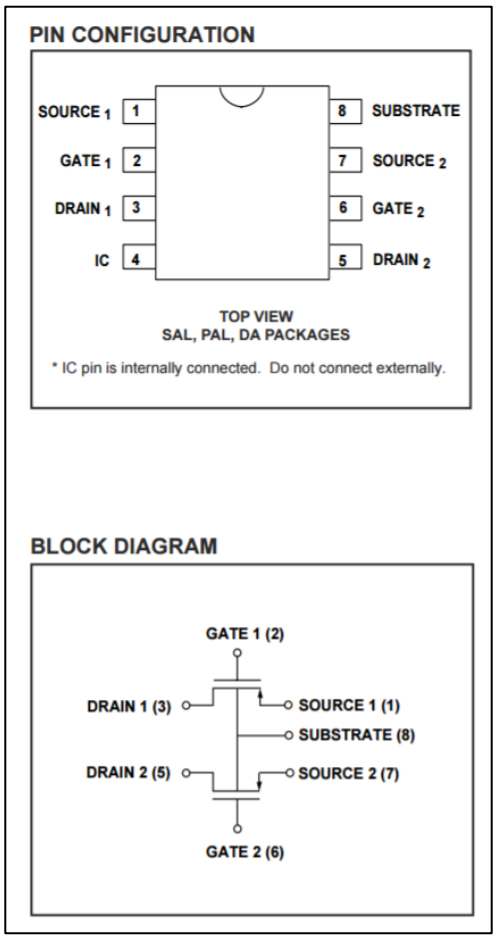

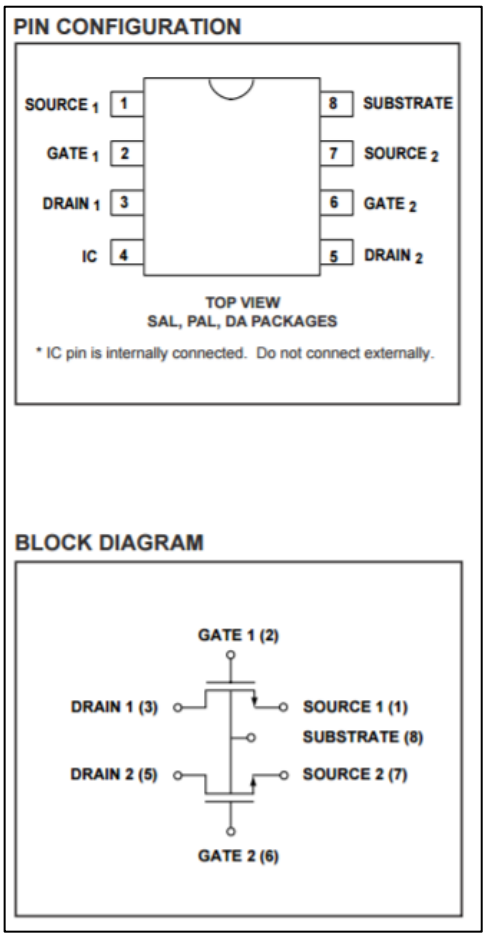

ALD1102 (PMOS) **ALD1101 (NMOS)**