ECE231: Introductory Electronics

Lab #6

Two Stage MOSFET Amplifier

Version: 1.3

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INTRODUCTION

The objective of this experiment is to explore two stage MOSFET amplifiers.

Goals:

1. Analyze and test a MOSFET based amplifier.
2. Discuss common MOSFET applications.

Lab Preparations

PE1. The amplifier circuit shown in Fig. 5 is more complex than many of the circuits you are used to studying. A simplified version of this amplifier circuit is shown in Fig. 4. Regardless of the circuit complexity, remember that the same techniques of DC analysis and small-signal analysis can be applied to any circuit in order to study its operation.

a) Draw the complete small-signal circuit for the two-stage amplifier shown in Fig. 4 and confirm eq. (3).

Background

The objective of this experiment is to perform a basic transistor-level design of a multistage amplifier. A general amplifier is shown in Fig. 1. (a) and the equivalent circuit is shown in Fig. 1. (b). On the *MOSFETs* board, the signal source is a function generator connected via the *OpAmp* board, and the load resistance is provided by a POTENTIOMETER. The signal source is set to provide a very weak output voltage with a peak-to-peak voltage of approximately 100 $mV_{p\text{-}p}$. This is designed to model the output from many types of sensors that require amplifiers including Microphones, Accelerometers, and Thermocouples. The amplifier must meet the following specifications:

- High gain
- High input resistance
- Low output resistance

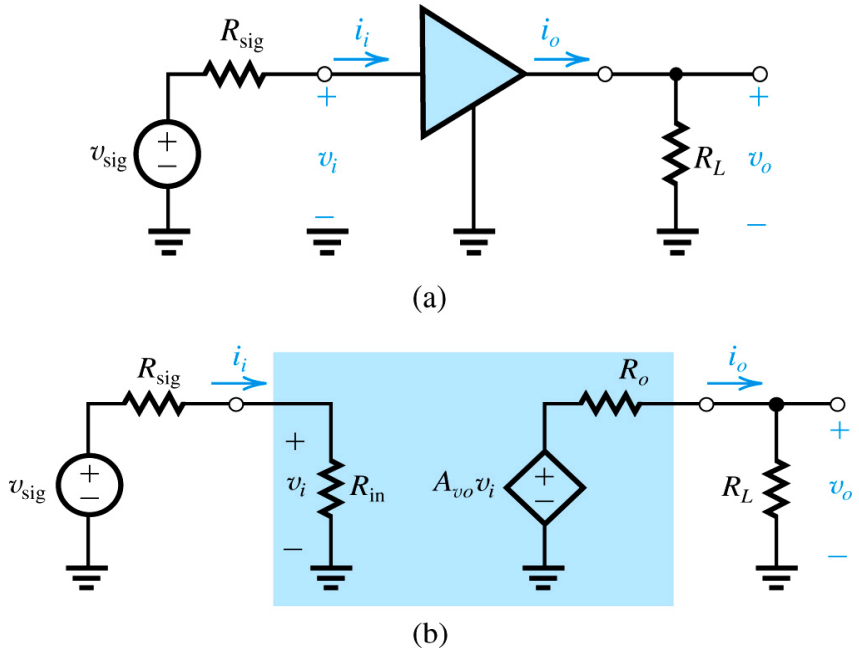
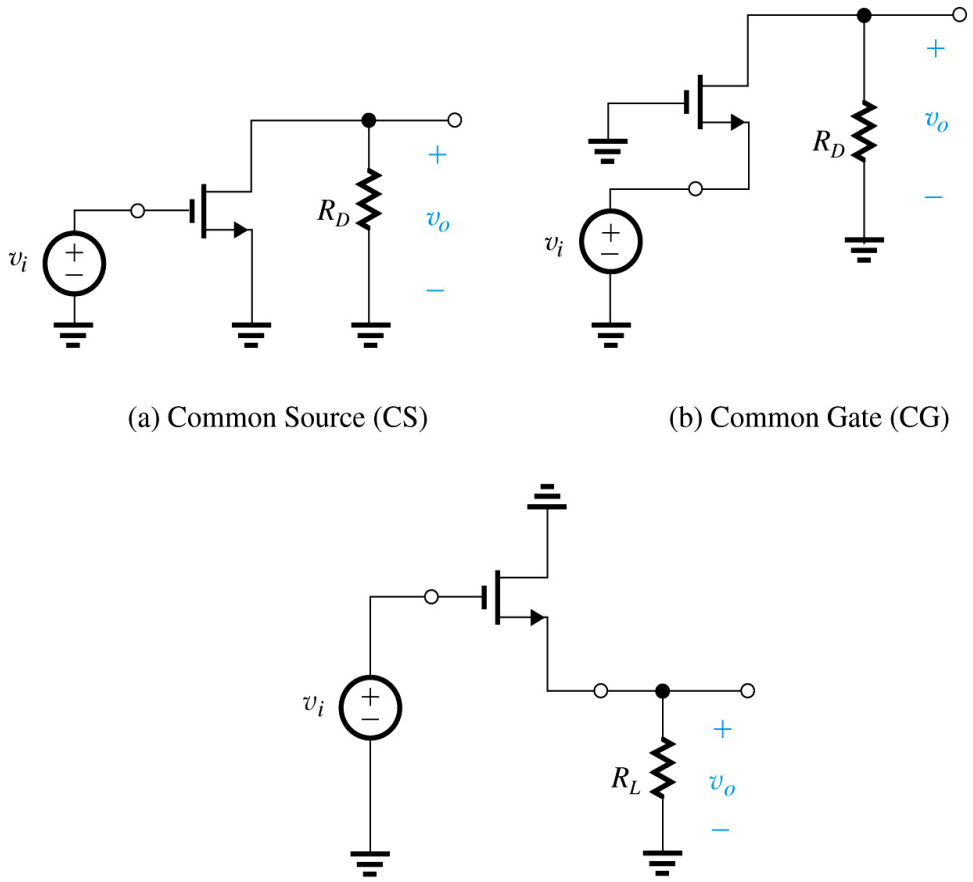


Fig. 1: (a) Functional block of an amplifier and (b) equivalent circuit representation.

Achieving these three characteristics with a single-stage MOSFET amplifier is not practical. Instead, we employ the cascaded amplifier approach, where the first stage has high input resistance and high gain, while the second stage provides low output resistance to drive the load resistance. The three most common MOS amplifier configurations are shown in Fig. 2.



(a) Common Source (CS) (b) Common Gate (CG)

(c) Common Drain (CD)

Fig. 2: Three basic MOSFET amplifier configurations.

Based on the characteristics summarized in Table 5.4 in the textbook, the common-source (CS) and common-drain (CD) configurations are selected for the first and second stages, respectively, as shown in Fig. 3.

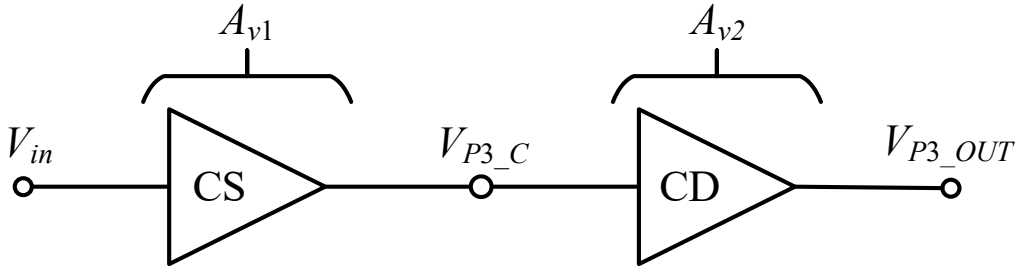


Fig. 3: Functional block diagram of a two-stage MOSFET amplifier.

The simplified two-stage amplifier is shown in Fig. 4. The drain current for the transistors Q_7 and Q_8 is set by the current sources I_{D7} and I_{D8}, respectively. Assuming that all transistors are in saturation, the small-signal gain of the common-source first stage, is given by:

$$A_{v1} = \frac{v_{d7}}{v_{in}} = -g_{m7}\left(R_{10} \parallel r_{o7}\right) \tag{1}$$

The small-signal gain of the common-drain second stage is given by:

$$A_{v2} = \frac{v_{P3\_OUT}}{v_{d7}} = \frac{R_{P3\_Load}}{\left(R_{P3\_Load} + 1/g_{m8}\right)} \tag{2}$$

where R_{P3_Load} is the total load resistance at the output node and is set by the R_{P3_Load} POTENTIOMETER. The overall gain, $G_v = v_o/v_{sig}$ is therefore

$$G_v = \frac{v_{P3\_OUT}}{v_{in}} = A_{v1}A_{v2} = \frac{-g_{m7}\left(R_{10} \parallel r_{o7}\right)R_{P3\_Load}}{\left(R_{P3\_Load} + 1/g_{m8}\right)} \tag{3}$$

The full schematic for the configurable two-stage amplifier is shown in Fig. 5, where the two current sources are implemented using a series of NMOS and PMOS MOSFET current mirrors. Refer to Section 8.2.1 in the textbook for a detailed explanation of MOSFET based current mirrors. The reference current, I_{ref}, is the drain current of Q_9. The switches SW_{P3_1} and SW_{P3_2} are used to configure I_{D7} to either I_{ref}, $2I_{ref}$, or $3I_{ref}$. The switches SW_{P3_3} to SW_{P3_4} are used to set I_{D8} between I_{ref}, $2I_{ref}$, or $3I_{ref}$. The reference current can be configured using the POTENTIOMETER R_{P3_MIRROR}, according to:

$$I_{ref} = \frac{\left(VDD2 - VSS2 - V_{GS9}\right)}{R_{P3\_MIRROR}} \tag{4}$$

The versatile amplifier can be configured in the following ways:

- The reference current is set using R_{P3_MIRROR}
- The bias current of both amplifier stages is set using the switches SW_{P3_1} to SW_{P3_4}
- The load resistance is set using R_{P3_Load}
- The drain resistance of Q_7 is set using R_{10}

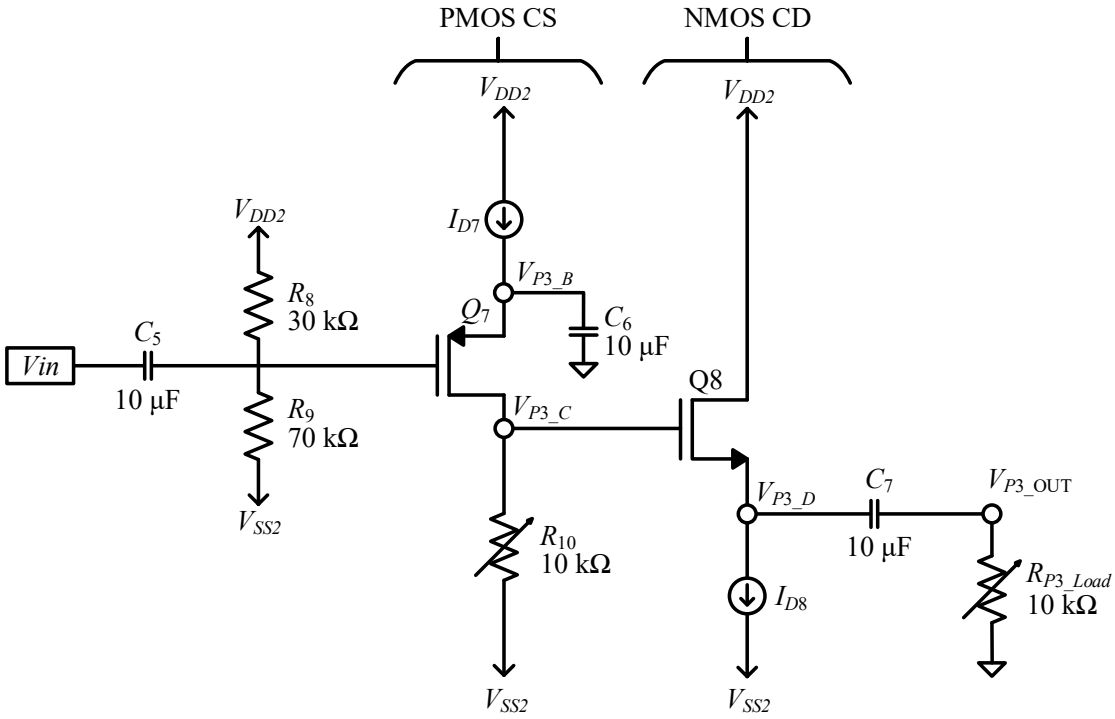


Fig. 4: Simplified two-stage MOSFET amplifier.

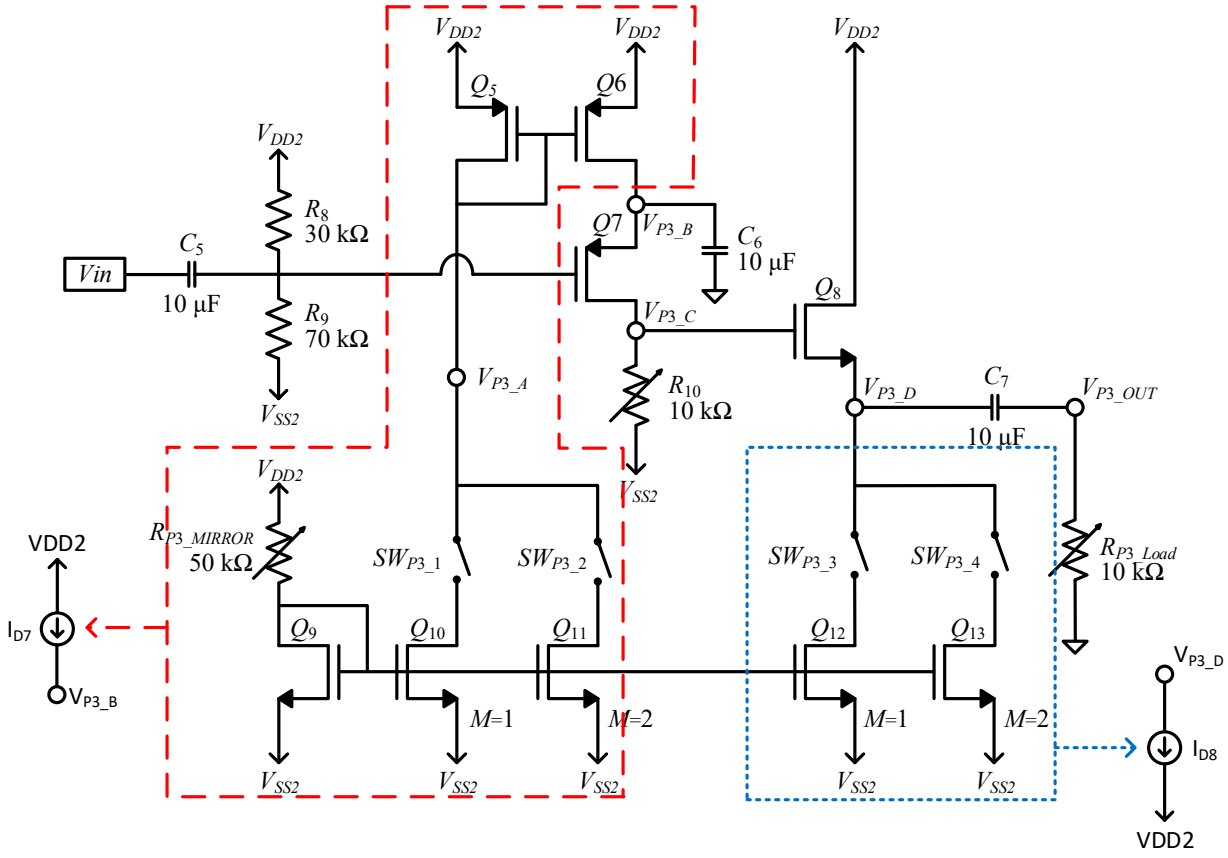
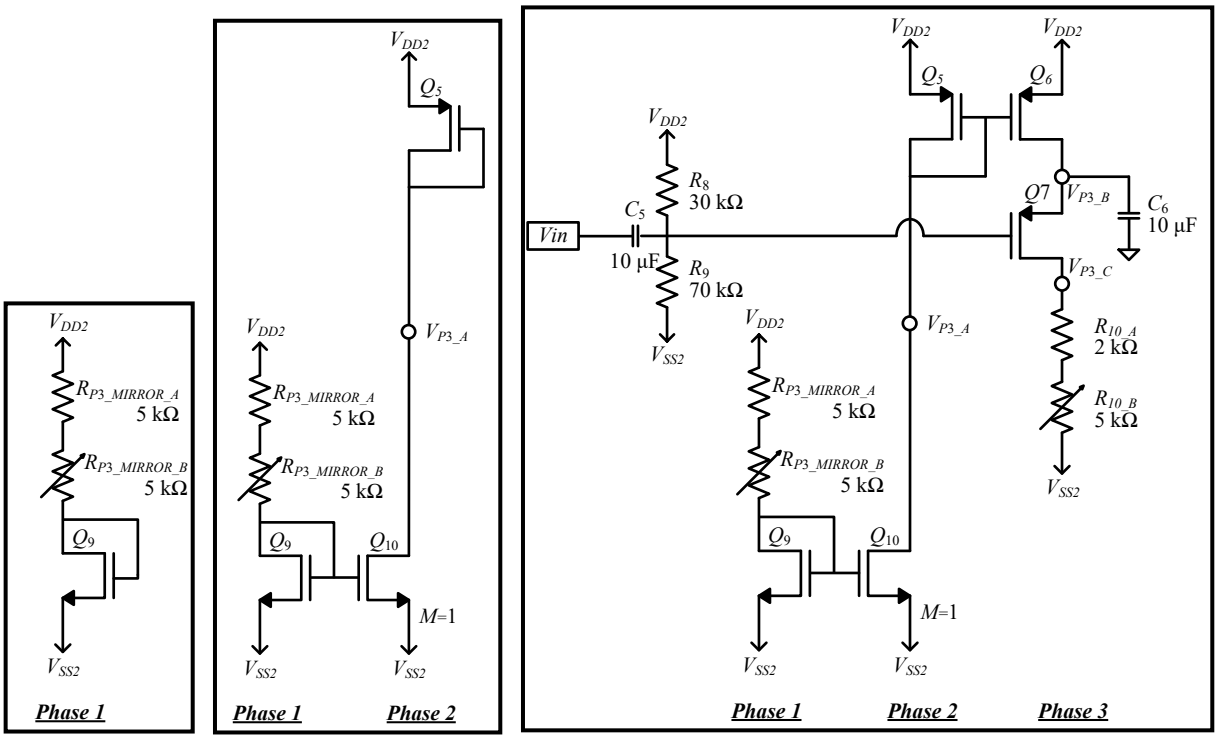


Fig. 5: Two-stage MOSFET amplifier with biasing setup and load resistor.

Lab Experiments

In this portion of the lab we will use the circuit shown in Fig. 6 to investigate the behavior of a two stage CMOS amplifier.

E1 Build the circuit as shown in Fig 6 phase by phase. **Set all the variable resistors to 0 ohm**. Set V_{dd2} = 5V, V_{SS2} = -5V. Connect the substrates of the PMOS to V_{dd2} and NMOS to V_{SS2}. Using a multimeter, measure the DC voltage at V_{P3_B}, V_{P3_C}, and V_{P3_D}. Based on your measurements, what is the operating mode for transistors Q_7 and Q_8. Note that you need to calculate the gate voltage of Q_7 based on Fig. 6.
You should **build the circuit phase by phase** as shown in Fig 6. **Measure the DC operating point in each phase. Ask your TA to check after you've done each phase.** Note that Q_8 is an NMOS.



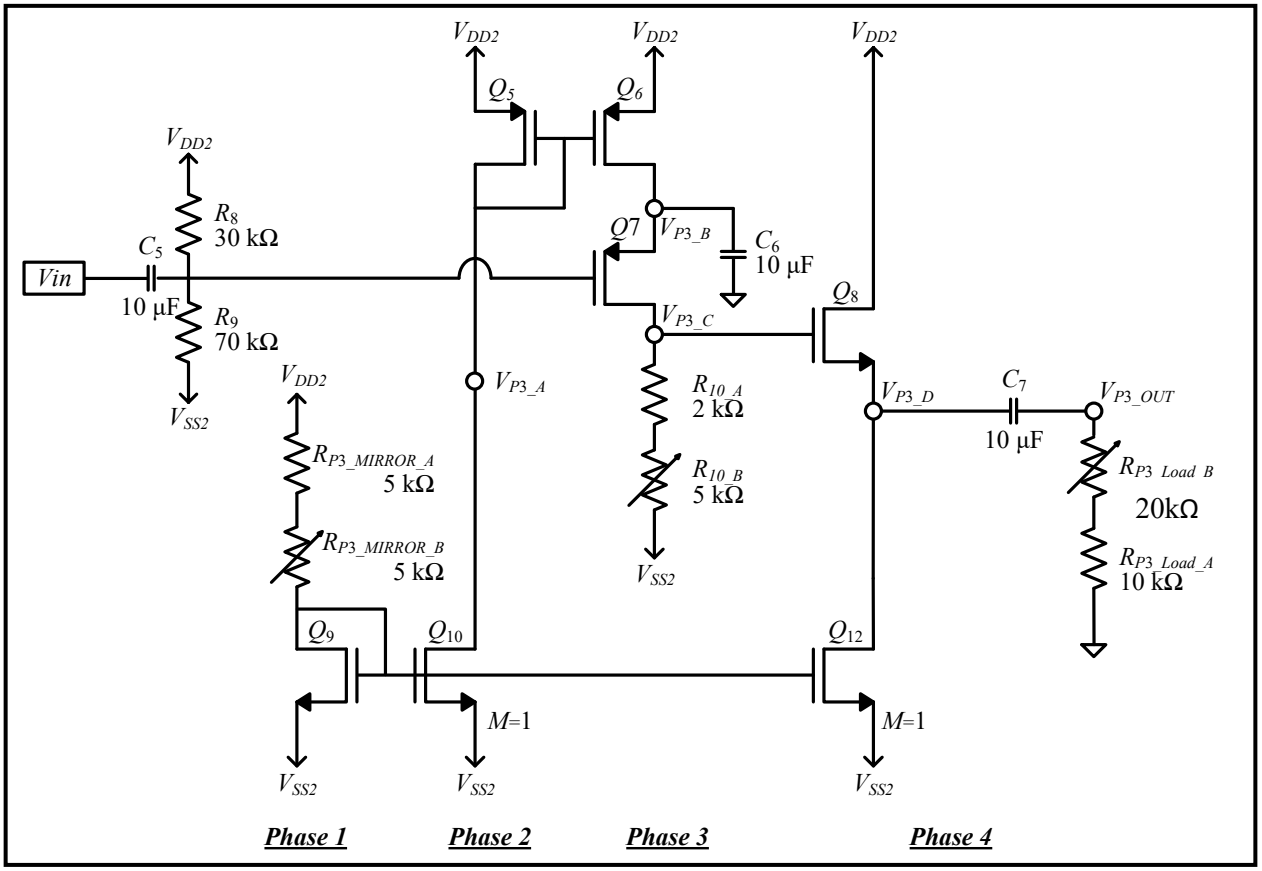


Fig. 6 Two-stage MOSFET amplifier

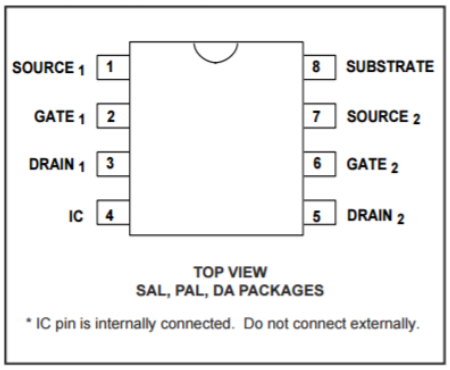
E2 **Set the function generator to output a 0.1 $V_{p\text{-}p}$, 1 kHz, sine wave**. This is a very small signal, so you will need to use the "SYNC" feature of your oscilloscope. **Do not connect to the circuit until you have checked right input is correct.** Measure the small-signal gain of the first stage, A_{v1}, and the second stage, A_{v2}. Confirm that the first stage is inverting. **Show your TA the input and output waveforms.**

E3 Gradually increase the gain of the first stage, A_{v1}, by slowly increasing R_{10_B}. Once you begin to notice visible distortion at V_{P3_C}, stop increasing R_{10_B}. Then try to adjust the bias current in Q_7 until the signal at V_{P3_C} is no longer distorted (use $R_{P3\_MIRROR\_B}$). How does the drain current affect the gain based on eq. (1)? Take note of which changes helped to decrease the output distortion. Now begin to slowly increase R_{10_B} again until you notice the distortion returning. Repeat the above process until you reach a gain of roughly 5 V/V without any output distortion. Write down the value of V_{P3_C} used to achieve this gain. **Show your TA the input and output waveforms.**

E4 Measure the second-stage gain, A_{v2}. Vary $R_{P3\_Load\_B}$ and observe the effect on A_{v2}. Does your observed effect of R_{P3_Load} on A_{v2} match the prediction from eq. (2)? Calculate g_{m8} based on the observed gain. (Note that you may need to find the resistance of the potentiometer**.** To do this, **turn off the power supply,** and measure the resistance using the multimeter with the resistance setting.)

Appendix

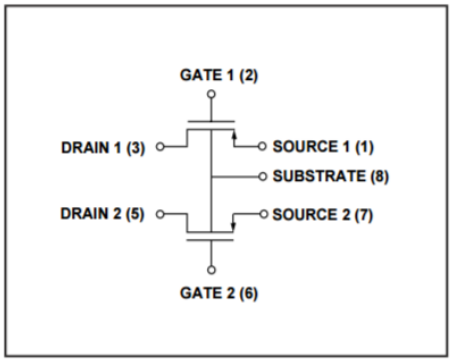
PIN CONFIGURATION



TOP VIEW
SAL, PAL, DA PACKAGES

* IC pin is internally connected. Do not connect externally.

BLOCK DIAGRAM



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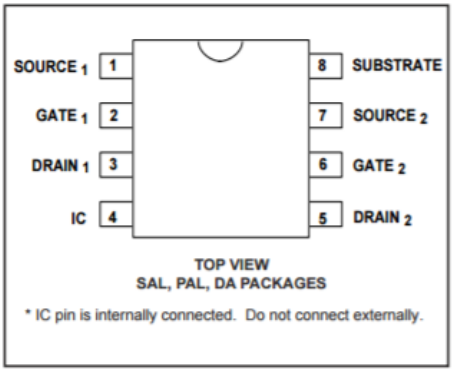
PIN CONFIGURATION



TOP VIEW
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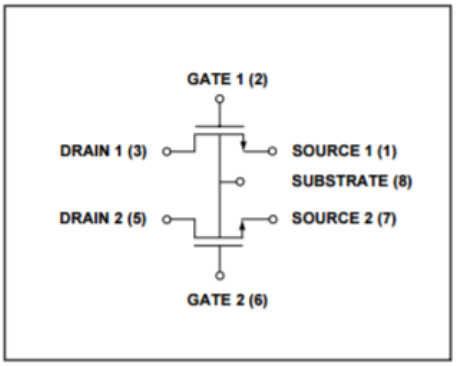
BLOCK DIAGRAM



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