Problem 3

Consider a processor with the following characteristics. Word size is 16 bits and memory size 8K x16. The ALU performs the operations ADD, logic AND on two operands, right shift and logic complement of an operand via gate B. Instructions:

mnemonic	meaning
LOAD *X*	AC ←MEM(*X*) loads content position *X* into accumulator
STORE *X*	MEM(*X*) ←AC puts content of AC into memory position *X*
ADD *X*	AC ←AC+MEM(*X*) adds content memory position X to accumulator
AND *X*	AC ←AC^MEM(*X*) logical AND on memory position X and accumulator
JUMP *X*	PC← *X* unconditional jump to address *X*
JUMPZ *X*	If *Z*, PC← *X* if result zero, jump to address *X*
COMP	AC ←$\overline{AC}$ logical complement of accumulator
RSHIFT	AC ←0,AC[15:1] right shift accumulator

Design the corresponding instruction format, datapath and control unit.

Problem 4

Change the datapath and control of a MIPS processor in order to be able to handle the new instruction LUI:

LUI rd,constant rd←constant,0,0,..,0