Problem 1

Consider a processor with the following instructions

instruction		format
mnemonic	meaning	XXXX : not used
AD1 *rs, rf*	*rs ←ADD(rs,rf)*	00||*rs*||*rf*||XXXX||00
AD2 *rs, #cte*	*rs ←ADD(rs,cte)*	00||*rs*||*cte*||01
AD3 *rs, (rf)*	*rs ←ADD(rs,M[rf])*	00||*rs*||*rf*||XXXX||10
AD4 *rs, dir*	*rs ←ADD(rs,M[PC+1+dir])*	00||*rs*||*dir*||11
JZ *offset*	*if Z==1* *PC ←ADD(PC+1,offset)*	10||*offset*

Words of 16 bits; register file with 16 registers;
2 last bits of ADj represent the addressing mode of the second operand; PC increases by 1

a. Draw the design of the datapath.
b. Design the control unit.
c. Add to the design the instruction

LAC *rd*, *rd← M[AC]*, 11||xxxxxxx||*rd*
where AC is a specific use register

Problem 2

Suppose we have a working processor of Problem 1.
Given the memory content shown in the table having the PC content 0045_{hex} and assuming the registers are clean, i.e. they have a content of 0.
Let the binary *cte*, *dir* and *offset* represent two's complement numbers; e.g. see Section 2.4 of HP.

Determine now for the empty table the development of the memory and register content when we step through the corresponding program.

pos	content
…	…
29_{hex}	0033_{hex}
$2a_{hex}$	0042_{hex}
$2b_{hex}$	0008_{hex}
…	…
41_{hex}	0023_{hex}
42_{hex}	$000a_{hex}$
43_{hex}	$0c01_{hex}$
44_{hex}	0001_{hex}
45_{hex}	1793_{hex}
46_{hex}	0542_{hex}
47_{hex}	$0bd5_{hex}$
48_{hex}	0480_{hex}
49_{hex}	0405_{hex}
$4a_{hex}$	8002_{hex}
$4b_{hex}$	0801_{hex}
$4c_{hex}$	$0c01_{hex}$
$4d_{hex}$	1001_{hex}
$4e_{hex}$	1401_{hex}

Instruction address	mnemonic	Operands source	Operand destination	Value to write