Problem 1

(HP 4.12) Let the five stages of the datapath have the following latencies.

IF	ID	EX	MEM	WB
200ps	150ps	120ps	190ps	140ps

a. Give the clock cycle time in a corresponding pipelined and nonpipelined processor.
b. Give the total latency of a `lw` instruction in a pipelined and nonpipelined processor?
c. Assume we are able to split one of the stages into two new ones with half the latency of the original one. Which stage would you split and what is the new clock cycle time?

Problem 2

(H.P. 4.13) Consider the following sequence of instructions:

```
a.   lw $1, 40($6)        b.   lw $5, -16($5)
     add $6, $2, $2            sw $5, -16($5)
     sw $6, 50($1)             add $5, $5, $5
```

a. Indicate dependences and their type
b. Indicate hazards and add `nop` instructions to eliminate them.

Problem 3

(HP 4.15) Consider the following new instructions.

bezi **`(rt),`** offs	opec |*r0*|*rt*|*offs*	**If Mem[rt]=0 then PC ← PC+4+offs**
swi `rd, rs(rt)`	opec |*rs*|*rt*|*rd*|*xxxx*	**Mem[rs+rt] ← rd**

a. Give the changes in the datapath of the pipelined processor to deal with these instructions.

b. Give the new control signals that should be added to your design.

d. Are there new hazards introduced?

Problem 4

(H.P. 4.16) For each of the following instructions:

a. `lw $1, 40($6)`   b. `add $5, $5, $5`

a. Indicate what is kept in each register located between two pipeline stages.

b. Which registers need to be read and which registers are actually read?

c. Indicate what the instruction does in the EX and MEM stages.

Problem 5

Consider the following code that will be run on a pipelined MIPS.

```
        ori $2, $0, 1000
loop:   lw  $1, 2800($2)
        sub $4, $1, $0
        jal rotate
        sw  $7, 1400($2)
        sw  $1, C400($2)
        subi $2, $2, 4
        bne $2, $0, loop

rotate: add $10, $4, $4
        muli $7, $10, 2
        jr $31
```

Give the (pairs of) instructions that might produce a hazard and classify the type in the following tables:

Data hazard

Instruction pair mnemonics	Involved register

Control hazard

Instruction mnemonic