

+5 Points EC for turning in early

3.32

10 Points (5 for each definition)

Memory Address - refers to a location in memory.

Memory's addressability - is the number of bits stored in each memory location.

3.31

5 Points

$$8 * (2^3) = 64 \text{ bytes}$$

3.33

10 Points (5 points each)

a) $A[1,0] = 11$, $WE = 0$

b) A total of **6 address lines** are required for a memory with 60 locations.

The addressability of the memory will remain unchanged.

3.34

15 Points (5 points)

a) Address Space: **3**

b) addressability: **4 bits**

c) Address 2: **0001**

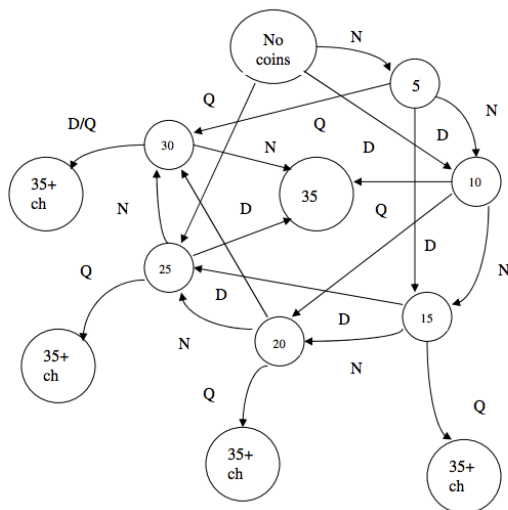
3.35

5 Points

$$\text{Total bits of storage} = 2^{22} * 3 = 12582912 \text{ bits}$$

3.41

15 Points



NB: There could be arrows from each of the final states to “money” states with coin inputs

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3.27 15 Points (5 points each)

- a) When $S = 0$, $Z = A$
- b) When $S = 1$, Z retains previous value
- c) **Yes**; the circuit is a storage element.

Custom Problem 25 Points Total

Truth Table 8 points (1 per row)

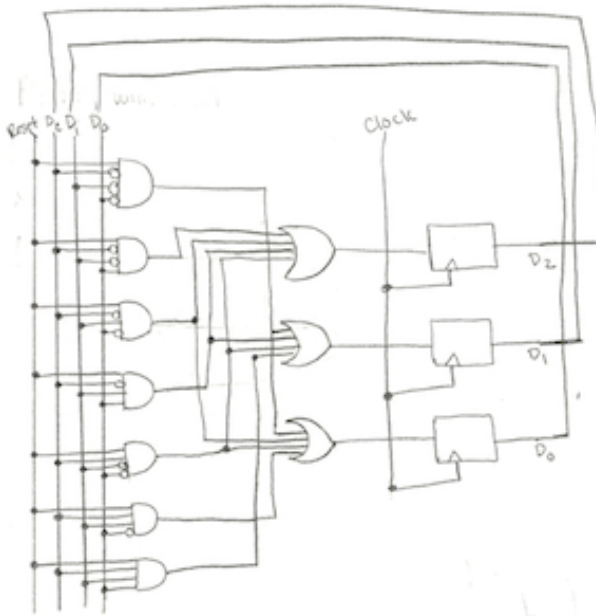
Present State (t)			Next State (t+1)		
D_2	D_1	D_0	D_2	D_1	D_0
0	0	0	0	1	1
0	0	1	1	0	0
0	1	0	1	0	1
0	1	1	1	1	0
1	0	0	1	1	1
1	0	1	0	0	0
1	1	0	0	0	1
1	1	1	0	1	0

Finite State Machine 8 points (1 per arrow)



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PLA, with reset 9 Points (+ 1 EC for reset line)



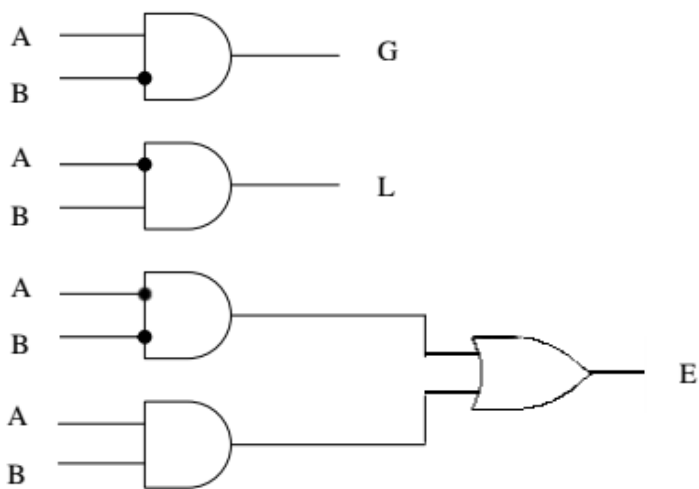
NB: when RESET = 0, counter resets to 000

For resetting to 000 when RESET = 1, simply put a NOT on the reset line for all the AND gates.

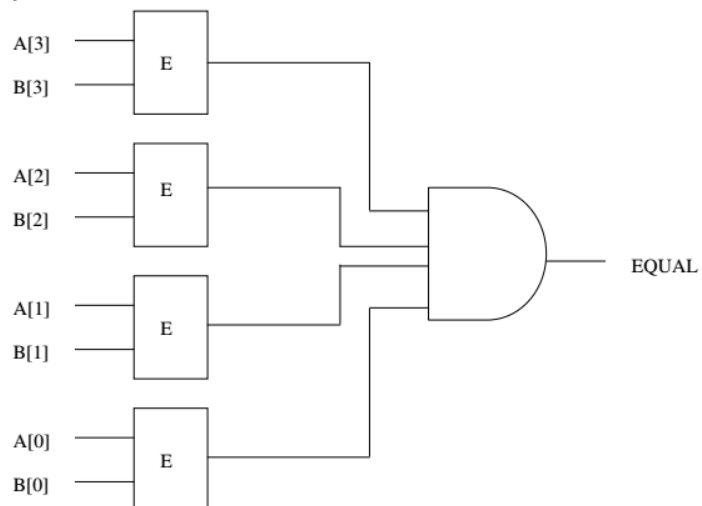
a)

A	B		G	E	L
0	0		0	1	0
0	1		0	0	1
1	0		1	0	0
1	1		0	1	0

b)



c)



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3.42 2.5 Points (All or nothing)

Since there are 3 states (states 01, 10 and 11) in which lights 1 and 2 are on, these lights are controlled by the output of the OR gate labeled Z, which ORs the three AND gates giving an output of 1 on those 3 states.

Storage element 2 should be set to 1 for the next clock cycle if the next state is 01 or 11. This is true when the current state is 00 or 10. So it is controlled by the output of the OR gate labeled U.