Static Timing Analysis (STA)

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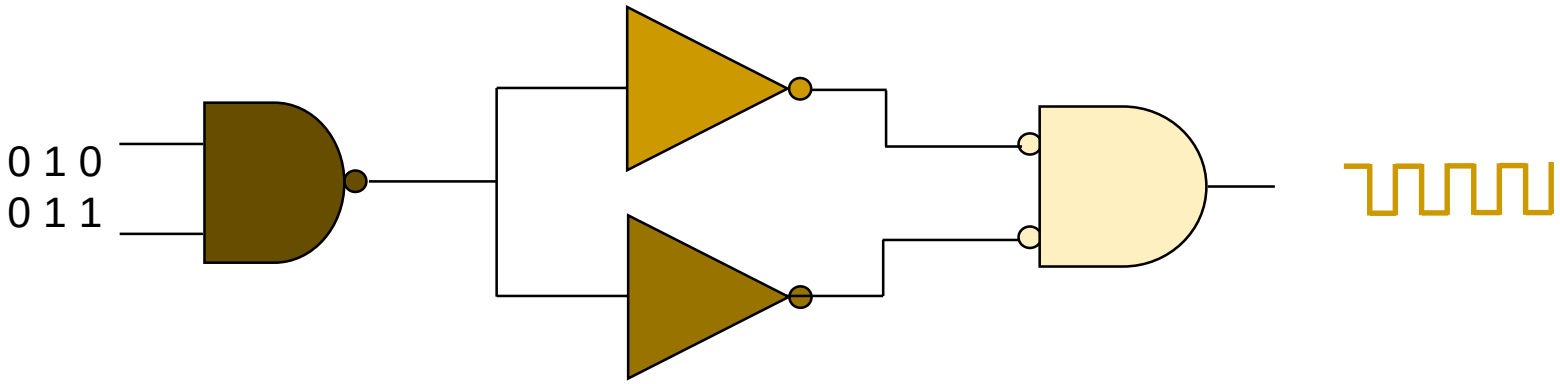
- STA is a technique for digital design verification. It:
  - Validates if the design can operate at the set timing constraints
  - Is a complete and exhaustive verification of all timing checks of a design
  - Is used instead of simulation

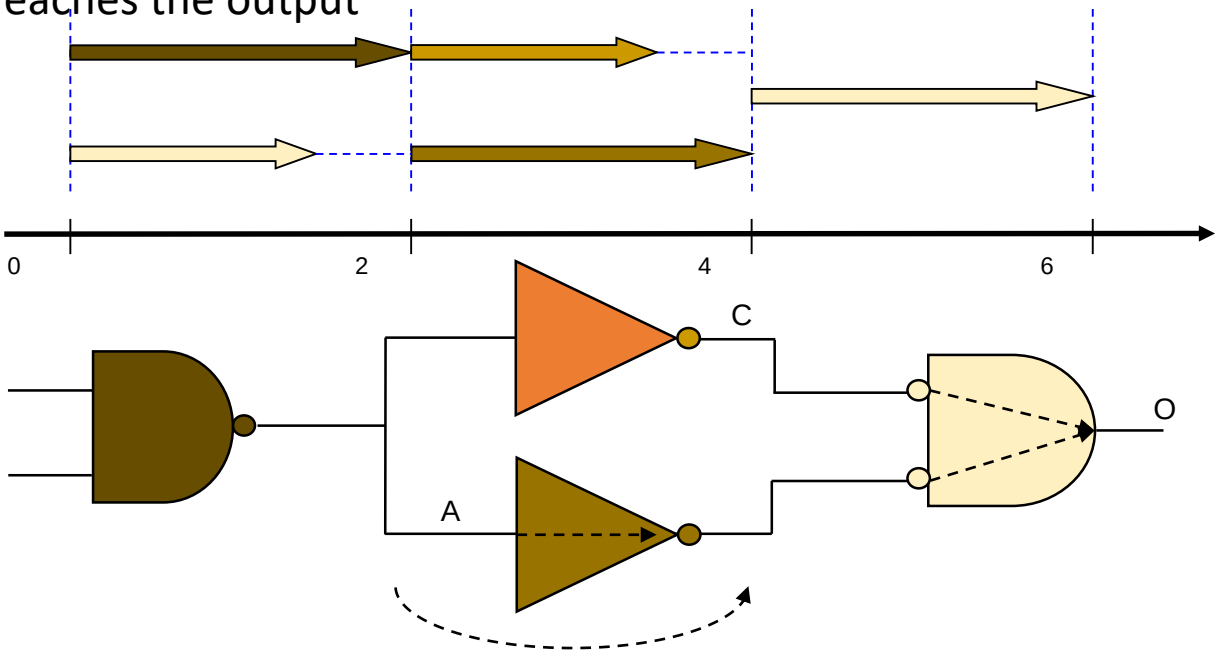
Simulation

- Simulating (dynamically) circuit response for a specified set of input patterns
  - Circuit modeled as network of capacitors, resistors and voltage/current sources



STA (2)

- Vector-less topological analysis of a circuit.
  - The signal at the input is propagated through the gates at each level till it reaches the output



STA vs. Simulation

Simulation

- Advantages
  - Can be very accurate (Spice-level)
- Disadvantages
  - Analysis quality depends on stimulus vectors
  - Non-exhaustive, slow

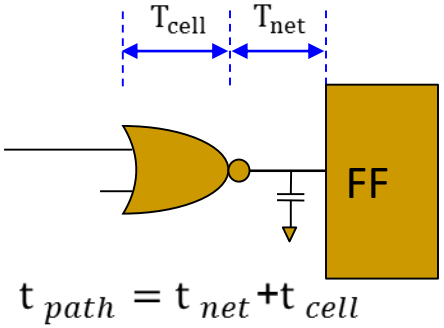
Static Timing Analysis (STA)

- Advantages
  - Exhaustive timing coverage
  - Does not require input vectors
  - Faster operation
- Disadvantages
  - Less accurate
  - Must define timing requirements/exceptions
  - Difficulty in handling asynchronous designs, false paths

Digital Circuits Timing Goals

- Achievement of required frequency
  - Digital circuits are constrained to work under specific frequencies
  - All separate parts of circuit are constrained to have delay smaller than clock period
- Meeting timing constraints
  - Avoiding collision of signals
  - Avoiding failure
- STA verifies these

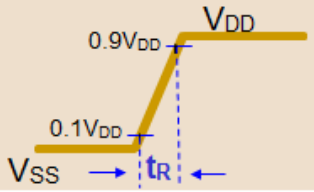
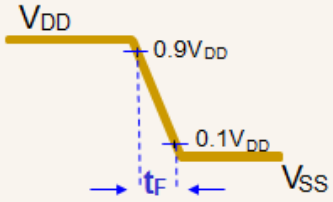
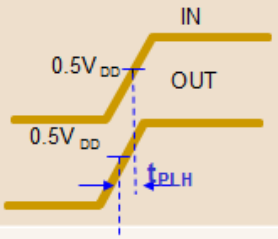
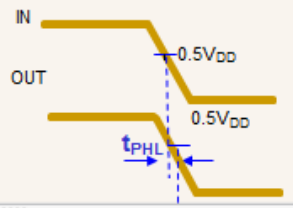
Components of Circuit Timing



- Delay components
  - Cells, Interconnects
- Constrained components
  - Clocked registers require setup/hold, recovery/removal constraints

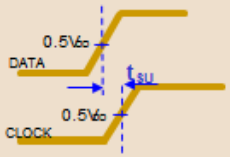
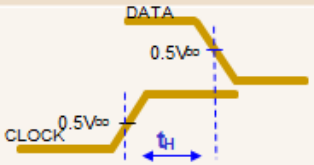
For circuit to operate without failure it is required that delay components at no point violate constraints of other components.

Cell Timing Parameters

N	Parameter	Unit	Symbol	Figure	Definition
1.	Rise transition time	ns	t_R		The time it takes a driving pin to make a transition from kV_{DD} to $(1-k)V_{DD}$ value. Usually k=0.1 (also possible k=0.2, 0.3, etc)
2.	Fall transition time	ns	t_F		The time it takes a driving pin to make a transition from $(1-k)V_{DD}$ to kV_{DD} value. Usually k=0.1 (also possible k=0.2, 0.3, etc)
3.	Propagation delay low-to-high (rise)	ns	t_{PLH} (t_{PR})		Time difference between the input signal crossing a $0.5V_{DD}$ and the output signal crossing its $0.5V_{DD}$ when the output signal is changing from low to high
4.	Propagation delay high-to-low (Fall)	ns	t_{PHL} (t_{PF})		Time difference between the input signal crossing a $0.5V_{DD}$ and the output signal crossing its $0.5V_{DD}$ when the output signal is changing from high to low

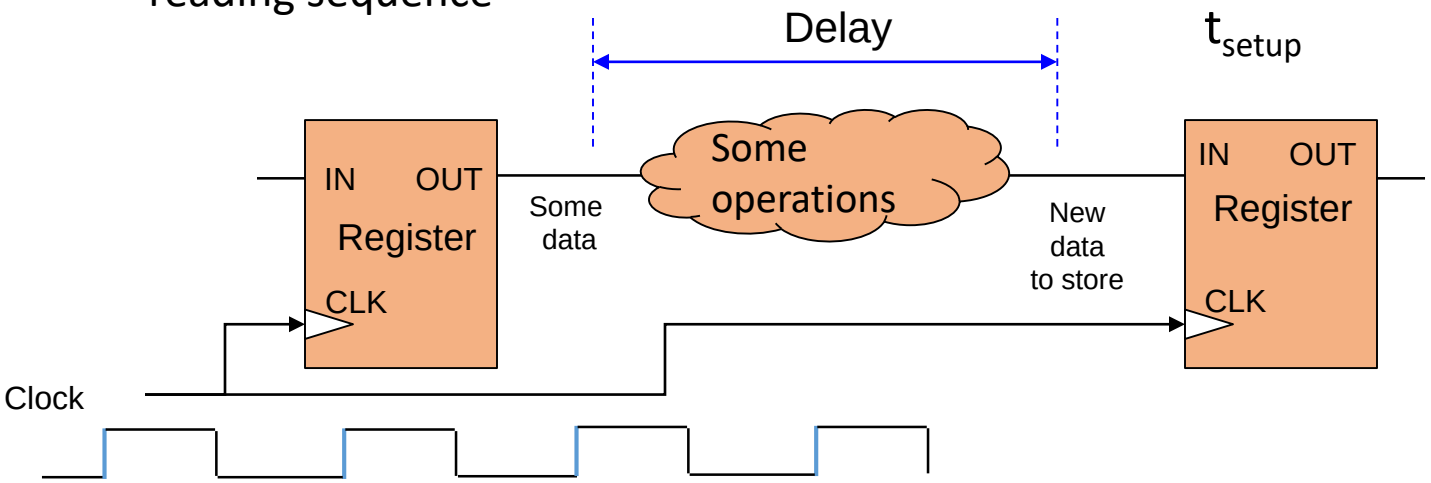
Cell Timing Constraints

Setup/Hold, Recovery/Removal Constraints

N	Parameter	Unit	Symbol	Figure	Definition
1	Setup time (only for flip-flops or latches)	ns	t_{SU}		The minimum period in which the input data to a flip-flop or a latch must be stable before the active edge of the clock occurs
2	Hold time (only for flip-flops or latches)	ns	t_H		The minimum period in which the input data to a flip-flop or a latch must remain stable after the active edge of the clock has occurred

Timing Closure Problem

- Problem
  - In clocked environment signals on the register inputs must arrive before next reading sequence



Clock: Both registers store new value at specific points of time (with some frequency, like 1GHz)

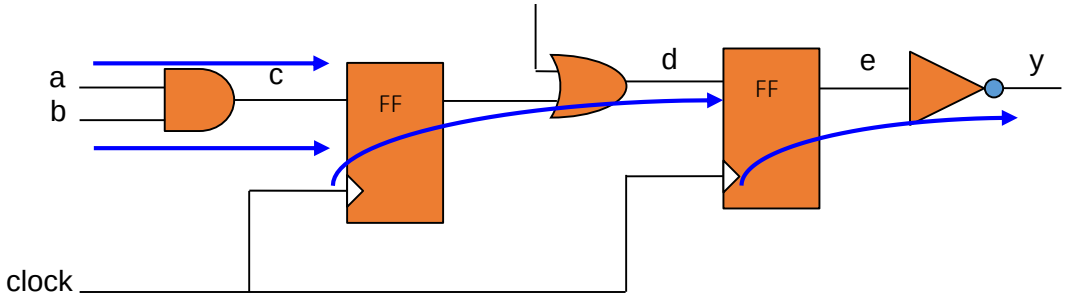
$$Delay + t_{setup} < T_{clock}$$

Static Timing Analysis Steps

Circuit is broken into timing paths

Delay of each path is calculated

For each path delays are checked against timing constraints



Path	Delay	Constraint
a → c	?	?
b → c	?	?
clock → d	?	?
clock → y	?	?

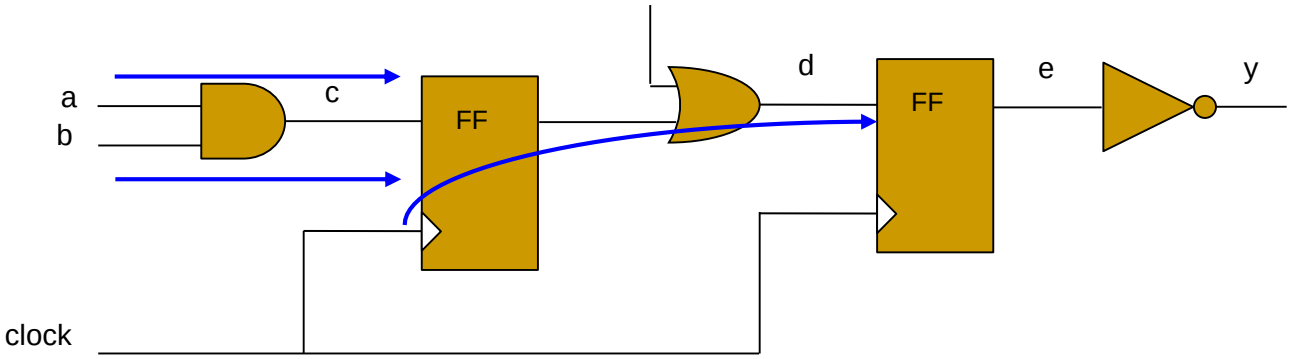
STA Concepts

- Timing Path
- Required Time
- Arrival Time
- Slack
- Critical Path

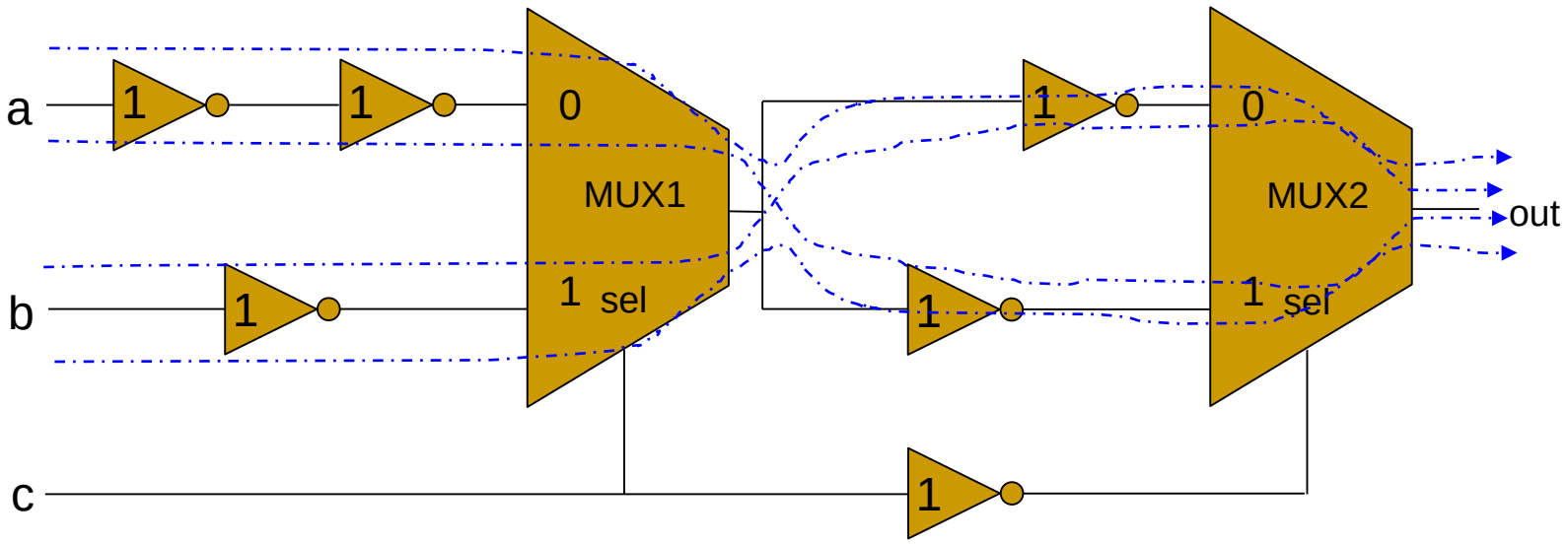
Timing Paths

- Timing path has a start point and an endpoint.
- Start point:
  - Input ports
  - Clock pins of flip-flops

- Endpoints:
  - Output ports
  - data input pins of flip-flops



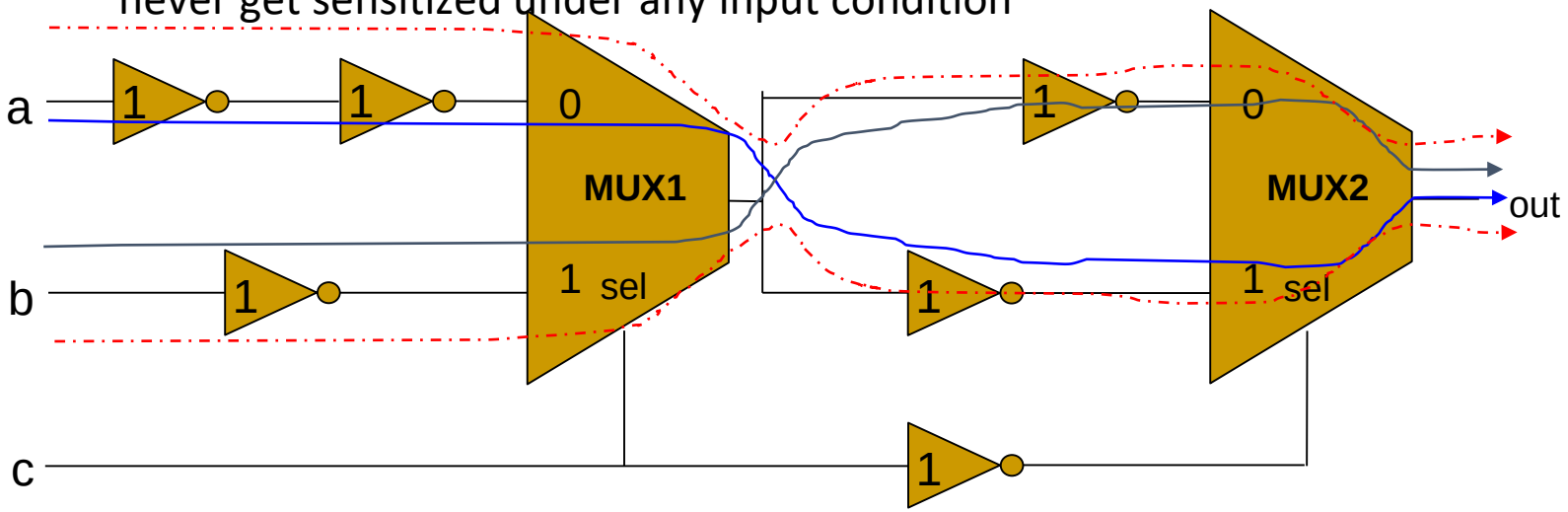
Possible Paths



Paths
a → MUX1.0 → MUX2.0 → out
a → MUX1.0 → MUX2.1 → out
b → MUX1.1 → MUX2.0 → out
b → MUX1.1 → MUX2.1 → out

False Paths

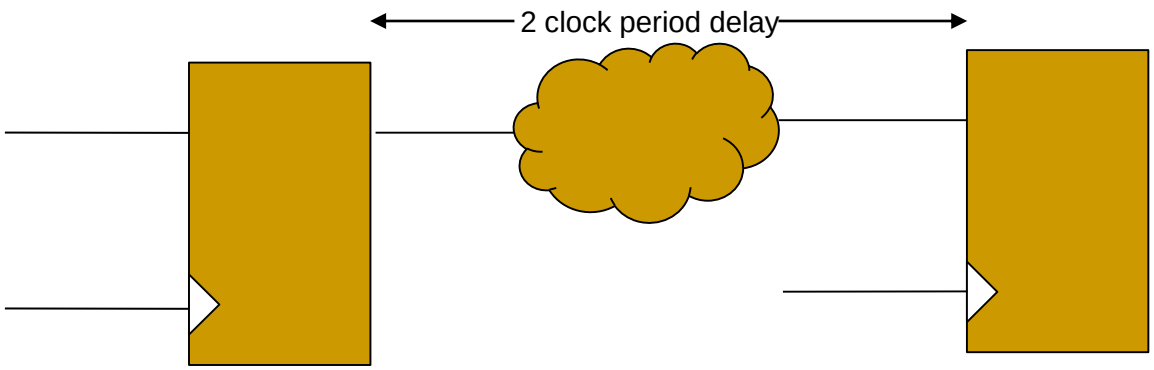
- Paths which physically exist in a design but are not logic paths. These paths never get sensitized under any input condition



Paths
~~a → MUX1.0 → MUX2.0 → out~~
a → MUX1.0 → MUX2.1 → out
b → MUX1.1 → MUX2.0 → out
~~b → MUX1.1 → MUX2.1 → out~~

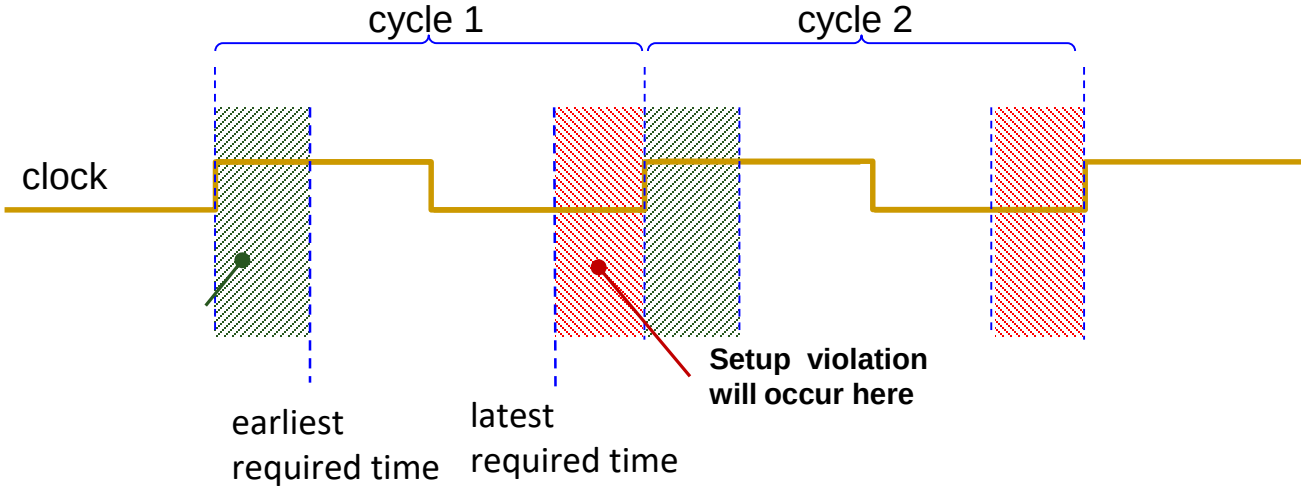
Multi-cycle Paths

- There are data paths that require more than one clock period for execution.



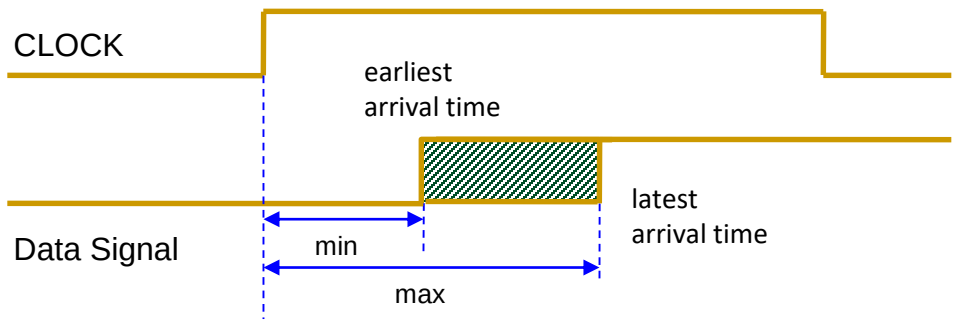
Required Time

- Required time specifies the time point (interval) at which data is required to arrive at end point (data is required to be stable after arrival).
  - Time point after which data can become unstable (change) is called earliest required time
  - Time point after which data cannot become unstable (change) is called latest required time
- The requirement is set by timing constraints like setup/hold, removal/recovery, etc.



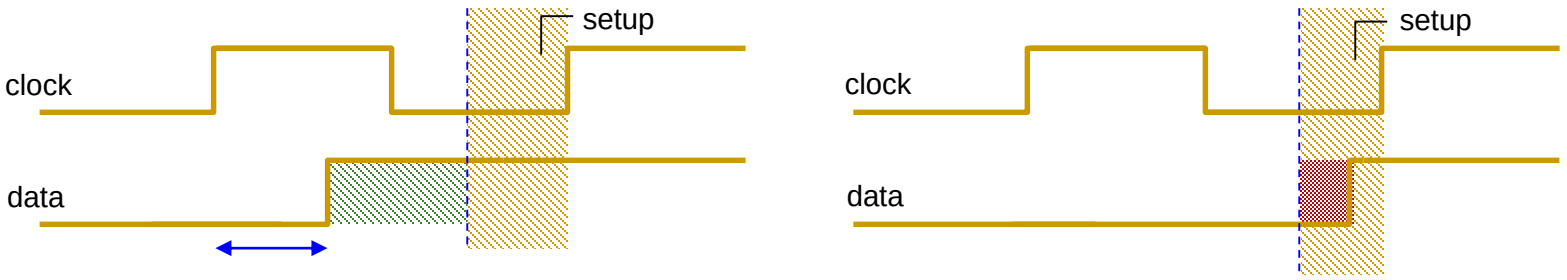
Arrival Time

- Arrival time defines the time interval during which a data signal will arrive at a path endpoint (after arrival time signal will be stable).
- Data is normally triggered by clock edge
- Data arrival depend on circuit delay, which vary (depend on temperature, supply voltage, etc.)
- Minimum delay, early arrival
- Maximum delay, late arrival



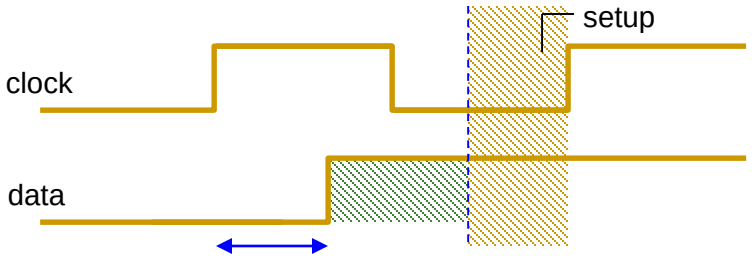
Slack and Critical Path

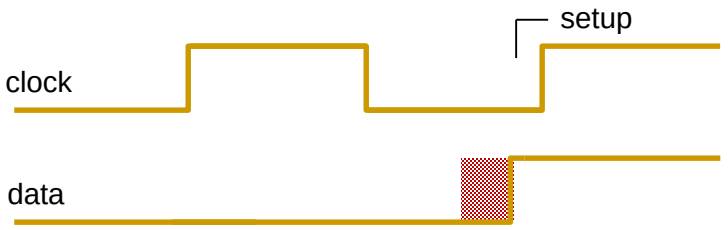
- Slack is the difference between the required time and the arrival time.
  - Negative slack → violation
  - Positive slack → constraints have been met
  - Critical path is a path in the design that has smallest slack



Early and Latest Analysis

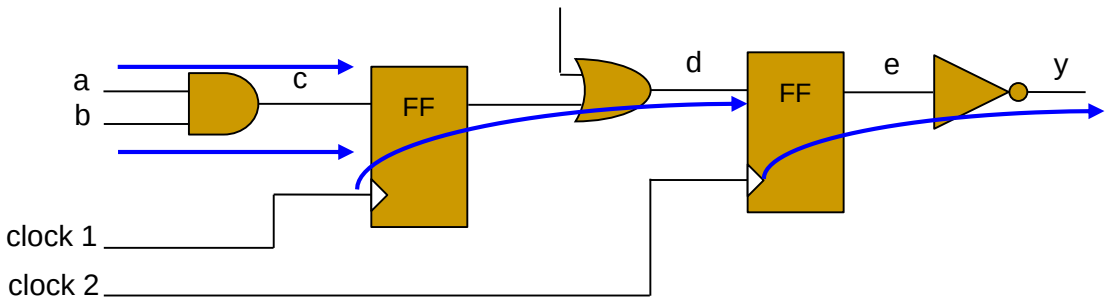
- STA tool calculates the slack of each logic path, in order to find critical path.
- Early and Latest analysis approaches:
  - Assumes circuits have minimum delay, compares arrival time to earliest required time (hold check)
  - Assumes circuits have maximum delay, compares arrival time to latest required time (setup check)

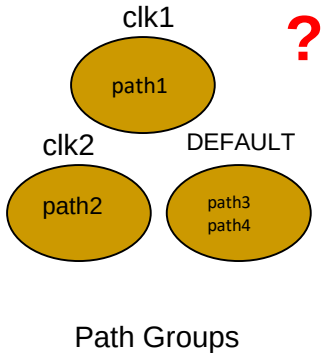




Path Groups

- Timing paths are grouped into path groups by the clocks controlling their endpoints
- Slack is calculated in relation to each clock





Thank You