**Report 4** 110652034 賴羿茗

1. Describe the input fields of each pipeline register.

- IF/ID:

  Input: instruction

- ID/EX:

  Input1: {RegWrite, ALUOp, ALUSrc, RegDst, MemRead, MemWrite, MemtoReg}

  Input2: RSdata

  Input3: RTdata

  Input4: extendData

  Input5: zeroData

  Input6: IFinstruction (From IF/ID)

- EX/MEM:

  Input1: {ID_RegWrite, ID_MemRead, ID_MemWrite, ID_MemtoReg} (From ID/EX)

  Input2: ID_RTdata (From ID/EX)

  Input3: Regdata

  Input4: RegAddr

- MEM/WB:

  Input1: {EX_RegWrite, EX_MemtoReg} (From EX/MEM)

  Input2: EX_RegAddr (From EX/MEM)

  Input3: EX_Regdata (From EX/MEM)

  Input4: MemData

2. Explain your control signals in the **sixth cycle**

**Picture:**

test_data test_1.txt

```
ID_ALUOp[1:0] =00
    ID_ALUSrc =0
    ID_RegDst =1
   EX_MemRead =0
  EX_MemWrite =0
 MEM_MemtoReg =0
 MEM_RegWrite =1
       Branch =0
```

test_data test_2.txt

```
ID_ALUOp[1:0] =01
    ID_ALUSrc =1
    ID_RegDst =0
   EX_MemRead =0
  EX_MemWrite =0
 MEM_MemtoReg =0
 MEM_RegWrite =1
       Branch =0
```