**Report 4** 110652034 賴羿茗

1. Describe the input fields of each pipeline register.

* IF/ID:

Input: instruction

* ID/EX:

Input1: {RegWrite, ALUOp, ALUSrc, RegDst, MemRead, MemWrite, MemtoReg}

Input2: RSdata

Input3: RTdata

Input4: extendData

Input5: zeroData

Input6: IFinstruction (From IF/ID)

* EX/MEM:

Input1: {ID\_RegWrite, ID\_MemRead, ID\_MemWrite, ID\_MemtoReg} (From ID/EX)

Input2: ID\_RTdata (From ID/EX)

Input3: Regdata

Input4: RegAddr

* MEM/WB:

Input1: {EX\_RegWrite, EX\_MemtoReg} (From EX/MEM)

Input2: EX\_RegAddr (From EX/MEM)

Input3: EX\_Regdata (From EX/MEM)

Input4: MemData

1. Explain your control signals in the **sixth cycle**

**Picture:**

|  |
| --- |
| test\_data test\_1.txt |
|  |

|  |
| --- |
| test\_data test\_2.txt |
| 一張含有 文字, 字型, 螢幕擷取畫面, 白色 的圖片  自動產生的描述 |