VECTOR INSTRUCTIONS (Tape Out Progress)

COMPLETE

LMUL = 1 | INSTRUCTIONS | Lmul >= 1

Configuration Instructions	Arithmethic Instructions	Store Instructions	Load Instructions
1) vsetvli	**1) Single-Width**	1) Unit Stride	1) Unit Stride
	5) Bitwise logical		
	8) Min/Max Instructions	i) Unit Stride Store	i) Unit Stride Load
vtype, vcsr (registers)	**12) Move Instructions**	vse8.v	vle8
	i) OPIVX	vse16.v	vle16
	vadd	vse32.v	vle32
	vsub		
	vrsub		
	vand		
	vor		
	vxor		
	vmin		
	vminu		
	vmax		
	vmaxu		
	vmv		
	ii) OPIVI		
	vadd		
	vrsub		
	vand		
	vor		
	vxor		
	vmv		
	iii) OPIVV		
	vadd.vv		
	vsub.vv		
	vmv.vv		
	vand.vv		
	vor.vv		
	vxor.vv		
	vminu.vv		
	vimin.vv		
	vmaxu.vv		
	vmax.vv		
	vmaxu		
	vmv		
	2) Widening Arithmethic Instructions		
	4) Narrowing Arithmethic Instructions		

TAILING AND MASKING

LMUL	Arithmetic	Load/Store
Lmul = 1	Done	Lmul >= 1
Lmul > 1		Emul <=> 1